TEXAS INSTRUMENTS

CSD87334Q3D Synchronous Buck NexFET™ Power Block

1 Features

- Half-Bridge Power Block
- Optimized for High Duty Cycle
- Up to 24 V_{in}
- 96.1% System Efficiency at 12 A
- 1.6 W P_{Loss} at 12 A
- Up to 20 A operation
- High-Frequency Operation (Up to 1.5 MHz)
- High Density – SON 3.3 mm × 3.3 mm Footprint
- Optimized for 5-V Gate Drive
- Low Switching Losses
- Ultra-Low Inductance Package
- RoHS Compliant
- Halogen-Free
- Pb-Free Terminal Plating

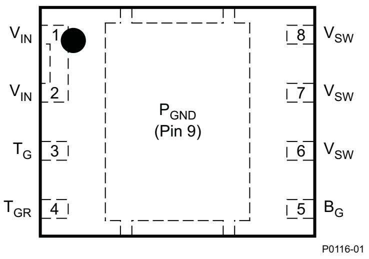
2 Applications

- Synchronous Buck Converters
  - High Frequency Applications
  - High Duty Cycle Applications
- Synchronous Boost Converters
- POL DC-DC Converters

3 Description

The CSD87334Q3D NexFET™ power block is an optimized design for synchronous buck and boost applications offering high current, high efficiency, and high frequency capability in a small 3.3 mm × 3.3 mm outline. Optimized for 5-V gate drive applications, this product offers a flexible solution in high duty cycle applications when paired with an external controller or driver.

Top View

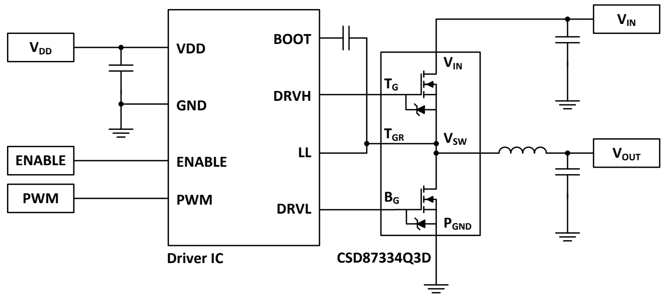


Device Information[1]

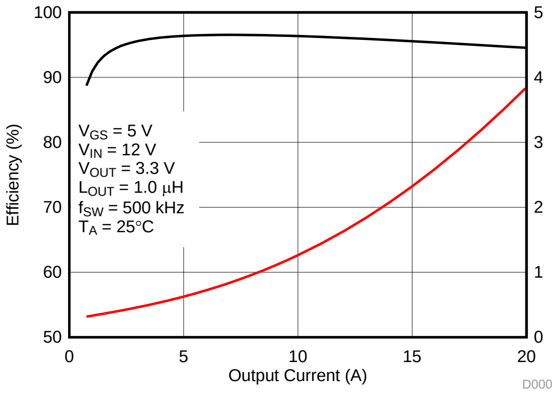
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD87334Q3D	2500	13-Inch Reel	SON 3.3 mm × 3.3 mm Plastic Package	Tape and Reel
CSD87334Q3DT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit



Typical Power Block Efficiency and Power Loss



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4 Revision History

DATE	REVISION	NOTES
July 2015	*	Initial release.

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (see [(1)])

			MIN	MAX	UNIT
	Voltage	V_{IN} to P_{GND}		30	V
		V_{SW} to P_{GND}		30	V
		V_{SW} to P_{GND} (10 ns)		32	V
		T_G to T_{GR}	–8	10	V
		B_G to P_{GND}	–8	10	V
I_{DM}	Pulsed current rating			60	A
P_D	Power dissipation			6	W
E_{AS}	Avalanche energy	Sync FET, I_D = 31 A, L = 0.1 mH		48	mJ
		Control FET, I_D = 31 A, L = 0.1 mH		48	
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

5.2 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

			MIN	MAX	UNIT
V_{GS}	Gate drive voltage		3.3	8	V
V_{IN}	Input supply voltage			24	V
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min)		1500	kHz
	Operating current			20	A
T_J	Operating temperature			125	°C

5.3 Power Block Performance

T_A = 25° (unless otherwise noted) (see [(1)])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{LOSS}	Power loss[(1)]	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, I_{OUT} = 12 A, f_{SW} = 500 kHz, L_{OUT} = 1 µH, T_J = 25ºC		1.6		W
I_{QVIN}	V_{IN} quiescent current	T_G to T_{GR} = 0 V B_G to P_{GND} = 0 V			10	µA

(1) Measurement made with six 10-µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5-V driver IC.

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance (min Cu)[(1)]			130	°C/W
	Junction-to-ambient thermal resistance (max Cu)[(1)][(2)]			75	
$R_{θJC}$	Junction-to-case thermal resistance (top of package)[(1)]			21	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)[(1)]			2.1	

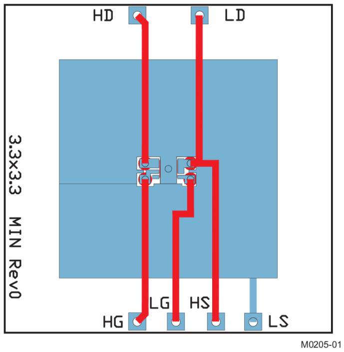
(1) $R_{θJC}$ is determined with the device mounted on a 1-inch^2 (6.45 cm^2), 2-oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06-inch (1.52 mm) thick FR4 board. $R_{θJC}$ is specified by design while $R_{θJA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch^2 (6.45 cm^2) Cu.

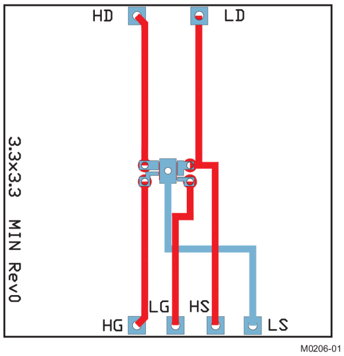
5.5 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0$ V, $I_{DS} = 250$ µA	30			30			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0$ V, $V_{DS} = 20$ V			1			1	µA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0$ V, $V_{GS} = +10 / –8$ V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$, $I_{DS} = 250$ µA	0.75	0.90	1.20	0.75	0.90	1.20	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 3.5$ V, $I_{DS} = 12$ A		6.3	8.3		6.3	8.3	mΩ
		$V_{GS} = 4.5$ V, $I_{DS} = 12$ A		5.6	7.0		5.6	7.0	
		$V_{GS} = 8$ V, $I_{DS} = 12$ A		4.9	6.0		4.9	6.0	
g_{fs}	Transconductance	$V_{DS} = 15$ V, $I_{DS} = 12$ A		62			62		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	$V_{GS} = 0$ V, $V_{DS} = 15$ V, $f = 1$ MHz		971	1260		971	1260	pF
C_{OSS}	Output capacitance			453	589		453	589	pF
C_{RSS}	Reverse transfer capacitance			16	21		16	21	pF
R_G	Series gate resistance			1.0	2.0		1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 15$ V, $I_{DS} = 12$ A		6.4	8.3		6.4	8.3	nC
Q_{gd}	Gate charge – gate to drain			1.0			1.0		nC
Q_{gs}	Gate charge – gate to source			1.9			1.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.9			0.9		nC
Q_{OSS}	Output charge	$V_{DS} = 15$ V, $V_{GS} = 0$ V		10.5			10.5		nC
$t_{d(on)}$	Turn on delay time	$V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_{DS} = 12$ A, $R_G = 2$ Ω		4			4		ns
t_r	Rise time			7			7		ns
$t_{d(off)}$	Turn off delay time			11			11		ns
t_f	Fall time			17			17		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	$I_{DS} = 12$ A, $V_{GS} = 0$ V		0.8	1.0		0.8	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 15$ V, $I_F = 12$ A, di/dt = 300 A/µs		23			23		nC
t_{rr}	Reverse Recovery Time			18			18		ns



Max $R_{\theta JA}$ = 75°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 130°C/W when mounted on minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.6 Typical Power Block Device Characteristics

The Typical Power Block System Characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4.0 inch (W) × 3.5 inch (L) × 0.062 inch (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following; V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L_{OUT} = 1.0 µH. T_A = 125°C, unless stated otherwise.

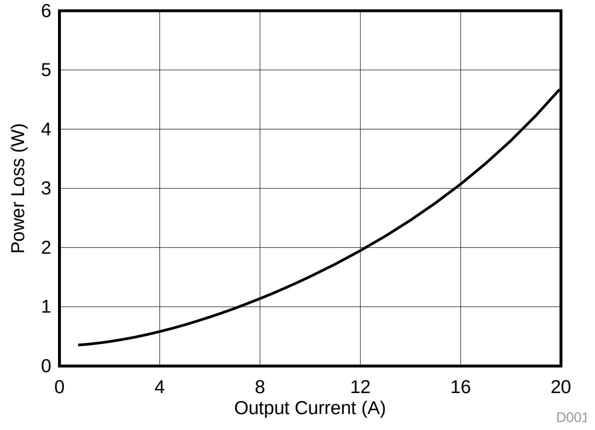


Figure 1. Power Loss vs Output Current

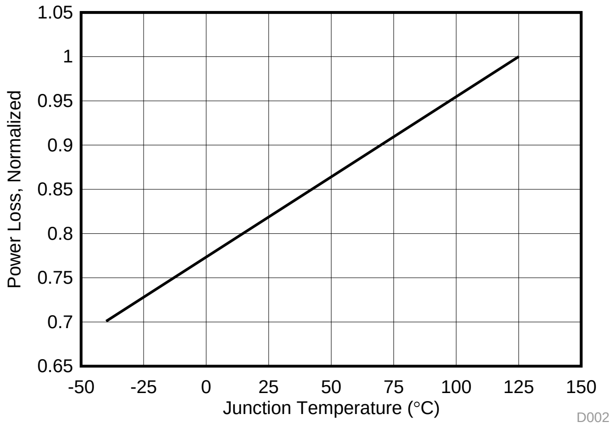


Figure 2. Power Loss vs Temperature

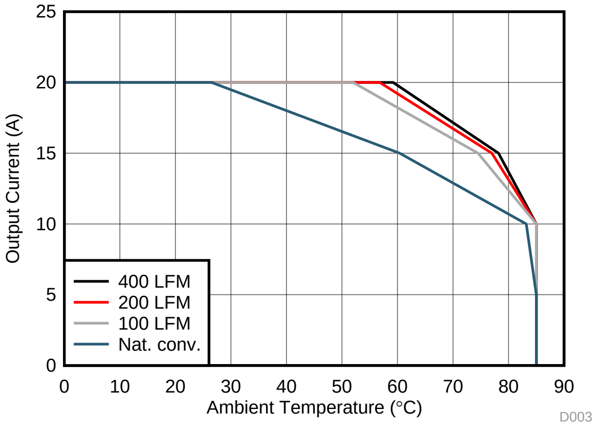


Figure 3. Safe Operating Area – PCB Horizontal Mount

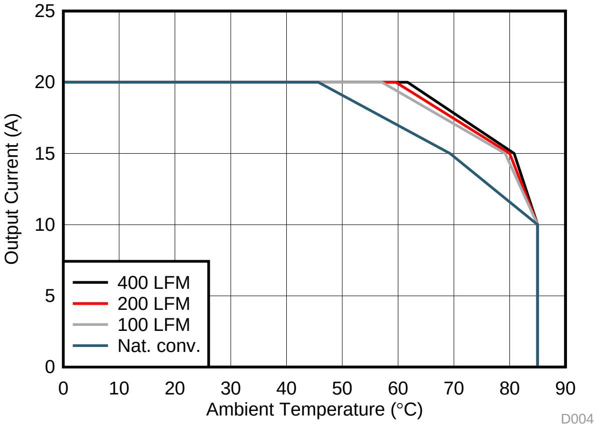


Figure 4. Safe Operating Area – PCB Vertical Mount

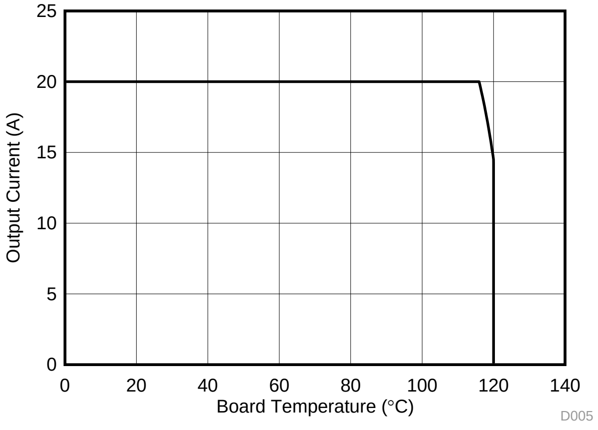
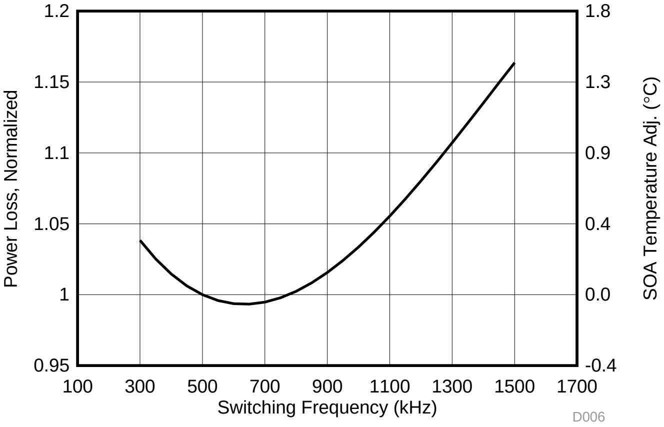


Figure 5. Typical Safe Operating Area

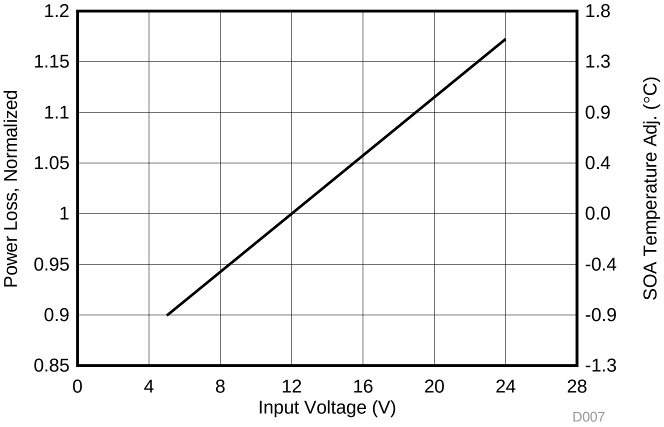
Typical Power Block Device Characteristics (continued)

The Typical Power Block System Characteristic curves (Figure 1 through Figure 9) are based on measurements made on a PCB design with dimensions of 4.0 inch (W) × 3.5 inch (L) × 0.062 inch (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation. Conditions for Figure 1 through Figure 5 are given by the following; V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L_{OUT} = 1.0 µH. T_A = 125°C, unless stated otherwise.



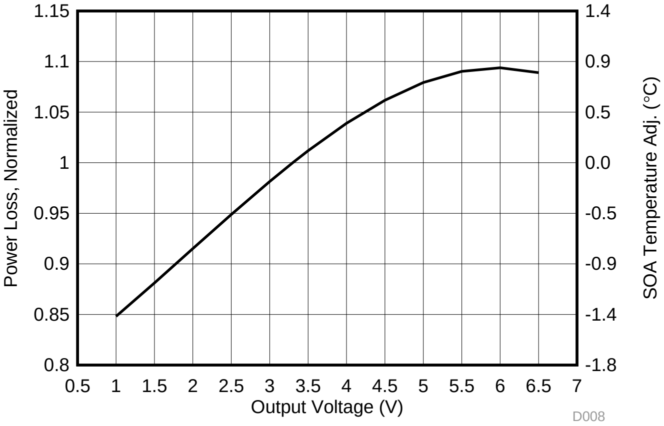
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 3.3 V
I_{OUT} = 15 A L_{OUT} = 1.0 µH

Figure 6. Normalized Power Loss vs Switching Frequency



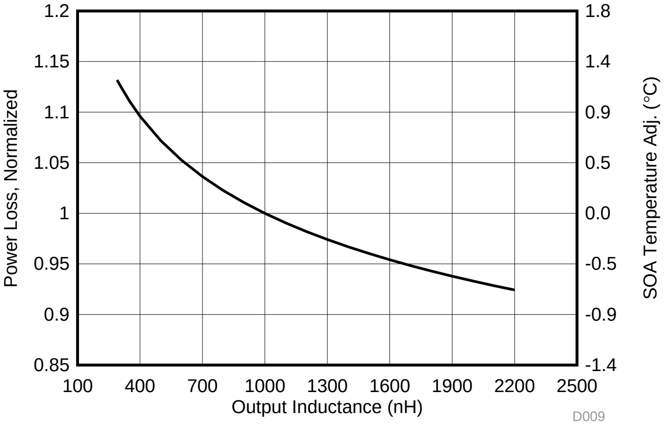
f_{SW} = 500 kHz V_{GS} = 5 V V_{OUT} = 3.3 V
I_{OUT} = 15 A L_{OUT} = 1.0 µH

Figure 7. Normalized Power Loss vs Input Voltage



V_{IN} = 12 V V_{GS} = 5 V I_{OUT} = 15 A
f_{SW} = 500 kHz L_{OUT} = 1.0 µH

Figure 8. Normalized Power Loss vs Output Voltage



V_{IN} = 12 V V_{GS} = 5 V I_{OUT} = 15 A
f_{SW} = 500 kHz V_{OUT} = 3.3 V

Figure 9. Normalized Power Loss vs Output Inductance

5.7 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

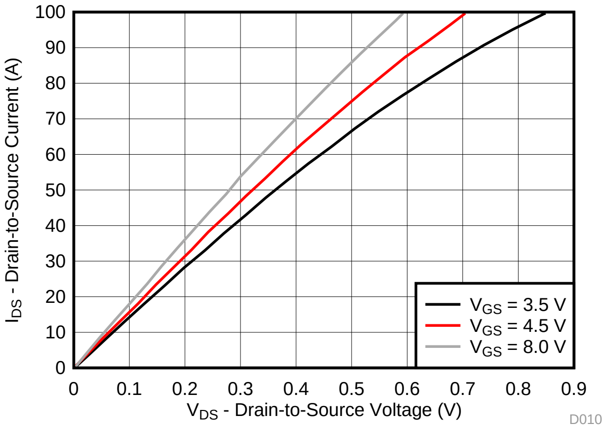
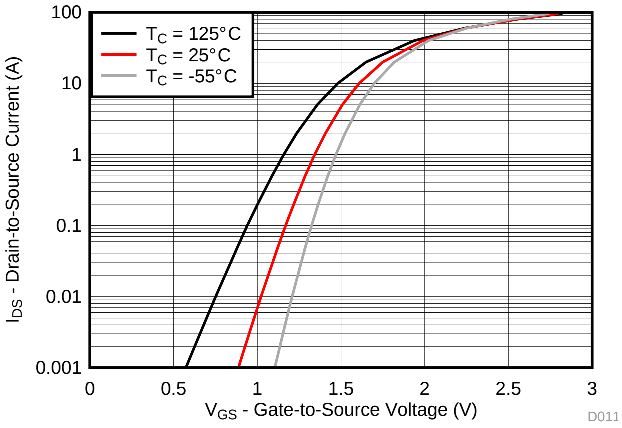
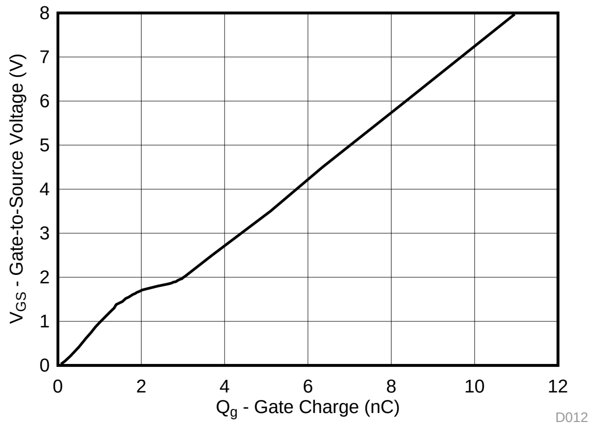


Figure 10. MOSFET Saturation Characteristics



V_{DS} = 5 V

Figure 11. MOSFET Transfer Characteristics



I_D = 12 A V_{DS} = 15 V

Figure 12. MOSFET Gate Charge

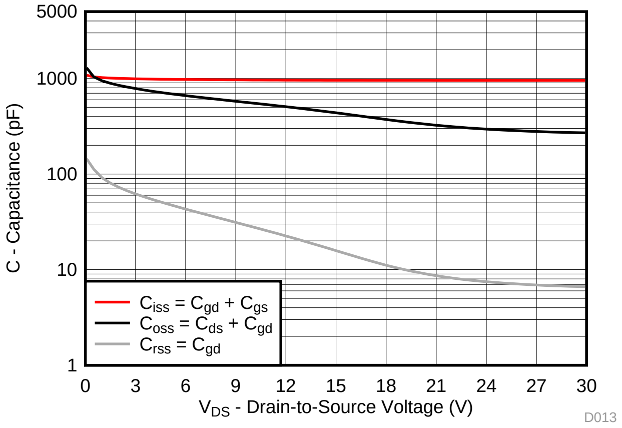
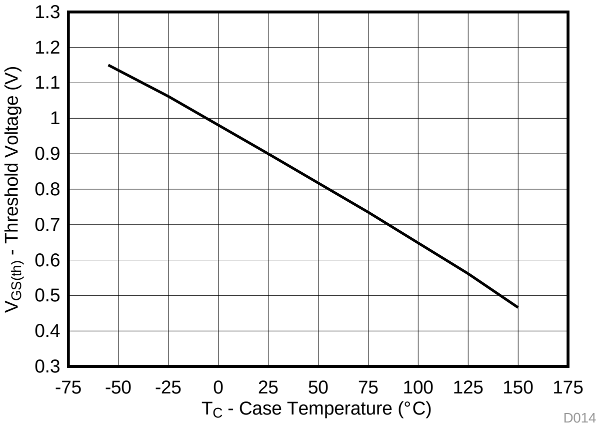


Figure 13. MOSFET Capacitance



I_D = 250 µA

Figure 14. MOSFET $V_{GS(th)}$

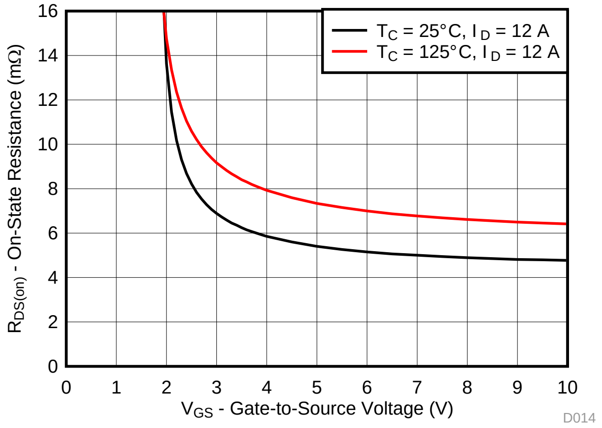


Figure 15. MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

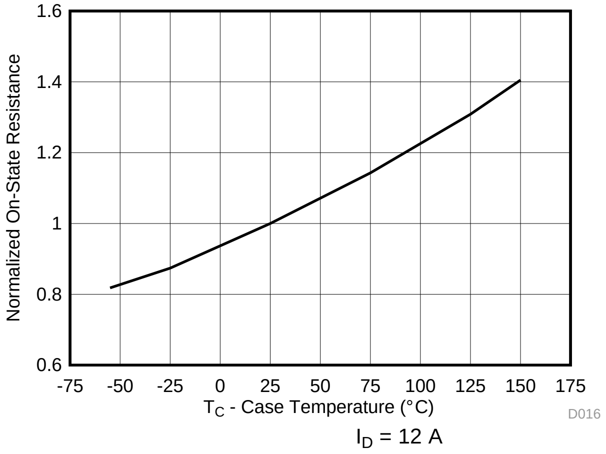


Figure 16. MOSFET Normalized $R_{DS(on)}$

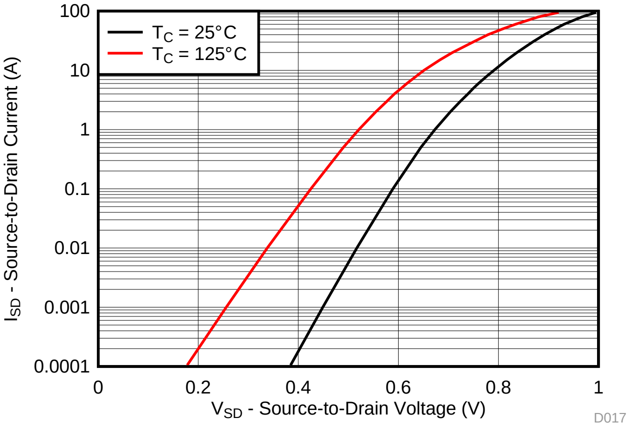


Figure 17. MOSFET Body Diode

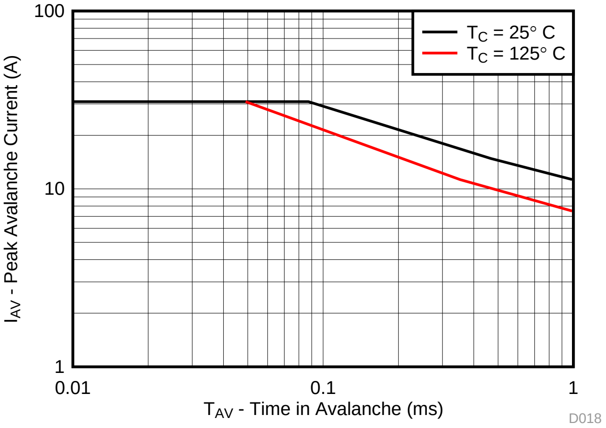


Figure 18. MOSFET Unclamped Inductive Switching

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87334Q3D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.2 Typical Application

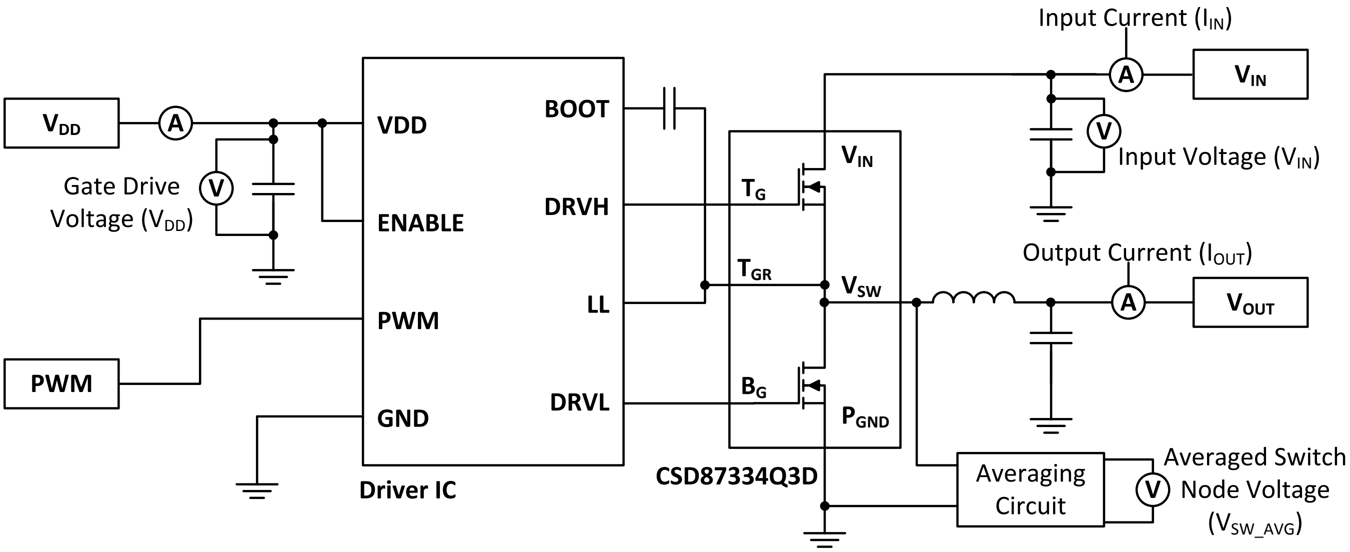


Figure 19. Typical Circuit Application

6.3 System Example

6.3.1 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87334Q3D as a function of load current. This curve is measured by configuring and running the CSD87334Q3D as it would be in the final application (see Figure 19). The measured power loss is the CSD87334Q3D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

System Example (continued)

6.3.2 Safe Operating Curves (SOA)

The SOA curves in the CSD87334Q3D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the SOA. All the curves are based on measurements made on a PCB design with dimensions of 4 inches (W) × 3.5 inches (L) × 0.062 inches (T) and 6 copper layers of 1-oz. copper thickness.

6.3.3 Normalized Curves

The normalized curves in the CSD87334Q3D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss, and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

6.3.4 Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Design Example*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure outlines the steps the user should take to predict product performance for any set of system conditions.

6.3.4.1 Design Example

Operating Conditions:

- Output Current = 15 A
- Input Voltage = 16 V
- Output Voltage = 5 V
- Switching Frequency = 1000 kHz
- Inductor = 0.6 µH

6.3.4.2 Calculating Power Loss

- Power Loss at 15 A = 2.8 W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.05 (Figure 7)
- Normalized Power Loss for output voltage ≈ 1.08 (Figure 8)
- Normalized Power Loss for switching frequency ≈ 1.03 (Figure 6)
- Normalized Power Loss for output inductor ≈ 1.05 (Figure 9)
- **Final calculated Power Loss = 2.8 W x 1.05 × 1.08 × 1.03 × 1.05 ≈ 3.4 W**

6.3.4.3 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 0.5ºC (Figure 7)
- SOA adjustment for output voltage ≈ 0.7ºC (Figure 8)
- SOA adjustment for switching frequency ≈ 0.3ºC (Figure 6)
- SOA adjustment for output inductor ≈ 0.5ºC (Figure 9)
- **Final calculated SOA adjustment = 0.5 + 0.7 + 0.3 + 0.5 ≈ 2.0ºC**

In the design example, the estimated power loss of the CSD87334Q3D would increase to 3.4 W. In addition, the maximum allowable board or ambient temperature, or both, would have to decrease by 2.0ºC. Figure 20 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board or ambient temperature.
3. Adjust the SOA board or ambient temperature by subtracting the temperature adjustment value.

System Example (continued)

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 2.0ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board or ambient temperature.

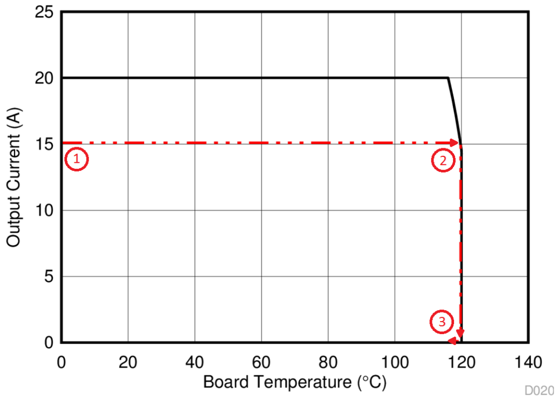


Figure 20. Power Block SOA

7 Layout

7.1 Layout Guidelines

7.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is provided.

7.1.2 Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's V_{IN} and P_{GND} pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the V_{IN} and P_{GND} pins (see Figure 21). The example in Figure 21 uses six 10=µF ceramic capacitors (TDK part number C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, and so forth). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block V_{SW} pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.(1) In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a Boost Resistor or RC snubber can be an effective way to easily reduce the peak ring level. The recommended Boost Resistor value will range between 1.0 to 4.7 Ω depending on the output characteristics of Driver IC used in conjunction with the Power Block. The RC snubber values can range from 0.5 to 2.2 Ω for the R, and from 330 to 2200 pF for the C. Please refer to *Snubber Circuits: Theory, Design and Application* (SLUP100) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the V_{SW} node and P_{GND} (see Figure 21). (1)

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(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.2 Layout Example

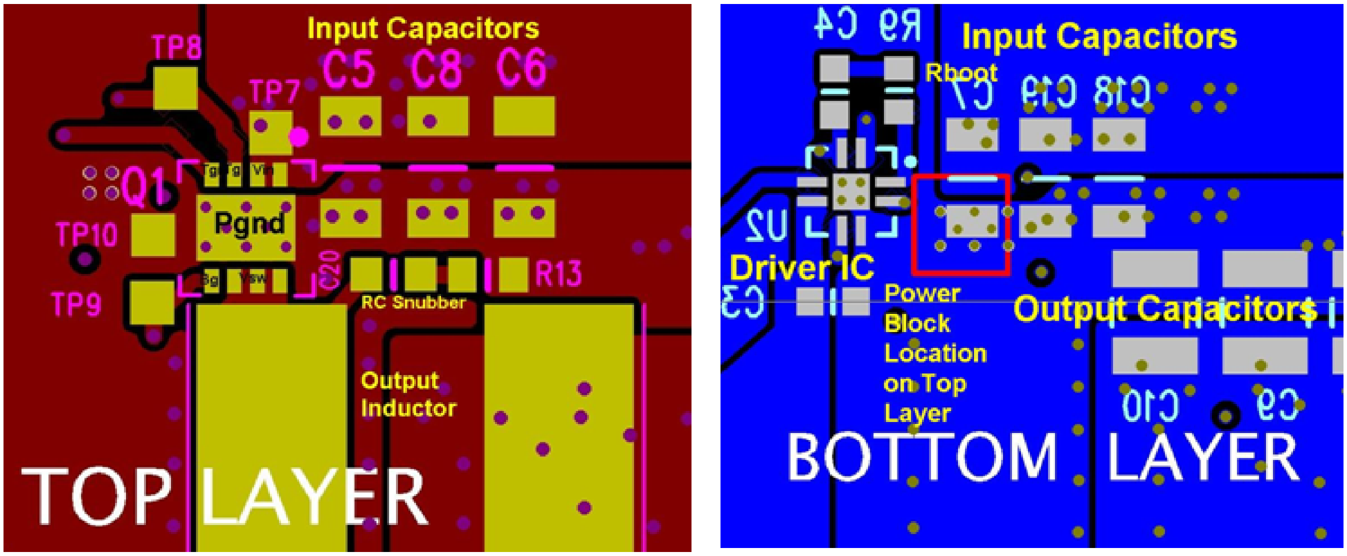

Figure 21. Recommended PCB Layout (Top Down)

7.3 Thermal Considerations

The Power Block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 21 uses vias with a 10-mil drill hole and a 16-mil capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias should align with the PCB design rules and manufacturing capabilities of the end user.

8 Device and Documentation Support

8.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.2 Trademarks

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8.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

8.4 Glossary

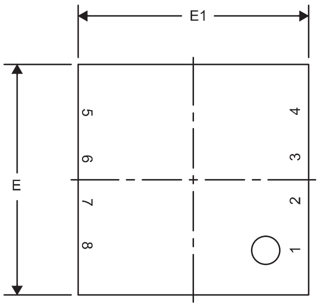
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

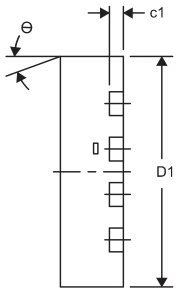
9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

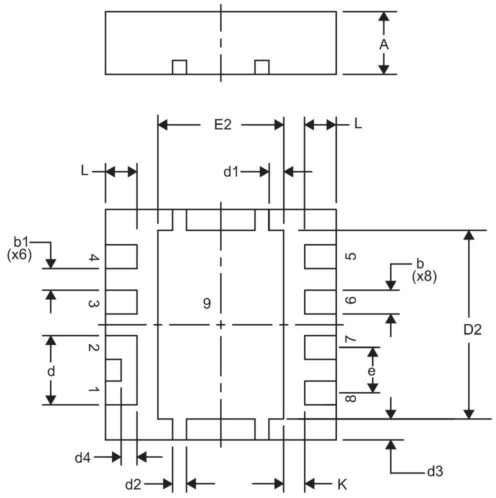
9.1 Q3D Package Dimensions



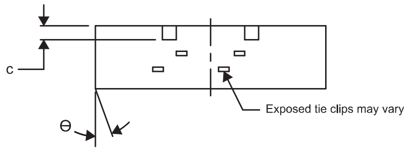
Top View



Side View



Bottom View

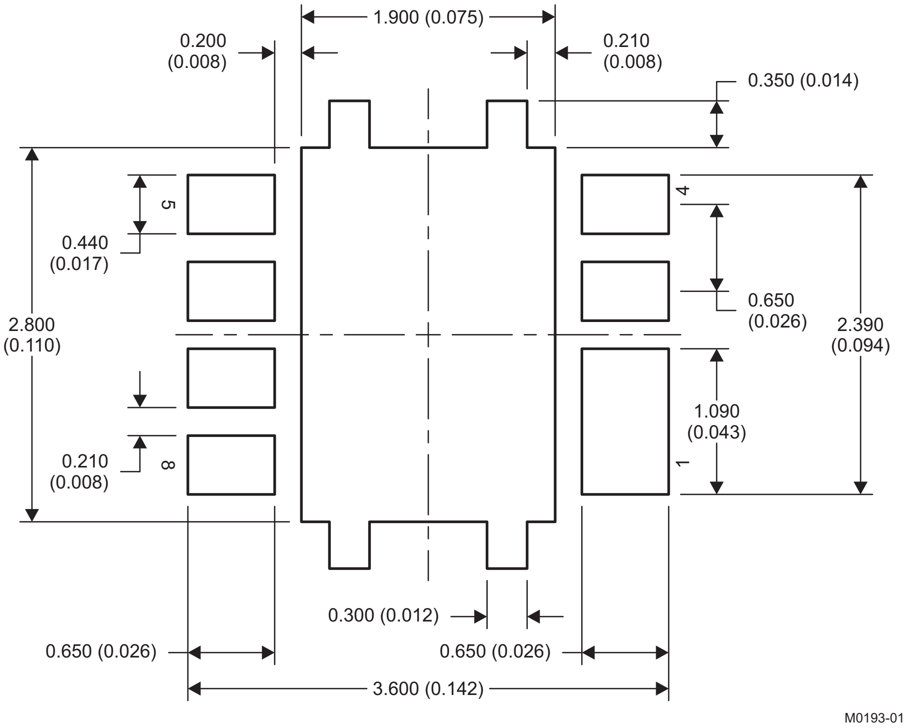


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.850		1.050	0.033		0.041
b	0.280		0.400	0.011		0.016
b1		0.310			0.012	
c	0.150		0.250	0.006		0.010
c1	0.150		0.250	0.006		0.010
d	0.940		1.040	0.037		0.041
d1	0.160		0.260	0.006		0.010
d2	0.150		0.250	0.006		0.010
d3	0.250		0.350	0.010		0.014
d4	0.175		0.275	0.007		0.011
D1	3.200		3.400	0.126		0.134
D2	2.650		2.750	0.104		0.108
E	3.200		3.400	0.126		0.134
E1	3.200		3.400	0.126		0.134
E2	1.750		1.850	0.069		0.073
e		0.650 TYP			0.026 TYP	
L	0.400		0.500	0.016		0.020
θ	0.000		–	–		–
K		0.300 TYP			0.012 TYP	

Pinout Configuration

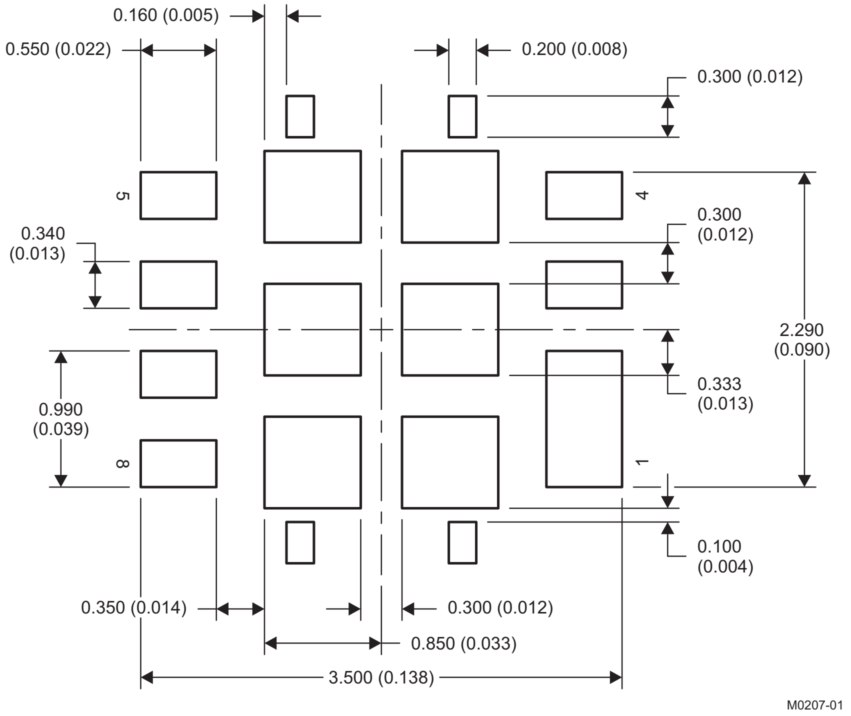
POSITION	DESIGNATION
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

9.2 Land Pattern Recommendation



NOTE: Dimensions are in mm (inches).

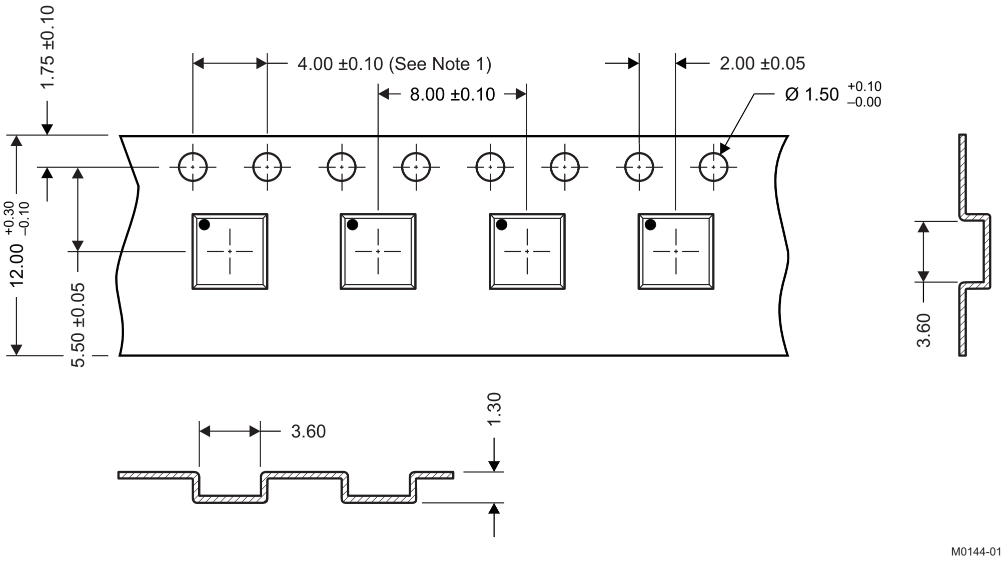
9.3 Stencil Recommendation



NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

9.4 Q3D Tape and Reel Information



NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ± 0.2

2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87334Q3D	ACTIVE	VSON	DPB	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D	Samples
CSD87334Q3DT	ACTIVE	VSON	DPB	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 150	87334D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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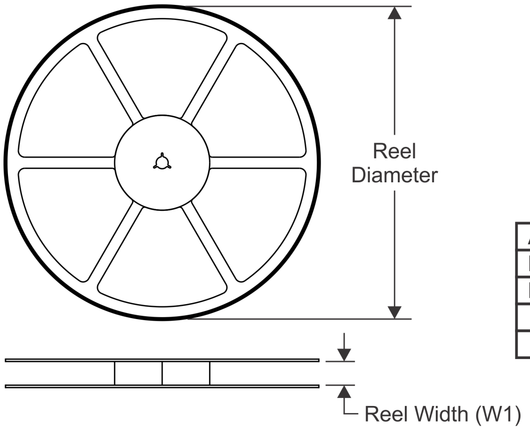
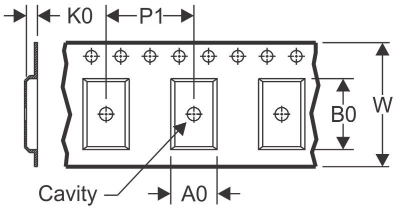
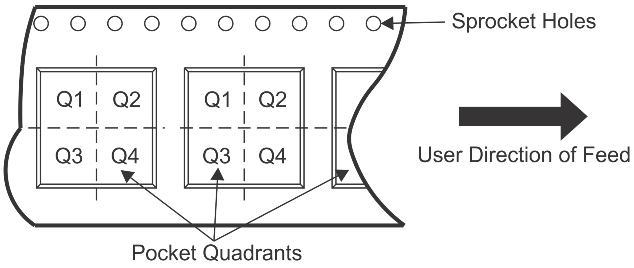
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

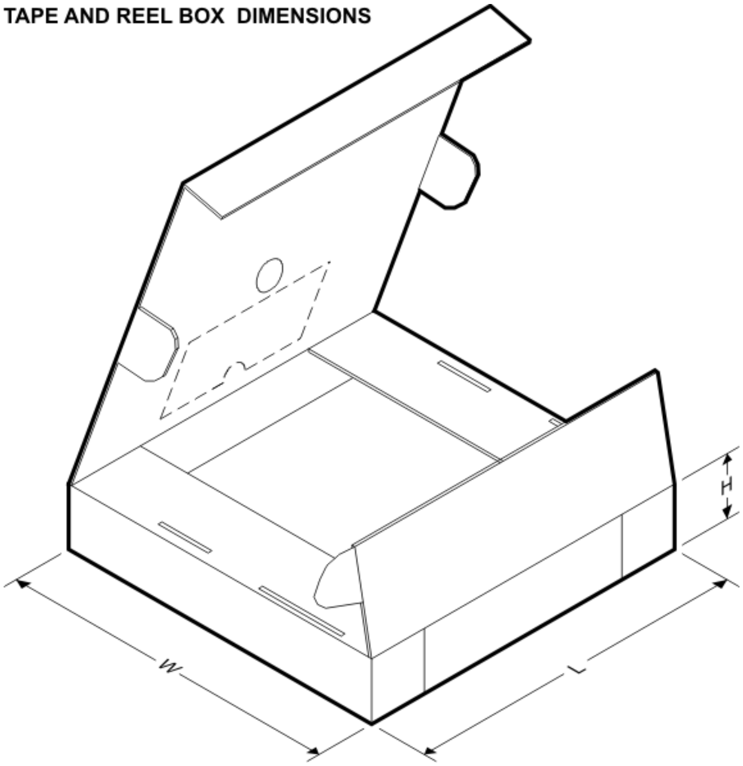
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87334Q3D	VSON	DPB	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87334Q3DT	VSON	DPB	8	250	180.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87334Q3D	VSON	DPB	8	2500	367.0	367.0	35.0
CSD87334Q3DT	VSON	DPB	8	250	210.0	185.0	35.0

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