

# P-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD22202W15](#)

## FEATURES

- Low Resistance
- Small Footprint 1.5-mm x 1.5-mm
- Pb Free
- Gate ESD Protection
- RoHS Compliant
- Halogen Free
- Gate-Source Voltage Clamp

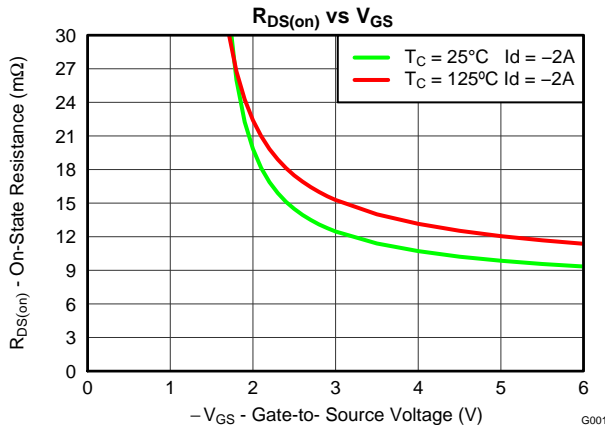
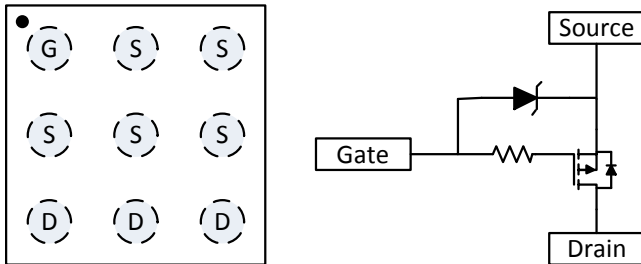
## APPLICATIONS

- Battery Management
- Battery Protection
- Load Switch Applications

## DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View and Circuit Configuration



## PRODUCT SUMMARY

V <sub>DS</sub>	Drain to Drain Voltage	-8	V
Q <sub>g</sub>	Gate Charge Total (-4.5V)	6.5	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	1.0	nC
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = -2.5V	14.5 mΩ
		V <sub>GS</sub> = -4.5V	10.2 mΩ
V <sub>GS(th)</sub>	Threshold Voltage	-0.8	V

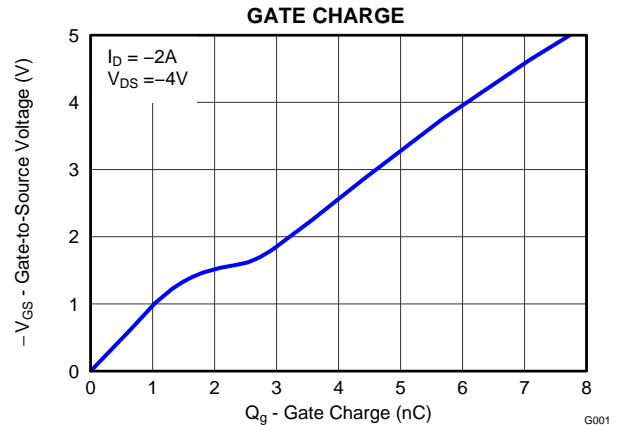
## ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD22202W15	1.5-mm x 1.5-mm Wafer BGA Package	7-Inch Reel	3000	Tape and Reel

## ABSOLUTE MAXIMUM RATINGS

T <sub>A</sub> = 25°C unless otherwise stated		VALUE	UNIT
V <sub>DS</sub>	Drain to Source Voltage	-8	V
V <sub>GS</sub>	Gate to Source Voltage	-6.0	V
I <sub>D</sub>	Continuous Drain Current <sup>(1)</sup> (Silicon Limited)	-10	A
	Pulsed Drain Current <sup>(2)</sup>	-48	A
I <sub>G</sub>	Continuous Gate Current <sup>(3)</sup>	-0.5	A
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	1.5	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) R<sub>θJA</sub> = 75°C/W on 1in<sup>2</sup> Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300μs, duty cycle ≤2%
- (3) Limited by gate resistance.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = -250\mu A$	-8			V
$BV_{GSS}$	Gate to Source Voltage	$V_{DS} = 0V, I_G = -250\mu A$	-6.0			V
$I_{DDs}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -4V$			-1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -4V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\mu A$	-0.6	-0.8	-1.1	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -2.5V, I_{DS} = -2A$		14.5	17.4	m $\Omega$
		$V_{GS} = -4.5V, I_{DS} = -2A$		10.2	12.2	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = -4V, I_{DS} = -2A$		15.3		S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = -4V,$ $f = 1MHz$		1060	1390	pF
$C_{OSS}$	Output Capacitance			588	765	pF
$C_{RSS}$	Reverse Transfer Capacitance			192	250	pF
$R_G$	Series Gate Resistance			28		$\Omega$
$Q_g$	Gate Charge Total (-4.5V)	$V_{DS} = -4V,$ $I_D = -2A$		6.5	8.4	nC
$Q_{gd}$	Gate Charge - Gate to Drain			1.0		nC
$Q_{gs}$	Gate Charge - Gate to Source			1.6		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			0.8		nC
$Q_{OSS}$	Output Charge		$V_{DS} = -4V, V_{GS} = 0V$		2.7	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -4V, V_{GS} = -4.5V,$ $I_{DS} = -2A, R_G = 10\Omega$		10.4		ns
$t_r$	Rise Time			8.4		ns
$t_{d(off)}$	Turn Off Delay Time			109		ns
$t_f$	Fall Time			38		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{DS} = -2A, V_{GS} = 0V$		-0.75	-1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = -4V, I_F = -2A,$ $di/dt = 200A/\mu s$		22		nC
$t_{rr}$	Reverse Recovery Time			19		ns

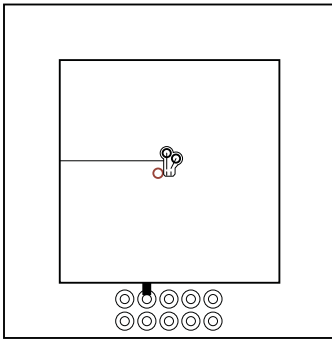
## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction to Ambient Thermal Resistance <sup>(1)</sup>	75	$^\circ\text{C/W}$
	Junction to Ambient Thermal Resistance <sup>(2)</sup>	210	$^\circ\text{C/W}$

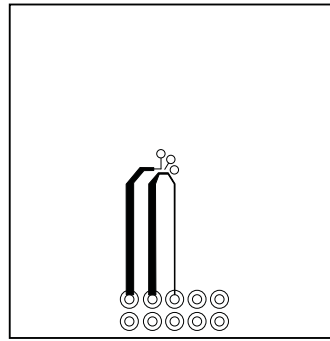
(1) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.



M0149-01

Typ  $R_{\theta JA} = 75^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> of 2 oz. Cu.



M0150-01

Typ  $R_{\theta JA} = 210^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of 2  
oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

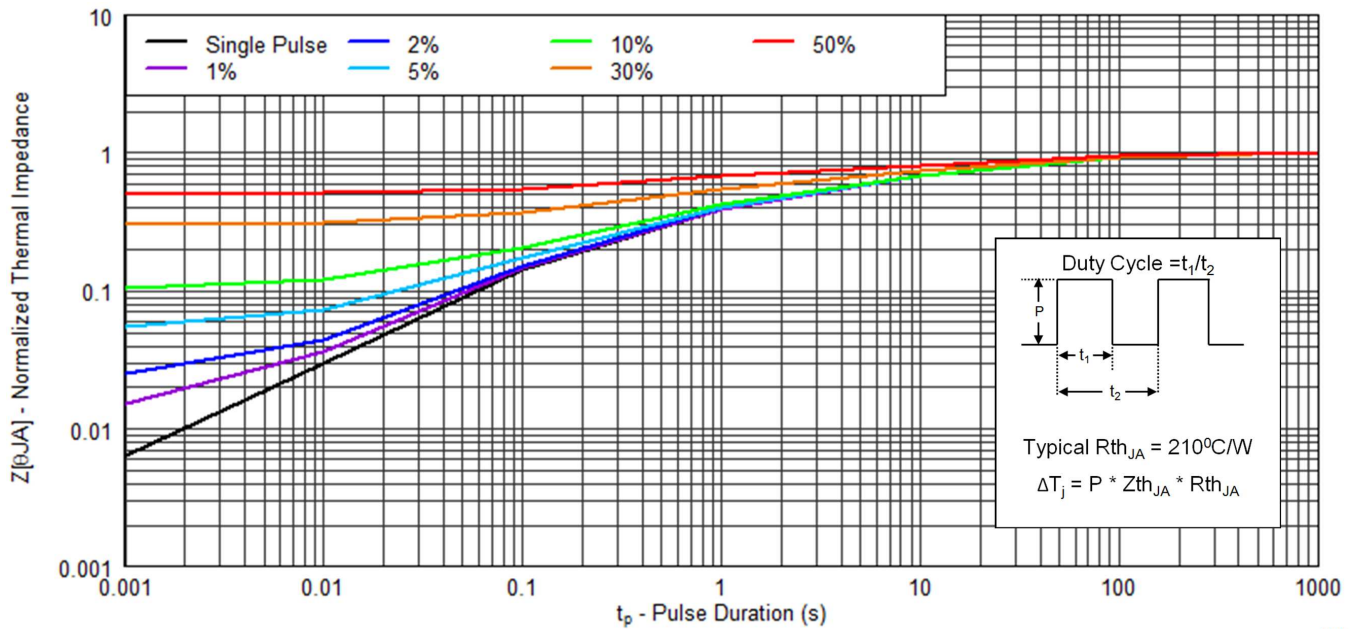
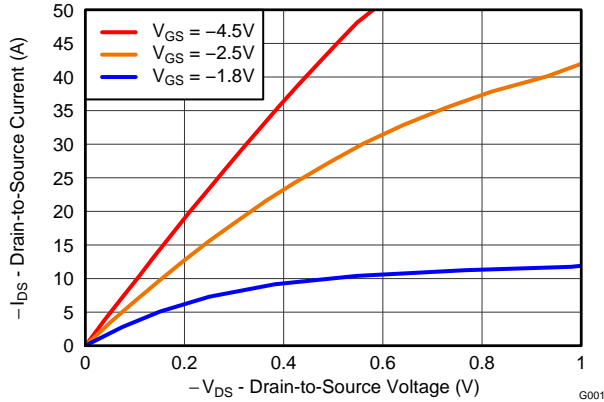


Figure 1. Transient Thermal Impedance

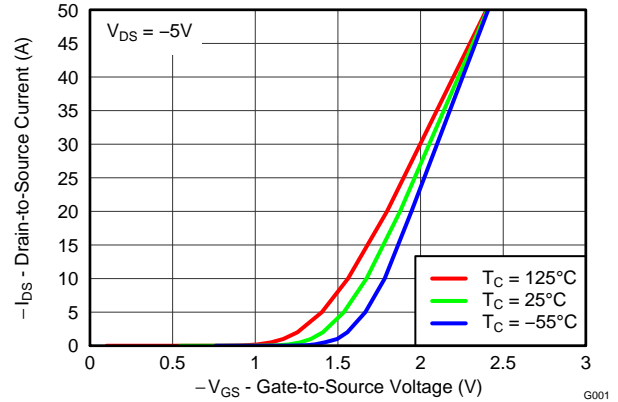
3201

**TYPICAL MOSFET CHARACTERISTICS (continued)**

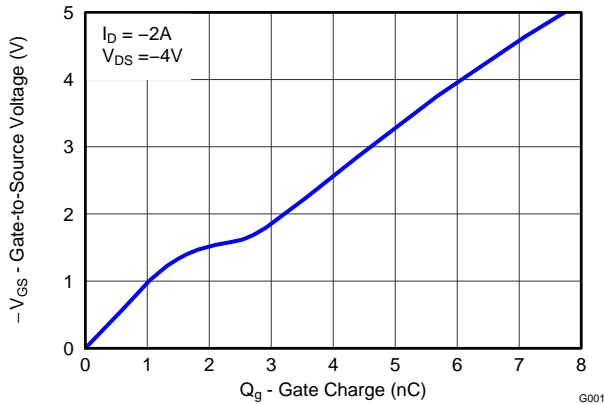
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



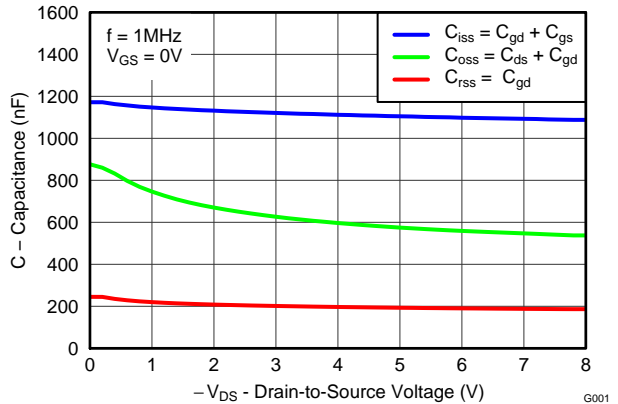
**Figure 2. Saturation Characteristics**



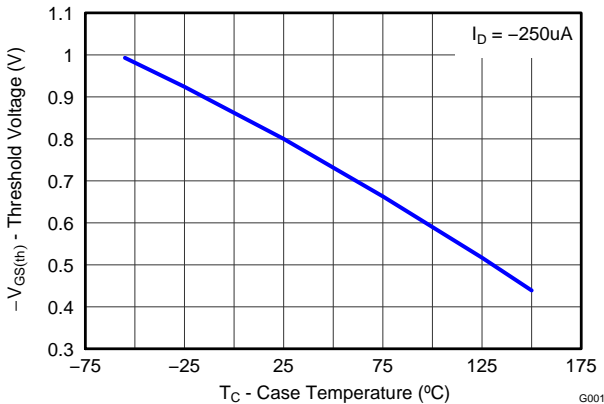
**Figure 3. Transfer Characteristics**



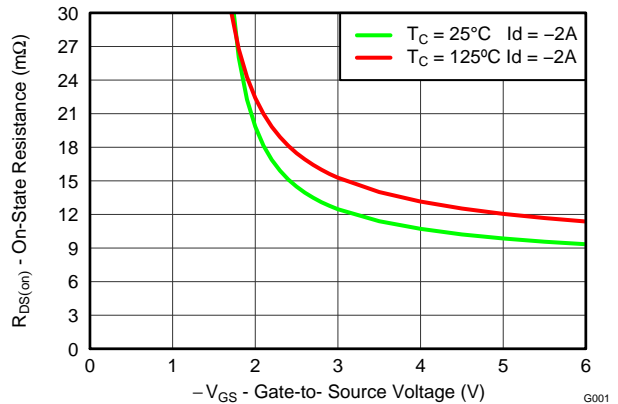
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

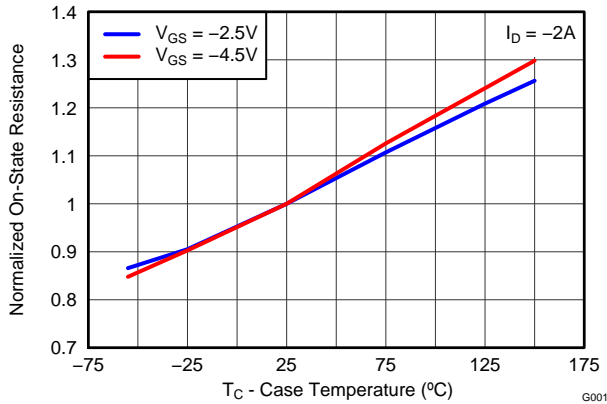


Figure 8. Normalized On-State Resistance vs. Temperature

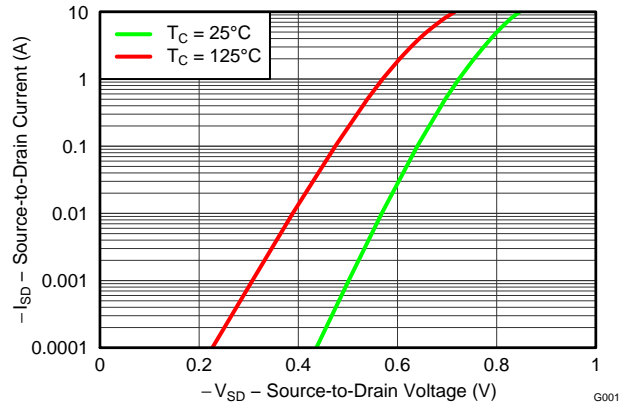


Figure 9. Typical Diode Forward Voltage

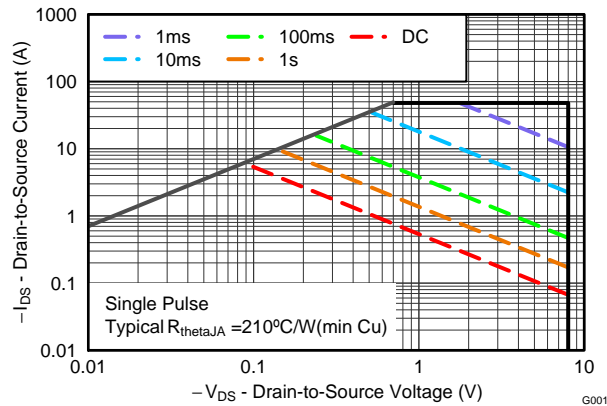


Figure 10. Maximum Safe Operating Area

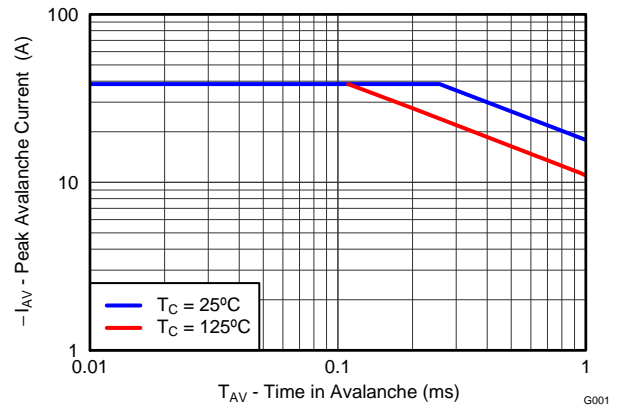


Figure 11. Single Pulse Unclamped Inductive Switching

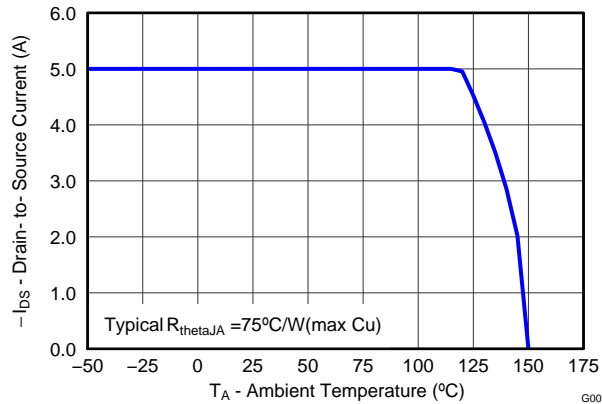
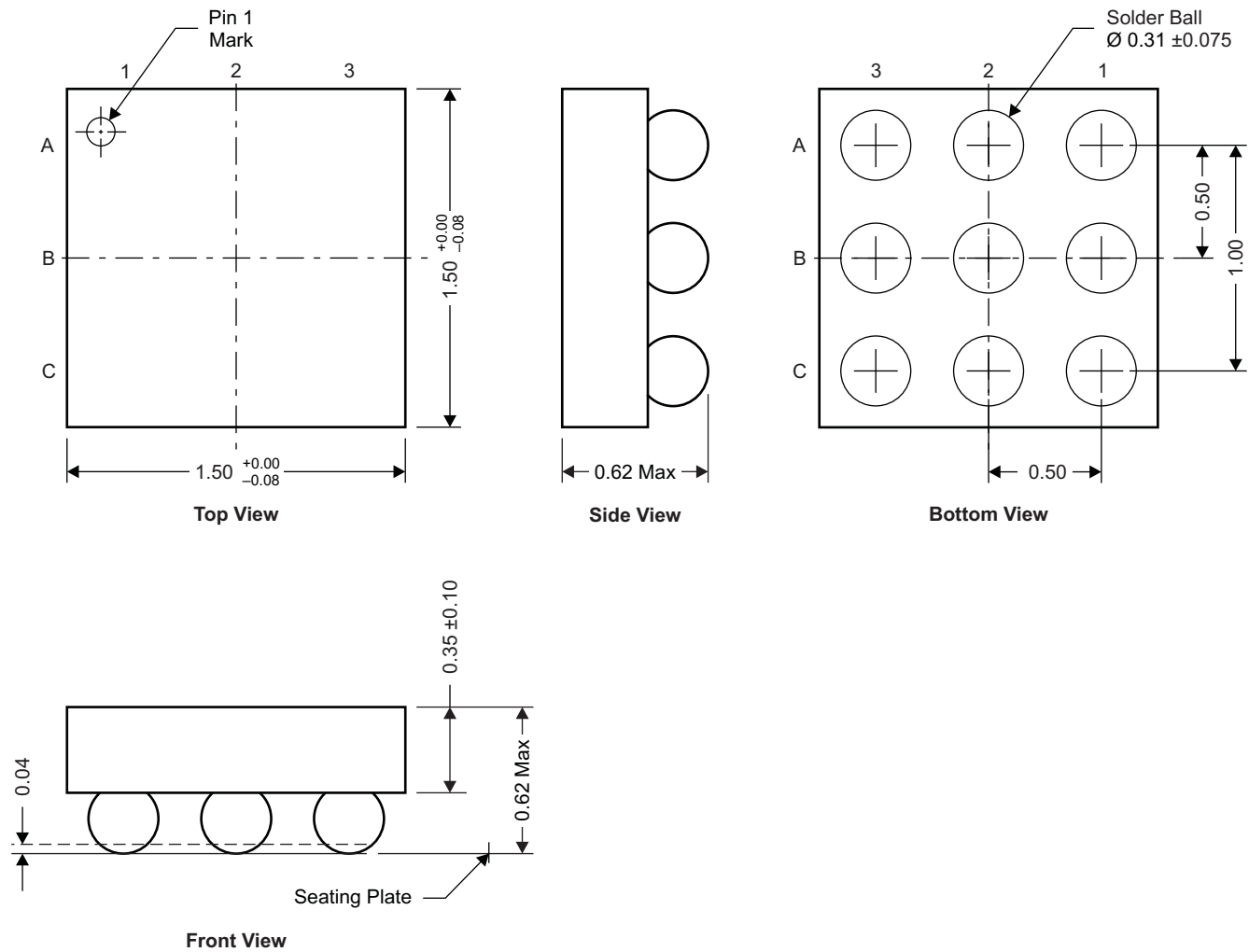


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

**CSD22202W15 Package Dimensions**



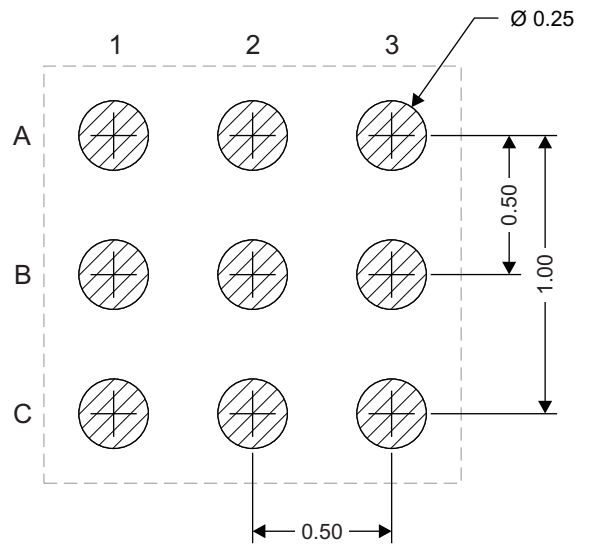
NOTE: All dimensions are in mm (unless otherwise specified)

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**Pinout**

POSITION	DESIGNATION
A1	Gate
A2, A3, B1, B2, B3	Source
C1, C2, C3	Drain

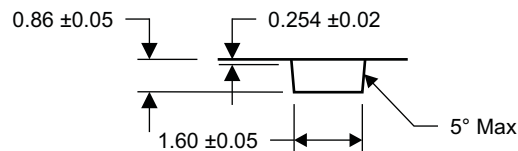
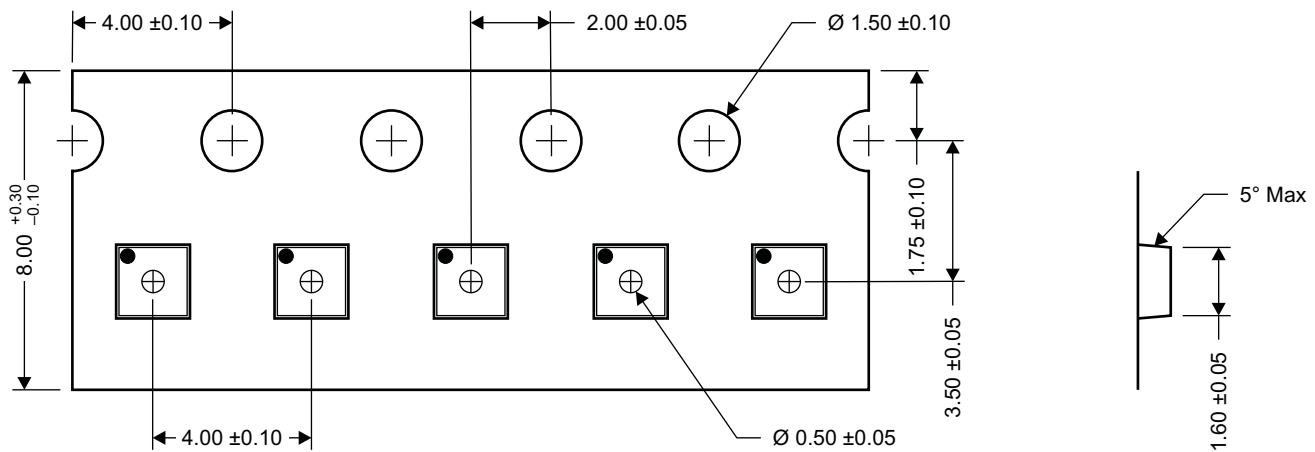
### Recommended Land Pattern



M0172-01

NOTE: All dimensions are in mm (unless otherwise specified)

### Tape and Reel Information



M0173-01

- NOTES:
1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
  2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
  3. Material: black static-dissipative polystyrene
  4. All dimensions are in mm (unless otherwise specified)
  5. Thickness: 0.30 ± 0.05mm
  6. MSL1 260°C (IR and convection) PbF reflow compatible

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD22202W15	ACTIVE	DSBGA	YZF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	22202	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD22202W15	DSBGA	YZF	9	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

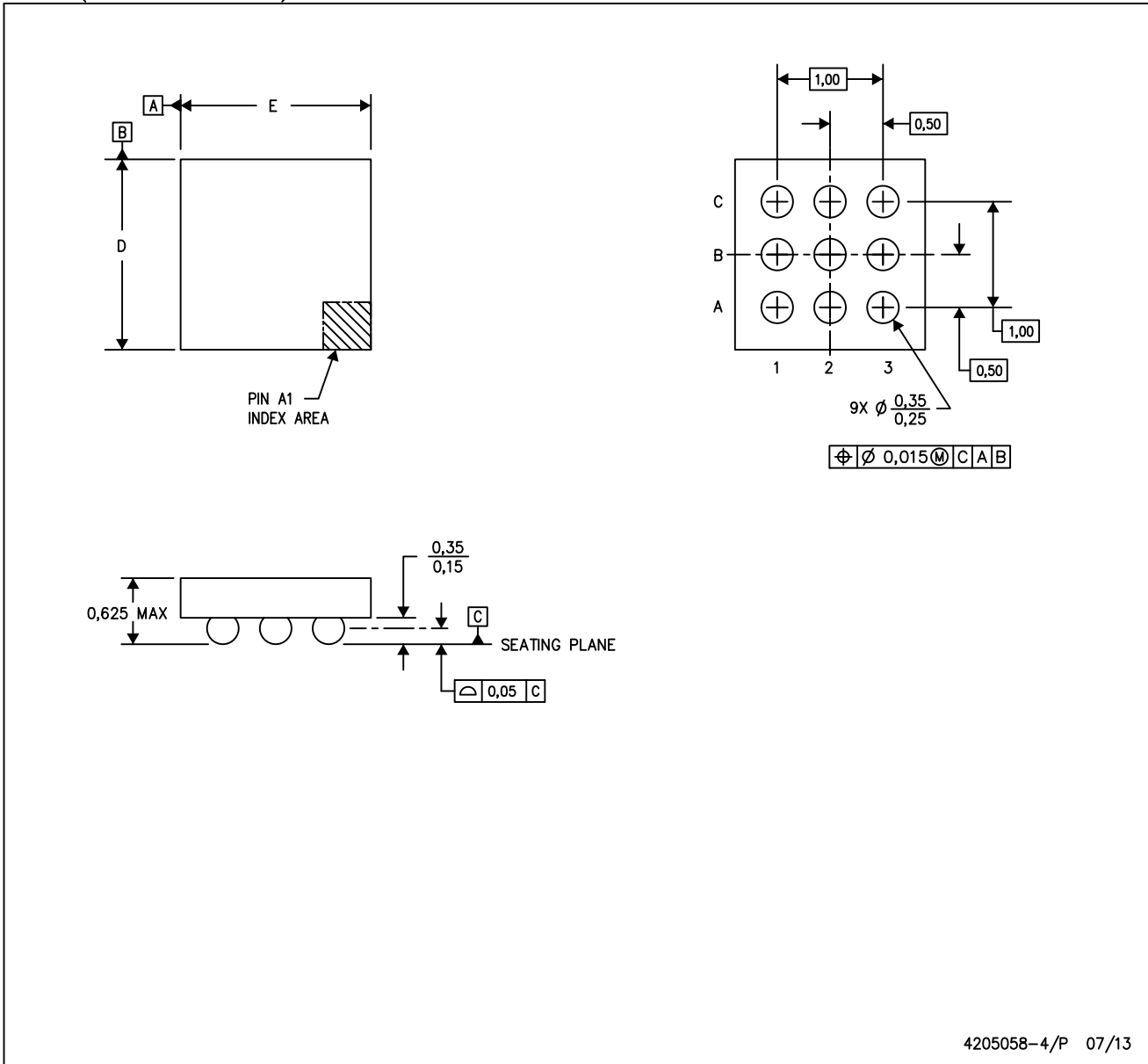


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD22202W15	DSBGA	YZF	9	3000	210.0	185.0	35.0

YZF (S-XBGA-N9)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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### Applications

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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