



CSD16408Q5

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N-Channel NexFET[™] Power MOSFET

FEATURES

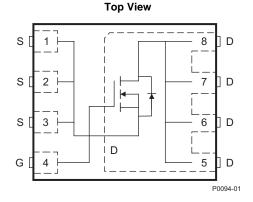
- Ultra Low Q_g and Q_{gd}
- Low Thermal Resistance
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- SON 5-mm x 6-mm Plastic Package •

APPLICATIONS

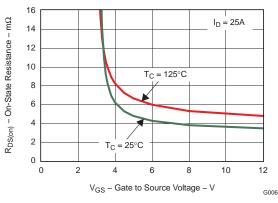
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- **Optimized for Control FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.







PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	/oltage 25		
Qg	Gate Charge Total (4.5V)	6.7		nC
Q _{gd}	Gate Charge Gate to Drain	1.9		nC
P	Drain to Source On Resistance	$V_{GS} = 4.5V$	5.4	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 10V$	3.6	mΩ
V _{GS(th)}	Threshold Voltage	1.8		V

ORDERING INFORMATION

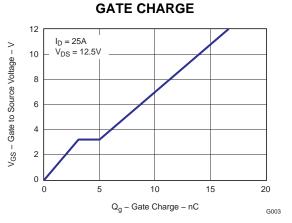
Device	Package	Media	Qty	Ship
CSD16408Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 2$	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / -12	V
	Continuous Drain Current, $T_C = 25^{\circ}C$	113	А
ID	Continuous Drain Current ⁽¹⁾	22	А
I _{DM}	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$	141	А
PD	Power Dissipation ⁽¹⁾	3.1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I_D = 23A, L = 0.1mH, R _G = 25 Ω	126	mJ

Typical $R_{\theta JA} = 41^{\circ}C/W$ on 1-inch² (6.45-cm²), 2-oz. (1) (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300µs, duty cycle ≤2%



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ELECTRICAL CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static C	haracteristics					
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
I _{DSS}	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = 20V$			1	μA
I _{GSS}	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = +16/-12V$			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.4	1.8	2.1	V
	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 25A$		5.4	6.8	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 25A$		3.6	4.5	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 25A		60		S
Dynamic	c Characteristics					
C _{ISS}	Input Capacitance			990	1300	pF
C _{OSS}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		760	1000	pF
C _{RSS}	Reverse Transfer Capacitance			75	100	pF
R _g	Series Gate Resistance			0.8	1.6	Ω
Qg	Gate Charge Total (4.5V)			6.7	8.9	nC
Q _{gd}	Gate Charge – Gate to Drain	$V_{DS} = 12.5V, I_D = 25A$		1.9		nC
Q _{gs}	Gate Charge – Gate to Source	$v_{DS} = 12.5 \text{ V}, \text{ I}_{D} = 25 \text{ A}$		3.1		nC
Q _{g(th)}	Gate Charge at Vth			1.8		nC
Q _{OSS}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		15.7		nC
t _{d(on)}	Turn On Delay Time			11.3		ns
t _r	Rise Time	V _{DS} = 12.5V, V _{GS} = 4.5V,		25		ns
t _{d(off)}	Turn Off Delay Time	$I_D = 20A, R_G = 2\Omega$		11		ns
t _f	Fall Time		10.8			ns
Diode C	haracteristics					
V _{SD}	Diode Forward Voltage	$I_{\rm S} = 25 {\rm A}, {\rm V}_{\rm GS} = 0 {\rm V}$		0.8	1	V
Q _{rr}	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 25A, di/dt = 300A/\mu s$		17		nC
t _{rr}	Reverse Recovery Time	V _{DD} = 13V, I _F = 25A, di/dt = 300A/µs		21		ns

THERMAL CHARACTERISTICS

 $T_A = 25^{\circ}C$ unless otherwise stated

PARAMETER			TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.9	°C/W
R_{\thetaJA}	Thermal Resistance Junction to Ambient ⁽¹⁾ ⁽²⁾			51	°C/W

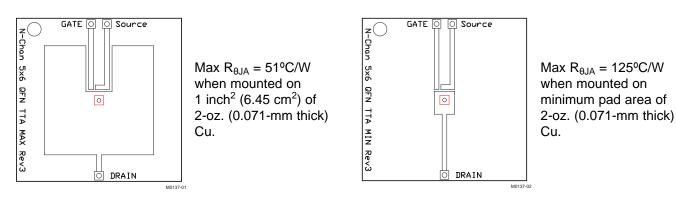
(1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.





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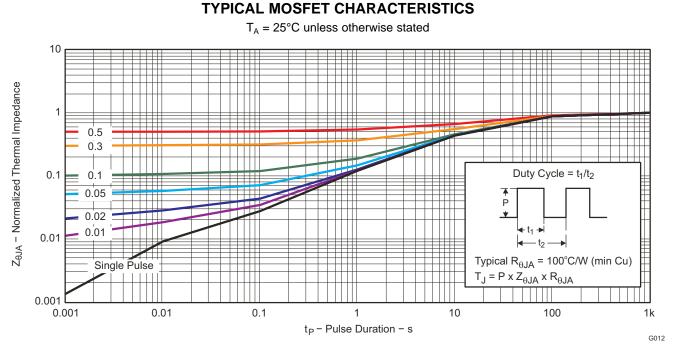
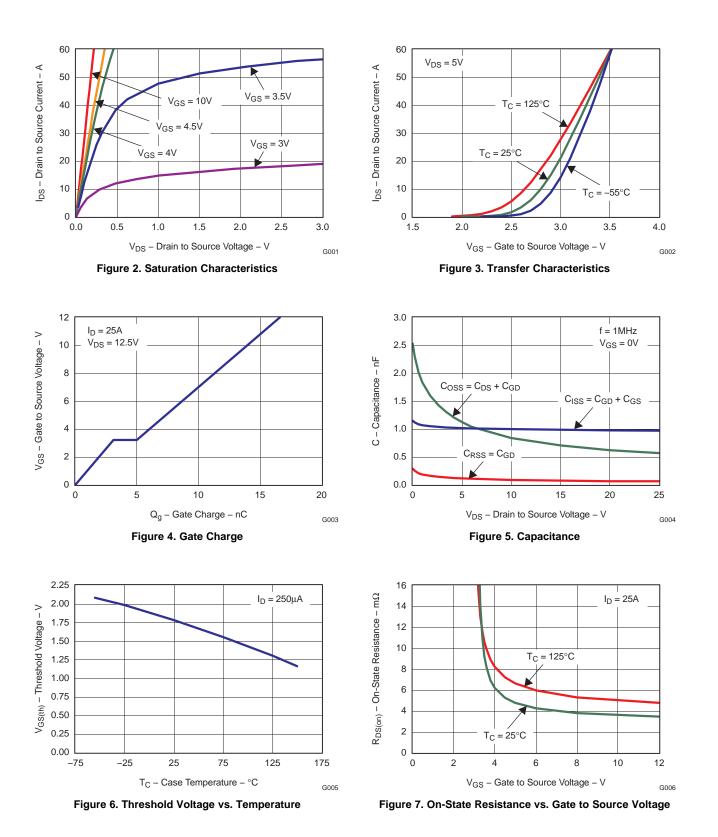


Figure 1. Transient Thermal Impedance



$T_A = 25^{\circ}C$ unless otherwise stated





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TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^{\circ}C$ unless otherwise stated

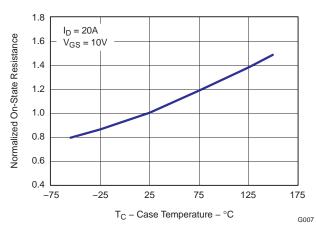
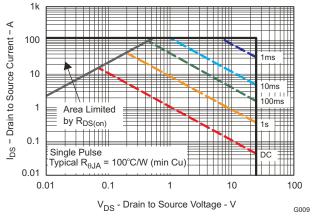
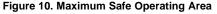


Figure 8. Normalized On-State Resistance vs. Temperature





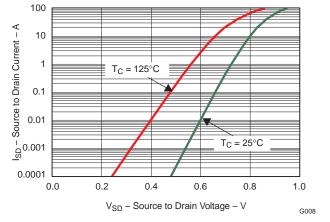


Figure 9. Typical Diode Forward Voltage

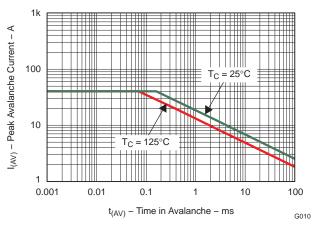


Figure 11. Single Pulse Unclamped Inductive Switching

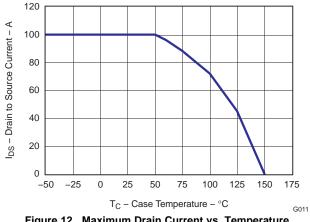


Figure 12. Maximum Drain Current vs. Temperature

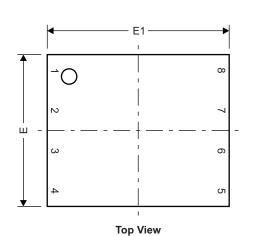
TEXAS INSTRUMENTS

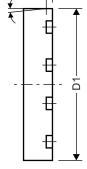
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MECHANICAL DATA

- c1

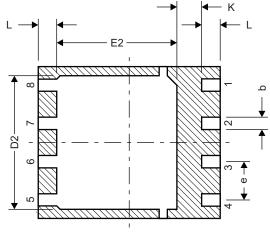
Q5 Package Dimensions



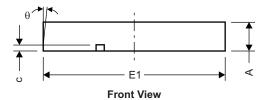


Side View

θ



Bottom View



M0140-01

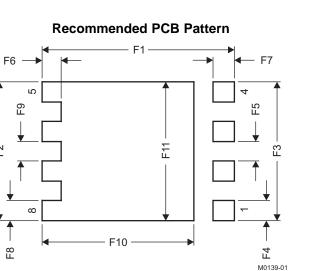
DIM	MILLIM	ETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
С	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
е	1.27 typ		0.0)50
L	0.510	0.710	0.020	0.028
θ	0.00	-	-	-



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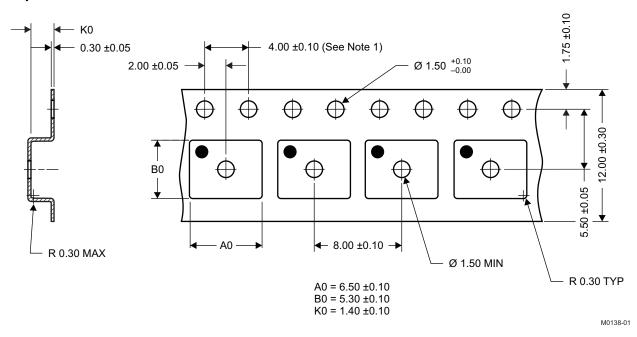
F2



DIM	MILLIM	ETERS	INC	HES
DIN	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

Q5 Tape and Reel Information



Notes:

- 1. 10-sprocket hole-pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- 3. Material: black static-dissipative polystyrene
- 4. All dimensions are in mm, unless otherwise specified.
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- 6. MSL1 260°C (IR and convection) PbF reflow compatible

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Package Marking Information

Location		_	^
1st Line	8 5	5	8
CSD = Fixed Characters			
NNNNN = Product Code			
2nd Line (Date Code)	CSDNNNNN		
YY = Last 2 digits of the Year	YYWWC		
WW = 2-digit Work Week			
C = Country of Origin	LLLLL		
> Philippines = P			
> Taiwan = T			
> China = C			
3rd LineLLLLL= Last 5 digits of the Wafer Lot #	1 4	4	1
	Pin 1 Identifier		

M0141-01

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Pa	ackage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD16408Q5	ACTIVE	SON	DQH	8	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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