

CSD13380F3 12-V N-Channel FemtoFET™ MOSFET

1 Features

- Low On Resistance
- Ultra-Low Q_g and Q_{gd}
- High Operating Drain Current
- Ultra-Small Footprint
 - 0.73 mm × 0.64 mm
- Low Profile
 - 0.35-mm Max Height
- Integrated ESD Protection Diode
 - Rated > 3-kV HBM
 - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

3 Description

This 63-m Ω , 12-V N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.

Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	0.91		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.15		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 1.8\text{ V}$	96	m Ω
		$V_{GS} = 2.5\text{ V}$	73	
		$V_{GS} = 4.5\text{ V}$	63	
$V_{GS(th)}$	Threshold Voltage	0.85		V

Device Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD13380F3	3000	7-Inch Reel	Femto 0.73 mm × 0.64 mm Land Grid Array (LGA)	Tape and Reel
CSD13380F3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

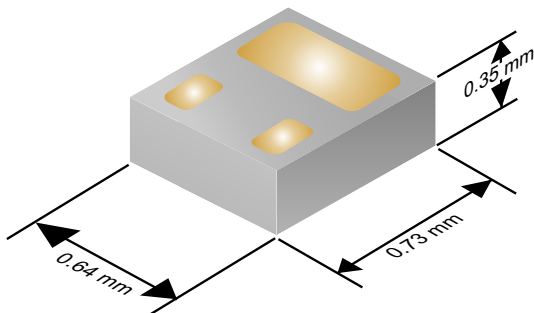
$T_A = 25^\circ\text{C}$ (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	8	V
I_D	Continuous Drain Current ⁽¹⁾	3.6	A
	Continuous Drain Current ⁽²⁾	2.1	
I_{DM}	Pulsed Drain Current ⁽²⁾⁽³⁾	13.5	A
P_D	Power Dissipation ⁽¹⁾	1.4	W
	Power Dissipation ⁽²⁾	0.5	
$V_{(ESD)}$	Human-Body Model (HBM)	3	kV
	Charged-Device Model (CDM)	2	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

(1) Max Cu, typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

(2) Min Cu, typical $R_{\theta JA} = 255^\circ\text{C/W}$.

(3) Pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$.

Typical Part Dimensions



Top View

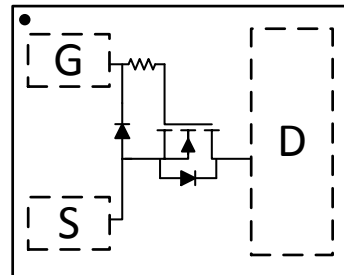


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4 Revision History

DATE	REVISION	NOTES
October 2016	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	12			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 9.6\text{ V}$			50	nA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 8\text{ V}$			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.55	0.85	1.30	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 1.8\text{ V}, I_{DS} = 0.1\text{ A}$		96	135	m Ω
		$V_{GS} = 2.5\text{ V}, I_{DS} = 0.4\text{ A}$		73	92	
		$V_{GS} = 4.5\text{ V}, I_{DS} = 0.4\text{ A}$		63	76	
g_{fs}	Transconductance	$V_{DS} = 1.2\text{ V}, I_{DS} = 0.4\text{ A}$		4.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 6\text{ V},$ $f = 1\text{ MHz}$		120	156	pF
C_{oss}	Output capacitance			81	105	pF
C_{rss}	Reverse transfer capacitance			9.6	12.5	pF
R_G	Series gate resistance			16		Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 6\text{ V}, I_{DS} = 0.4\text{ A}$		0.91	1.2	nC
Q_{gd}	Gate charge gate-to-drain			0.15		nC
Q_{gs}	Gate charge gate-to-source			0.19		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.15		nC
Q_{oss}	Output charge	$V_{DS} = 6\text{ V}, V_{GS} = 0\text{ V}$		0.81		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 6\text{ V}, V_{GS} = 4.5\text{ V},$ $I_{DS} = 0.4\text{ A}, R_G = 2\ \Omega$		4		ns
t_r	Rise time			4		ns
$t_{d(off)}$	Turnoff delay time			11		ns
t_f	Fall time			3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 0.4\text{ A}, V_{GS} = 0\text{ V}$		0.71	1	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 6\text{ V}, I_F = 0.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		2.1		nC
t_{rr}	Reverse recovery time			8		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾		90		$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance ⁽²⁾		255		

(1) Device mounted on FR4 material with 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

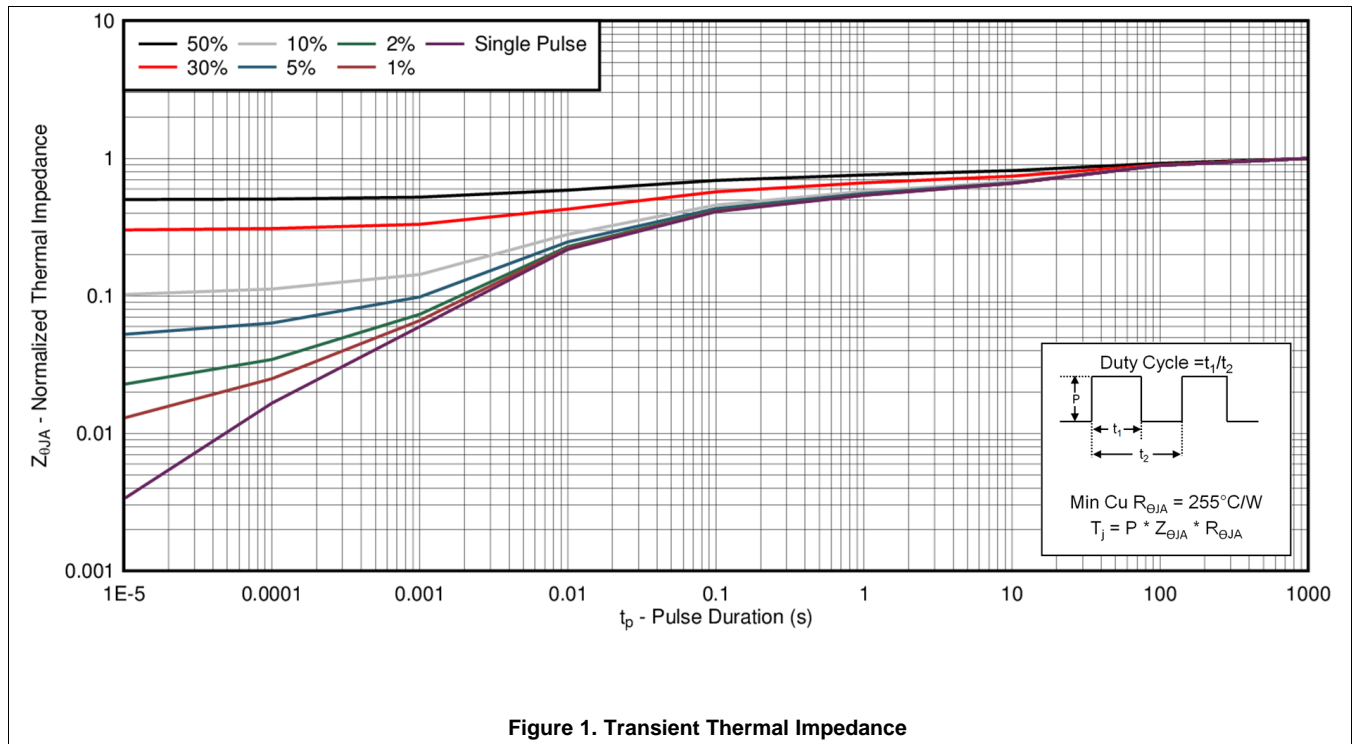


Figure 1. Transient Thermal Impedance

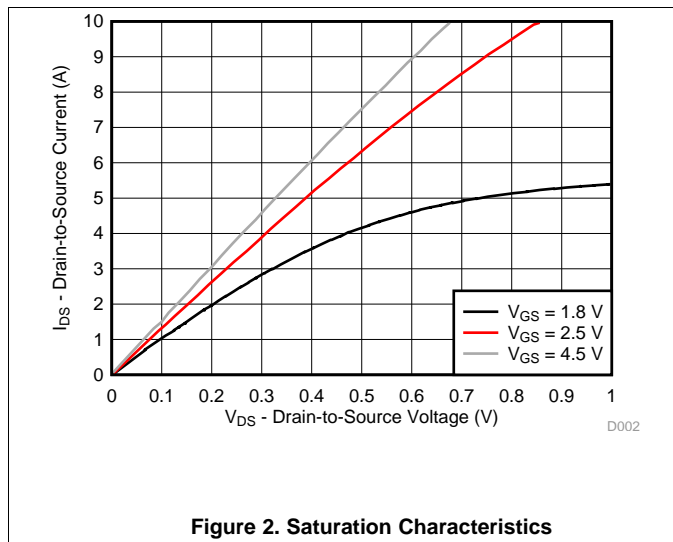


Figure 2. Saturation Characteristics

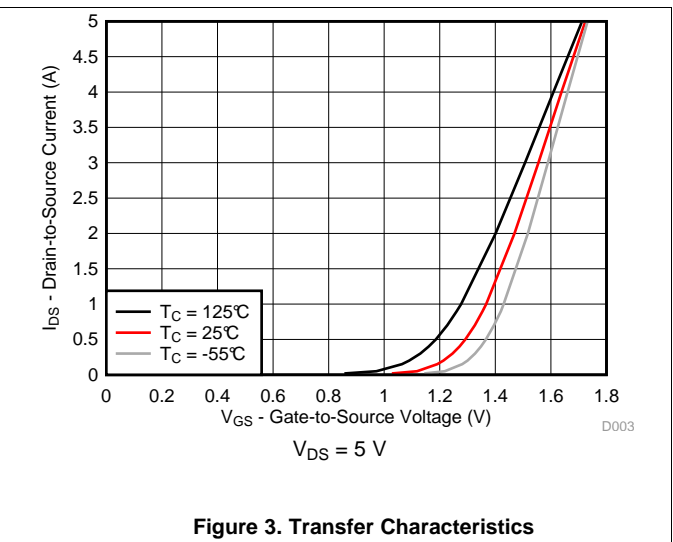
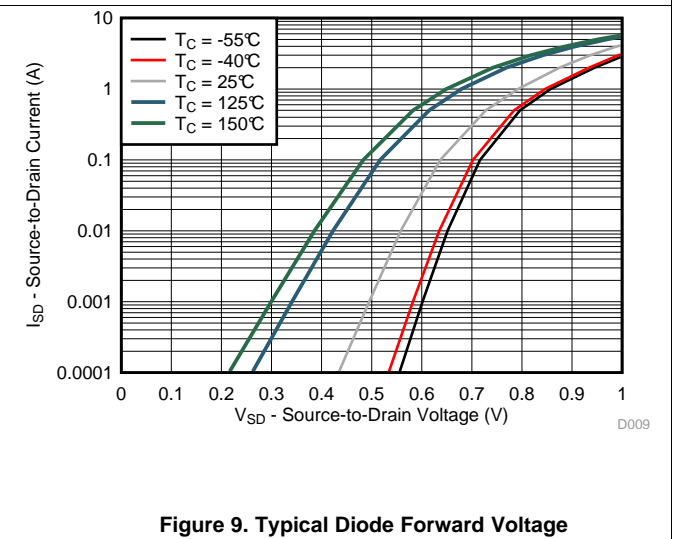
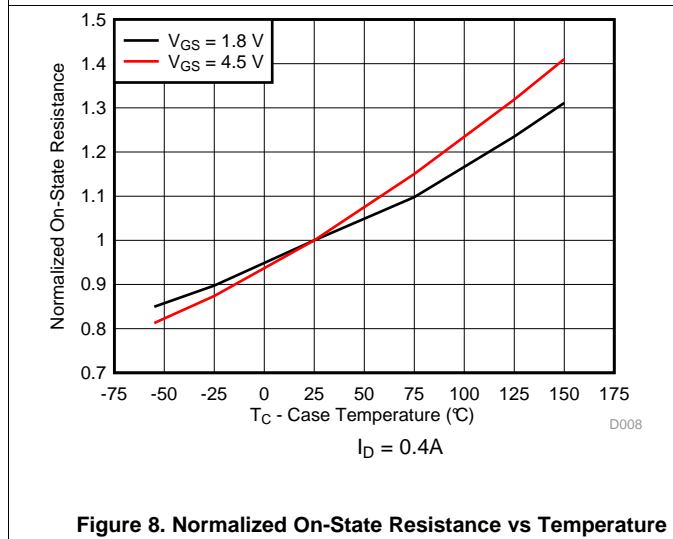
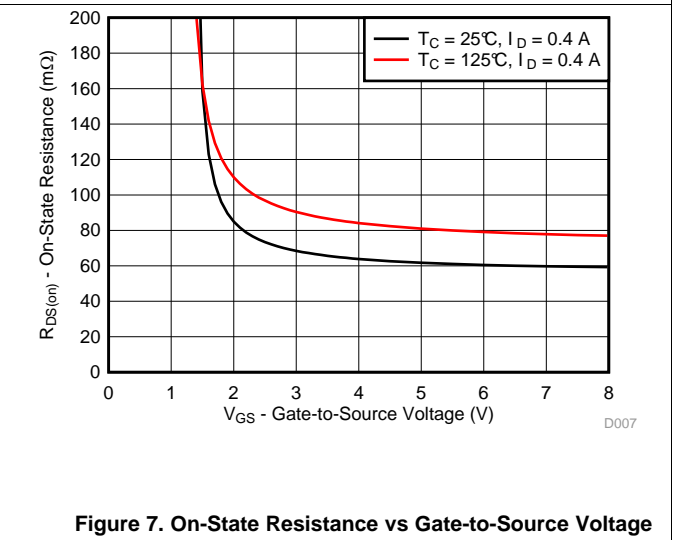
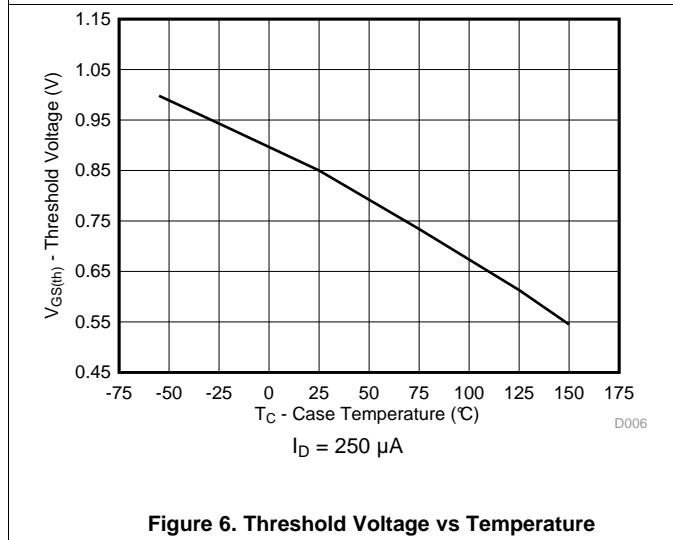
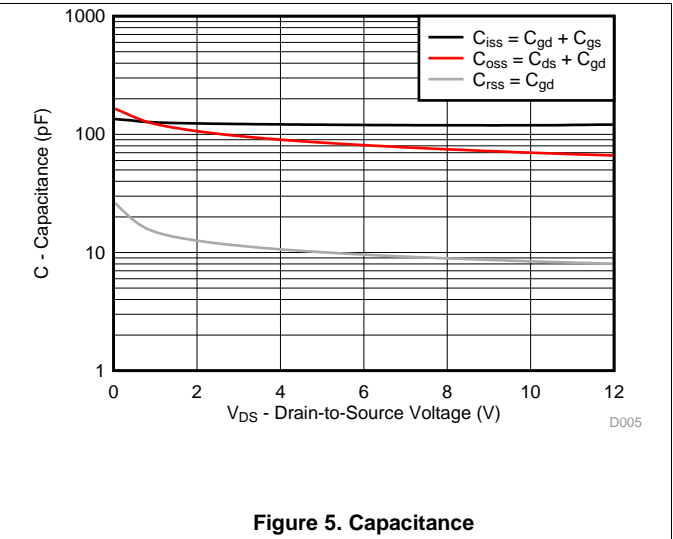
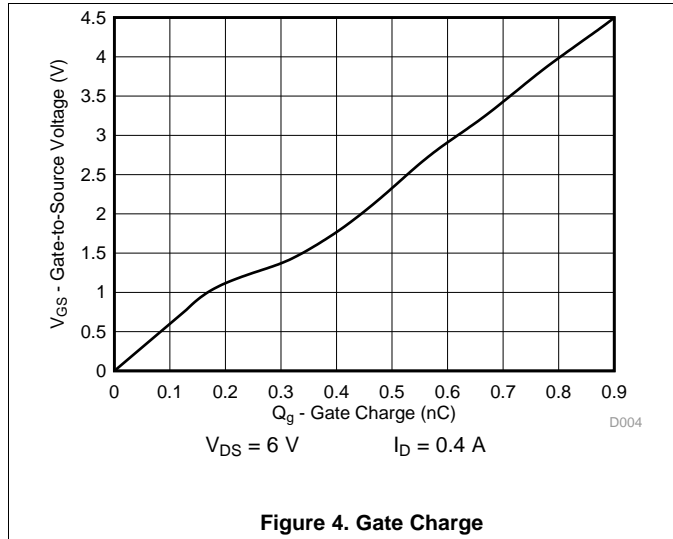


Figure 3. Transfer Characteristics

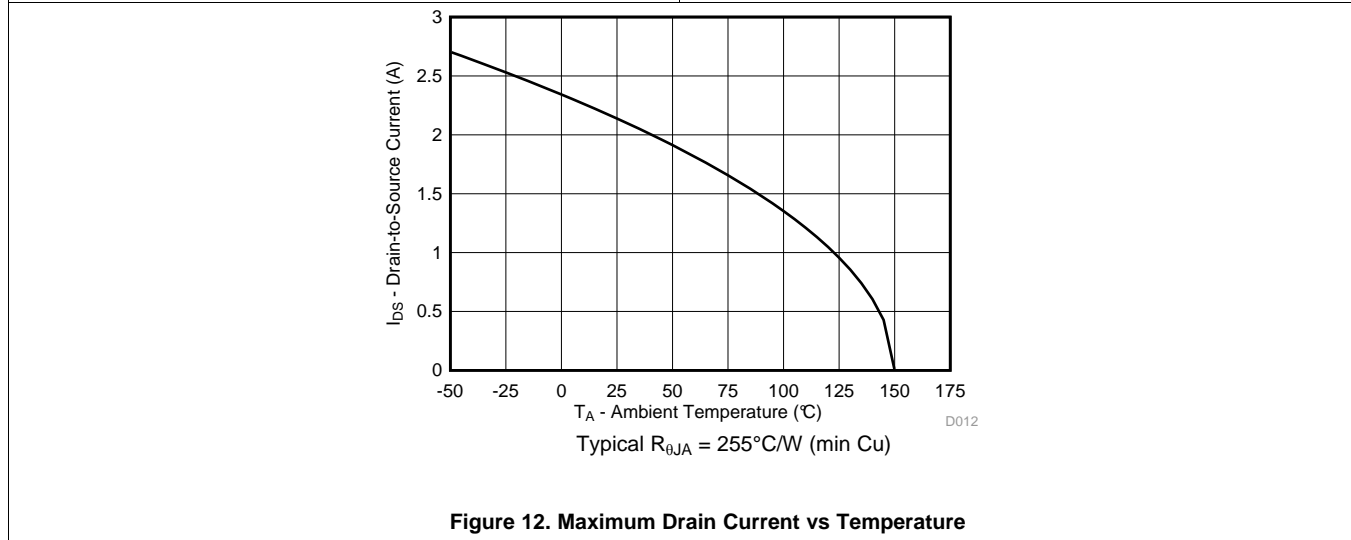
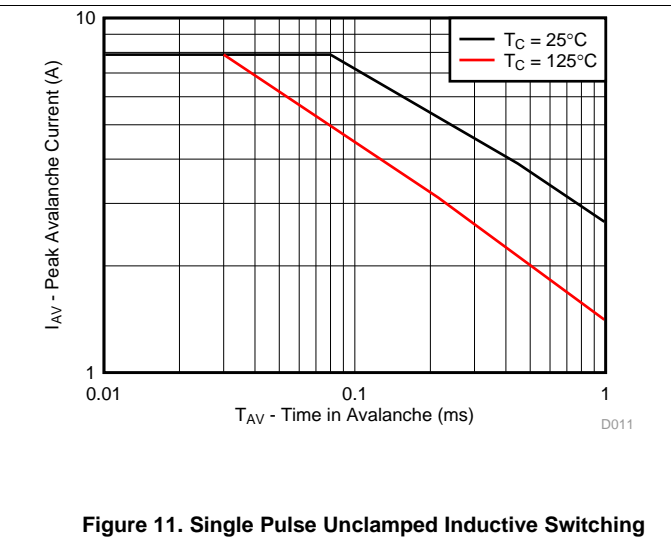
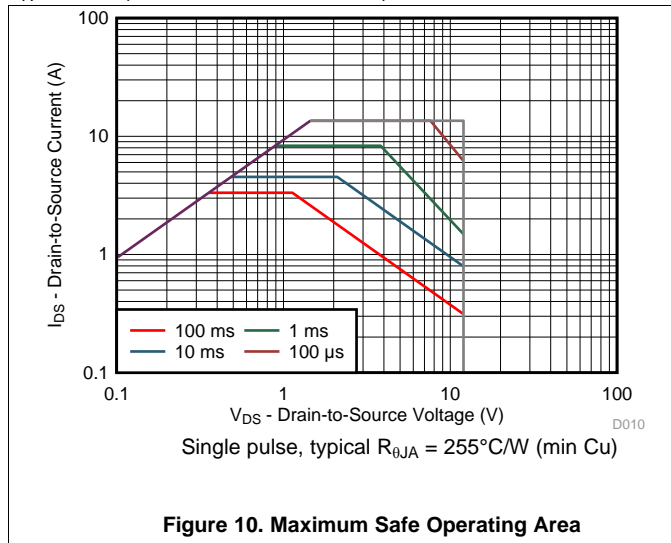
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)



6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

FemtoFET, E2E are trademarks of Texas Instruments.
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6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

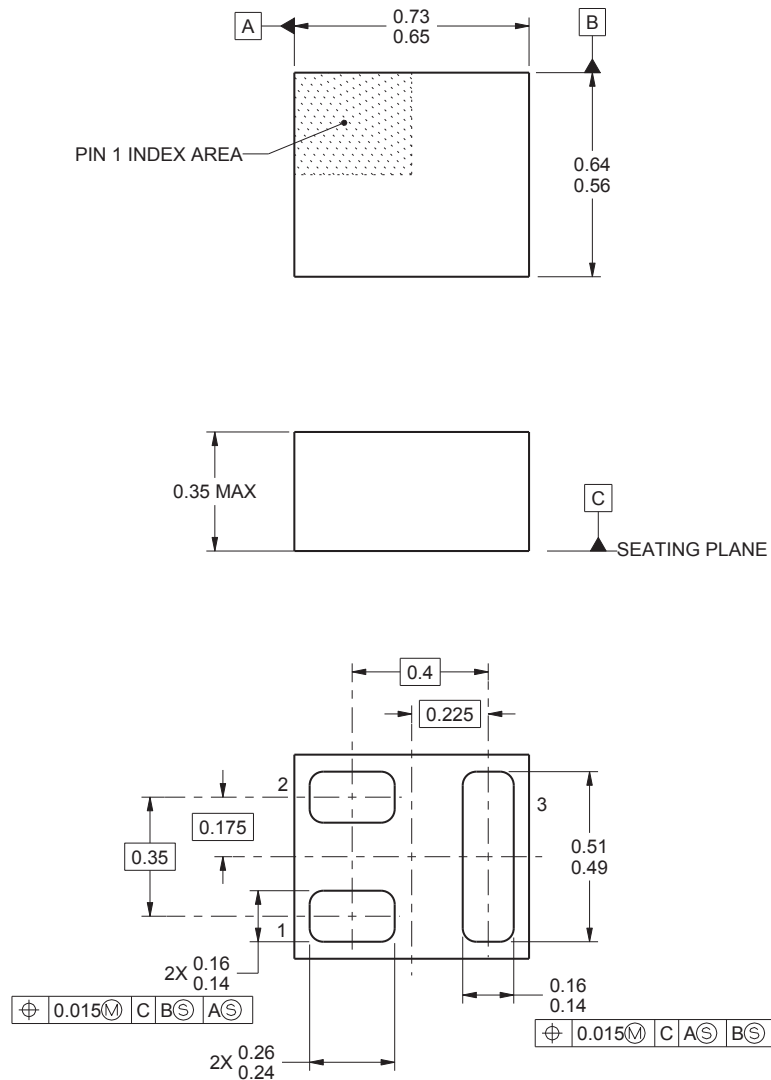
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

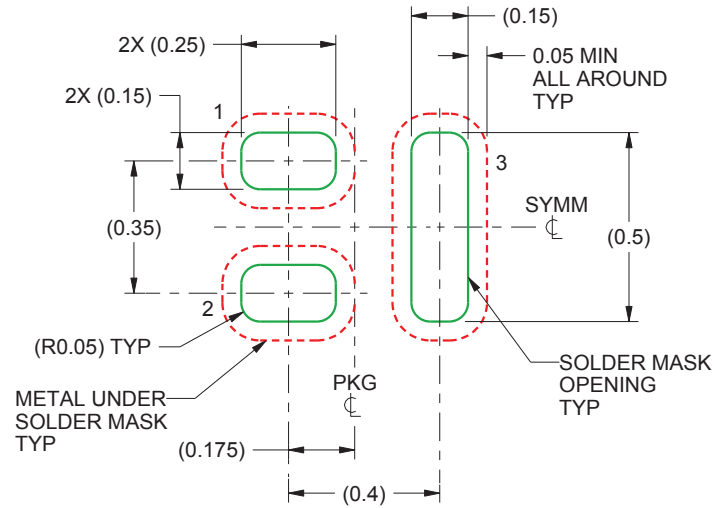


- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

Table 1. Pin Configuration

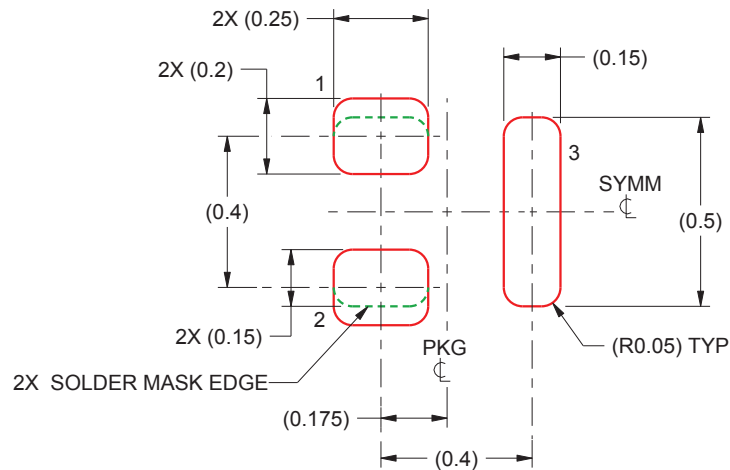
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13380F3	ACTIVE	PICOSTAR	YJM	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	D	Samples
CSD13380F3T	ACTIVE	PICOSTAR	YJM	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13380F3	PICOST AR	YJM	3	3000	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0

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