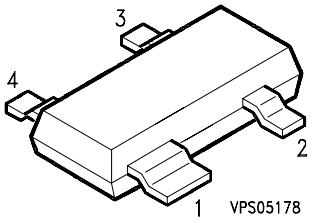
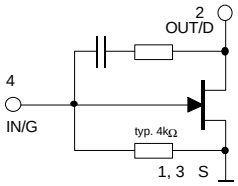
D a t a s h e e t

- ***** Single-stage monolithic microwave IC (MMIC-amplifier)
- ***** Cascadable 50 Ω gain block
- ***** Application range: 100 MHz to 3 GHz
- ***** IP3 30 dBm typ. @ 1.8 GHz
- ***** Gain 8.5 dB typ. @ 1.8 GHz
- * Low noise figure: 3.0 dB typ @ 1.8 GHz
- * Gain control dynamic range 20 dB



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (tape and reel)	Circuit diagram Pin Configuration	Package 1)
CGY 50	G2	Q68000-A8370		SOT-143

Maximum ratings	**Symbol**	**Value**	**Unit**
Drain-voltage	V_D	5.5	V
Peak drain-voltage	V_{DP}	7.5	V
Current control gate voltage	V_G	-3 ... 0	V
Drain-gate voltage	V_{DG}	7.5	V
Input power [2]	P_{IN}	16	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature range	T_{stg}	-40...+150	°C
Total power dissipation ($TS \leq 82°C$) [3]	P_{tot}	400	mW
Thermal resistance			
Channel-soldering point [3]	R_{thChS}	<170	K/W

Note: exceeding any of the max. ratings may cause permanent damage to the device. Appropriate handling is required to protect the electrostatic sensitive MMIC against degradation due to excess current spikes. Proper ground connection of leads 1 and 3 (with minimum inductance) is required to achieve the guaranteed RF performance, stable operating conditions and adequate tuning.

1) Dimensions see chapter Package Outlines
2) See application circuit.
3) T_S is measured on the source 1 lead at the soldering point to the PCB.

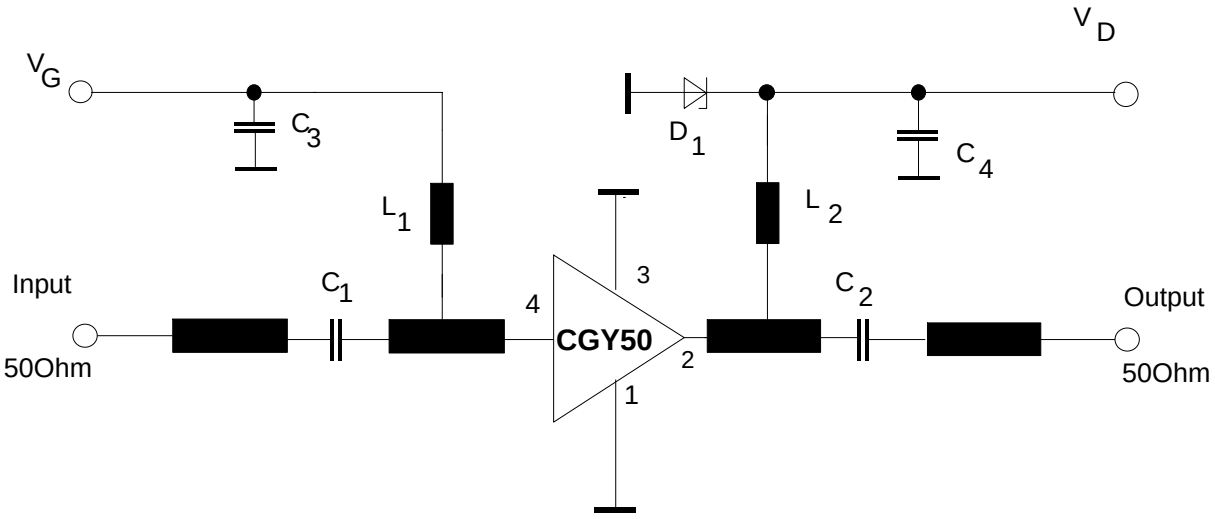
Electrical characteristics

T_A = 25 °C, V_G = 0 V, V_D = 4.5 V, $R_S = R_L$ = 50 Ω, unless otherwise specified

(for application circuit see next page)

Characteristics	Symbol	min	typ	max	Unit
Drain current	I_D	-	60	75	mA
Power gain f = 200 MHz f = 1800 MHz	G	 - 7.5	 10.0 8.5	 - -	dB
Gain flatness f = 200 to 1000 MHz f = 800 to 1800 MHz	ΔG	 - -	 0.4 1.1	 - 2	dB
Noise figure f = 200 to 1800 MHz	F	-	3.0	4.0	dB
Input return loss f = 200 to 1800 MHz	RL_{IN}	9.5	12	-	dB
Output return loss f = 200 to 1800 MHz	RL_{OUT}	9.5	12	-	dB
Third order intercept point Two tone intermodulation test f_1 = 806 MHz, f_2 = 810 MHz P_0 = 10 dBm (both carriers)	$IP3$	29	31	-	dBm
1dB gain compression f = 200 to 1800 MHz	$P_{1\,dB}$	-	16	-	dBm
Gain control dynamic range f = 200 to 1800 MHz	ΔG	-	20	-	dB

Application Circuit (f = 800 to 1800 MHz)

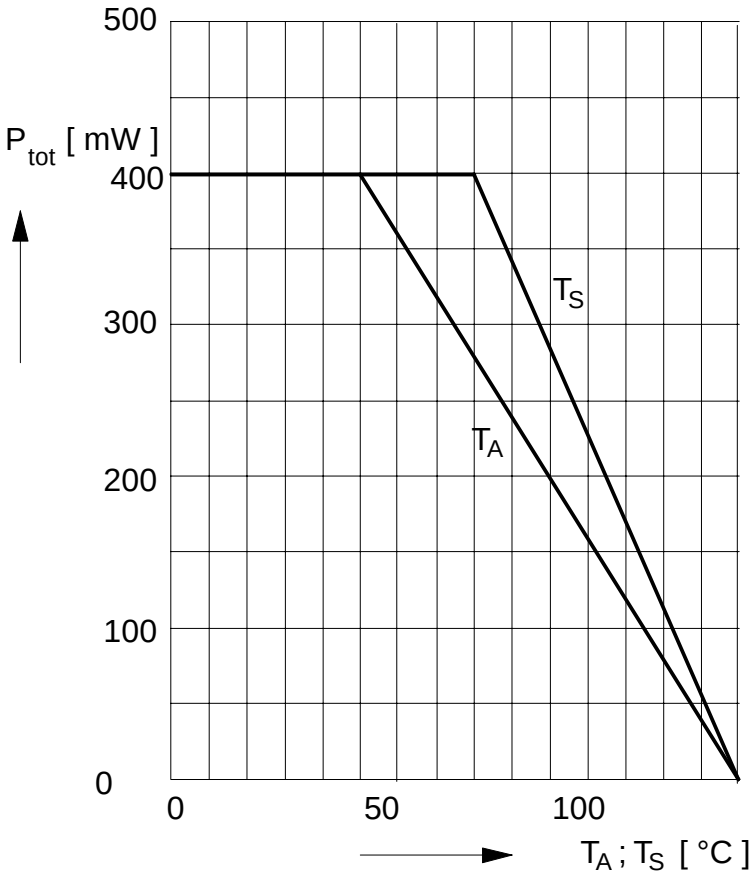


Legend of components

C_1 , C_2 C_3 , C_4	Chip capacitors 100 pF Chip capacitors 1 nF
L_1 , L_2	Discrete inductor 1 µH or printed microstrip inductor
D_1	Z diode 5.6 V (type BZW 22 C5 V 6)

Note: Operating conditions for $P_{IN, max}$: $R_G = R_L = 50\ \Omega$, $C_{1, max} = 220$ pF, $V_D = 4.5$ V, V_G current limited < 2 mA.

Total Power Dissipation $P_{tot} = f(T_s;T_A)$



Typical Common Source S-Parameters

V_G = 0V V_D = 4.5 V Z_0 = 50 Ω

f	S11		S21		S12		S22	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
0.2	0.25	-31	3.30	164	0.14	5.0	0.05	-144
0.4	0.27	-34	3.20	158	0.14	0.0	0.05	-133
0.6	0.21	-44	3.17	150	0.13	-2.0	0.08	105
0.8	0.20	-54	3.09	142	0.13	-3.0	0.10	91
1.0	0.19	-65	3.00	134	0.13	-4.0	0.12	81
1.2	0.18	-77	2.90	126	0.13	-5.0	0.14	74
1.4	0.18	-93	2.81	118	0.13	-5.0	0.16	68
1.6	0.17	-103	2.70	111	0.13	-6.0	0.17	62
1.8	0.17	-119	2.60	103	0.13	-5.0	0.18	56
2.0	0.17	-130	2.50	96	0.12	-5.0	0.19	51
2.2	0.18	-141	2.42	94	0.12	-4.0	0.20	46
2.4	0.18	-152	2.33	83	0.12	-4.0	0.21	42
2.6	0.19	-163	2.24	77	0.12	-3.0	0.21	39
2.8	0.20	-172	2.16	71	0.13	-3.0	0.21	36
3.0	0.21	179	2.07	65	0.13	-2.0	0.21	33
3.2	0.22	172	2.01	60	0.13	-2.0	0.21	30
3.4	0.23	162	1.94	54	0.13	-2.0	0.21	29
3.6	0.24	153	1.87	49	0.14	-1.0	0.21	28
3.8	0.26	148	1.81	43	0.14	-1.0	0.21	27
4.0	0.28	142	1.75	38	0.15	-1.0	0.20	27