

Programmable 4-PLL VCXO Clock Synthesizer with 1.8V, 2.5V and 3.3V LVCMOS Outputs

Check for Samples: [CDCE949](#), [CDCEL949](#)

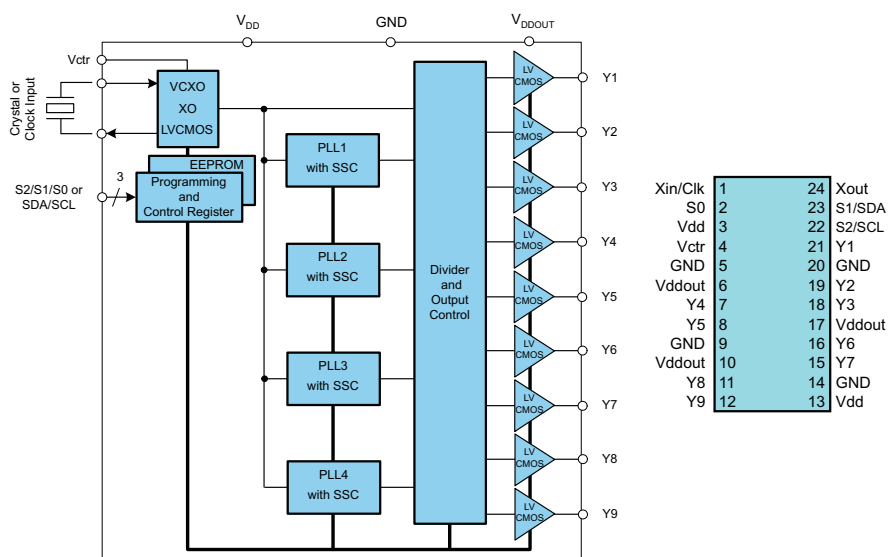
FEATURES

- Member of Programmable Clock Generator Family
 - CDCE913/CDCEL913: 1 PLLs, 3 Outputs
 - CDCE925/CDCEL925: 2 PLLs, 5 Outputs
 - CDCE937/CDCEL937: 3 PLLs, 7 Outputs
 - CDCE949/CDCEL949: 4 PLLs, 9 Outputs
- In-System Programmability and EEPROM
 - Serial Programmable Volatile Register
 - Non-Volatile EEPROM to Store Customer Settings
- Highly Flexible Clock Driver
 - Three User-Definable Control Inputs [S0/S1/S2] e.g. SSC-Selection, Frequency Switching, Output Enable or Power Down
 - Generates Highly-Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Generates Common Clock Frequencies Used with TI DaVinci™, OMAP™, DSPs
 - Bluetooth™, WLAN, Ethernet and GPS
 - Programmable SSC Modulation
 - Enables 0-PPM Clock Generation
- Selectable Output Frequency up to 230 MHz

- Flexible Input Clocking Concept
 - External Crystal: 8 to 32 MHz
 - On-Chip VCXO: Pull-Range ±150 ppm
 - Single-Ended LVCMOS up to 160 MHz
- Low-Noise PLL Core
 - Integrated PLL Loop Filter Components
 - Very Low Period Jitter (typ 60 ps)
- Separate Output Supply Pins
 - CDCE949: 3.3 V and 2.5 V
 - CDCEL949: 1.8 V
- 1.8 V Device Power Supply
- Wide Temperature Range –40° C to 85° C
- Packaged in TSSOP
- Development and Programming Kit for Ease PLL Design and Programming (TI-Pro Clock)

APPLICATIONS

- D-TV, HD-TV, STB, IP-STB, DVD-Player, DVD-Recorder, Printer
- General Purpose Frequency Synthesizing



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION

The CDCE949 and CDCEL949 are modular PLL-based low cost, high-performance, programmable clock synthesizers, multipliers and dividers. They generate up to 9 output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to four independent configurable PLLs.

The CDCx949 has separate output supply pins, V_{DDOUT} , 1.8 V for the CDCEL949, and 2.5 V to 3.3 V for CDCE949.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, an on-chip VCXO is selectable, allowing synchronization of the output frequency to an external control signal, that is, a PWM signal.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, BlueTooth™, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency, such as 27 MHz.

All PLLs support SSC (Spread-Spectrum Clocking). SSC can be Center-Spread or Down-Spread clocking. This is a common technique to reduce electro-magnetic interference (EMI).

Based on the PLL frequency and the divider settings, the internal loop-filter components are automatically adjusted to achieve high stability, and to optimize the jitter-transfer characteristics of each PLL.

The device supports non-volatile EEPROM programming for easy customization of the device to the application. It is preset to a factory-default configuration (see the [Default Device Configuration](#) section). It can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection, changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for the output-disable function.

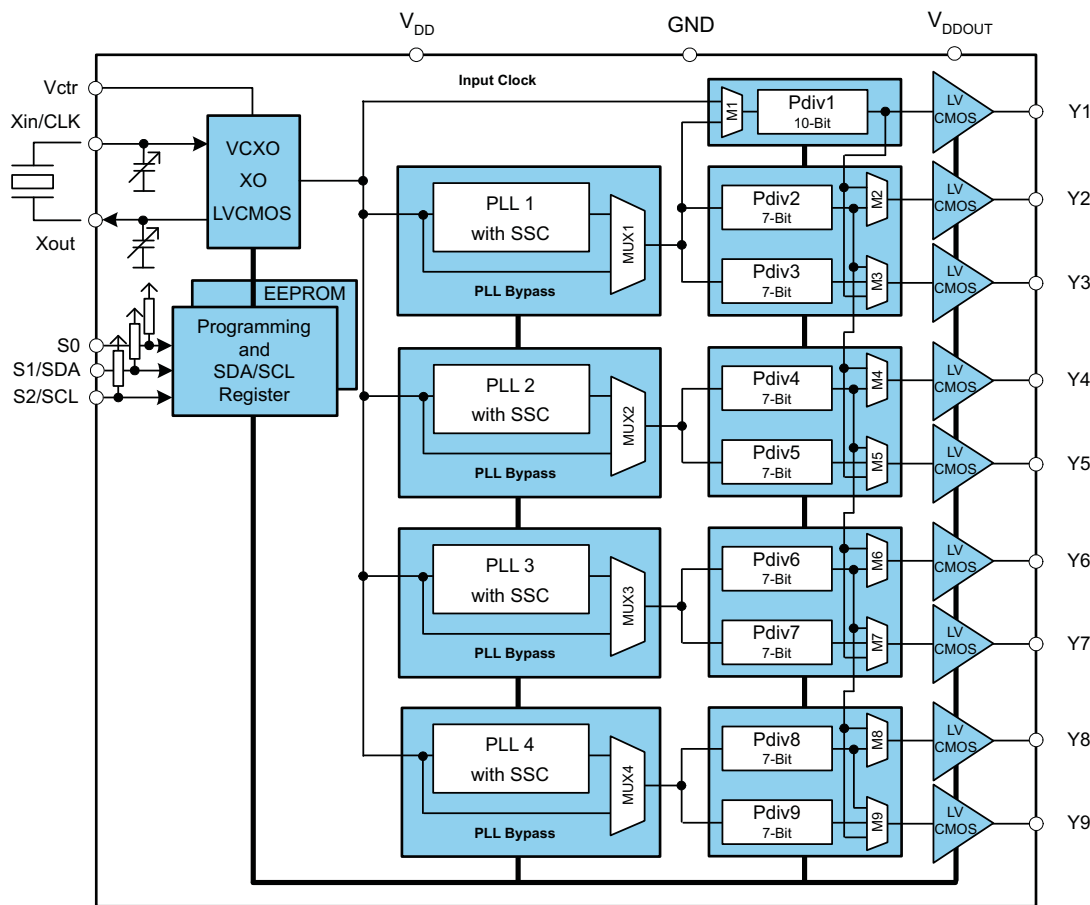
The CDCx949 operates in a 1.8 V environment. It operates within a temperature range of -40°C to 85°C .

DEVICE INFORMATION

TERMINAL FUNCTIONS

| TERMINAL | | I/O | |
|---------------|-------------------------------------|---------|---|
| NAME | NO. (TSSOP24) | | |
| Y1, Y2, ...Y9 | 21, 19, 18, 7, 8, 16, 15, 11, 12 | O | LVCMOS outputs |
| Xin/CLK | 1 | I | Crystal oscillator input or LVCMOS clock input (selectable via SDA/SCL bus) |
| Xout | 24 | O | Crystal oscillator output (leave open or pull up when not used) |
| V_{Ctrl} | 4 | I | VCXO control voltage (leave open or pull up when not used) |
| V_{DD} | 3, 13 | Power | 1.8V power supply for the device |
| V_{DDOUT} | 6, 10, 17 | Power | CDCEL949: 1.8 V supply for all outputs |
| | | | CDCE949: 3.3 V or 2.5 V supply for all outputs |
| GND | 5, 9, 14, 20 | Ground | Ground |
| S0 | 2 | I | User-programmable control input S0; LVCMOS inputs; internal pull-up 500 k Ω |
| SDA / S1 | 23 | I/O / I | SDA: Bi-directional serial data input/output (default configuration), LVCMOS; internal pull-up 500 k Ω ; or S1: User-programmable control input; LVCMOS inputs; internal pull-up 500 k Ω |
| SCL / S2 | 22 | I | SCL: Serial clock input (default configuration), LVCMOS; internal pull-up 500 k Ω ; or S2: User-programmable control input; LVCMOS inputs; internal pull-up 500 k Ω |

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | VALUE | UNIT |
|------------------|---|----------------------------------|------|
| V _{DD} | Supply voltage range | -0.5 to 2.5 | V |
| V _I | Input voltage range ⁽²⁾ ⁽³⁾ | -0.5 to V _{DD} + 0.5 | V |
| V _O | Output voltage range ⁽²⁾ | -0.5 to V _{DDOUT} + 0.5 | V |
| I _I | Input current (V _I < 0, V _I > V _{DD}) | 20 | mA |
| I _O | Continuous output current | 50 | mA |
| T _{stg} | Storage temperature range | -65 to 150 | °C |
| T _J | Maximum junction temperature | 125 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) SDA and SCL can go up to 3.6V as stated in the *Recommended Operating Conditions* table.

THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE⁽¹⁾

| PARAMETER | | AIRFLOW (lfm) | TSSOP24 °C/W |
|------------------|--|------------------|-----------------|
| T _{JA} | Thermal Resistance Junction to Ambient | 0 | 91 |
| | | 150 | 75 |
| | | 200 | 74 |
| | | 250 | 73 |
| | | 500 | 65 |
| T _{JC} | Thermal Resistance Junction to Case | — | 27 |
| T _{JB} | Thermal Resistance Junction to Board | — | 52 |
| R _{θJT} | Thermal Resistance Junction to Top | — | 0.5 |
| R _{θJB} | Thermal Resistance Junction to Bottom | — | 50 |

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|-----------------------------------|--------------------------------------|--|-----------------------|-----------------------|-----------------------|------|
| V _{DD} | Device supply voltage | | 1.7 | 1.8 | 1.9 | V |
| V _{DD(OUT)} | Output Yx supply voltage | CDCE949 | 2.3 | | 3.6 | V |
| | | CDCEL949 | 1.7 | | 1.9 | |
| V _{IL} | Low level input voltage LVCMOS | | | | 0.3 × V _{DD} | V |
| V _{IH} | High level input voltage LVCMOS | | 0.7 × V _{DD} | | | V |
| V _{I(thresh)} | Input voltage threshold LVCMOS | | | 0.5 × V _{DD} | | V |
| V _{IS} | Input voltage range S0 | | 0 | | 1.9 | V |
| | Input voltage range S1, S2, SDA, SCL | V _{Ithresh} = 0.5 V _{DD} | 0 | | 3.6 | |
| V _{ICLK} | Input voltage range CLK | | 0 | | 1.9 | V |
| I _{OH} / I _{OL} | Output current | V _{DDout} = 3.3 V | | | ±12 | mA |
| | | V _{DDout} = 2.5 V | | | ±10 | mA |
| | | V _{DDout} = 1.8 V | | | ±8 | mA |
| C _L | Output load LVCMOS | | | | 10 | pF |
| T _A | Operating free-air temperature | | −40 | | 85 | °C |

RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS⁽¹⁾

| | | MIN | NOM | MAX | UNIT |
|--------------------------------|--|------|------|-----------------|------|
| f _{Xtal} | Crystal Input frequency range (fundamental mode) | 8 | 27 | 32 | MHz |
| ESR | Effective series resistance | | | 100 | Ω |
| f _{PR} | Pulling range (0 V ≤ V _{Ctrl} ≤ 1.8 V) ⁽²⁾ | ±120 | ±150 | | ppm |
| V _(Ctrl) | Frequency control voltage | 0 | | V _{DD} | V |
| C ₀ /C ₁ | Pullability ratio | | | 220 | |
| C _L | On-chip load capacitance at Xin and Xout | 0 | | 20 | pF |

(1) For more information about VCXO configuration and crystal recommendation see application report [SCAA085](#).

(2) Pulling range depends on crystal type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ±120 ppm applies for crystal listed in the application report [SCAA085](#).

EEPROM SPECIFICATION

| | | MIN | TYP | MAX | UNIT |
|-------|------------------------------------|------|-----|-----|--------|
| EEcyc | EEcyc programming cycles of EEPROM | 1000 | | | cycles |
| EEret | EEret data retention | 10 | | | years |

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free-air temperature

| CLK_IN Requirements | | | MIN | NOM | MAX | UNIT |
|---------------------|--|-----------------|-----|-----|-----|------|
| $f_{(CLK)}$ | LVCMOS clock input frequency | PLL Bypass Mode | 0 | | 160 | MHz |
| | | PLL Mode | 8 | | 160 | |
| t_r / t_f | Rise and fall time CLK signal (20% to 80%) | | | | 3 | ns |
| $duty_{CLK}$ | Duty cycle CLK at $V_{DD} / 2$ | | 40% | | 60% | |

| SDA/SCL TIMING REQUIREMENTS (see Figure 12) | | STANDARD MODE | | FAST MODE | | UNIT |
|---|--|---------------|------|-----------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{su}(START)$ | START setup time (SCL high before SDA low) | 4.7 | | 0.6 | | μ s |
| $t_h(START)$ | START hold time (SCL low after SDA low) | 4 | | 0.6 | | μ s |
| $t_w(SCLL)$ | SCL low-pulse duration | 4.7 | | 1.3 | | μ s |
| $t_w(SCLH)$ | SCL high-pulse duration | 4 | | 0.6 | | μ s |
| $t_h(SDA)$ | SDA hold time (SDA valid after SCL low) | 0 | 3.45 | 0 | 0.9 | μ s |
| $t_{su}(SDA)$ | SDA setup time | 250 | | 100 | | ns |
| t_r | SCL/SDA input rise time | | 1000 | | 300 | ns |
| t_f | SCL/SDA input fall time | | 300 | | 300 | ns |
| $t_{su}(STOP)$ | STOP setup time | 4.0 | | 0.6 | | μ s |
| t_{BUF} | Bus free time between a STOP and START condition | 4.7 | | 1.3 | | μ s |

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------|--|---|---------------------------------|--------------------|---------|---------|
| OVERALL PARAMETER | | | | | | |
| I_{DD} | Supply current (see Figure 3) | All outputs off, $f_{CLK} = 27$ MHz, $f_{VCO} = 135$ MHz; | All PLLs on | | 38 | mA |
| | | | Per PLL | | 9 | |
| $I_{DD(OUT)}$ | Supply current (see Figure 4 and Figure 5) | No load, all outputs on, $f_{out} = 27$ MHz | CDCE949 $V_{DDOUT} = 3.3$ V | | 4 | mA |
| | | | CDCEL949 $V_{DDOUT} = 1.8$ V | | 2 | |
| $I_{DD(PD)}$ | Power down current. Every circuit powered down except SDA/SCL | $f_{IN} = 0$ MHz, $V_{DD} = 1.9$ V | | 50 | | μ A |
| $V_{(PUC)}$ | Supply voltage V_{DD} threshold for power up control circuit | | 0.85 | | 1.45 | V |
| f_{VCO} | VCO frequency range of PLL | | 80 | | 230 | MHz |
| f_{OUT} | LVCMOS output frequency | | 230 | | | MHz |
| LVCMOS PARAMETER | | | | | | |
| V_{IK} | LVCMOS input voltage | $V_{DD} = 1.7$ V; $I_I = -18$ mA | | | -1.2 | V |
| I_I | LVCMOS input current | $V_I = 0$ V or V_{DD} ; $V_{DD} = 1.9$ V | | | ± 5 | μ A |
| I_{IH} | LVCMOS input current for S0/S1/S2 | $V_I = V_{DD}$; $V_{DD} = 1.9$ V | | | 5 | μ A |
| I_{IL} | LVCMOS input current for S0/S1/S2 | $V_I = 0$ V; $V_{DD} = 1.9$ V | | | -4 | μ A |
| C_I | Input capacitance at Xin/Clk | $V_{ICLK} = 0$ V or V_{DD} | | | 6 | pF |
| | Input capacitance at Xout | $V_{IXout} = 0$ V or V_{DD} | | | 2 | |
| | Input capacitance at S0/S1/S2 | $V_{IS} = 0$ V or V_{DD} | | | 3 | |

(1) All typical values are at respective nominal V_{DD} .

DEVICE CHARACTERISTICS (Continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--|---|---|-----|--------------------|-----|------|
| CDCE949 – LVCMOS PARAMETER FOR V_{DDOUT} = 3.3 V – MODE | | | | | | |
| V _{OH} | LVCMOS high-level output voltage | V _{DDOUT} = 3 V, I _{OH} = -0.1 mA | 2.9 | | | V |
| | | V _{DDOUT} = 3 V, I _{OH} = -8 mA | 2.4 | | | |
| | | V _{DDOUT} = 3 V, I _{OH} = -12 mA | 2.2 | | | |
| V _{OL} | LVCMOS low-level output voltage | V _{DDOUT} = 3 V, I _{OL} = 0.1 mA | | | 0.1 | V |
| | | V _{DDOUT} = 3 V, I _{OL} = 8 mA | | | 0.5 | |
| | | V _{DDOUT} = 3 V, I _{OL} = 12 mA | | | 0.8 | |
| t _{PLH} , t _{PHL} | Propagation delay | PLL bypass | | 3.2 | | ns |
| t _r /t _f | Rise and fall time | V _{DDOUT} = 3.3 V (20%–80%) | | 0.6 | | ns |
| t _{jit(cc)} | Cycle-to-cycle jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 60 | 90 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 120 | 170 | |
| t _{jit(per)} | Peak-to-peak period jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 70 | 100 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 130 | 180 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ | f _{OUT} = 50 MHz; Y1-to-Y3 | | | 60 | ps |
| | | f _{OUT} = 50 MHz; Y2-to-Y5 or Y6-to-Y9 | | | 160 | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz; Pdiv = 1 | 45 | | 55 | % |
| CDCE949 – LVCMOS PARAMETER FOR V_{DDOUT} = 2.5 V – MODE | | | | | | |
| V _{OH} | LVCMOS high-level output voltage | V _{DDOUT} = 2.3 V, I _{OH} = -0.1 mA | 2.2 | | | V |
| | | V _{DDOUT} = 2.3 V, I _{OH} = -6 mA | 1.7 | | | |
| | | V _{DDOUT} = 2.3 V, I _{OH} = -10 mA | 1.6 | | | |
| V _{OL} | LVCMOS low-level output voltage | V _{DDOUT} = 2.3 V, I _{OL} = 0.1 mA | | | 0.1 | V |
| | | V _{DDOUT} = 2.3 V, I _{OL} = 6 mA | | | 0.5 | |
| | | V _{DDOUT} = 2.3 V, I _{OL} = 10 mA | | | 0.7 | |
| t _{PLH} , t _{PHL} | Propagation delay | PLL bypass | | 3.4 | | ns |
| t _r /t _f | Rise and fall time | V _{DDOUT} = 2.5 V (20%–80%) | | 0.8 | | ns |
| t _{jit(cc)} | Cycle-to-cycle jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 60 | 90 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 120 | 170 | |
| t _{jit(per)} | Peak-to-peak period jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 70 | 100 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 130 | 180 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ | f _{OUT} = 50 MHz; Y1-to-Y3 | | | 60 | ps |
| | | f _{OUT} = 50 MHz; Y2-to-Y5 or Y6-to-Y9 | | | 160 | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz; Pdiv = 1 | 45 | | 55 | % |

(1) All typical values are at respective nominal V_{DD}.

(2) 10000 cycles.

(3) Jitter depends on device configuration. Data is taken under the following conditions: 1-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz, (measured at Y2), 4-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz, (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz, Y8/9 = 48 MHz.

(4) The t_{sk(o)} specification is only valid for equal loading of each bank of outputs and outputs are generated from the same divider; data sampled on rising edge (t_r).

(5) odc depends on output rise- and fall-time (t_r/t_f).

DEVICE CHARACTERISTICS (Continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|---|---|--|--------------------|---------------------|------|----|
| SAVE THIS CDCEL949 – LVCMOS PARAMETER FOR V_{DDOUT} = 1.8 V – MODE | | | | | | |
| V _{OH} | LVCMOS high-level output voltage | V _{DDOUT} = 1.7 V, I _{OH} = -0.1 mA | | 1.6 | V | |
| | | V _{DDOUT} = 1.7 V, I _{OH} = -4 mA | | 1.4 | | |
| | | V _{DDOUT} = 1.7 V, I _{OH} = -8 mA | | 1.1 | | |
| V _{OL} | LVCMOS low-level output voltage | V _{DDOUT} = 1.7 V, I _{OL} = 0.1 mA | | 0.1 | V | |
| | | V _{DDOUT} = 1.7 V, I _{OL} = 4 mA | | 0.3 | | |
| | | V _{DDOUT} = 1.7 V, I _{OL} = 8 mA | | 0.6 | | |
| t _{PLH} , t _{PHL} | Propagation delay | PLL bypass | | 2.6 | ns | |
| t _r /t _f | Rise and fall time | V _{DDOUT} = 1.8 V (20%–80%) | | 0.7 | ns | |
| t _{jit(cc)} | Cycle-to-cycle jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 70 | 120 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 120 | 170 | |
| t _{jit(per)} | Peak-to-peak period jitter ^{(2) (3)} | 1 PLL switching, Y2-to-Y3 | | 90 | 140 | ps |
| | | 4 PLLs switching, Y2-to-Y9 | | 130 | 190 | |
| t _{sk(o)} | Output skew ⁽⁴⁾ | f _{OUT} = 50 MHz; Y1-to-Y3 | | 60 | | ps |
| | | f _{OUT} = 50 MHz; Y2-to-Y5 or Y6-to-Y9 | | 160 | | |
| odc | Output duty cycle ⁽⁵⁾ | f _{VCO} = 100 MHz; Pdiv = 1 | | 45 | 55 | % |
| SDA/SCL PARAMETER | | | | | | |
| V _{IK} | SCL and SDA input clamp voltage | V _{DD} = 1.7 V; I _I = -18 mA | | -1.2 | | V |
| I _{IH} | SCL and SDA input current | V _I = V _{DD} ; V _{DD} = 1.9 V | | ±10 | | µA |
| V _{IH} | SDA/SCL input high voltage ⁽⁶⁾ | | | 0.7 V _{DD} | | V |
| V _{IL} | SDA/SCL input low voltage ⁽⁶⁾ | | | 0.3 V _{DD} | | V |
| V _{OL} | SDA low-level output voltage | I _{OL} = 3 mA, V _{DD} = 1.7 V | | 0.2 V _{DD} | | V |
| C _I | SCL/SDA input capacitance | V _I = 0 V or V _{DD} | | 3 | 10 | pF |

- (1) All typical values are at respective nominal V_{DD}.
- (2) 10000 cycles.
- (3) Jitter depends on device configuration. Data is taken under the following conditions: 1-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz, (measured at Y2), 4-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz, (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz, Y8/9 = 48 MHz.
- (4) The t_{sk(o)} specification is only valid for equal loading of each bank of outputs and outputs are generated from same divider; data sampled on rising edge (t_r).
- (5) odc depends on output rise- and fall-time (t_r/t_f).
- (6) SDA and SCL pins are 3.3-V tolerant.

PARAMETER MEASUREMENT INFORMATION

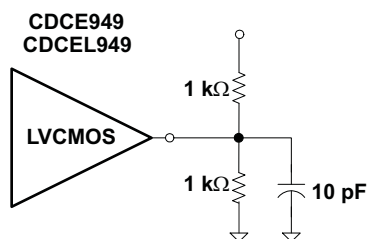


Figure 1. Test Load

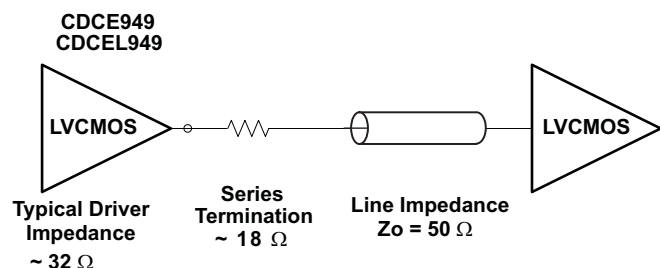


Figure 2. Test Load for 50 Ω Board Environment

TYPICAL CHARACTERISTICS

CDCE949 AND CDCEL949 SUPPLY CURRENT
vs
PLL FREQUENCY

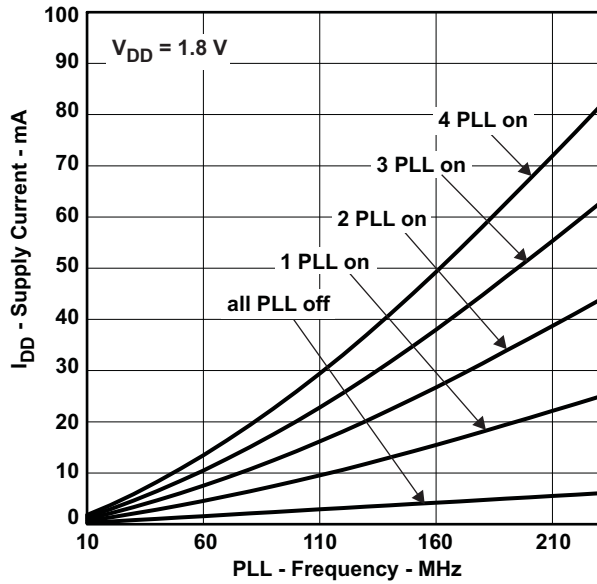


Figure 3.

CDCE949 OUTPUT CURRENT
vs
OUTPUT FREQUENCY

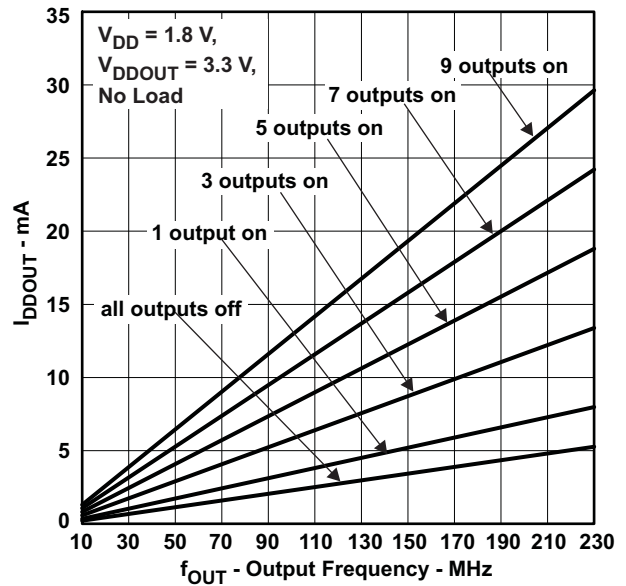


Figure 4.

CDCEL949 OUTPUT CURRENT
vs
OUTPUT FREQUENCY

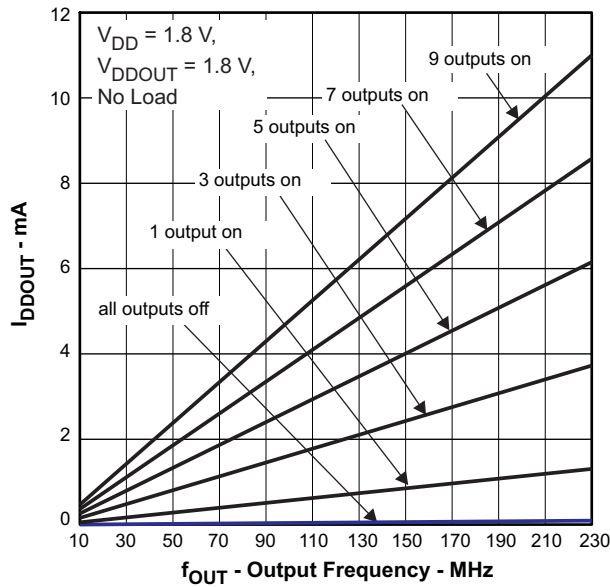


Figure 5.

APPLICATION INFORMATION

Control Terminal Configuration

The CDCE949/CDCEL949 has three user-definable control terminals (S0, S1 and S2) which allow external control of device settings. They can be programmed to perform any of the following functions:

- Spread-Spectrum Clcking selection: Spread-type and spread-amount selection
- Frequency selection: Switching between any of two user-defined frequencies
- Output-State selection: Output configuration and power-down control

The user can predefine up to eight different control settings. [Table 1](#) and [Table 2](#) explain these settings.

Table 1. Control Terminal Definition

| External Control-Bits | PLL1 Setting | | | PLL2 Setting | | | PLL3 Setting | | | PLL4 Setting | | | Y1 Setting |
|-----------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|-------------------------|---------------|------------------------|------------------------------------|
| Control Function | PLL Frequency Selection | SSC Selection | Output Y2/Y3 Selection | PLL Frequency Selection | SSC Selection | Output Y4/Y5 Selection | PLL Frequency Selection | SSC Selection | Output Y6/Y7 Selection | PLL Frequency Selection | SSC Selection | Output Y8/Y9 Selection | Output Y1 and Power Down Selection |

Table 2. PLLx Setting (can be selected for each PLL individual)⁽¹⁾

| SSC Selection (Center/Down) | | | | |
|---|---|------------|----------|----------|
| SSCx [3-bits] | | | Center | Down |
| 0 | 0 | 0 | 0% (off) | 0% (off) |
| 0 | 0 | 1 | ±0.25% | -0.25% |
| 0 | 1 | 0 | ±0.5% | -0.5% |
| 0 | 1 | 1 | ±0.75% | -0.75% |
| 1 | 0 | 0 | ±1.0% | -1.0% |
| 1 | 0 | 1 | ±1.25% | -1.25% |
| 1 | 1 | 0 | ±1.5% | -1.5% |
| 1 | 1 | 1 | ±2.0% | -2.0% |
| FREQUENCY SELECTION ⁽²⁾ | | | | |
| FSx | | FUNCTION | | |
| 0 | | Frequency0 | | |
| 1 | | Frequency1 | | |
| OUTPUT SELECTION ⁽³⁾ (Y2 ... Y9) | | | | |
| YxYx | | FUNCTION | | |
| 0 | | State0 | | |
| 1 | | State1 | | |

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register;

(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.

(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 3. Y1 Setting⁽¹⁾

| Y1 SELECTION | |
|--------------|----------|
| Y1 | FUNCTION |
| 0 | State 0 |
| 1 | State 1 |

(1) State0 and State1 are user-definable in Generic Configuration Register and can be power down, 3-state, low or active.

The S1/SDA and S2/SCL pins of the CDCE949/CDCEL949 are dual-function pins. In the default configuration they are defined as SDA/SCL for the serial interface. They can be programmed as control pins (S1/S2) by setting the appropriate bits in the EEPROM. Note that changes to the Control register (Bit [6] of Byte 02) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL).

S0 is **not** a multi-use pin, it is a control pin only.

DEFAULT DEVICE SETTING

The internal EEPROM of CDCE949/CDCEL949 is preconfigured as shown in Figure 6. (The input frequency is passed through to the output as a default.) This allows the device to operate in default mode without the extra production step of programming it. The default setting appears after power is supplied or after a power-down/up sequence until it is reprogrammed by the user to a different application configuration. A new register setting is programmed via the serial SDA/SCL Interface.

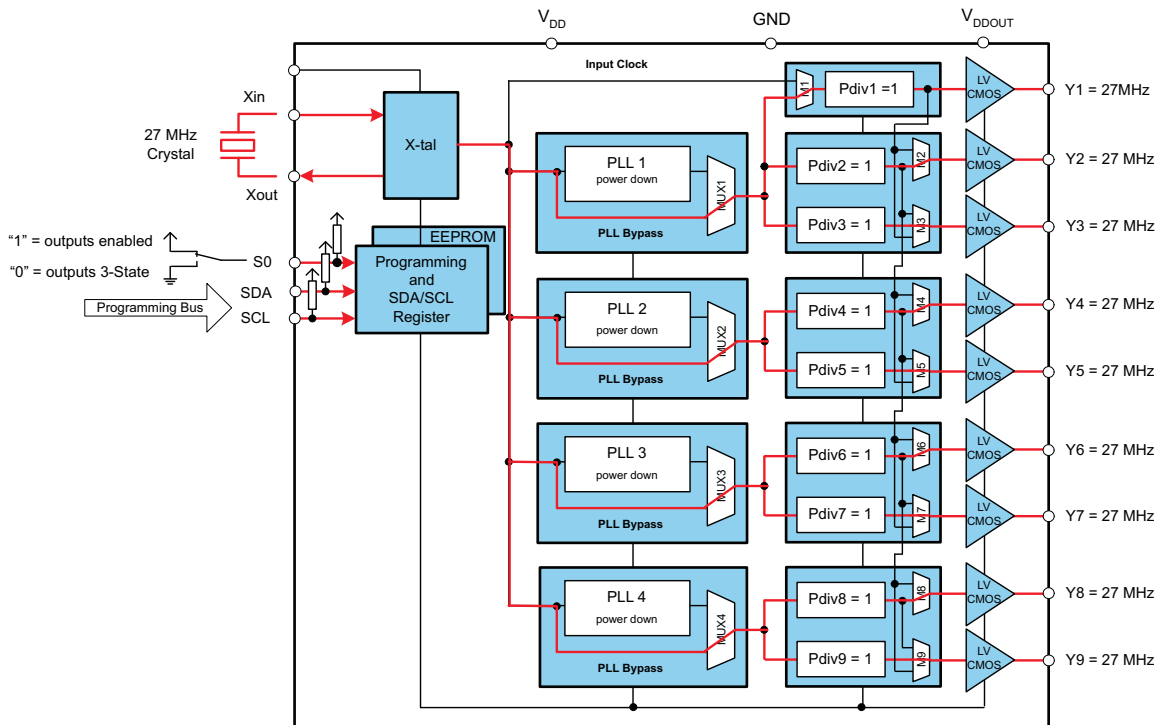


Figure 6. Default Configuration

Table 4 shows the default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in default mode.

Table 4. Factory Default Setting for Control Terminal Register

| EXTERNAL CONTROL-PINS ⁽¹⁾ | | | Y1 | PLL1 SETTING | | | PLL2 SETTING | | | PLL3 SETTING | | | PLL4 SETTING | | |
|--------------------------------------|------------------------|----|---------------|---------------------|----------|---------------|---------------------|----------|---------------|---------------------|----------|---------------|---------------------|----------|---------------|
| | | | Output Select | Freq. Select | SSC Sel. | Output Select | Freq. Select | SSC Sel. | Output Select | Freq. Select | SSC Sel. | Output Select | Freq. Select | SSC Sel. | Output Select |
| S2 | S1 | S0 | Y1 | FS1 | SSC1 | Y2Y3 | FS2 | SSC2 | Y4Y5 | FS3 | SSC3 | Y6Y7 | FS4 | SSC4 | Y8Y9 |
| SCL (I ² C) | SDA (I ² C) | 0 | 3-State | f _{VC01_0} | off | 3-State | f _{VC02_0} | off | 3-State | f _{VC03_0} | off | 3-State | f _{VC04_0} | off | 3-State |
| SCL (I ² C) | SDA (I ² C) | 1 | enabled | f _{VC01_0} | off | enabled | f _{VC02_0} | off | enabled | f _{VC03_0} | off | enabled | f _{VC04_0} | off | enabled |

(1) In default mode or when programmed respectively, S1 and S2 act as a serial programming interface, SDA/SCL. In this mode, they have no control-pin function, but are internally interpreted as if S1=0 and S2=0. S0, however, is a control-pin which in the default mode switches all outputs ON or OFF (as pre-defined above).

SDA/SCL SERIAL INTERFACE

The CDCE949/CDCEL949 operates as a slave device on the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I²C™ specification. It operates in the standard-mode transfer (up to 100 kbps) and fast-mode transfer (up to 400 kbps) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDC9xx are dual-function pins. In the default configuration they are used as SDA/SCL serial programming interface. They can be reprogrammed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].

DATA PROTOCOL

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The number of bytes read out is defined by the Byte Count field in the Generic Configuration Register. During a Block Read instruction, the entire number of bytes defined in Byte Count must be read out to correctly finish the read cycle.

When a byte is sent to the device, it is written into the internal register and immediately takes effect. This applies to each transferred byte, whether in a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA register contents are written into the EEPROM. During this write cycle, data is not accepted at the SDA/SCL bus until the write cycle is completed. However, data can be read during the programming sequence (Byte Read or Block Read). The programming status can be monitored by reading *EEPIP*, Byte 01–Bit [6].

The offset of the indexed byte is encoded in the command code, as described in [Table 6](#).

Table 5. Slave Receiver Address (7 bits)

| Device | A6 | A5 | A4 | A3 | A2 | A1 ⁽¹⁾ | A0 ⁽¹⁾ | R/W |
|-------------------------|----------|----------|----------|----------|----------|-------------------|-------------------|------------|
| CDCE913/CDCEL913 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1/0 |
| CDCE925/CDCEL925 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 |
| CDCE937/CDCEL937 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1/0 |
| CDCE949/CDCEL949 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1/0 |

(1) Address bits A0 and A1 are programmable via the SDA/SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least significant bit of the address byte designates a write or read operation.

Table 6. Command Code Definition

| BIT | DESCRIPTION |
|-------|--|
| 7 | 0 = <i>Block Read</i> or <i>Block Write</i> operation 1 = <i>Byte Read</i> or <i>Byte Write</i> operation |
| (6:0) | Byte Offset for <i>Byte Read</i> , <i>Block Read</i> , <i>Byte Write</i> and <i>Block Write</i> operation. |

Generic Programming Sequence

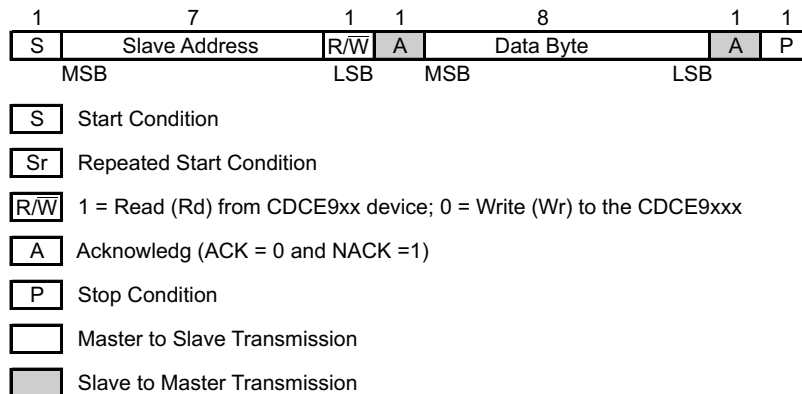


Figure 7. Generic Programming Sequence

Byte Write Programming Sequence



Figure 8. Byte Write Protocol

Byte Read Programming Sequence

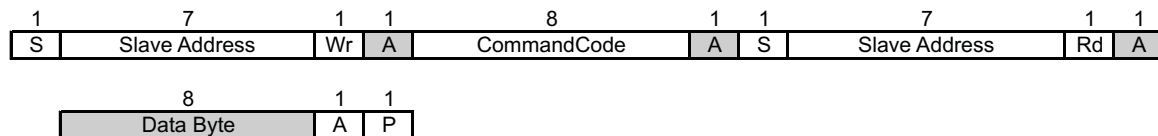
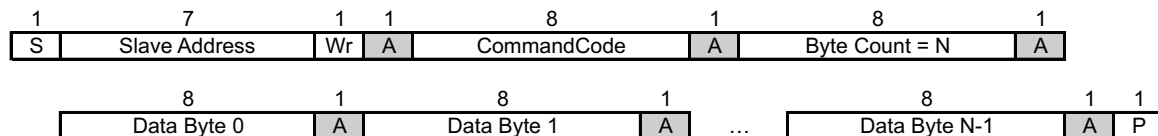


Figure 9. Byte Read Protocol

Block Write Programming Sequence



NOTE: Data Byte 0 Bits [7:0] is reserved for Revision Code and Vendor Identification. Also it is used for internal test purpose and should not be overwritten.

Figure 10. Block Write Programming

Block Read Programming Sequence

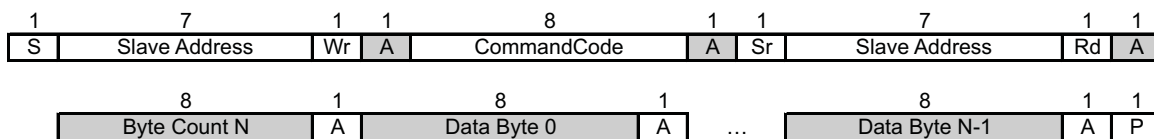


Figure 11. Block Read Protocol

Timing Diagram for the SDA/SCL Serial Control Interface

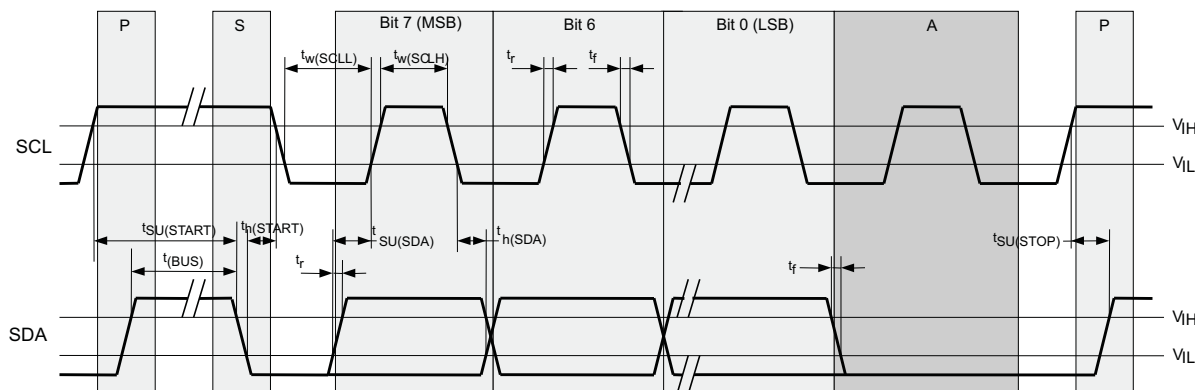


Figure 12. Timing Diagram for the SDA/SCL Serial Control Interface

SDA/SCL Hardware Interface

Figure 13 shows how the CDCE949/CDCEL949 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus but the speed may need to be reduced (400 kHz is the maximum) if many devices are connected.

Note that the pull-up resistor value (R_p) depends on the supply voltage, bus capacitance and number of connected devices. The recommended pull-up value is 4.7 k Ω . It must meet the minimum sink current of 3 mA at $V_{OLmax} = 0.4$ V for the output stages (for more details see the SMBus or I²C Bus specification).

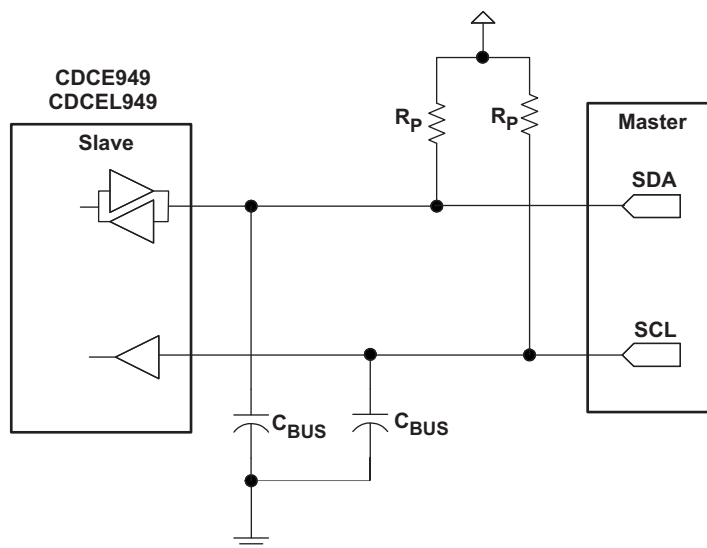


Figure 13. SDA/SCL Hardware Interface

SDA/SCL CONFIGURATION REGISTERS

The clock input, control pins, PLLs and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE949/CDCEL949. All settings can be manually written to the device via the SDA/SCL bus, or are easily programmable by using the TI Pro Clock software. TI Pro Clock software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA/SCL Registers

| ADDRESS OFFSET | REGISTER DESCRIPTION | TABLE |
|----------------|--------------------------------|--------------------------|
| 00h | Generic Configuration Register | Table 9 |
| 10h | PLL1 Configuration Register | Table 10 |
| 20h | PLL2 Configuration Register | Table 11 |
| 30h | PLL3 Configuration Register | Table 12 |
| 40h | PLL4 Configuration Register | Table 13 |

The grey-highlighted Bits described in the Configuration Registers tables on the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2 (See the [Control Terminal Configuration](#) section).

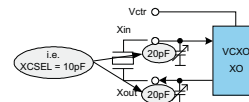
Table 8. Configuration Register, External Control Terminals

| EXTERNAL CONTROL PINS | | | Y1 | PLL1 SETTING | | | PLL2 SETTING | | | PLL3 SETTING | | | PLL4 SETTING | | |
|-----------------------------|----|----|---------------|--------------|------------|---------------|--------------|------------|---------------|--------------|------------|---------------|--------------|------------|---------------|
| | | | Output Select | Freq. Select | SSC Select | Output Select | Freq. Select | SSC Select | Output Select | Freq. Select | SSC Select | Output Select | Freq. Select | SSC Select | Output Select |
| S2 | S1 | S0 | Y1 | FS1 | SSC1 | Y2Y3 | FS2 | SSC2 | Y4Y5 | FS3 | SSC3 | Y6Y7 | FS4 | SSC4 | Y8Y9 |
| 0 | 0 | 0 | Y1_0 | FS1_0 | SSC1_0 | Y2Y3_0 | FS2_0 | SSC2_0 | Y4Y5_0 | FS3_0 | SSC3_0 | Y6Y7_0 | FS4_0 | SSC4_0 | Y8Y9_0 |
| 0 | 0 | 1 | Y1_1 | FS1_1 | SSC1_1 | Y2Y3_1 | FS2_1 | SSC2_1 | Y4Y5_1 | FS3_1 | SSC3_1 | Y6Y7_1 | FS4_1 | SSC4_1 | Y8Y9_1 |
| 0 | 1 | 0 | Y1_2 | FS1_2 | SSC1_2 | Y2Y3_2 | FS2_2 | SSC2_2 | Y4Y5_2 | FS3_2 | SSC3_2 | Y6Y7_2 | FS4_2 | SSC4_2 | Y8Y9_2 |
| 0 | 1 | 1 | Y1_3 | FS1_3 | SSC1_3 | Y2Y3_3 | FS2_3 | SSC2_3 | Y4Y5_3 | FS3_3 | SSC3_3 | Y6Y7_3 | FS4_3 | SSC4_3 | Y8Y9_3 |
| 1 | 0 | 0 | Y1_4 | FS1_4 | SSC1_4 | Y2Y3_4 | FS2_4 | SSC2_4 | Y4Y5_4 | FS3_4 | SSC3_4 | Y6Y7_4 | FS4_4 | SSC4_4 | Y8Y9_4 |
| 1 | 0 | 1 | Y1_5 | FS1_5 | SSC1_5 | Y2Y3_5 | FS2_5 | SSC2_5 | Y4Y5_5 | FS3_5 | SSC3_5 | Y6Y7_5 | FS4_5 | SSC4_5 | Y8Y9_5 |
| 1 | 1 | 0 | Y1_6 | FS1_6 | SSC1_6 | Y2Y3_6 | FS2_6 | SSC2_6 | Y4Y5_6 | FS3_6 | SSC3_6 | Y6Y7_6 | FS4_6 | SSC4_6 | Y8Y9_6 |
| 1 | 1 | 1 | Y1_7 | FS1_7 | SSC1_7 | Y2Y3_7 | FS2_7 | SSC2_7 | Y4Y5_7 | FS3_7 | SSC3_7 | Y6Y7_7 | FS4_7 | SSC4_7 | Y8Y9_7 |
| Addr. Offset ⁽¹⁾ | | | 04h | 13h | 10h-12h | 15h | 23h | 20h-22h | 25h | 33h | 30h-32h | 35h | 43h | 40h-42h | 45h |

(1) Address Offset refers to the byte address in the Configuration Register on following pages.

Table 9. Generic Configuration Register

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|-------------|------------------------|---|
| 00h | 7 | E_EL | xb | Device Identification (read only): '1' is CDCE949 (3.3V), '0' is CDCEL949 (1.8V) |
| | 6:4 | RID | Xb | Revision Identification Number (read only) |
| | 3:0 | VID | 1h | Vendor Identification Number (read only) |
| 01h | 7 | – | 0b | Reserved - always write 0 |
| | 6 | EEPIP | 0b | EEPROM Programming Status ⁽⁴⁾ : (read only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode |
| | 5 | EELOCK | 0b | Permanently Lock EEPROM Data ⁽⁵⁾ : 0 – EEPROM is not locked 1 – EEPROM will be permanently locked |
| | 4 | PWDN | 0b | Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (all PLLs and all outputs are enabled) 1 – device power down (all PLLs in power down and all outputs in 3-State) |
| | 3:2 | INCLK | 00b | Input clock selection: 00 – X-tal 10 – LVCMOS 01 – VCXO 11 – reserved |
| | 1:0 | SLAVE_ADR | 00b | Programmable Address Bits A0 and A1 of the Slave Receiver Address |
| 02h | 7 | M1 | 1b | Clock source selection for output Y1: 0 – input clock 1 – PLL1 clock |
| | 6 | SPICON | 0b | Operation mode selection for pin 22/23 ⁽⁶⁾ 0 – serial programming interface SDA (pin 23) and SCL (pin 22) 1 – control pins S1 (pin 23) and S2 (pin 22) |
| | 5:4 | Y1_ST1 | 11b | Y1-State0/1 Definition (applies to Y1_ST1 and Y1_ST0) |
| | 3:2 | Y1_ST0 | 01b | 00 – device power down (all PLLs in power down and all outputs in 3-state) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled (normal operation) |
| | 1:0 | Pdiv1 [9:8] | 001h | 10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value |
| 03h | 7:0 | Pdiv1 [7:0] | | |
| 04h | 7 | Y1_7 | 0b | Y1_x State Selection ⁽⁷⁾ 0 – State0 (predefined by Y1-State0 Definition [Y1_ST0]) 1 – State1 (predefined by Y1-State1 Definition [Y1_ST1]) |
| | 6 | Y1_6 | 0b | |
| | 5 | Y1_5 | 0b | |
| | 4 | Y1_4 | 0b | |
| | 3 | Y1_3 | 0b | |
| | 2 | Y1_2 | 0b | |
| | 1 | Y1_1 | 1b | |
| | 0 | Y1_0 | 0b | |
| 05h | 7:3 | XCSEL | 0Ah | Crystal load capacitor selection ⁽⁸⁾ : 00h → 0 pF 01h → 1 pF 02h → 2 pF 14h-to-1Fh → 20 pF |
| | 2:0 | – | 0b | Reserved - do not write others than 0 |



- (1) Writing data beyond '50h' may adversely affect device function.
- (2) All data is transferred MSB-first.
- (3) Unless custom setting is used.
- (4) During EEPROM programming, no data is allowed to be sent to the device via the SDA/SCL bus until the programming sequence is completed. Data, however, can be read during the programming sequence (Byte Read or Block Read).
- (5) If this bit is set high in the EEPROM, the actual data in the EEPROM is permanently locked, and no further programming is possible. Data, however can still be written via SDA/SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM
- (6) Selection of *control-pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL), and the two slave receiver address bits are reset to A0 = 0 and A1 = 0.
- (7) These are the bits of the Control Terminal Register. The user can pre-define up to eight different control settings. These settings can then be selected by the external control pins, S0, S1, and S2.
- (8) The internal load capacitor (C₁, C₂) must be used to achieve the best clock performance. External capacitors should be used only to do a fine adjustment of C_L by few pF. The value of C_L can be programmed with a resolution of 1 pF for a total crystal load range of 0 pF to 20 pF. For C_L > 20 pF use additional external capacitors. Also, the device input capacitance must be considered; this adds 1.5 pF (6pF//2pF) to the selected C_L. For more information about VCXO configuration and crystal recommendations, see application report [SCAA085](#)

Table 9. Generic Configuration Register (continued)

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|---------|------------------------|---|
| 06h | 7:1 | BCOUNT | 50h | 7-Bit Byte Count (Defines the number of Bytes which will be sent from this device at the next Block Read transfer; all bytes must be read out to correctly finish the read cycle.) Initiate EEPROM Write Cycle ⁽⁴⁾ ⁽⁹⁾ 0 – no EEPROM write cycle 1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM) |
| | 0 | EEWRITE | 0b | |
| 07h-0Fh | — | — | 0h | Reserved – do not write others than 0 |

- (9) **NOTE: The EEPROM WRITE bit must be sent last.** This ensures that the content of all internal registers are written into the EEPROM. The EEWRITE cycle is initiated by the rising edge of the EEWRITE-Bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE-Bit must be reset low after the programming is completed. The programming status can be monitored by readout EEPIP. If EELOCK is set high, no EEPROM programming will be possible.

Table 10. PLL1 Configuration Register

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|---|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 10h | 7:5 | SSC1_7 [2:0] | 000b | SSC1: PLL1 SSC Selection (Modulation Amount) ⁽⁴⁾ <table style="width: 100%; border: none;"> <tr> <td style="width: 50%;">Down</td> <td style="width: 50%;">Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC1_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC1_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 11h | 7 | | SSC1_5 [0] | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC1_4 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 12h | 3:1 | SSC1_3 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 0 | SSC1_2 [2] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7:6 | SSC1_2 [1:0] | | | | | | | | | | | | | | | | | | | | |
| 13h | 5:3 | SSC1_1 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 2:0 | SSC1_0 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7 | FS1_7 | 0b | FS1_x: PLL1 Frequency Selection ⁽⁴⁾ 0 – f_{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS1_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS1_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS1_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS1_3 | 0b | | | | | | | | | | | | | | | | | | | |
| 2 | FS1_2 | 0b | | | | | | | | | | | | | | | | | | | | |
| 1 | FS1_1 | 0b | | | | | | | | | | | | | | | | | | | | |
| 0 | FS1_0 | 0b | | | | | | | | | | | | | | | | | | | | |
| 14h | 7 | MUX1 | 1b | PLL1 Multiplexer: 0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down) | | | | | | | | | | | | | | | | | | |
| | 6 | M2 | 1b | Output Y2 Multiplexer: 0 – Pdiv1 1 – Pdiv2 | | | | | | | | | | | | | | | | | | |
| | 5:4 | M3 | 10b | Output Y3 Multiplexer: 00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved | | | | | | | | | | | | | | | | | | |
| | 3:2 | Y2Y3_ST1 | 11b | Y2, Y3-State0/1 definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State (PLL1 on) 10 – Y2/Y3 disabled to low (PLL1 on) 11 – Y2/Y3 enabled (normal operation, PLL1 on) | | | | | | | | | | | | | | | | | | |
| | 1:0 | Y2Y3_ST0 | 01b | | | | | | | | | | | | | | | | | | | |
| 15h | 7 | Y2Y3_7 | 0b | Y2Y3_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1) | | | | | | | | | | | | | | | | | | |
| | 6 | Y2Y3_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | Y2Y3_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | Y2Y3_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | Y2Y3_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | Y2Y3_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | Y2Y3_1 | 1b | | | | | | | | | | | | | | | | | | | |
| | 0 | Y2Y3_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 16h | 7 | SSC1DC | 0b | PLL1 SSC down/center selection: 0 – down 1 – center | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv2 | 01h | 7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |
| 17h | 7 | — | 0b | Reserved – do not write others than 0 | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv3 | 01h | 7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION |
|-----------------------|--------------------|----------------|------------------------|--|
| 18h | 7:0 | PLL1_0N [11:4] | 004h | PLL1_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information see PLL Multiplier/Divider Definition) |
| 19h | 7:4 | PLL1_0N [3:0] | | |
| 1Ah | 3:0 | PLL1_0R [8:5] | 000h | |
| | 7:3 | PLL1_0R[4:0] | 10h | |
| 1Bh | 2:0 | PLL1_0Q [5:3] | | |
| | 7:5 | PLL1_0Q [2:0] | | |
| | 4:2 | PLL1_0P [2:0] | 00b | f_{VCO1_0} range selection: 00 – $f_{VCO1_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_0} < 175$ MHz 11 – $f_{VCO1_0} \geq 175$ MHz |
| 1Ch | 7:0 | PLL1_1N [11:4] | 004h | PLL1_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph PLL Multiplier/Divider Definition) |
| 1Dh | 7:4 | PLL1_1N [3:0] | | |
| 1Eh | 3:0 | PLL1_1R [8:5] | 000h | |
| | 7:3 | PLL1_1R[4:0] | 10h | |
| 1Fh | 2:0 | PLL1_1Q [5:3] | | |
| | 7:5 | PLL1_1Q [2:0] | | |
| | 4:2 | PLL1_1P [2:0] | 00b | f_{VCO1_1} range selection: 00 – $f_{VCO1_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO1_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO1_1} < 175$ MHz 11 – $f_{VCO1_1} \geq 175$ MHz |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

Table 11. PLL2 Configuration Register

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|---|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 20h | 7:5 | SSC2_7 [2:0] | 000b | SSC2: PLL2 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td style="text-align: left;">Down</td> <td style="text-align: left;">Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC2_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC2_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 21h | 7 | | SSC2_5 [0] | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC2_4 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 3:1 | SSC2_3 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 22h | 0 | SSC2_2 [2] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7:6 | SSC2_2 [1:0] | | | | | | | | | | | | | | | | | | | | |
| | 5:3 | SSC2_1 [2:0] | | 000b | | | | | | | | | | | | | | | | | | |
| | 2:0 | SSC2_0 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 23h | 7 | FS2_7 | 0b | FS2_x: PLL2 Frequency Selection ⁽⁴⁾ 0 – f_{VCO2_0} (predefined by PLL2_0 – Multiplier/Divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS2_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS2_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS2_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS2_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | FS2_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | FS2_1 | 0b | | | | | | | | | | | | | | | | | | | |
| | 0 | FS2_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 24h | 7 | MUX2 | 1b | PLL2 Multiplexer: 0 – PLL2 1 – PLL2 Bypass (PLL2 is in power down) | | | | | | | | | | | | | | | | | | |
| | 6 | M4 | 1b | Output Y4 Multiplexer: 0 – Pdiv2 1 – Pdiv4 | | | | | | | | | | | | | | | | | | |
| | 5:4 | M5 | 10b | Output Y5 Multiplexer: 00 – Pdiv2-Divider 01 – Pdiv4-Divider 10 – Pdiv5-Divider 11 – reserved | | | | | | | | | | | | | | | | | | |
| | 3:2 | Y4Y5_ST1 | 11b | Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down) 01 – Y4/Y5 disabled to 3-State (PLL2 on) 10 – Y4/Y5 disabled to low (PLL2 on) 11 – Y4/Y5 enabled (normal operation, PLL2 on) | | | | | | | | | | | | | | | | | | |
| | 1:0 | Y4Y5_ST0 | 01b | | | | | | | | | | | | | | | | | | | |
| 25h | 7 | Y4Y5_7 | 0b | Y4Y5_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1) | | | | | | | | | | | | | | | | | | |
| | 6 | Y4Y5_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | Y4Y5_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | Y4Y5_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | Y4Y5_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | Y4Y5_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | Y4Y5_1 | 1b | | | | | | | | | | | | | | | | | | | |
| | 0 | Y4Y5_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 26h | 7 | SSC2DC | 0b | PLL2 SSC down/center selection: 0 – down 1 – center | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv4 | 01h | 7-Bit Y4-Output-Divider Pdiv4: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |
| 27h | 7 | — | 0b | Reserved – do not write others than 0 | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv5 | 01h | 7-Bit Y5-Output-Divider Pdiv5: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 11. PLL2 Configuration Register (continued)

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | |
|-----------------------|--------------------|----------------|------------------------|---|---|
| 28h | 7:0 | PLL2_0N [11:4] | 004h | PLL2_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) | |
| 29h | 7:4 | PLL2_0N [3:0] | | | |
| 2Ah | 3:0 | PLL2_0R [8:5] | 000h | | |
| | 7:3 | PLL2_0R[4:0] | | | |
| 2Bh | 2:0 | PLL2_0Q [5:3] | 10h | | |
| | 7:5 | PLL2_0Q [2:0] | | | |
| | 4:2 | PLL2_0P [2:0] | | | 010b |
| | 1:0 | VCO2_0_RANGE | 00b | | f_{VCO2_0} range selection: 00 – $f_{VCO2_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO2_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO2_0} < 175$ MHz 11 – $f_{VCO2_0} \geq 175$ MHz |
| 2Ch | 7:0 | PLL2_1N [11:4] | 004h | | PLL2_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) |
| 2Dh | 7:4 | PLL2_1N [3:0] | | | |
| 2Eh | 3:0 | PLL2_1R [8:5] | 000h | | |
| | 7:3 | PLL2_1R[4:0] | | | |
| 2Fh | 2:0 | PLL2_1Q [5:3] | 10h | | |
| | 7:5 | PLL2_1Q [2:0] | | | |
| | 4:2 | PLL2_1P [2:0] | | 010b | |
| | 1:0 | VCO2_1_RANGE | 00b | f_{VCO2_1} range selection: 00 – $f_{VCO2_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO2_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO2_1} < 175$ MHz 11 – $f_{VCO2_1} \geq 175$ MHz | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

Table 12. PLL3 Configuration Register

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|---|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 30h | 7:5 | SSC3_7 [2:0] | 000b | SSC3: PLL3 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td style="text-align: center;">Down</td> <td style="text-align: center;">Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC3_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC3_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 31h | 7 | | SSC3_5 [0] | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC3_4 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 3:1 | SSC3_3 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 32h | 0 | SSC3_2 [2] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7:6 | SSC3_2 [1:0] | | | | | | | | | | | | | | | | | | | | |
| | 5:3 | SSC3_1 [2:0] | | 000b | | | | | | | | | | | | | | | | | | |
| | 2:0 | SSC3_0 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 33h | 7 | FS3_7 | 0b | FS3_x: PLL3 Frequency Selection ⁽⁴⁾ 0 – f_{VCO3_0} (predefined by PLL3_0 – Multiplier/Divider value) 1 – f_{VCO3_1} (predefined by PLL3_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | 6 | FS3_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | FS3_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | FS3_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | FS3_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | FS3_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | FS3_1 | 0b | | | | | | | | | | | | | | | | | | | |
| | 0 | FS3_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 34h | 7 | MUX3 | 1b | PLL3 Multiplexer: 0 – PLL3 1 – PLL3 Bypass (PLL3 is in power down) | | | | | | | | | | | | | | | | | | |
| | 6 | M6 | 1b | Output Y6 Multiplexer: 0 – Pdiv4 1 – Pdiv6 | | | | | | | | | | | | | | | | | | |
| | 5:4 | M7 | 10b | Output Y7 Multiplexer: 00 – Pdiv4-Divider 01 – Pdiv6-Divider 10 – Pdiv7-Divider 11 – reserved | | | | | | | | | | | | | | | | | | |
| | 3:2 | Y6Y7_ST1 | 11b | Y6, Y7-State0/1definition: 00 – Y6/Y7 disabled to 3-State (PLL3 is in power down) 01 – Y6/Y7 disabled to 3-State (PLL3 on) 10 – Y6/Y7 disabled to low (PLL3 on) 11 – Y6/Y7 enabled (normal operation, PLL3 on) | | | | | | | | | | | | | | | | | | |
| | 1:0 | Y6Y7_ST0 | 01b | | | | | | | | | | | | | | | | | | | |
| 35h | 7 | Y6Y7_7 | 0b | Y6Y7_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y6Y7_ST0) 1 – state1 (predefined by Y6Y7_ST1) | | | | | | | | | | | | | | | | | | |
| | 6 | Y6Y7_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | Y6Y7_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | Y6Y7_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | Y6Y7_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | Y6Y7_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | Y6Y7_1 | 1b | | | | | | | | | | | | | | | | | | | |
| | 0 | Y6Y7_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 36h | 7 | SSC3DC | 0b | PLL3 SSC down/center selection: 0 – down 1 – center | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv6 | 01h | 7-Bit Y6-Output-Divider Pdiv6: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |
| 37h | 7 | — | 0b | Reserved – do not write others than 0 | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv7 | 01h | 7-Bit Y7-Output-Divider Pdiv7: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 12. PLL3 Configuration Register (continued)

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | |
|-----------------------|--------------------|----------------|------------------------|---|---|
| 38h | 7:0 | PLL3_0N [11:4] | 004h | PLL3_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO3_0} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) | |
| 39h | 7:4 | PLL3_0N [3:0] | | | |
| 3Ah | 3:0 | PLL3_0R [8:5] | 000h | | |
| | 7:3 | PLL3_0R[4:0] | | | |
| 3Bh | 2:0 | PLL3_0Q [5:3] | 10h | | |
| | 7:5 | PLL3_0Q [2:0] | | | |
| | 4:2 | PLL3_0P [2:0] | | | 010b |
| | 1:0 | VCO3_0_RANGE | 00b | | f_{VCO3_0} range selection: 00 – $f_{VCO3_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO3_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO3_0} < 175$ MHz 11 – $f_{VCO3_0} \geq 175$ MHz |
| 3Ch | 7:0 | PLL3_1N [11:4] | 004h | | PLL3_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO3_1} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) |
| 3Dh | 7:4 | PLL3_1N [3:0] | | | |
| 3Eh | 3:0 | PLL3_1R [8:5] | 000h | | |
| | 7:3 | PLL3_1R[4:0] | | | |
| 3Fh | 2:0 | PLL3_1Q [5:3] | 10h | | |
| | 7:5 | PLL3_1Q [2:0] | | | |
| | 4:2 | PLL3_1P [2:0] | | 010b | |
| | 1:0 | VCO3_1_RANGE | 00b | f_{VCO3_1} range selection: 00 – $f_{VCO3_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO3_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO3_1} < 175$ MHz 11 – $f_{VCO3_1} \geq 175$ MHz | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

Table 13. PLL4 Configuration Register

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | | | | | | | | | | | | | | | | | | |
|-----------------------|--------------------|---------------|------------------------|---|-------------|---------------|-----------|-----------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|-------------|-------------|------------|------------|------------|------------|
| 40h | 7:5 | SSC4_7 [2:0] | 000b | SSC4: PLL4 SSC Selection (Modulation Amount) ⁽⁴⁾ <table border="0"> <tr> <td style="text-align: center;">Down</td> <td style="text-align: center;">Center</td> </tr> <tr> <td>000 (off)</td> <td>000 (off)</td> </tr> <tr> <td>001 – 0.25%</td> <td>001 ± 0.25%</td> </tr> <tr> <td>010 – 0.5%</td> <td>010 ± 0.5%</td> </tr> <tr> <td>011 – 0.75%</td> <td>011 ± 0.75%</td> </tr> <tr> <td>100 – 1.0%</td> <td>100 ± 1.0%</td> </tr> <tr> <td>101 – 1.25%</td> <td>101 ± 1.25%</td> </tr> <tr> <td>110 – 1.5%</td> <td>110 ± 1.5%</td> </tr> <tr> <td>111 – 2.0%</td> <td>111 ± 2.0%</td> </tr> </table> | Down | Center | 000 (off) | 000 (off) | 001 – 0.25% | 001 ± 0.25% | 010 – 0.5% | 010 ± 0.5% | 011 – 0.75% | 011 ± 0.75% | 100 – 1.0% | 100 ± 1.0% | 101 – 1.25% | 101 ± 1.25% | 110 – 1.5% | 110 ± 1.5% | 111 – 2.0% | 111 ± 2.0% |
| | Down | Center | | | | | | | | | | | | | | | | | | | | |
| | 000 (off) | 000 (off) | | | | | | | | | | | | | | | | | | | | |
| 001 – 0.25% | 001 ± 0.25% | | | | | | | | | | | | | | | | | | | | | |
| 010 – 0.5% | 010 ± 0.5% | | | | | | | | | | | | | | | | | | | | | |
| 011 – 0.75% | 011 ± 0.75% | | | | | | | | | | | | | | | | | | | | | |
| 100 – 1.0% | 100 ± 1.0% | | | | | | | | | | | | | | | | | | | | | |
| 101 – 1.25% | 101 ± 1.25% | | | | | | | | | | | | | | | | | | | | | |
| 110 – 1.5% | 110 ± 1.5% | | | | | | | | | | | | | | | | | | | | | |
| 111 – 2.0% | 111 ± 2.0% | | | | | | | | | | | | | | | | | | | | | |
| 4:2 | SSC4_6 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 1:0 | SSC4_5 [2:1] | 000b | | | | | | | | | | | | | | | | | | | | |
| 41h | 7 | | SSC4_5 [0] | | | | | | | | | | | | | | | | | | | |
| | 6:4 | SSC4_4 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| 42h | 3:1 | SSC4_3 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 0 | SSC4_2 [2] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7:6 | SSC4_2 [1:0] | | | | | | | | | | | | | | | | | | | | |
| 5:3 | SSC4_1 [2:0] | 000b | | | | | | | | | | | | | | | | | | | | |
| 43h | 2:0 | SSC4_0 [2:0] | 000b | | | | | | | | | | | | | | | | | | | |
| | 7 | FS4_7 | 0b | FS4_x: PLL4 Frequency Selection ⁽⁴⁾ 0 – f_{VCO4_0} (predefined by PLL4_0 – Multiplier/Divider value) 1 – f_{VCO4_1} (predefined by PLL4_1 – Multiplier/Divider value) | | | | | | | | | | | | | | | | | | |
| | | FS4_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | | FS4_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | | FS4_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | | FS4_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | | FS4_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | | FS4_1 | 0b | | | | | | | | | | | | | | | | | | | |
| FS4_0 | | 0b | | | | | | | | | | | | | | | | | | | | |
| 44h | 7 | MUX4 | 1b | PLL4 Multiplexer: 0 – PLL4 1 – PLL4 Bypass (PLL4 is in power down) | | | | | | | | | | | | | | | | | | |
| | 6 | M8 | 1b | Output Y8 Multiplexer: 0 – Pdiv6 1 – Pdiv8 | | | | | | | | | | | | | | | | | | |
| | 5:4 | M9 | 10b | Output Y9 Multiplexer: 00 – Pdiv6-Divider 01 – Pdiv8-Divider 10 – Pdiv9-Divider 11 – reserved | | | | | | | | | | | | | | | | | | |
| | 3:2 | Y8Y9_ST1 | 11b | Y8, Y9-State0/1definition: 00 – Y8/Y9 disabled to 3-State (PLL4 is in power down) 01 – Y8/Y9 disabled to 3-State (PLL4 on) 10 – Y8/Y9 disabled to low (PLL4 on) 11 – Y8/Y9 enabled (normal operation, PLL4 on) | | | | | | | | | | | | | | | | | | |
| | 1:0 | Y8Y9_ST0 | 01b | | | | | | | | | | | | | | | | | | | |
| 45h | 7 | Y8Y9_7 | 0b | Y8Y9_x Output State Selection ⁽⁴⁾ 0 – state0 (predefined by Y8Y9_ST0) 1 – state1 (predefined by Y8Y9_ST1) | | | | | | | | | | | | | | | | | | |
| | 6 | Y8Y9_6 | 0b | | | | | | | | | | | | | | | | | | | |
| | 5 | Y8Y9_5 | 0b | | | | | | | | | | | | | | | | | | | |
| | 4 | Y8Y9_4 | 0b | | | | | | | | | | | | | | | | | | | |
| | 3 | Y8Y9_3 | 0b | | | | | | | | | | | | | | | | | | | |
| | 2 | Y8Y9_2 | 0b | | | | | | | | | | | | | | | | | | | |
| | 1 | Y8Y9_1 | 1b | | | | | | | | | | | | | | | | | | | |
| | 0 | Y8Y9_0 | 0b | | | | | | | | | | | | | | | | | | | |
| 46h | 7 | SSC4DC | 0b | PLL4 SSC down/center selection: 0 – down 1 – center | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv8 | 01h | 7-Bit Y8-Output-Divider Pdiv8: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |
| 47h | 7 | — | 0b | Reserved – do not write others than 0 | | | | | | | | | | | | | | | | | | |
| | 6:0 | Pdiv9 | 01h | 7-Bit Y9-Output-Divider Pdiv9: 0 – reset and stand-by 1-to-127 – divider value | | | | | | | | | | | | | | | | | | |

(1) Writing data beyond 50h may adversely affect device function.

(2) All data is transferred MSB-first.

(3) Unless a custom setting is used

(4) The user can pre-define up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 13. PLL4 Configuration Register (continued)

| OFFSET ⁽¹⁾ | Bit ⁽²⁾ | Acronym | Default ⁽³⁾ | DESCRIPTION | |
|-----------------------|--------------------|----------------|------------------------|---|---|
| 48h | 7:0 | PLL4_0N [11:4] | 004h | PLL4_0 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO4_0} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) | |
| 49h | 7:4 | PLL4_0N [3:0] | | | |
| 4Ah | 3:0 | PLL4_0R [8:5] | 000h | | |
| | 7:3 | PLL4_0R[4:0] | | | |
| 4Bh | 2:0 | PLL4_0Q [5:3] | 10h | | |
| | 7:5 | PLL4_0Q [2:0] | | | |
| | 4:2 | PLL4_0P [2:0] | | | 010b |
| | 1:0 | VCO4_0_RANGE | 00b | | f_{VCO4_0} range selection: 00 – $f_{VCO4_0} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO4_0} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO4_0} < 175$ MHz 11 – $f_{VCO4_0} \geq 175$ MHz |
| 4Ch | 7:0 | PLL4_1N [11:4] | 004h | | PLL4_1 ⁽⁵⁾ : 30-Bit Multiplier/Divider value for frequency f_{VCO4_1} (for more information see paragraph <i>PLL Multiplier/Divider Definition</i>) |
| 4Dh | 7:4 | PLL4_1N [3:0] | | | |
| 4Eh | 3:0 | PLL4_1R [8:5] | 000h | | |
| | 7:3 | PLL4_1R[4:0] | | | |
| 4Fh | 2:0 | PLL4_1Q [5:3] | 10h | | |
| | 7:5 | PLL4_1Q [2:0] | | | |
| | 4:2 | PLL4_1P [2:0] | | 010b | |
| | 1:0 | VCO4_1_RANGE | 00b | f_{VCO4_1} range selection: 00 – $f_{VCO4_1} < 125$ MHz 01 – $125 \text{ MHz} \leq f_{VCO4_1} < 150$ MHz 10 – $150 \text{ MHz} \leq f_{VCO4_1} < 175$ MHz 11 – $f_{VCO4_1} \geq 175$ MHz | |

(5) PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$

PLL MULTIPLIER/DIVIDER DEFINITION

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCE949/CDCEL949 can be calculated by:

$$f_{OUT} = \frac{f_{IN}}{P_{div}} \times \frac{N}{M}$$

where

M (1 to 511) and N (1 to 4095) are the multiplier/divider values of the PLL;
Pdiv (1 to 127) is the output divider.

The target VCO frequency (f_{VCO}) of each PLL can be calculated:

$$f_{VCO} = f_{IN} \times \frac{N}{M}$$

The PLL operates as fractional divider and needs following multiplier/divider settings

N

$$P = 4 - \text{int}(\log_2 \frac{N}{M}) \quad \{\text{if } P < 0 \text{ then } P = 0\}$$

$$Q = \text{int}(\frac{N'}{M})$$

$$R = N' - M \times Q$$

Where:

$$N' = N \times 2^P;$$

$$N \geq M;$$

$$80 \text{ MHz} < f_{VCO} < 230 \text{ MHz};$$

$$16 \leq q \leq 63;$$

$$0 \leq p \leq 7;$$

$$0 \leq r \leq 511.$$

Example 1: for $f_{IN} = 27 \text{ MHz}$; $M = 1$; $N = 4$; $P_{div} = 2$;

$$\rightarrow f_{OUT} = 54 \text{ MHz};$$

$$\rightarrow f_{VCO} = 108 \text{ MHz};$$

$$\rightarrow P = 4 - \text{int}(\log_2 4) = 4 - 2 = 2;$$

$$\rightarrow N' = 4 \times 2^2 = 16;$$

$$\rightarrow Q = \text{int}(16) = 16;$$

$$\rightarrow R = 16 - 16 = 0;$$

Example 2: for $f_{IN} = 27 \text{ MHz}$; $M = 2$; $N = 11$; $P_{div} = 2$;

$$\rightarrow f_{OUT} = 75.25 \text{ MHz};$$

$$\rightarrow f_{VCO} = 148.50 \text{ MHz};$$

$$\rightarrow P = 4 - \text{int}(\log_2 5.5) = 4 - 2 = 2;$$

$$\rightarrow N' = 11 \times 2^2 = 44;$$

$$\rightarrow Q = \text{int}(22) = 22;$$

$$\rightarrow R = 44 - 44 = 0;$$

The values for P, Q, R and N' are automatically calculated when using TI Pro Clock™ Software.

REVISION HISTORY

| Changes from Original (August 2007) to Revision A | Page |
|--|-------------|
| • Changed the THERMAL RESISTANCE FOR TSSOP table | 4 |
| • Changed Table 9 RID From: 0h To: Xb | 15 |
| • Added note to the PWDN description, Table 9 | 15 |
| Changes from Revision A (December 2007) to Revision B | Page |
| • Added Note 3: SDA and SCL can go up to 3.6V as stated in the <i>Recommended Operating Conditions</i> table. | 3 |
| Changes from Revision B (September 2009) to Revision C | Page |
| • Deleted sentence - A different default setting can be programmed upon customer request. Contact Texas Instruments sales or marketing representative for more information. | 10 |
| Changes from Revision C (October 2009) to Revision D | Page |
| • Added PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$, $0 < N < 4096$ foot to PLL1, PLL2, PLL3, & PLL4 Configure Register Table | 18 |
| • Added PLL settings limits: $16 \leq q \leq 63$, $0 \leq p \leq 7$, $0 \leq r \leq 511$ to PLL Multiplier/Divider Definition Section | 25 |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| CDCE949PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCE949PWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCE949PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCE949PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCEL949PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCEL949PWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCEL949PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| CDCEL949PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

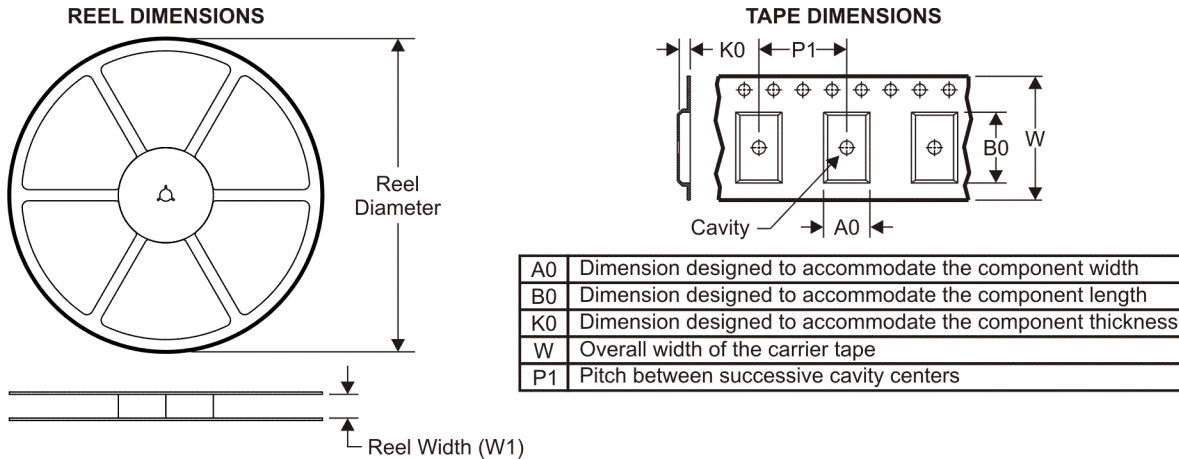
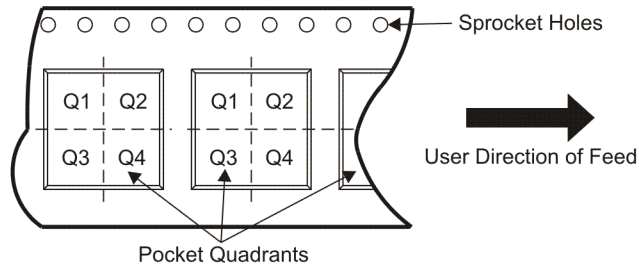
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCE949PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| CDCEL949PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCE949PWR | TSSOP | PW | 24 | 2000 | 346.0 | 346.0 | 33.0 |
| CDCEL949PWR | TSSOP | PW | 24 | 2000 | 346.0 | 346.0 | 33.0 |

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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