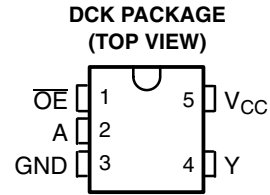


SN74AHCT1G125-Q1 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

SCLS504B – JUNE 2003 – REVISED JANUARY 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operating Range of 3 V to 5.5 V
- Max t_{pd} of 6 ns at 5 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible



description/ordering information

The SN74AHCT1G125 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING§
-40°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	CAHCT1G125QDCKRQ1	BM_

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

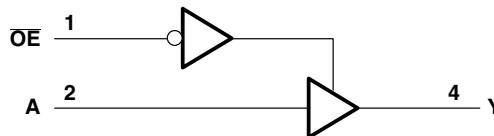
‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ The actual top-side marking has one additional character that designates the wafer fab/assembly site.

FUNCTION TABLE

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN74AHCT1G125-Q1

SINGLE BUS BUFFER GATE

WITH 3-STATE OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2)	252°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3.0$ V	1.4	V
		$V_{CC} = 4.5$ V to 5.5 V	2	
V_{IL}	Low-level input voltage	$V_{CC} = 3.0$ V	0.53	V
		$V_{CC} = 4.5$ V to 5.5 V	0.8	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		-8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	3 V	2.9	3		2.9	V	
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.34		
		4.5 V	3.94			3.66		
V _{OL}	I _{OL} = 50 μA	3 V and 4.5 V				0.1	V	
	I _{OL} = 4 mA	3 V				0.36		
	I _{OL} = 8 mA	4.5 V				0.36		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V				±0.1	±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V				±0.25	±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0, \overline{OE} high or low	3 V and 5.5 V				1	10	μA
ΔI _{CC} [†]	One input at 3.4 V, Other input at V _{CC} or GND	5.5 V				1.35	1.5	mA
C _i	V _I = V _{CC} or GND	5 V				4	10	pF
C _o	V _O = V _{CC} or GND	5 V				10		pF

[†] This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		5.6	8		12	ns
t _{PHL}					5.6	8		12	
t _{PZH}	\overline{OE}	Y	C _L = 15 pF		5.4	8		11.5	ns
t _{PZL}					5.4	8		11.5	
t _{PHZ}	\overline{OE}	Y	C _L = 15 pF		6.5	9.7		14.5	ns
t _{PLZ}					6.5	9.7		14.5	
t _{PLH}	A	Y	C _L = 50 pF		8.1	11.5		16	ns
t _{PHL}					8.1	11.5		16	
t _{PZH}	\overline{OE}	Y	C _L = 50 pF		7.9	11.5		15	ns
t _{PZL}					7.9	11.5		15	
t _{PHZ}	\overline{OE}	Y	C _L = 50 pF		8	13.2		18	ns
t _{PLZ}					8	13.2		18	

SN74AHCT1G125-Q1
SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

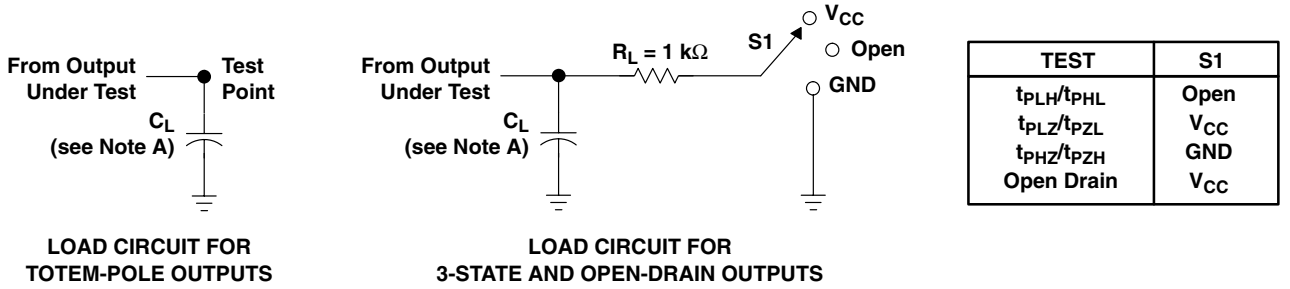
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8	5.5	8.5	ns		
t_{PHL}				3.8	5.5	8.5			
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	3.6	5.1	7.5	ns		
t_{PZL}				3.6	5.1	7.5			
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.8	6.8	10	ns		
t_{PLZ}				4.8	6.8	10			
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	10.5	ns		
t_{PHL}				5.3	7.5	10.5			
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	5.1	7.1	9.5	ns		
t_{PZL}				5.1	7.1	9.5			
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	7	8.8	12	ns		
t_{PLZ}				7	8.8	12			

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

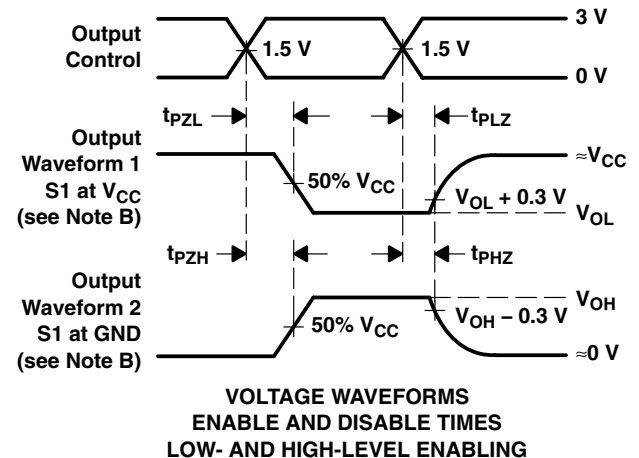
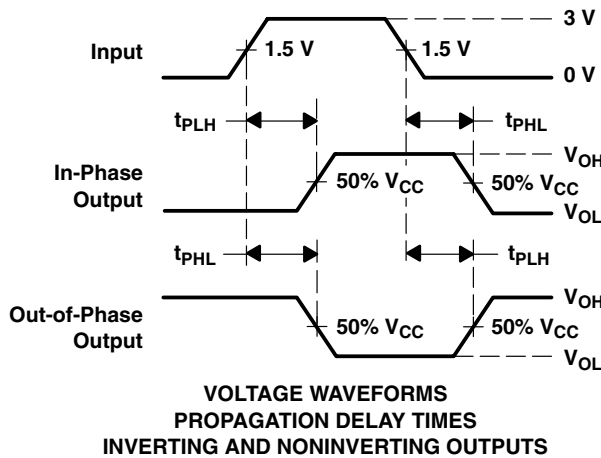
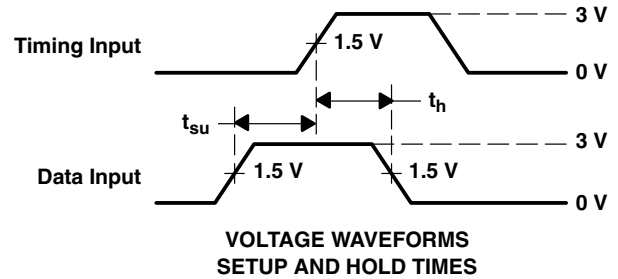
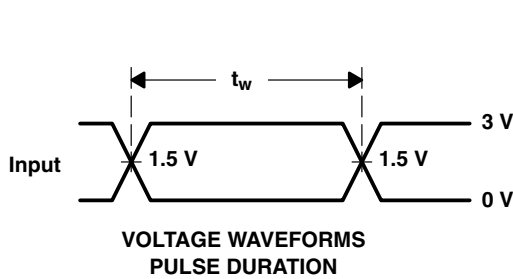


PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CAHCT1G125QDCKRG4Q	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CAHCT1G125QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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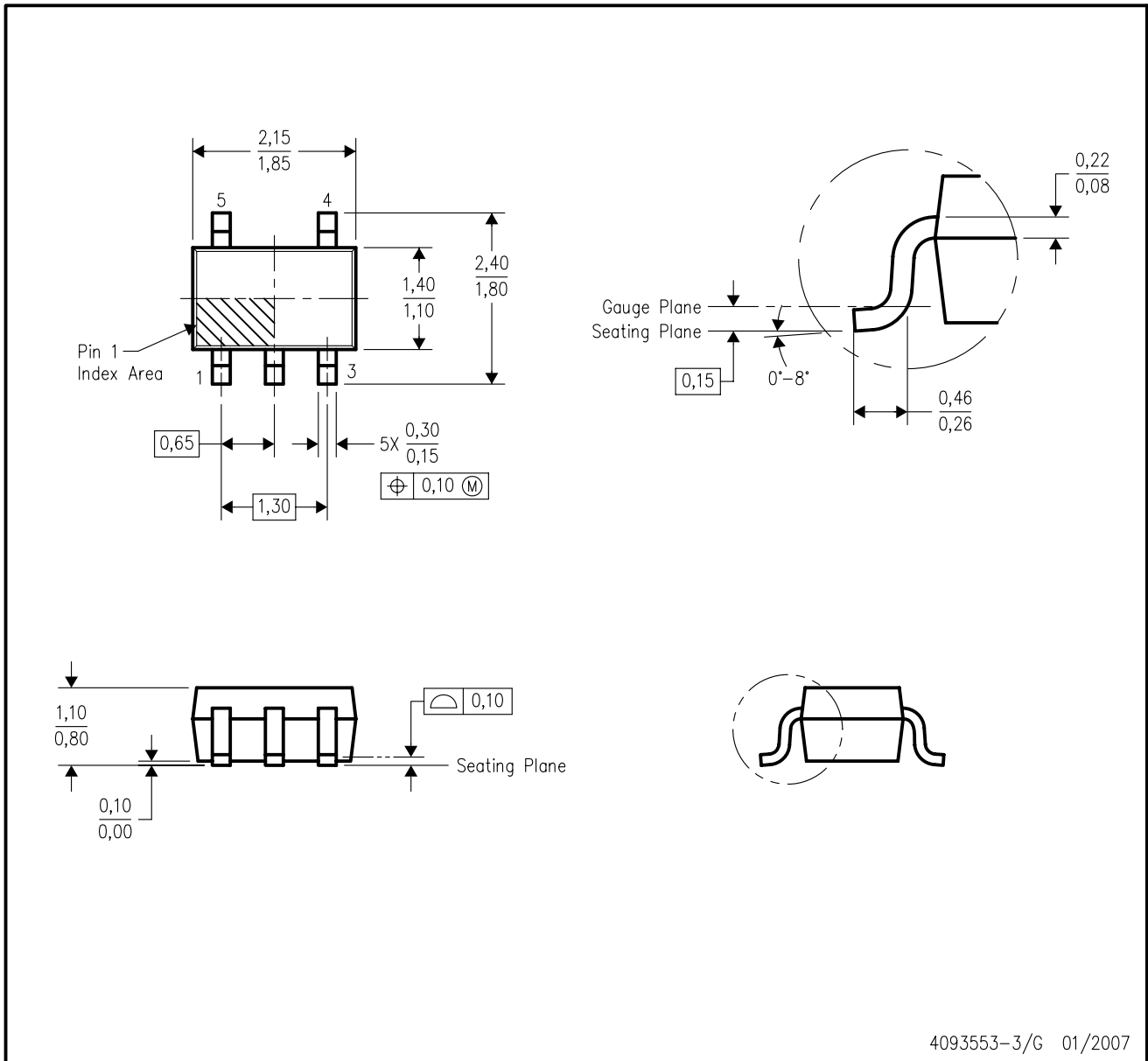
- Catalog: [SN74AHCT1G125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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