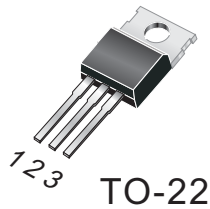
BT137-800E

Sensitive Gate Triacs

HAOPIN MICROELECTRONICS CO.,LTD.

Description

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

Symbol	Simplified outline
	

Pin	Description
1	Main terminal 1 (T1)
2	Main terminal 2 (T2)
3	gate (G)
TAB	Main terminal 2 (T2)

Applications:

- Motor control
- Industrial and domestic lighting
- Heating
- Static switching

Features

- Blocking voltage to 800 V
- On-state RMS current to 8 A

SYMBOL	PARAMETER	Value	Unit
V_{DRM}	Repetitive peak off-state voltages	800	V
$I_{T(RMS)}$	RMS on-state current	8	A
I_{TSM}	Non-repetitive peak on-state current	65	A

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance Junction to mounting base	Full cycle	-	-	2.0	K/W
		Half cycle	-	-	2.4	K/W
$R_{th\ j\text{-}a}$	Thermal resistance Junction to ambient	In free air	-	60	-	K/W

Limiting values in accordance with the Maximum system(IEC 134)

SYMBOL	PARAMETER	CONDITIONS		MIN	Value	UNIT
V_{DRM}	Repetitive peak off-state Voltages			-	800	V
$I_{T(RMS)}$	RMS on-state current	Full sine wave;$T_{mb}\leqslant 102℃$		-	8	A
I_{TSM}	Non-repetitive surge peak on-statecurrent	full sine wave;, T_j=25℃ prior to surge	t=20ms	-	65	A
			t=16.7ms	-	71	A
I^2t	I^2t for fusing	T=10ms		-	21	A^2S
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM}=12A; I_G=0.2A; DI_G/dt=0.2A/μs				
			T2+G+	-	50	A/μs
			T2+G-	-	50	A/μs
			T2-G-	-	50	A/μs
			T2-G+	-	10	A/μs
I_{GM}	Peak gate current			-	2	A
V_{GM}	Peak gate voltage			-	5	V
P_{GM}	Peak gate power			-	5	W
$P_{G(AV)}$	Average gate power	Over any 20 ms period		-	0.5	W
T_{stg}	Storage temperature			-40	150	℃
T_j	Operating junction Temperature			-	125	℃

T_J=25°C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Static characteristics							
I_{GT1}	Gate trigger current	V_D=12V; I_T=0.1A					
			T2+G+	-	2.5	10	mA
			T2+G-	-	4.0	10	mA
			T2-G-	-	5.0	10	mA
			T2-G+	-	11	25	mA
I_L	Latching current	V_D=12V; I_{GT}=0.1A					
			T2+G+	-	3.0	25	mA
			T2+G-	-	14	35	mA
			T2-G-	-	3.0	25	mA
			T2-G+	-	4.0	35	mA
I_H	Holding current	V_D=12V; I_{GT}=0.1A		-	2.5	20	mA
V_T	On-state voltage	I_T=10A		-	1.3	1.65	V
V_{GT}	Gate trigger voltage	V_D=12V;I_T=0.1A		-	0.7	1.5	V
		V_D=400V;I_T=0.1A;T_J=125℃		0.25	0.4	-	V
I_D	Off-state leakage current	V_D=$V_{DRM(max)}$;T_J=125℃		-	0.1	0.5	mA

Dynamic Characteristics

dV_D/dt	Critical rate of rise of Off-state voltage	V_{DM}=67% $V_{DRM(max)}$;Tj=125℃; Exponential wave form;gate open circuit	-	50	-	V/μs
t_{gt}	Gate controlled turn-on time	I_{TM}=12A;V_D=$V_{DRM(max)}$;I_G=0.1A; DI_G/dt=5A/μs	-	2	-	μs

Description

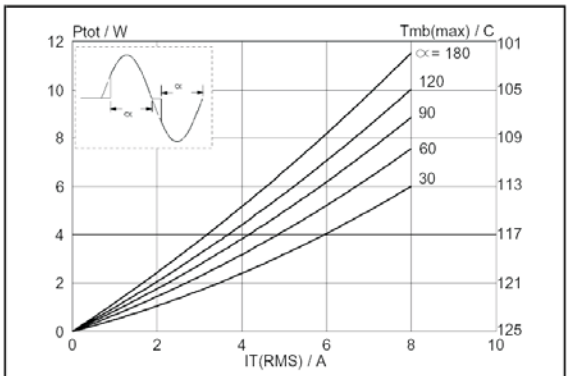


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

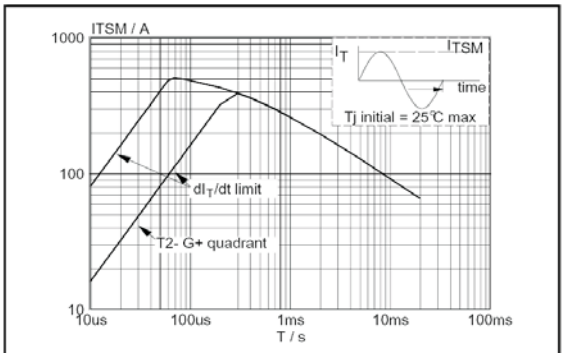


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

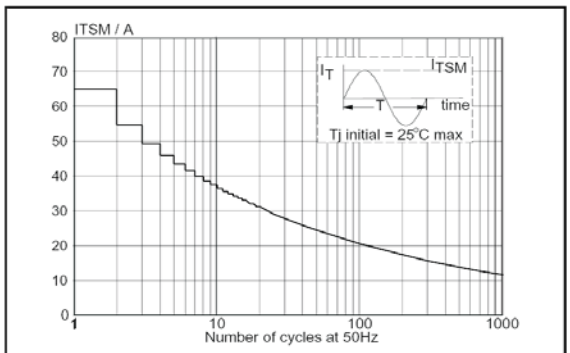


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

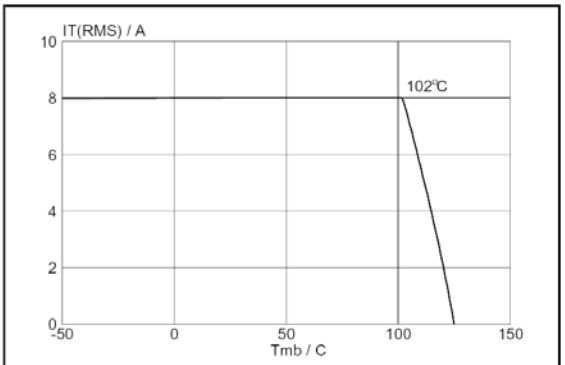


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

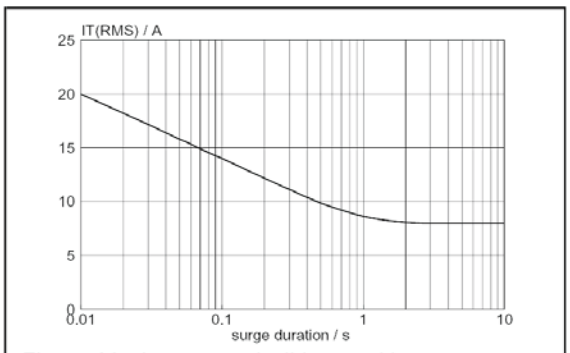


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 102°C$.

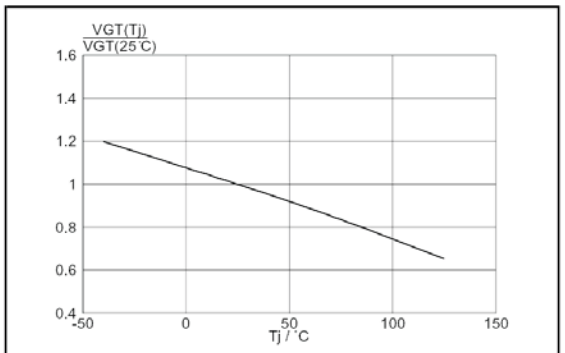


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

Description

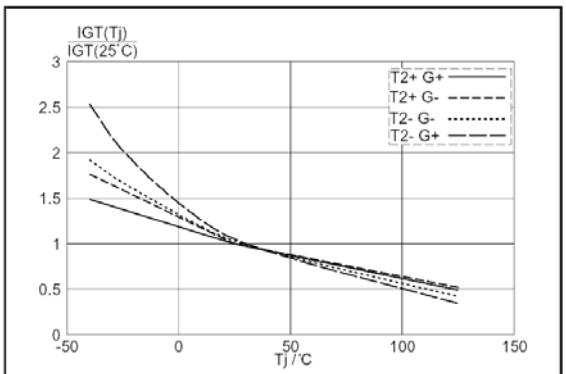


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25^{\circ}C)$, versus junction temperature T_j.

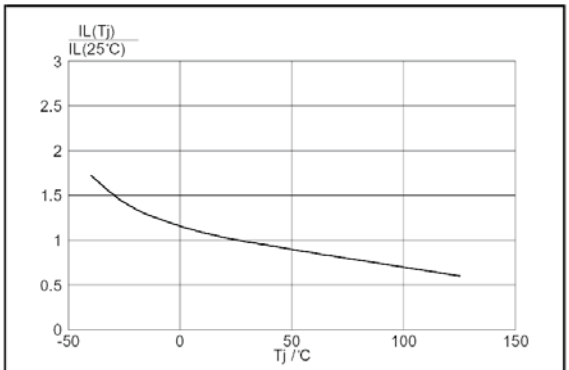


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25^{\circ}C)$, versus junction temperature T_j.

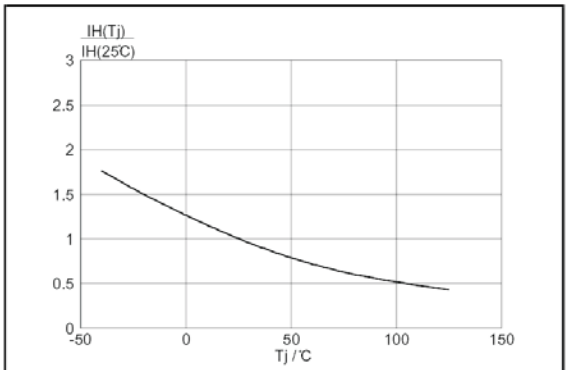


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25^{\circ}C)$, versus junction temperature T_j.

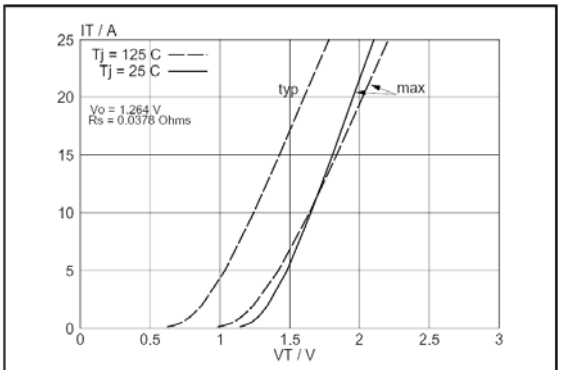


Fig.10. Typical and maximum on-state characteristic.

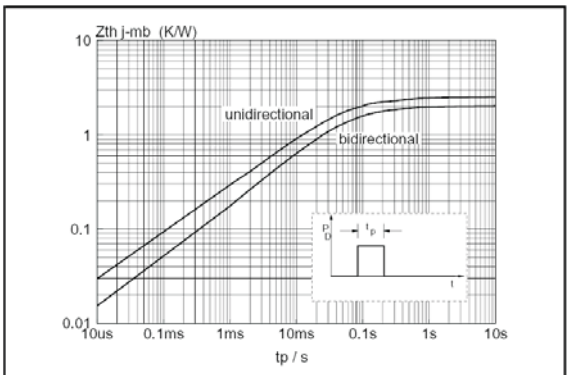


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

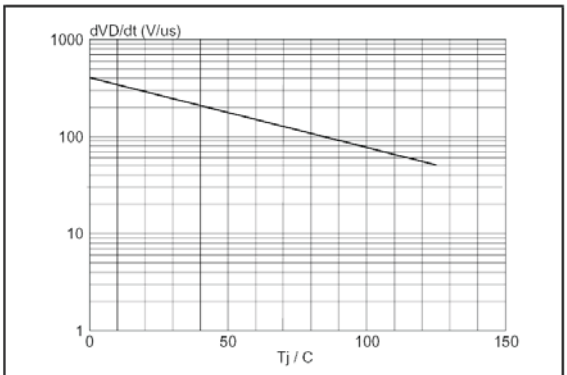


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Dimensions in mm
Net Mass: 2 g