

OptiMOS™3 Power-MOSFET
Features

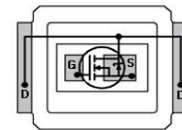
- Optimized for high switching frequency DC/DC converter
- Very low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Low parasitic inductance
- Low profile (<0.7 mm)
- 100% avalanche tested
- 100% Rg Tested
- Double-sided cooling
- Pb-free plating; RoHS compliant
- Compatible with DirectFET® package SQ footprint and outline ¹⁾
- Qualified according to JEDEC²⁾ for target applications

Product Summary

V_{DS}	30	V
$R_{DS(on),max}$	5	mΩ
I_D	60	A

**CanPAK™ S
MG-WDSO-2**


Type	Package	Outline	Marking
BSF050N03LQ3 G	MG-WDSO-2	SQ	1303


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	60	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	38	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}^2$	15	
Pulsed drain current ³⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	240	
Avalanche current, single pulse ⁴⁾	I_{AS}	$T_C=25\text{ °C}$	35	
Avalanche energy, single pulse	E_{AS}	$I_D=35\text{ A}, R_{GS}=25\text{ Ω}$	20	mJ
Gate source voltage	V_{GS}		±20	V

¹⁾ CanPAK™ uses DirectFET® technology licensed from International Rectifier Corporation. DirectFET® is a registered trademark of International Rectifier Corporation.

²⁾ J-STD20 and JESD22

³⁾ See figure 3 for more detailed information

⁴⁾ See figure 13 for more detailed information

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	28	W
		$T_A=25\text{ °C}$, $R_{\text{thJA}}=58\text{ K/W}$	2.2	
Operating and storage temperature	T_j, T_{stg}		-40 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}	bottom	-	1.0		K/W
		top	-	-	4.5	
Device on PCB	R_{thJA}	6 cm ² cooling area ⁵⁾	-	-	58	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=1\text{ mA}$	30	-	-	V
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\text{ }\mu\text{A}$	1	-	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	10	μA
		$V_{\text{DS}}=30\text{ V}, V_{\text{GS}}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=20\text{ A}$	-	5.6	7	m Ω
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=20\text{ A}$	-	4.2	5	
Gate resistance	R_{G}		0.1	0.4	0.7	Ω
Transconductance	g_{fs}	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}, I_{\text{D}}=30\text{ A}$	37	74	-	S

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	2250	3000	pF
Output capacitance	C_{oss}		-	1130	1500	
Reverse transfer capacitance	C_{rss}		-	39	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_G=1.6\ \Omega$	-	3.4	-	ns
Rise time	t_r		-	3.4	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	3.2	-	

Gate Charge Characteristics⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	5.7	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	3.5	-	
Gate to drain charge	Q_{gd}		-	2.7	-	
Switching charge	Q_{sw}		-	5.4	-	
Gate charge total	Q_g		-	11.9	21	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	
Gate charge total	Q_g	$V_{DD}=15\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	25	42	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	10.3	-	
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	18	-	

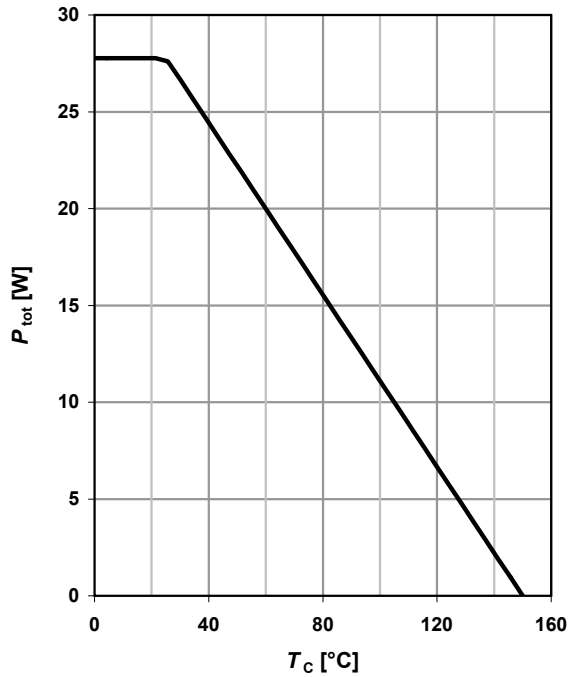
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	25	A
Diode pulse current	$I_{S,pulse}$		-	-	240	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.82	-	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	16	nC

⁶⁾ See figure 16 for gate charge parameter definition

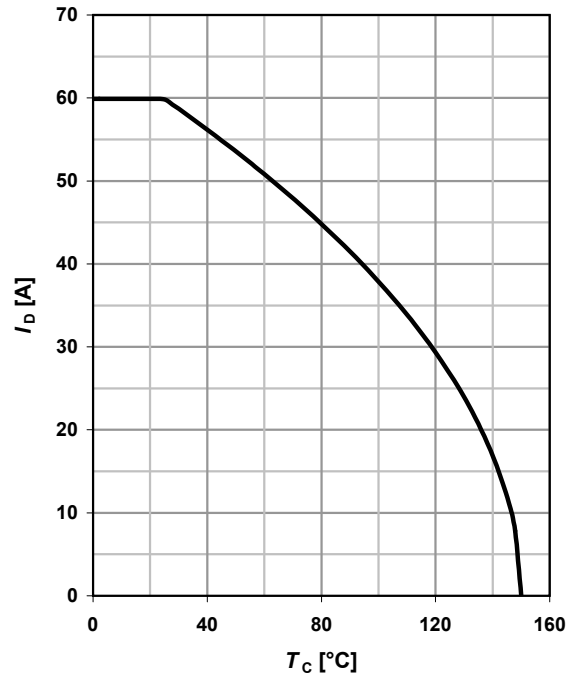
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Drain current

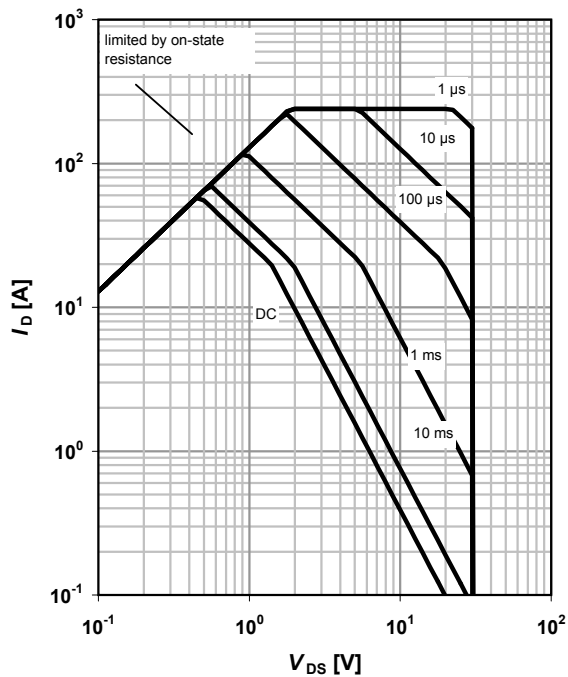
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

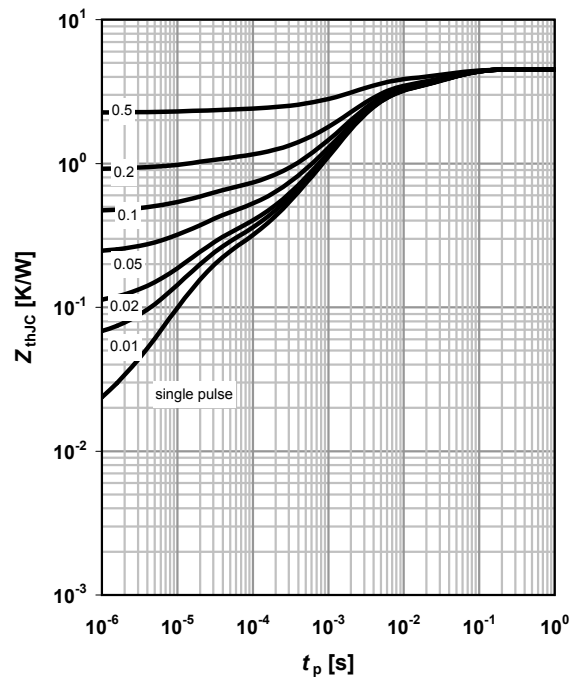
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

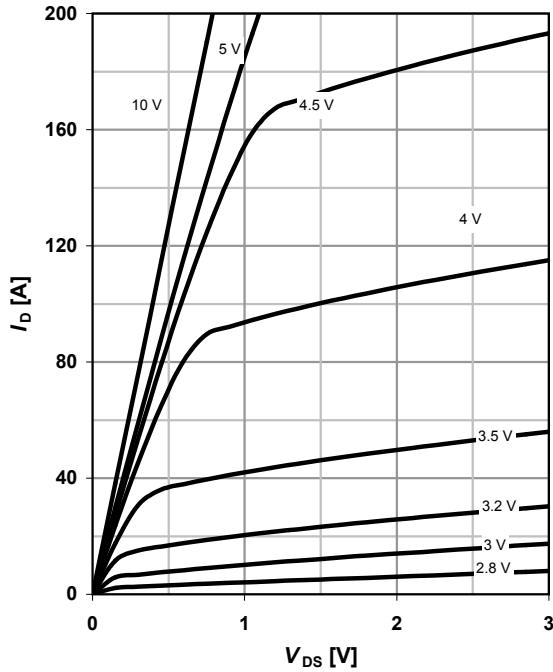
parameter: $D = t_p / T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

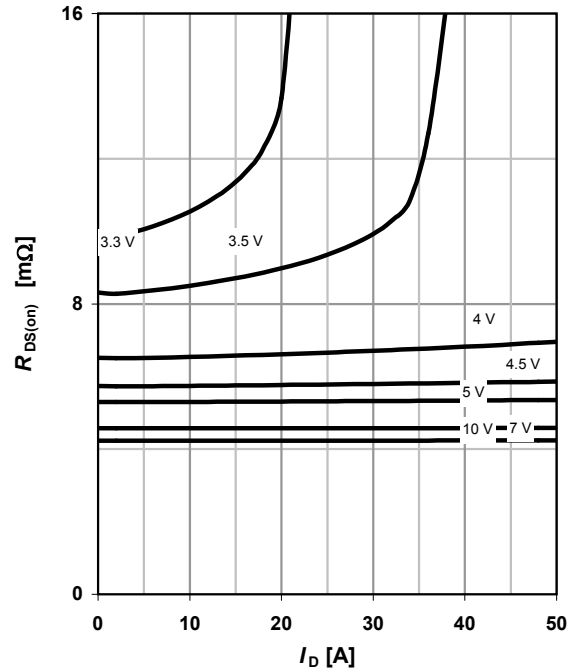
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

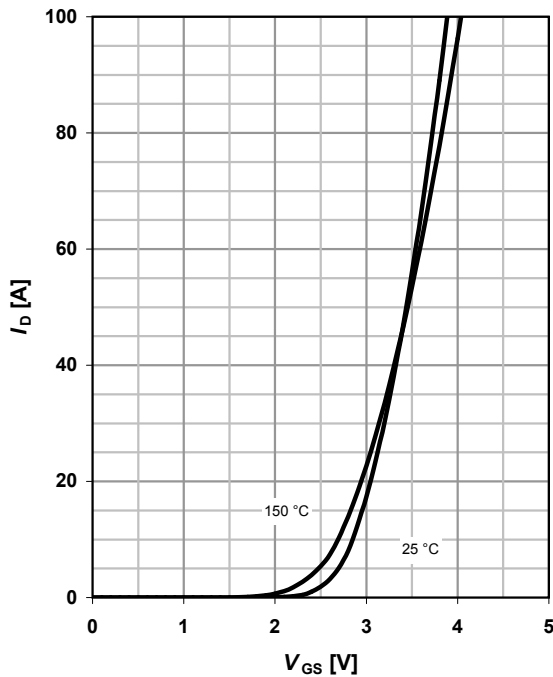
parameter: V_{GS}



7 Typ. transfer characteristics

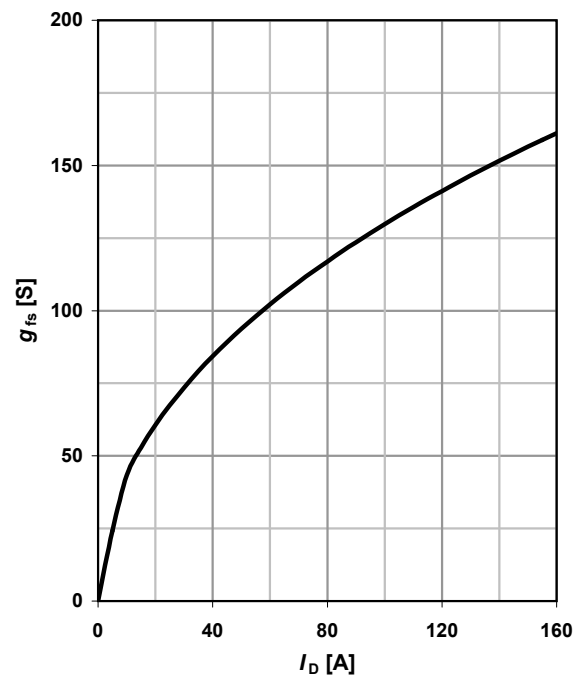
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



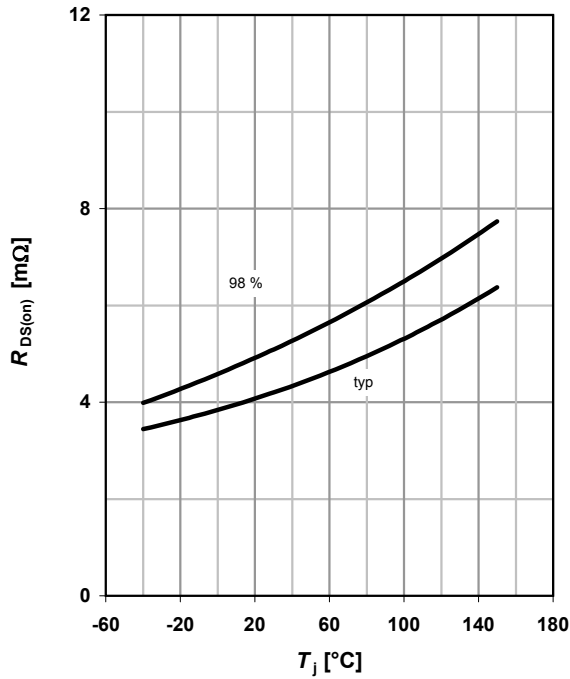
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

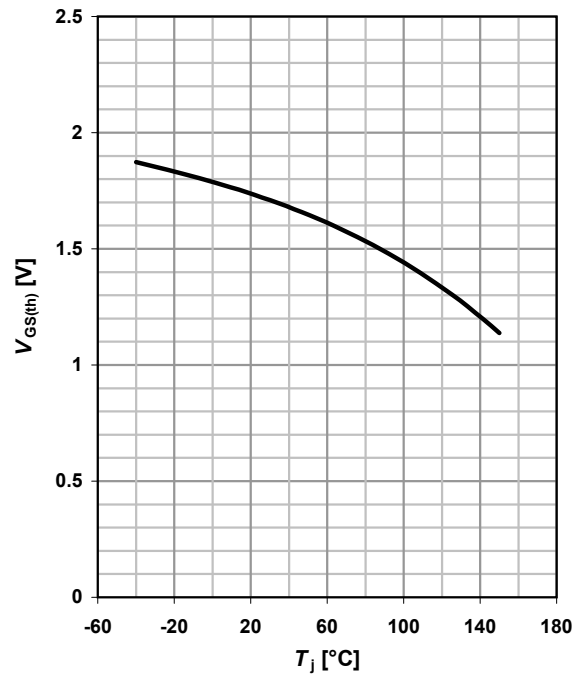


9 Drain-source on-state resistance

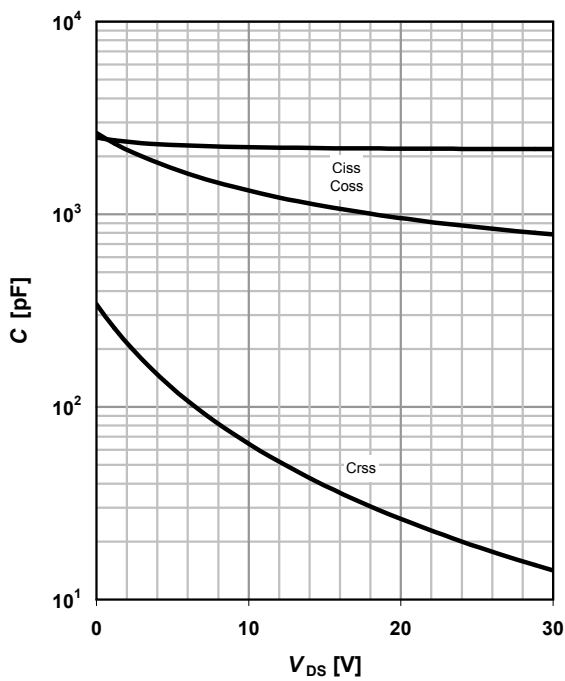
$$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$$


10 Typ. gate threshold voltage

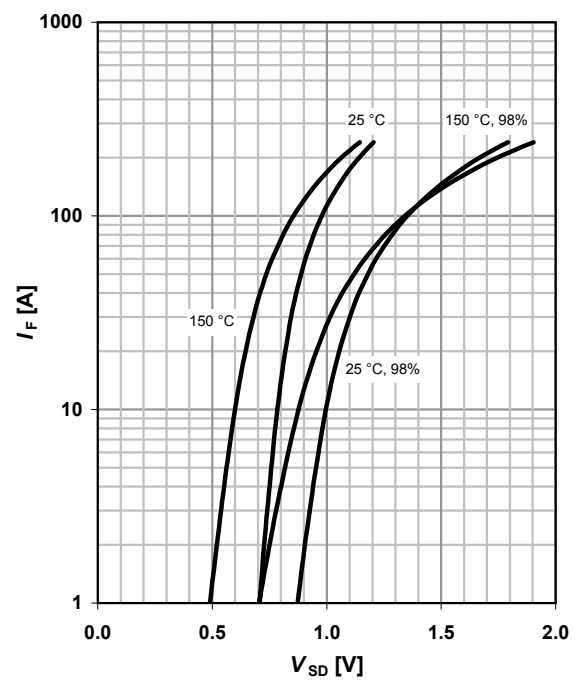
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$$


11 Typ. capacitances

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

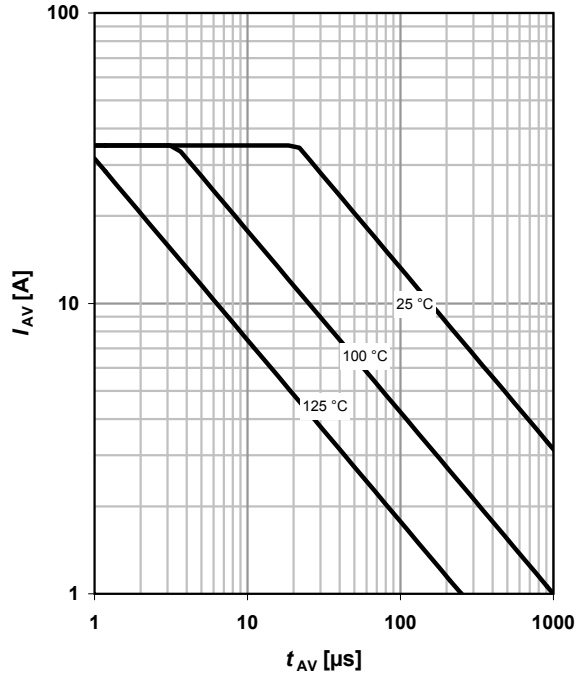

12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

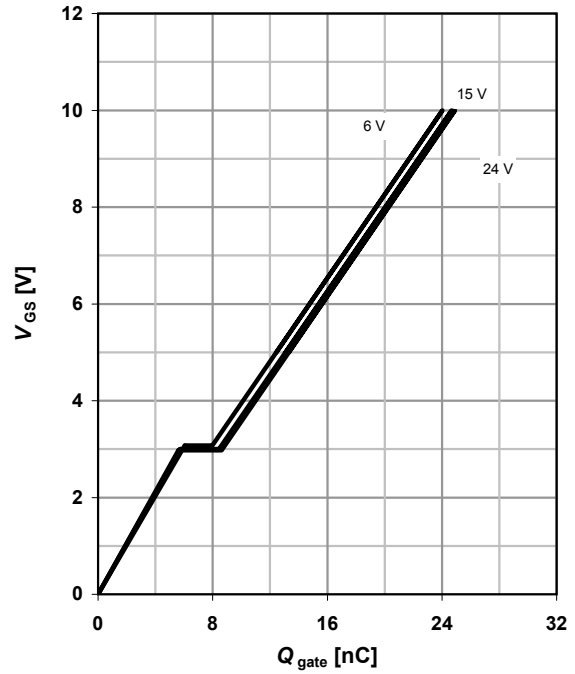
 parameter: T_j


13 Avalanche characteristics

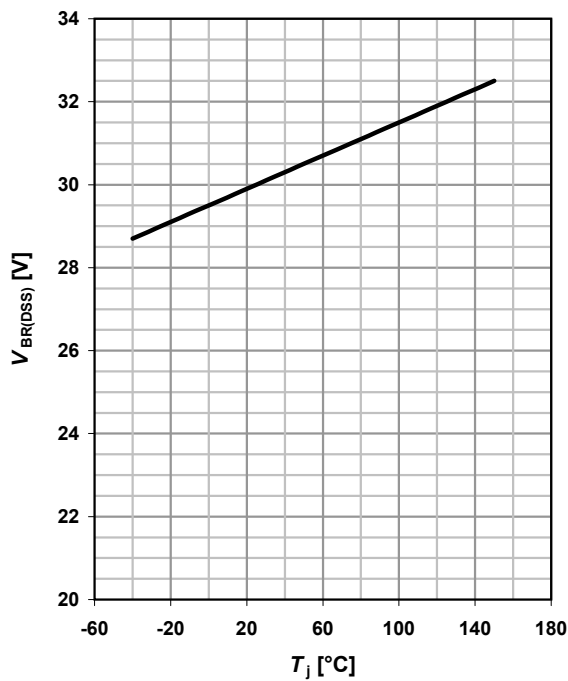
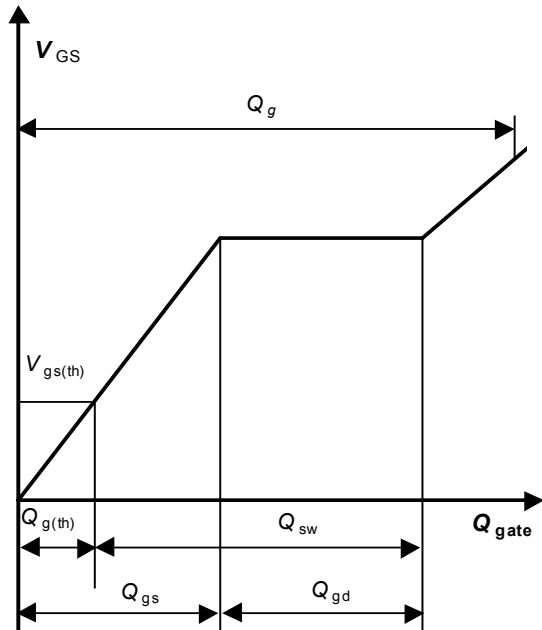
$$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$$

 parameter: $T_{j(\text{start})}$

14 Typ. gate charge

$$V_{GS}=f(Q_{\text{gate}}); I_D=20 \text{ A pulsed}$$

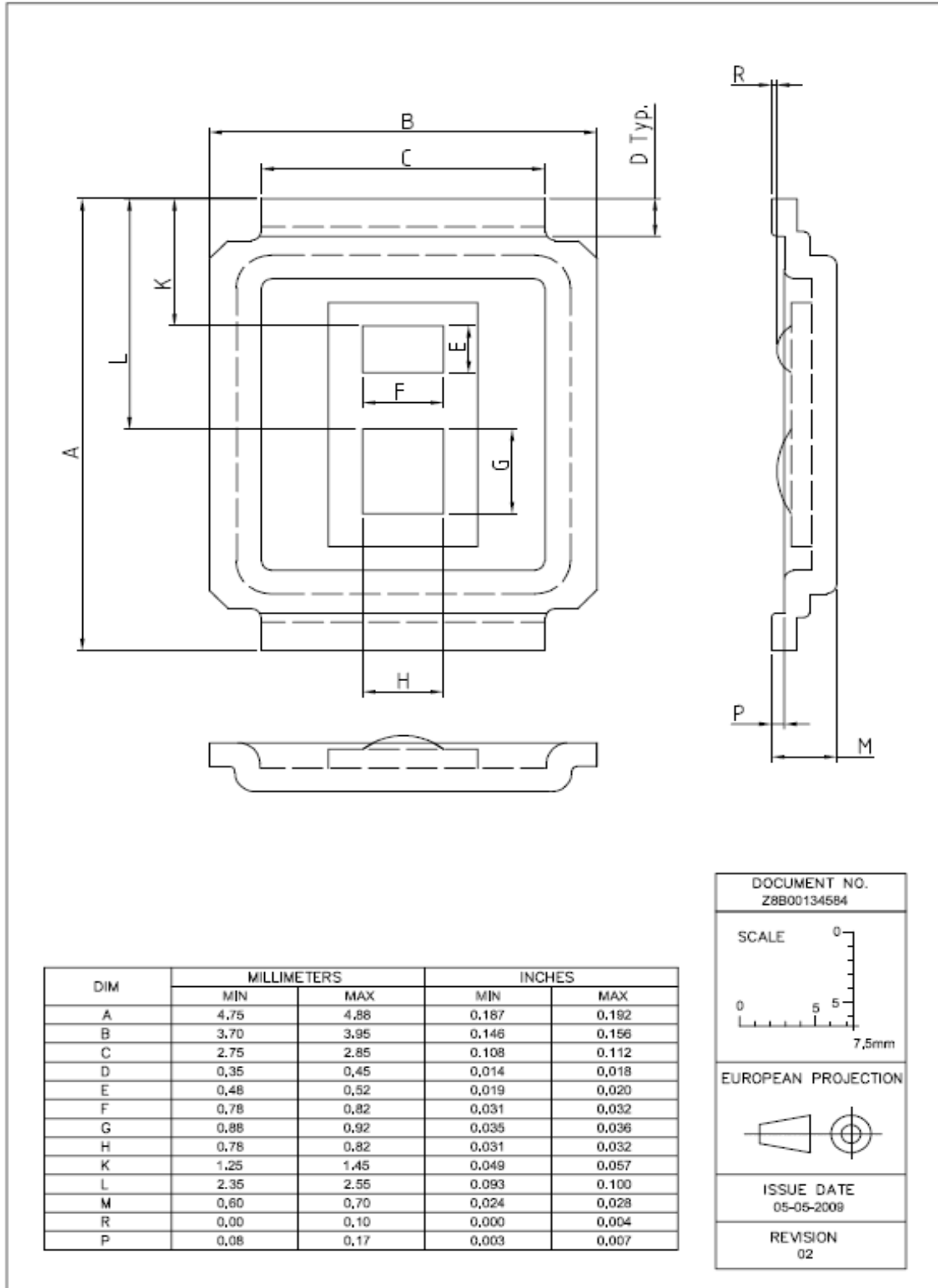
 parameter: V_{DD}

15 Drain-source breakdown voltage

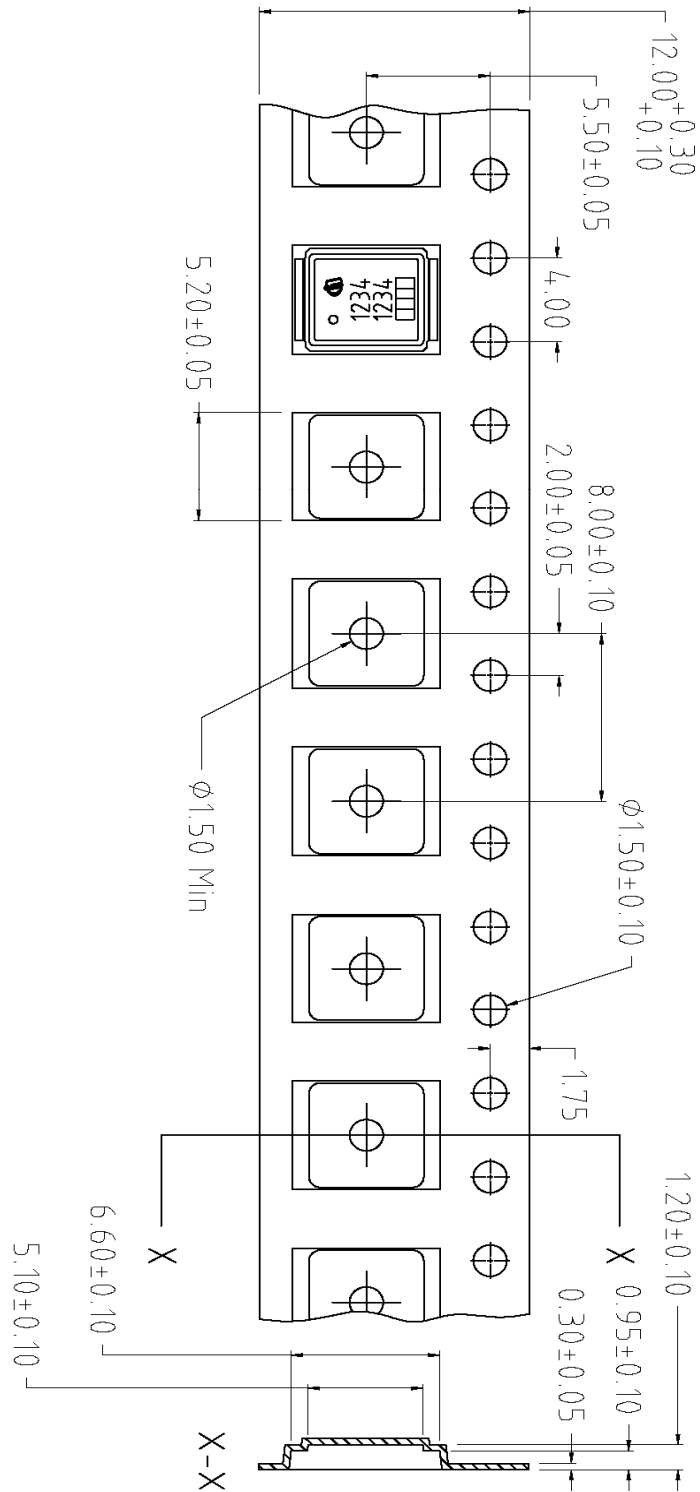
$$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$$

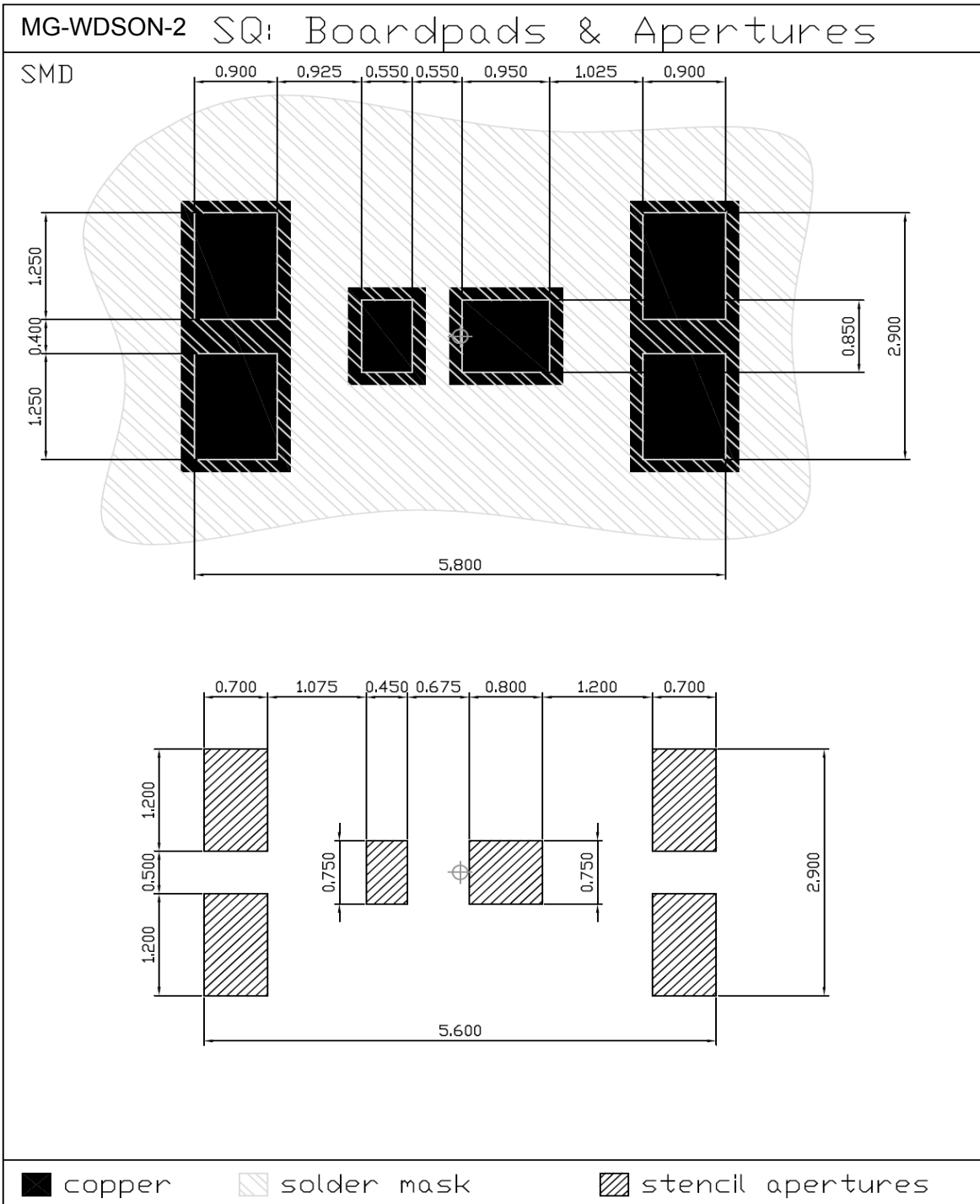

16 Gate charge waveforms


Package Outline

MG-WDSO_N-2



Package Outline
MG-WDSO-2

Dimensions in mm



Dimensions in mm

Recommended stencil thickness 150 μm

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