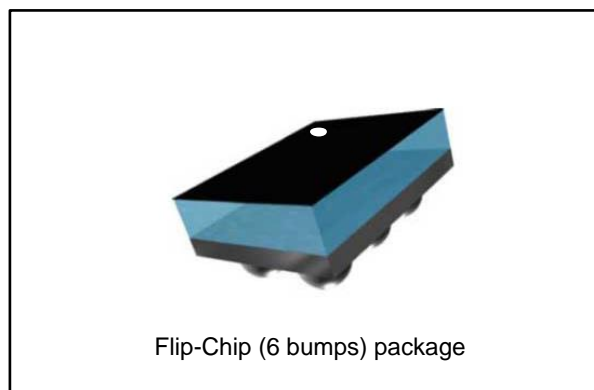


50 ohm nominal input / conjugate match balun to SPIRIT1 434 MHz, with integrated harmonic filter

Datasheet - production data



## Features

- 50  $\Omega$  nominal input / conjugate match to SPIRIT1
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint

## Benefits

- Very low profile < 670  $\mu\text{m}$  after reflow
- High RF performance
- RF BOM and area reduction

## Applications

- 434 MHz impedance matched balun filter
- Optimized for ST chip set SPIRIT1

## Description

STMicroelectronics BALF-SPI-02D3 is an ultra miniature balun. The BALF-SPI-02D3 integrates matching network and harmonics filter. Matching impedance has been customized for the SPIRIT1 ST transceiver.

The BALF-SPI-02D3 uses STMicroelectronics IPD technology on non-conductive glass substrate which optimize RF performance.

Figure 1: Pin coordinates (top view)

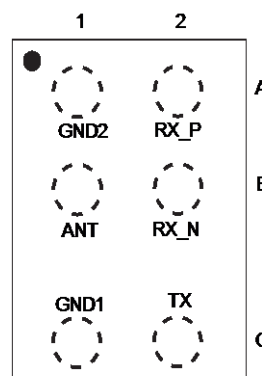


Figure 2: Application schematic (top view)

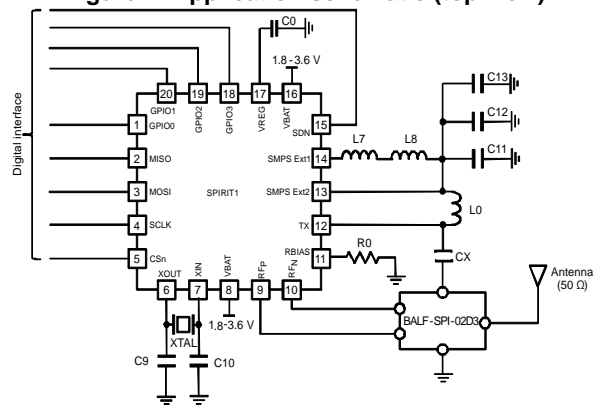


Table 1: Device summary

SMD	PN	Value
L0	LGQ15HSR15J02	150 nH
L7	LQM21FN100M70L	10 $\mu\text{H}$
L8	LQW15AN62NG00	62 nH
C11	GRM188R60J105KA01D	1 $\mu\text{F}$
C12	GRM155R71C104KA88D	100 nF
C13	GRM1555C1H331JA01D	330 pF
CX	GRM1555C1H221JA01	220 pF

# 1 Characteristics

**Table 2: Absolute ratings (limiting values)**

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P <sub>IN</sub>	Input power RF <sub>IN</sub>		-	20	dBm
V <sub>ESD</sub>	ESD ratings MIL STD883C (HBM: C = 100 pF, R = 1.5 kΩ, air discharge)	2000	-		V
	ESD ratings machine model (MM: C = 200 pF, R = 25 Ω, L = 500 nH)	200	-		
T <sub>OP</sub>	Operating temperature	-40	-	+85	°C

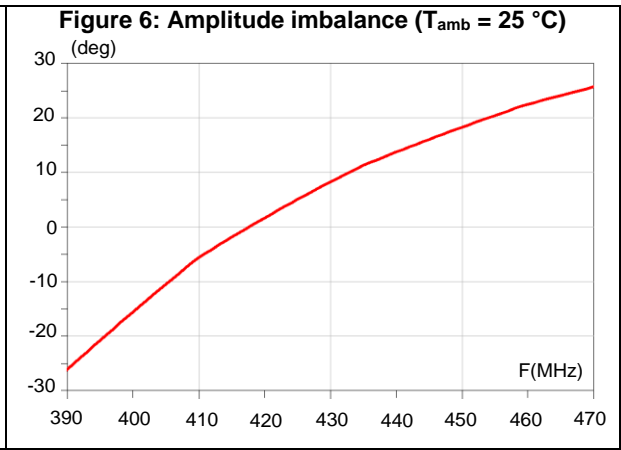
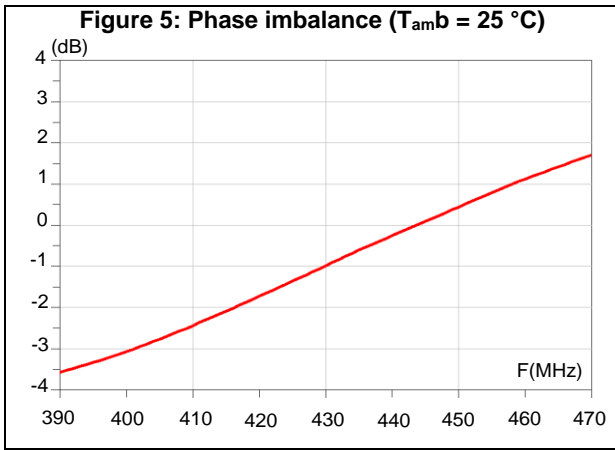
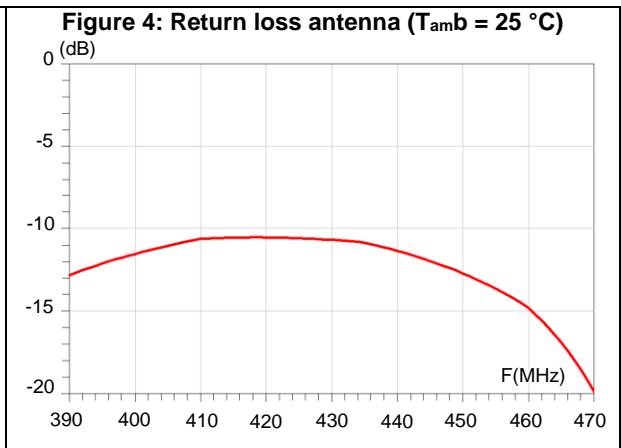
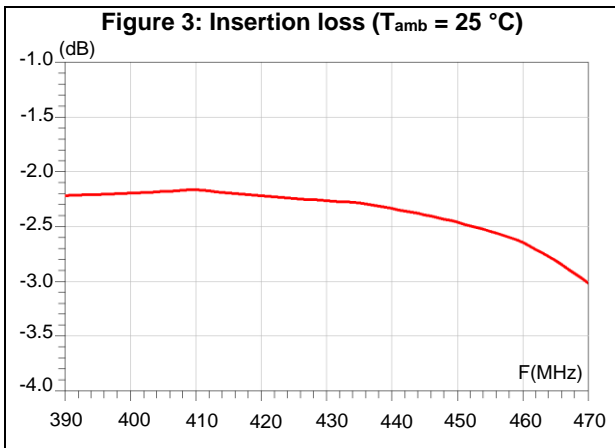
**Table 3: Impedances (T<sub>amb</sub> = 25 °C)**

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z <sub>RX</sub>	Nominal differential RX balun impedance	-	matched SPIRIT1	-	Ω
Z <sub>TX</sub>	Nominal TX filter impedance				
Z <sub>ANT</sub>	Antenna impedance	-	50	-	Ω

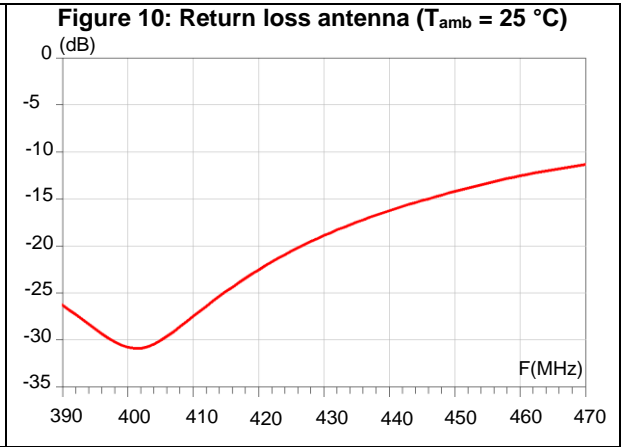
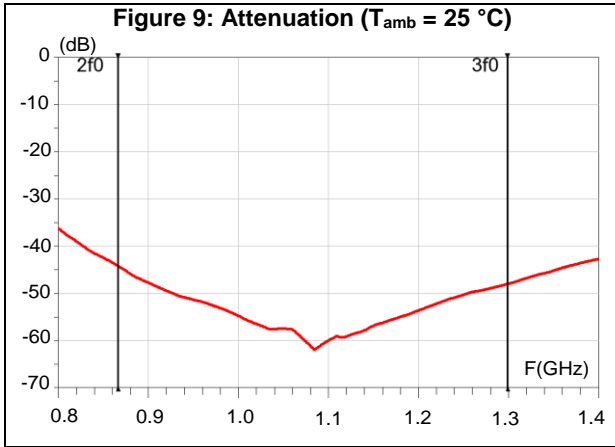
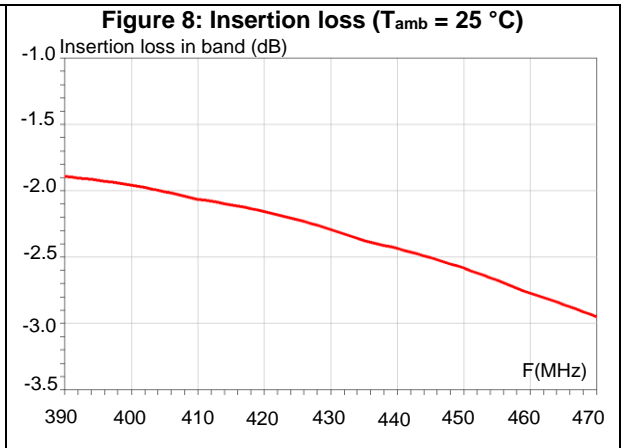
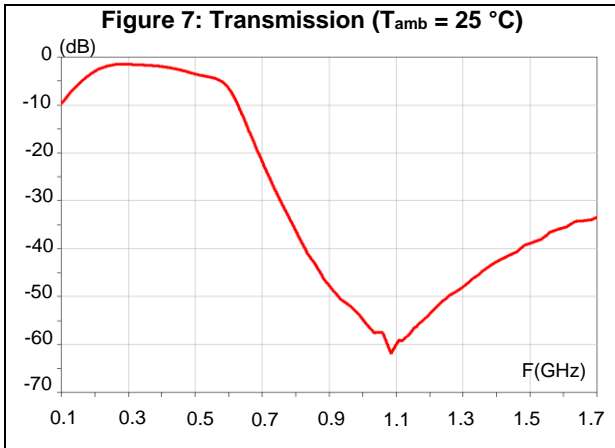
**Table 4: RF performances (T<sub>amb</sub> = 25 °C)**

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
F	Frequency range (bandwidth)			434		MHz
S <sub>21RX-ANT</sub>	Insertion loss in bandwidth without mismatch loss (RX balun)			-2.3	-3.2	dB
S <sub>21TX-ANT</sub>	Insertion loss in bandwidth without mismatch loss (TX filter)			-2.4	-3.2	dB
S <sub>11ANT</sub>	Input return loss in bandwidth (RX balun)			-20	-10.5	dB
S <sub>11ANT</sub>	Input return loss in bandwidth (TX filter)			-32	-11	dB
φ <sub>imb</sub>	Output phase imbalance (RX balun)		-30	10	30	°
A <sub>imb</sub>	Output amplitude imbalance (RX balun)		-3.5	-1	2	dB
Att	Harmonic levels (TX filter)	Attenuation at 2fo	-40	-44		dBm
		Attenuation at 2fo	-40	-45		

### 1.1 RF measurements (Rx balun)



### 1.2 RF measurements (Tx filter)



## 2 Application information

Figure 11: Application board EVB (4 layers)

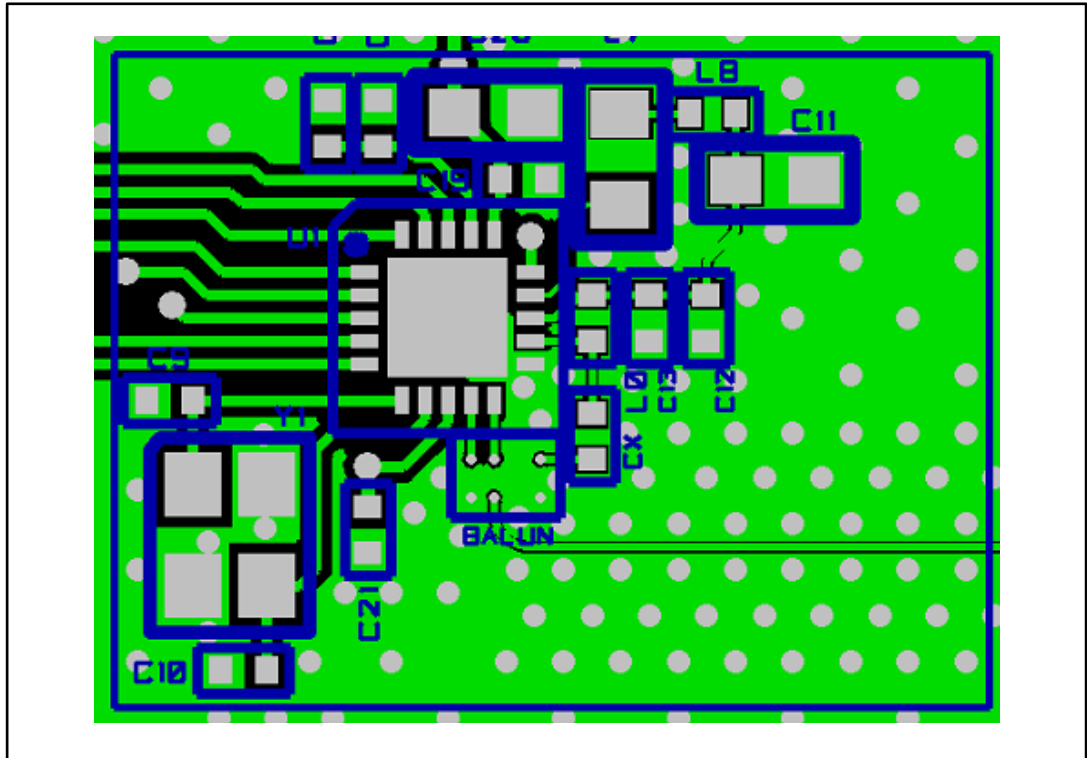


Figure 12: TX output measurements at 433 MHz (LQW15 62nH)

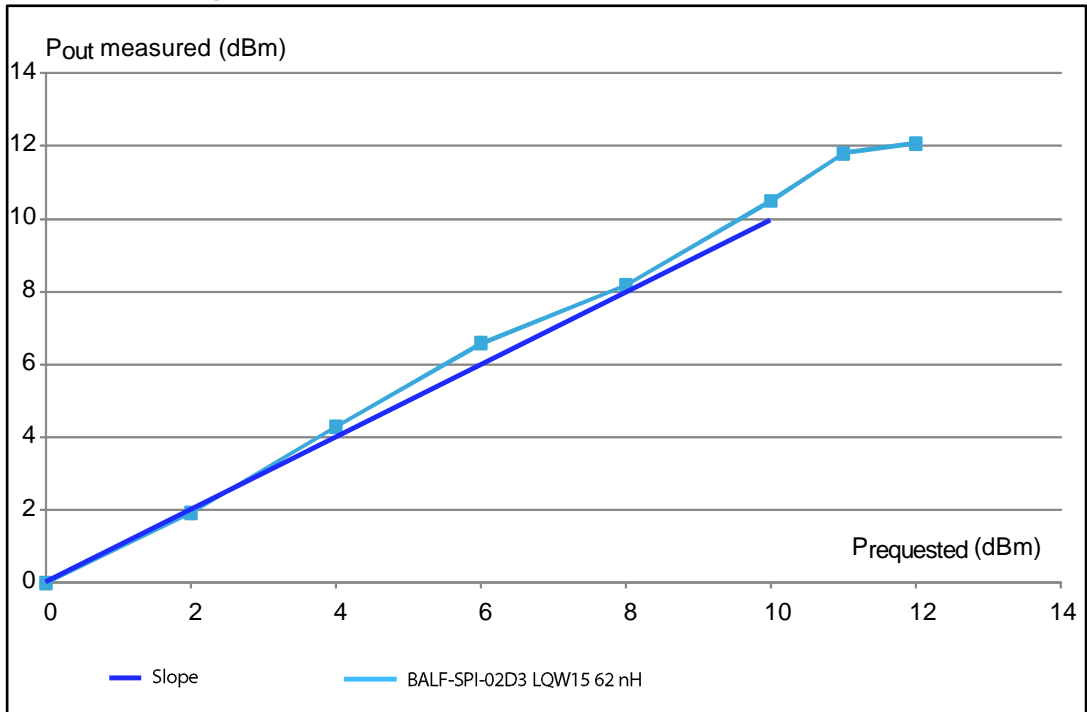
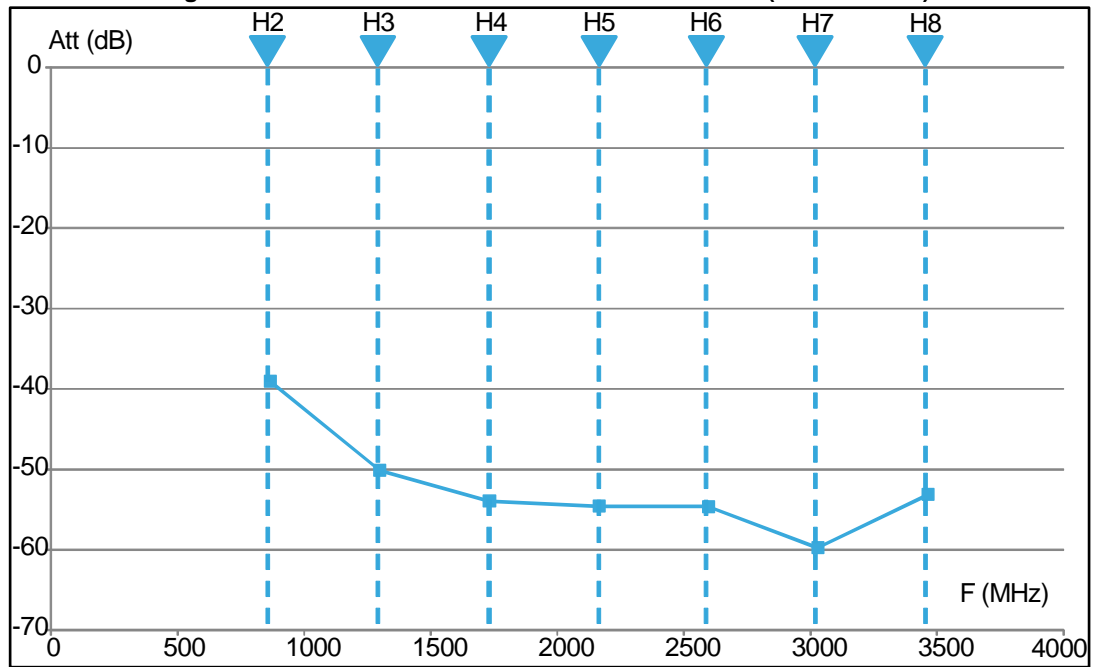


Figure 13: Harmonic measurements at  $P_{out} = 10\text{ dBm}$  (LQW15 62nH)



### 3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

- Epoxy meets UL94, V0
- Lead-free package

#### 3.1 Flip-Chip 6 bumps package information

Figure 14: Flip-Chip 6 bumps package outline (top and side view)

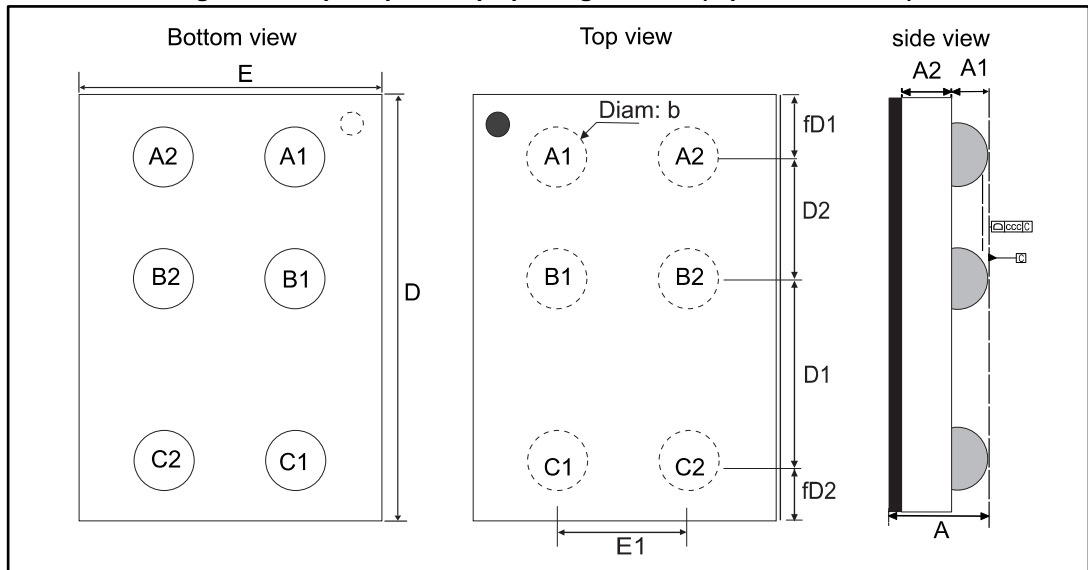
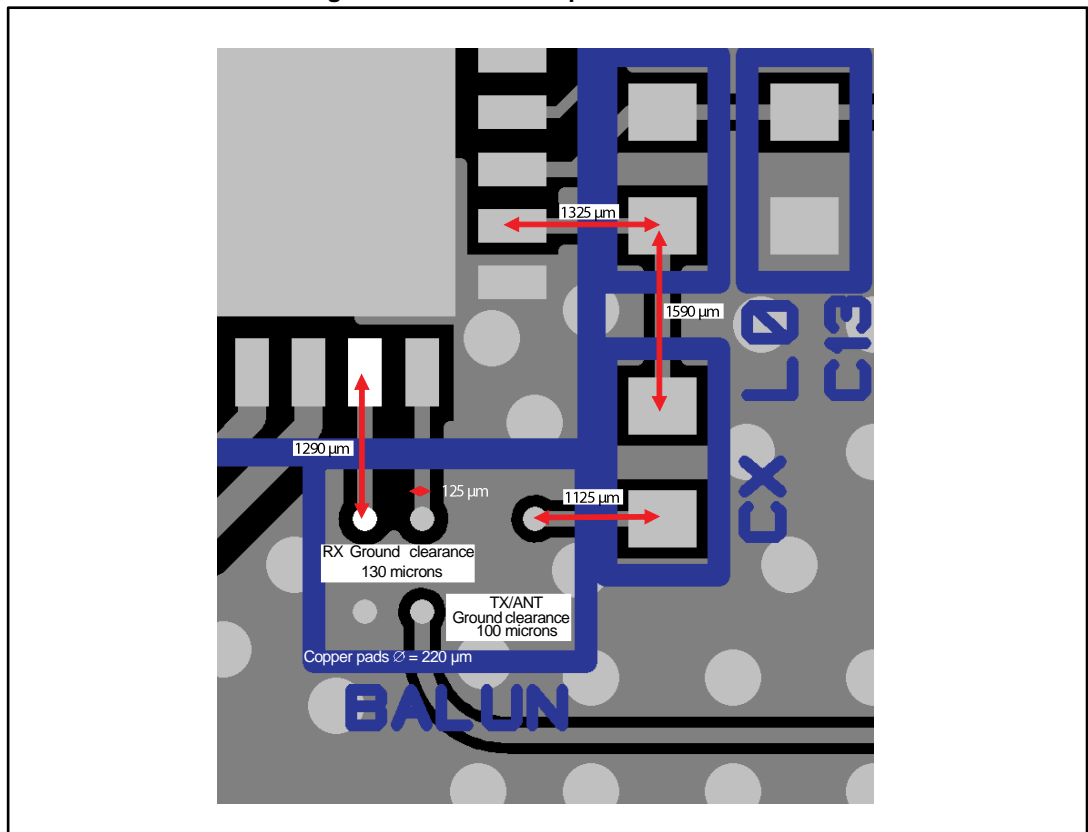


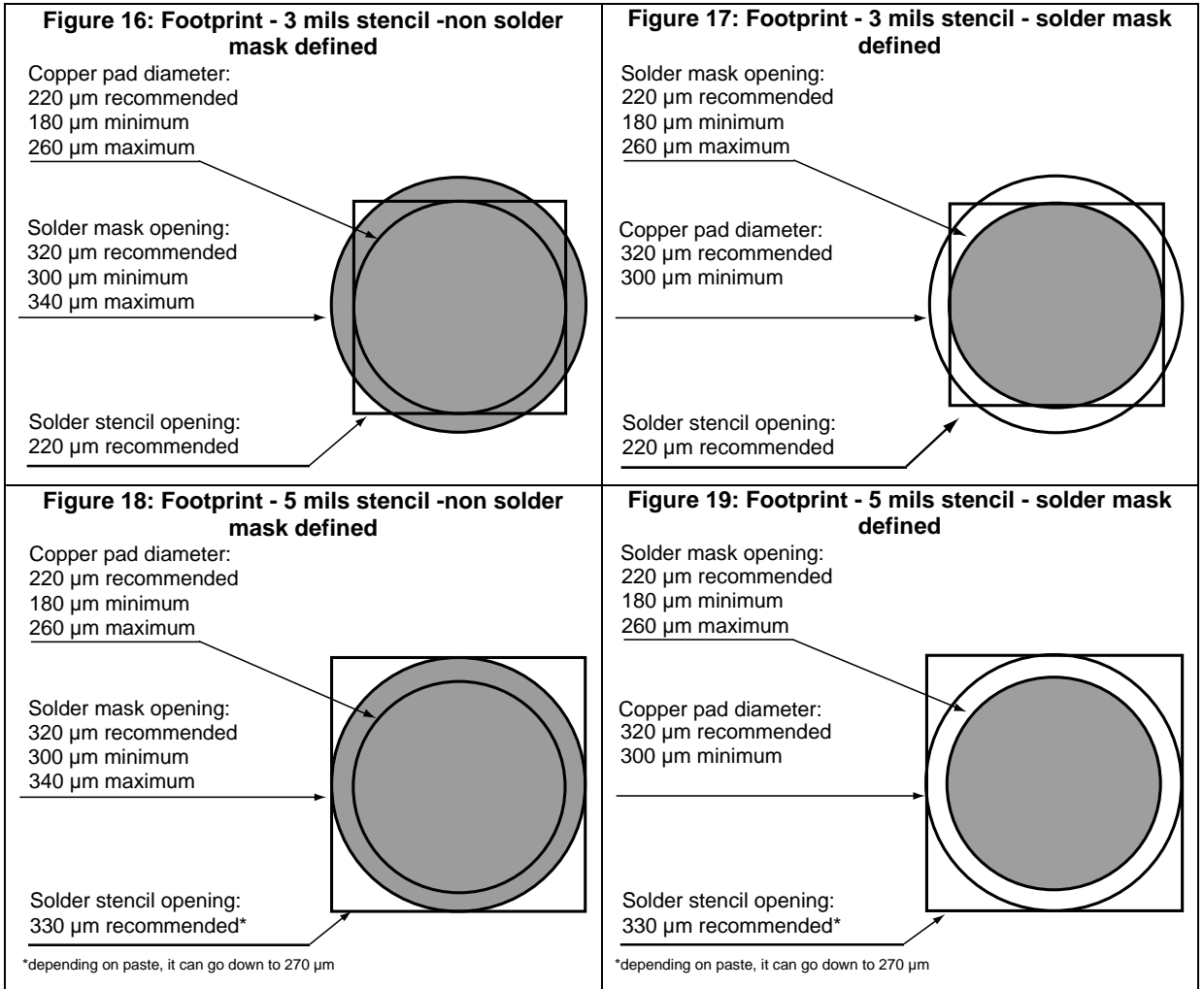
Table 5: Flip-Chip 6 bumps dimensions

Parameter	Description	Min.	Typ.	Max.	Unit
A	Bump height + substrate thickness	0.590	0.650	0.710	mm
A1	Bump height		0.200		mm
A2	Substrate thickness		0.400		mm
b	Bump diameter	0.210	0.250	0.290	mm
D	Y dimension of the die	1.950	2.000	2.050	mm
D1	Y pitch	0.960	1.000	1.040	mm
D2	Y pitch2	0.460	0.500	0.540	mm
E	X dimension of the die	1.350	1.400	1.450	mm
E1	X pitch	0.790	0.820	0.850	mm
fD1	Distance from bump to edge of die on Y axis		0.295		mm
fD2	Distance from bump to edge of die on Y axis		0.195		mm
ccc				005	mm

Figure 15: PCB stack-up recommendation







### 3.2 Flip-chip 6 bumps packing information

Figure 20: Marking

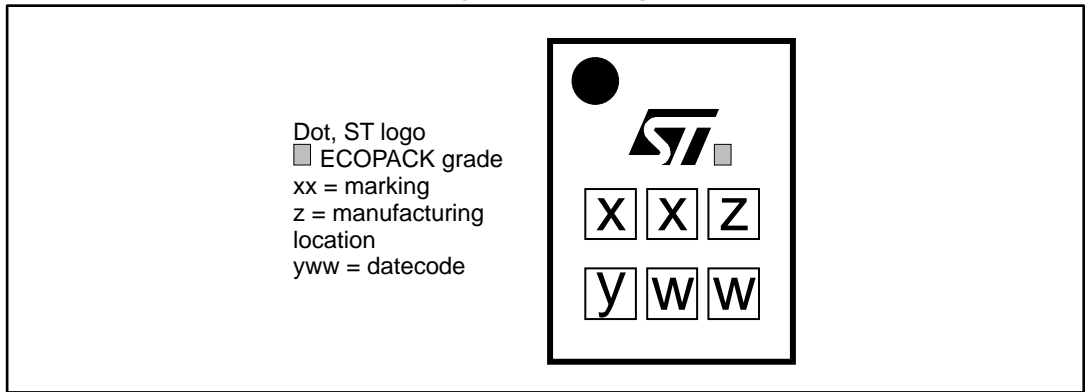
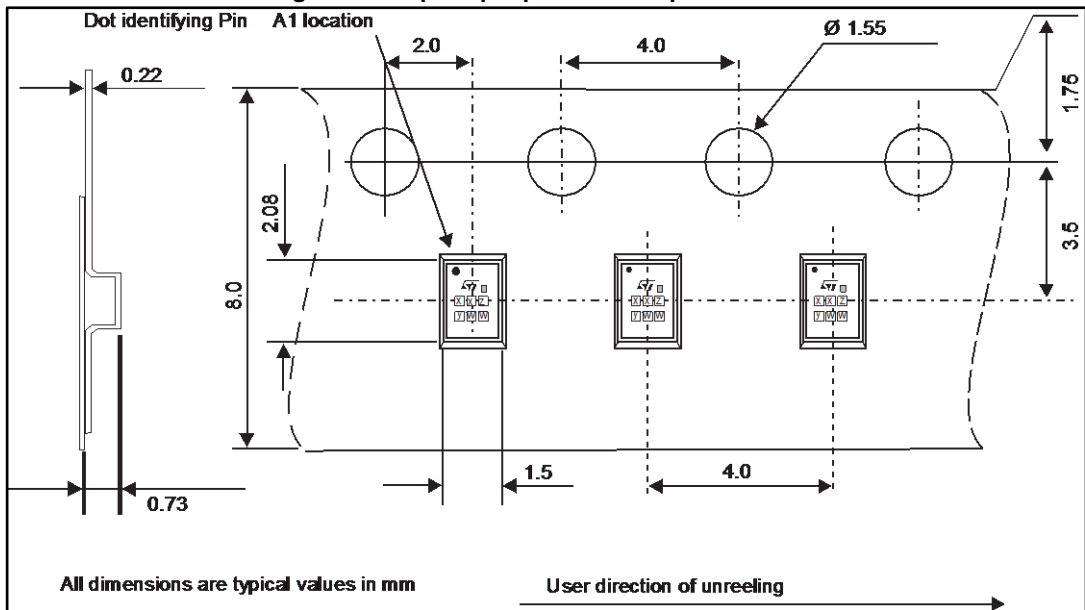


Figure 21: Flip Chip tape and reel specifications



More packing information is available in the application note:

- AN2348 Flip-Chip: “Package description and recommendations for use”

## 4 Ordering information

Table 6: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BALF-SPI-02D3	TD	Flip-Chip 6 bumps	3.0 mg	5000	Tape and reel

## 5 Revision history

Table 7: Document revision history

Date	Revision	Changes
13-Jan-2015	1	Initial release.
15-May-2015	2	Updated Table 4. Added Figure 12, Figure 13, Figure 18 and Figure 19.
18-Sep-2015	3	Updated Figure 14 and added Figure 5.
22-Mar-2017	4	Updated <a href="#">Figure 14: "Flip-Chip 6 bumps package outline (top and side view)"</a> .

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