

**Features**

- Leadfree, RoHS compliant
- Automotive qualified
- One high side output and internal low side Vs recharge.
- CMOS Schmitt trigger inverted input with pull up resistor
- CMOS Schmitt trigger inverted reset with pull down resistor
- 5V compatible logic level inputs
- Immune to -Vs spike and tolerant to dVs/dt

**Typical Applications**

- Common Rail Injections
- Diesel/Gasoline Direct Injections
- Solenoid Drivers
- Actuators and brushed DC motors

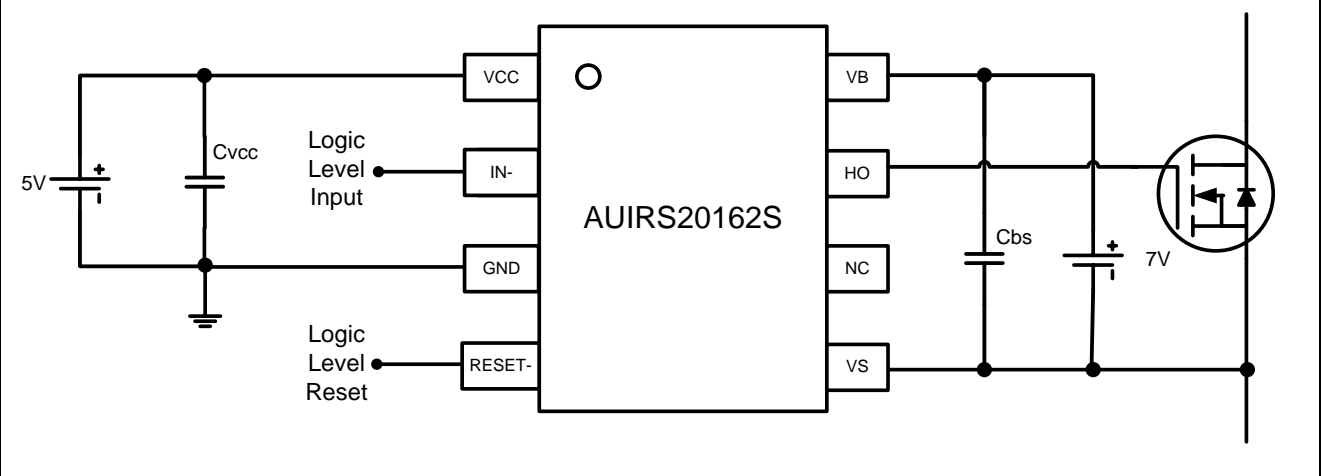
**Product Summary**

Topology	Low side input, high side driver with Vs recharge
V <sub>OFFSET</sub>	150 V
V <sub>OUT</sub>	4.4 V – 20 V
I <sub>o+</sub> & I <sub>o-</sub> (typical)	0.25 A
t <sub>ON</sub> & t <sub>OFF</sub> (typical)	150 ns
Deadtime DT <sub>ON</sub> / DT <sub>OFF</sub> (typical)	70ns / 6 us

**Package Options**



**Typical Connection Diagram**



Orderable Part Number	Package Type	Standard Pack		Note
		Form	Quantity	
AUIRS20162S(TR)	SOIC8	Tape and Reel	2500	

### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. These are stress ratings only, functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Condition" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. All voltage parameters are absolute voltages referenced to GND unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{BS}$	High Side Floating Supply Voltage	-0.3	20	V
$V_B$	High Side Driver Output Stage Voltage, Neg. transient: 0.5 ms, external MOSFET off	-5.0	166	V
$V_S$	High Side Floating Supply Offset Voltage Neg. transient 0.4 $\mu$ s	-8.0	150	V
$V_{HO}$	Output Voltage Gate Connection	$V_S - 0.3$	$V_B + 0.3$	V
$V_{CC}$	Supply Voltage	-0.3	20	V
$V_{IN}$	Input Voltage	-0.3	$V_{CC} + 0.3$	V
$I_{IN}$	Input Injection Current. Full function, no latch-up; (guaranteed by design). Test at 5V and 7V on Eng. Samples.	---	+1	mA
$V_{RES}$	Reset Input Voltage	-0.3	$V_{CC} + 0.3$	V
dV/dt	Allowable Offset Voltage Slew Rate	-50	50	V/nsec
RthJA	Thermal resistance, junction to ambient	-	200	$^{\circ}$ C/W
$T_J$	Junction Temperature	-55	150	$^{\circ}$ C
$T_S$	Storage Temperature	-55	150	$^{\circ}$ C

### Recommended Operating Conditions

For proper operations the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
$V_B^{\dagger}$	High Side Driver Output Stage Voltage	$V_S + 4.4$	$V_S + 20$	V
$V_S$	High Side Floating Supply Offset Voltage	-3	150	V
$V_{HO}$	Output Gate Voltage	$V_S$	$V_B$	V
$V_{CC}^{\dagger\dagger\dagger}$	Supply Voltage	4.4	6.5	V
$V_{IN}$	Input Voltage	0	$V_{CC}$	V
$V_{RES}$	Reset Input Voltage	0	$V_{CC}$	V
$T_a$	Ambient Temperature	-40	125	$^{\circ}$ C
$f_s$	Switching frequency <sup>††</sup> (load: 50 Ohm, 2.5nF into $V_S$ )	---	200	kHz
$t_{inlow\_min}$	Minimum low input width <sup>†††</sup>	1000	---	ns
$t_{inhigh\_min}$	Minimum high input width <sup>†††</sup>	60	---	ns

<sup>†</sup> Reset-logic functional for  $V_{BS} > 2V$

<sup>††</sup> Duty cycle = 0.5,  $V_{BS} = 7V$

<sup>†††</sup> Guaranteed by design. Pulse width below the specified values may be ignored. Output will either follow the input or will ignore it. No false output state is guaranteed when minimum input width is smaller than  $t_{in}$ .

<sup>††††</sup> Logic operation functional for  $V_{CC} > 2.7V$ , see also table Table 1 on page 10.

### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ . Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^\circ C \leq T_j \leq 125^\circ C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>V<sub>CC</sub> Supply Characteristics</b>						
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold			4.3	V	$V_{CC}$ rising from 0V
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	2.8				$V_{CC}$ dropping from 5V
$V_{CCUVHYS}$	$V_{CC}$ Supply Undervoltage Lockout Hysteresis	0.02	0.3	0.60		
$t_{dUVCC}$	Undervoltage Lockout Response Time	0.5		20	$\mu sec$	$V_{CC}$ steps either from 6.5V to 2.7V or from 2.7V to 6.5V
$I_{QCC}$	$V_{CC}$ Supply Current			400	$\mu A$	$V_{CC} = 3.6V \text{ \& } 6.5V$
<b>V<sub>BS</sub> Supply Characteristics</b>						
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold			5.4	V	$V_{BS}$ rising from 0V
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold	3.9				$V_{BS}$ dropping from 5V
$V_{BSUVHYS}$	$V_{BS}$ Supply Undervoltage Lockout Hysteresis	0.02	0.3	0.60		
$t_{dUVBS}$	Undervoltage Lockout Response Time	0.5		20	$\mu sec$	$V_{BS}$ steps either from 6.5V to 2.7V or from 2.7V to 6.5V
$I_{QBS1}$	$V_{BS}$ Supply Current			130	$\mu A$	static mode, $V_{BS} = 7V$ , $I_N = 0V$ or 5V
$I_{QBS2}$	$V_{BS}$ Supply Current			300	$\mu A$	static mode, $V_{BS} = 16V$ , $I_N = 0V$ or 5V
$\Delta V_{BS}^\dagger$	$V_{BS}$ Drop Due to Output Turn-On			210	mV	$V_{BS} = 7V$ , $C_{BS} = 1\mu F$ , $t_{d\_Igen-IN} = 3\mu sec$ , $t_{TEST} = 100\mu sec$ , No load

<sup>†</sup> See also Fig. 4 and 5

### Electrical Characteristics

Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ . Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^\circ C \leq T_j \leq 125^\circ C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Gate Driver Characteristics</b>						
$I_{PKSo1}$	Peak Output Source Current	120	250		mA	$T_j = 25^\circ C$ , <sup>††</sup>
$I_{PKSo2}$	Peak Output Source Current	70			mA	<sup>††</sup>
$I_{PKSo3}$	Peak Output Source Current	250	500		mA	$V_{BS} = 16V$ , $T_j = 25^\circ C$ <sup>††</sup>
$I_{PKSo4}$	Peak Output Source Current	150			mA	$V_{BS} = 16V$ <sup>††</sup>
$t_{r1}$	Output Rise Time		0.2	0.4	$\mu sec$	$T_j = 25^\circ C$
$t_{r2}$	Output Rise Time			0.5	$\mu sec$	
$t_{r3}$	Output Rise Time		0.1	0.2	$\mu sec$	$V_{BS} = 16V$ , $T_j = 25^\circ C$
$t_{r4}$	Output Rise Time			0.3	$\mu sec$	$V_{BS} = 16V$
$I_{PKSi1}$	Peak Output Sink Current	120	250		mA	$I_N = 5V$ , $T_j = 25^\circ C$ <sup>††</sup>
$I_{PKSi2}$	Peak Output Sink Current	70			mA	$I_N = 5V$ , <sup>††</sup>
$I_{PKSi3}$	Peak Output Sink Current	250	500		mA	$V_{BS} = 16V$ , $I_N = 5V$ , $T_j = 25^\circ C$ <sup>††</sup>
$I_{PKSi4}$	Peak Output Sink Current	150			mA	$V_{BS} = 16V$ , $I_N = 5V$ <sup>††</sup>
$t_{f1}$	Output Fall Time		0.2	0.4	$\mu sec$	$I_N = 5V$ , $T_j = 25^\circ C$
$t_{f2}$	Output Fall Time			0.5	$\mu sec$	$I_N = 5V$
$t_{f3}$	Output Fall Time		0.1	0.2	$\mu sec$	$V_{BS} = 16V$ , $I_N = 5V$ , $T_j = 25^\circ C$
$t_{f4}$	Output Fall Time			0.3	$\mu sec$	$V_{BS} = 16V$ , $I_N = 5V$
$t_{p1h}$	Input-to-Output Turn-On Propagation Delay (50% input level to 10% output level)		0.15	0.35	$\mu sec$	
$t_{p1l}$	Input-to-Output Turn-Off Propagation Delay (50% input level to 90% output level)		0.15	0.35	$\mu sec$	
$t_{p1h\_res}$	RES-to-Output Turn-Off Propagation Delay (50% input level to 90% [ $t_{p1l}$ ] output levels)		0.15	0.35	$\mu sec$	
$t_{p1h\_res}$	RES-to-Output Turn-On Propagation Delay (50% input level to 10% [ $t_{p1h}$ ] output levels)		0.15	0.35	$\mu sec$	

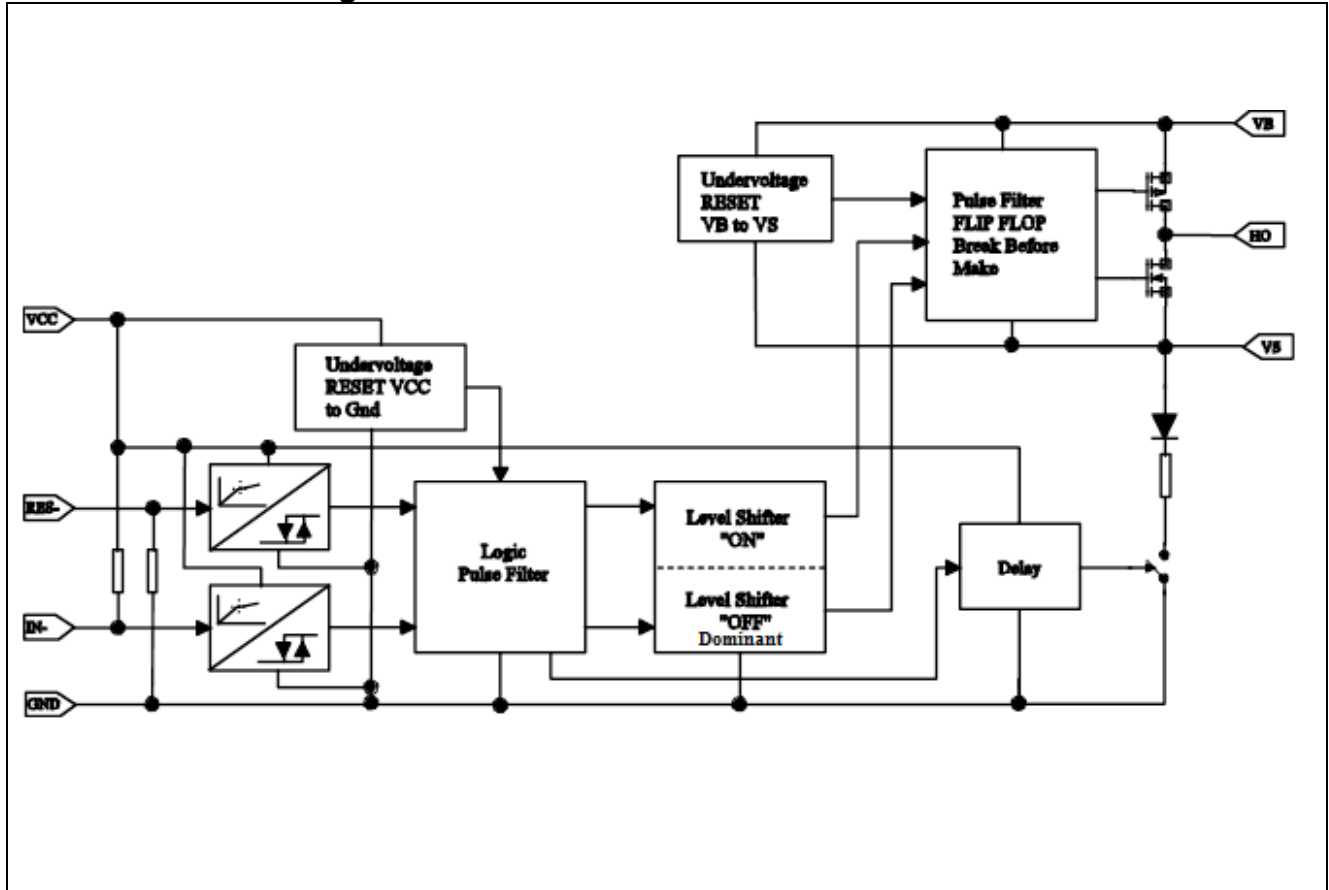
<sup>††</sup>: Peak Output Sink and Source Current tests are performed with the output shorted and therefore highly dissipative. Therefore, it is not recommended that this test be performed for longer than 10 $\mu sec$  at a time.

### Electrical Characteristics

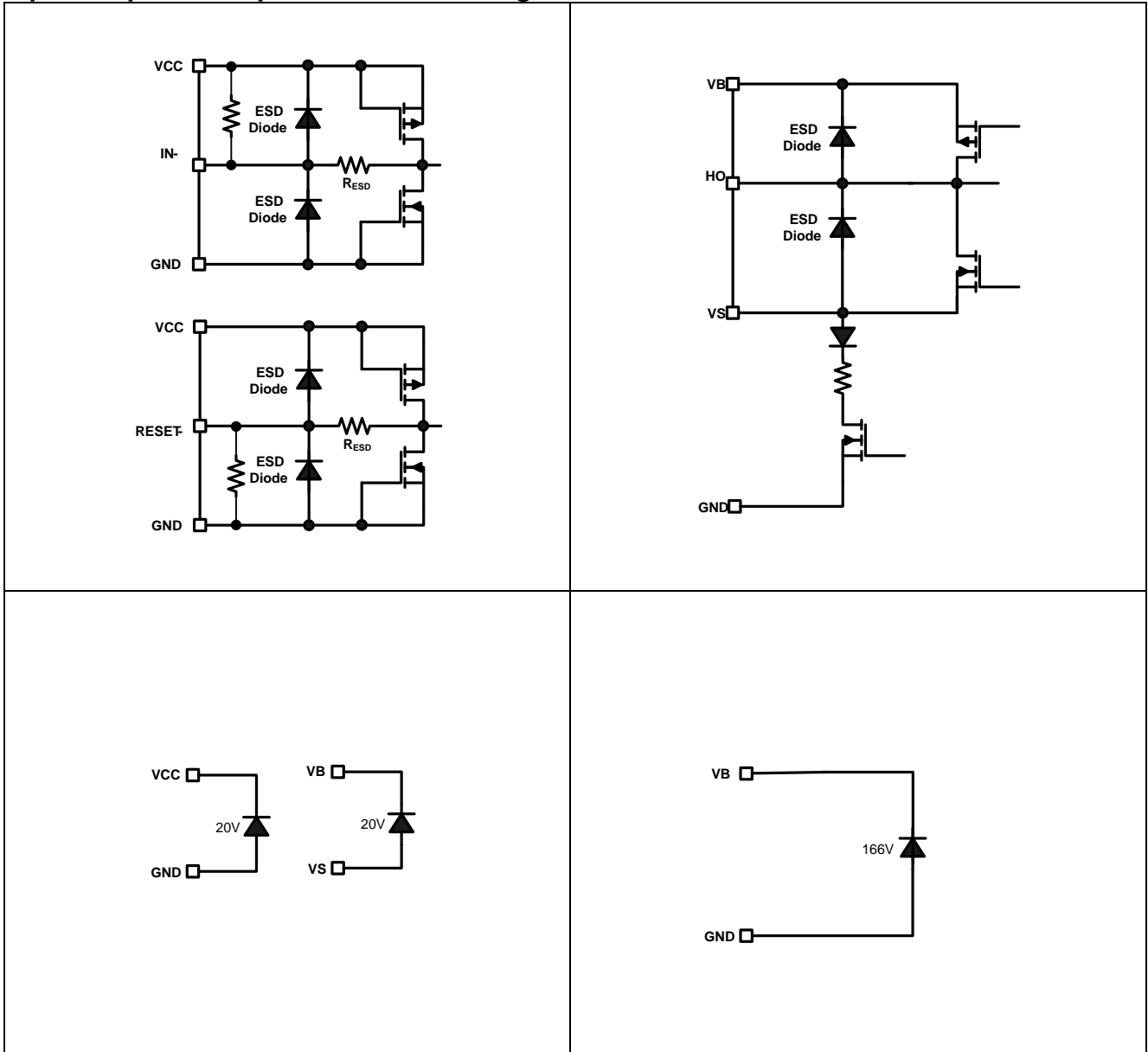
Unless otherwise specified,  $V_{CC} = 5V$ ,  $V_{BS} = 7V$ ,  $V_S = 0V$ ,  $I_N = 0V$ ,  $R_{ES} = 5V$ , load  $R = 50\Omega$ ,  $C = 2.5nF$ . Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}C \leq T_j \leq 125^{\circ}C$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
<b>Input Characteristics</b>						
$V_{INH}$	High Logic Level Input Threshold	0.66* $V_{CC}$			V	$V_{CC}=5V$
$V_{INL}$	Low Logic Level Input Threshold			0.28* $V_{CC}$	V	$V_{CC}=5V$
$R_{IN}$	IN pull up Input Resistance	60	100	220	$k\Omega$	
$I_{IN}$	High Logic Level Input Current			5	$\mu A$	$V_{IN}=V_{CC}$
$V_{H\_RES}$	High Logic Level RES Input Threshold	0.66* $V_{CC}$			V	$V_{CC}=5V$
$V_{L\_RES}$	Low Logic Level RES Input Threshold			0.28* $V_{CC}$	V	$V_{CC}=5V$
$R_{RES}$	RES pull down Input Resistance	60	100	220	$k\Omega$	
$I_{RES}$	Low Logic Level Input Current			5	$\mu A$	$V_{RES}=0$
<b>Recharge Characteristics</b>						
$t_{on\_rech}$	Recharge Transistor Turn-On Propagation Delay	3	6	9	$\mu sec$	$V_S = 5V$
$t_{off\_rech}$	Recharge Transistor Turn-Off Propagation Delay		0.08	0.24	$\mu sec$	
$V_{RECH}$	Recharge Output Transistor On-State Voltage Drop			1.2	V	$I_S = 1mA, I_N = 5V$ .
<b>Deadtime Characteristics</b>						
$DT_{HOFF}$	High Side Turn-Off to Recharge gate Turn-On	3	6	9	$\mu sec$	$V_{CC} = 5V, V_{BS} = 7V$
$DT_{HON}$	Recharge gate Turn-Off to High Side Turn-On	0.005	0.07	0.4	$\mu sec$	$V_{CC} = 5V, V_{BS} = 7V$

**Functional Block Diagram**



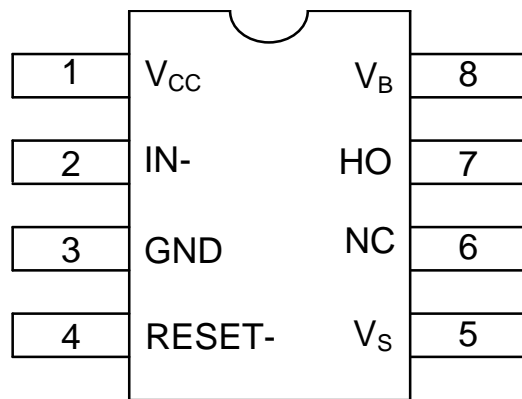
**Input/Output Pin Equivalent Circuit Diagrams**



**Lead Definitions**

Pin Number	Symbol	Pin description
1	V <sub>CC</sub>	Driver Supply, typically 5.0V
2	IN-	Driver Control Signal Input (negative logic)
3	GND	Ground
4	RESET-	Driver Enable Signal Input (negative logic)
5	V <sub>S</sub>	MOSFET Source Connection
6	NC	No Connection (no Bond-wire)
7	HO	MOSFET Gate Connection
8	V <sub>B</sub>	Driver Output Stage Supply

**Lead Assignments**



8 Lead SOIC



### Application Information and Additional Details

The AUIRS20162S is a high voltage power MOSFET and IGBT high side driver with internal VS-to-GND recharge NMOS. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard 5V CMOS or LSTTL logic. The output driver features a 250mA high pulse current buffer stage. The channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration, which operates up to 150 volts above GND ground.

A Truth table for  $V_{CC}$ ,  $V_{BS}$ , RESET, IN,  $H_O$  and RechFET is shown as follows.

This table is valid for voltages ranges defined in the recommended operating conditions section.

Supply voltages and thresholds		Signals		Output $H_O$	Recharge Path
$V_{CC}$	$V_{BS}$	RESET-	IN-		
$< V_{CCUV-}$	X	X	X	OFF	ON
$> V_{CCUV+}$	X	LOW	X	OFF	ON
$> V_{CCUV+}$	X	X	HIGH	OFF	ON
$> V_{CCUV+}$	$> V_{BSUV+}$	HIGH	LOW	ON	OFF
$> V_{CCUV+}$	$< V_{BSUV-}$	HIGH	LOW	OFF	OFF

Table 1: logic operation

Recharge Path = ON indicates that the recharge MOSFET is on.

Recharge Path = OFF indicates that the recharge MOSFET is off.

In the case that  $V_{CC}$  will be removed during operation,  $H_O$  will be turned off if the resulting  $dV_{CC}/dt$  is slow enough to allow UVLO response time as defined in the  $t_{dUVCC}$  parameter.

If  $H_O$  was low it will remain low.

### Timing Diagrams and Additional Information

#### Input / Output

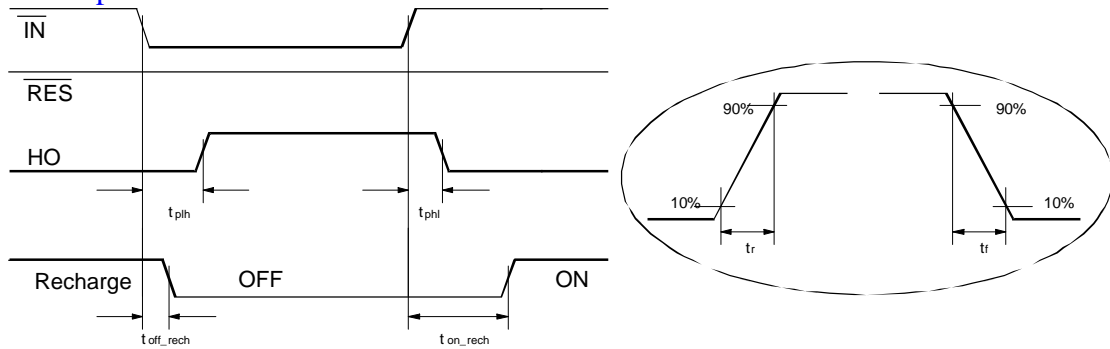


Figure 1: Input/Output Timing Diagram

#### Reset

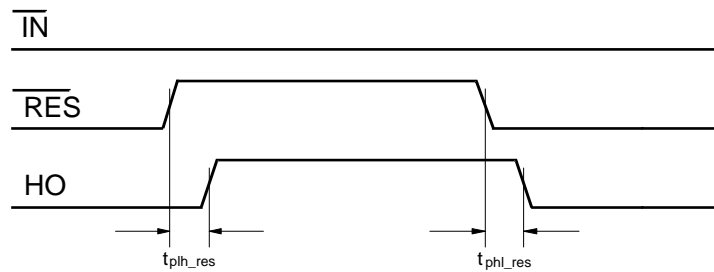


Figure 2: Reset Timing Diagram

#### Start-up

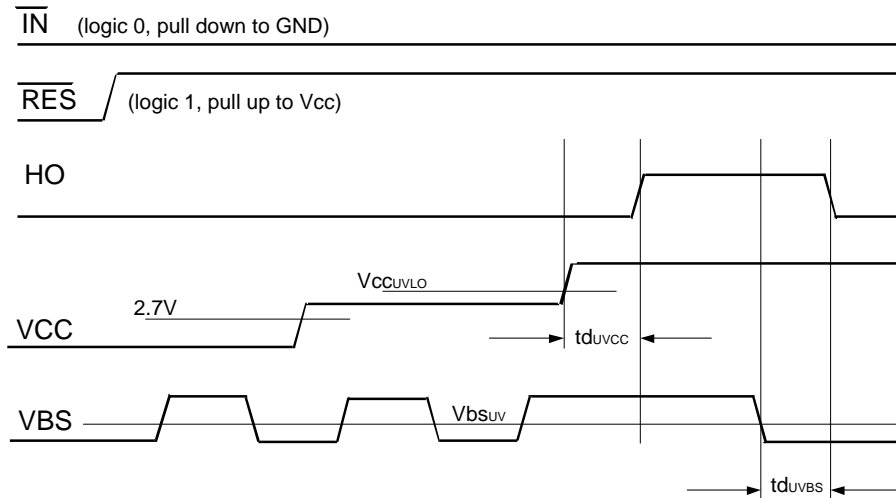


Figure 3: Start up Diagram

VB Drop Voltage Test

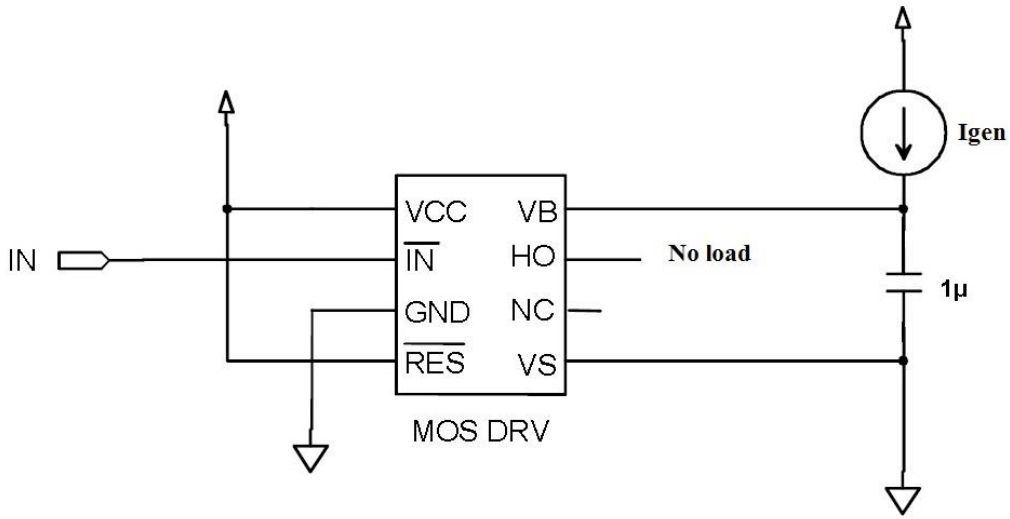
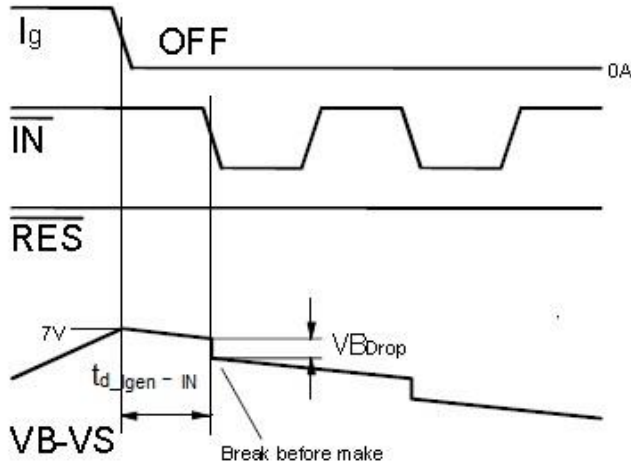


Figure 4: Vbs drop Voltage test



Vbs voltage drop due to the high side section activation at no load

Figure 5: Vbs drop Voltage waveforms

**Performance Graphs**

**RESET Functionality Graph:**

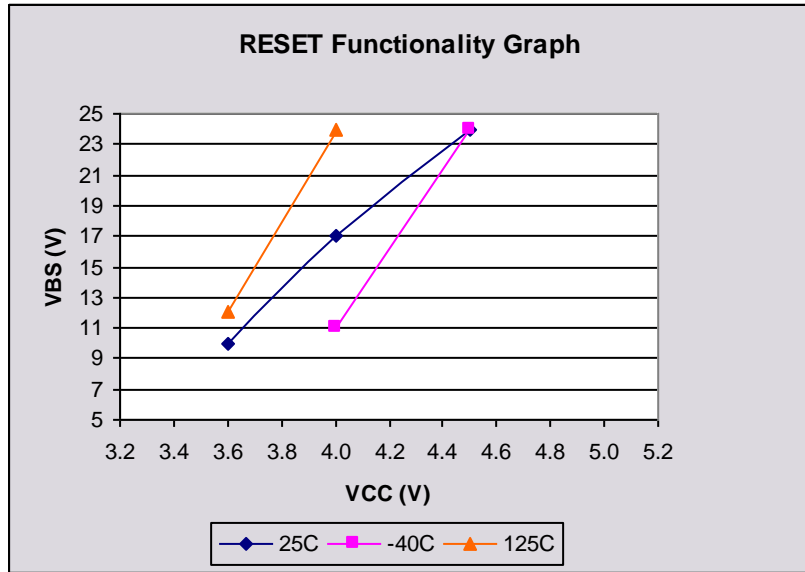


Figure 6-1

**Figure 6. RESET Functionality:**

This graph explains the functionality limitation as a function of  $V_{CC}$ ,  $V_{BS}$  and temperature. For each particular temperature and  $V_{CC}$ , the output is non-functional for any value of  $V_{BS}$  above the drawn curve. But for any value of  $V_{BS}$  below the curve the functionality is fine.

**RESET Functional Diagram:**

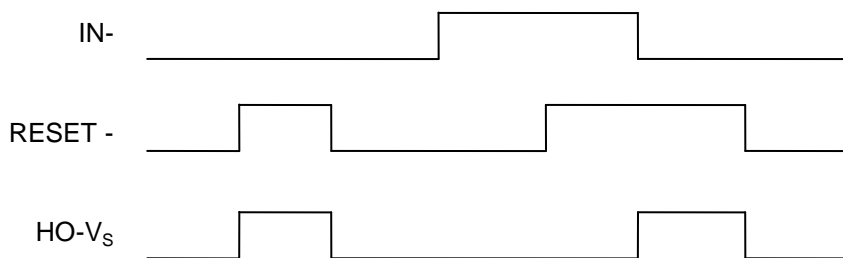


Figure 6-2

### Parameter Temperature Trends

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS20162S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

#### Input and Reset Thresholds:

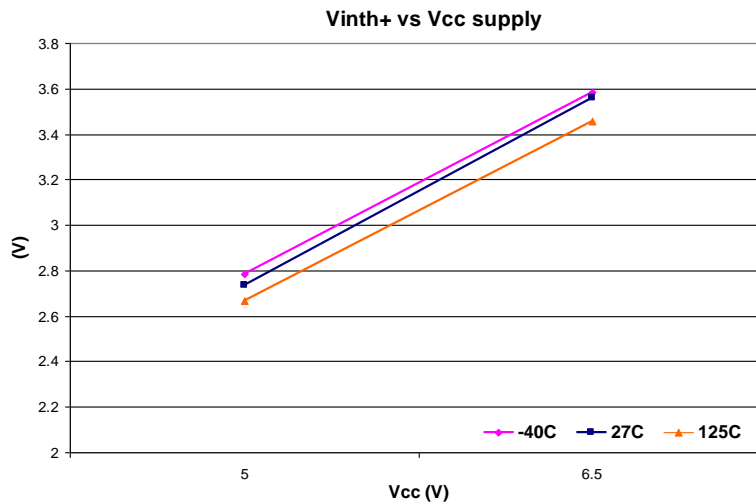


Figure 7-1: Positive Input and Reset Threshold Voltage Distribution Curves

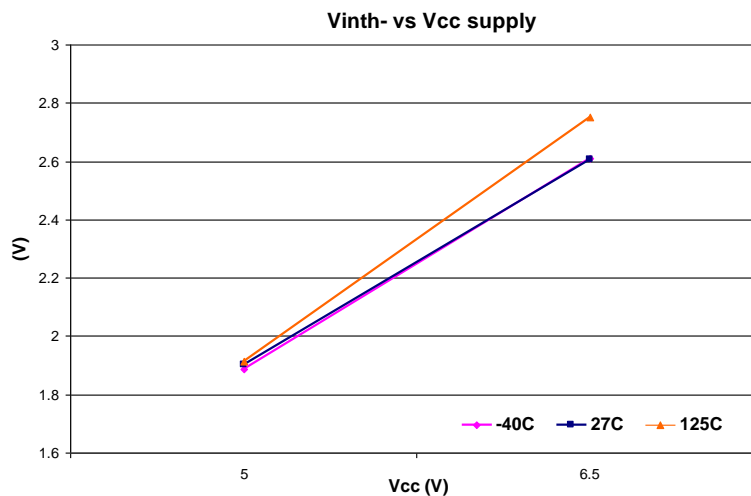


Figure 7-2: Negative Input and Reset Threshold Voltage Distribution Curves

**V<sub>BUV</sub> Undervoltage Shutdown Threshold V<sub>B</sub>:**

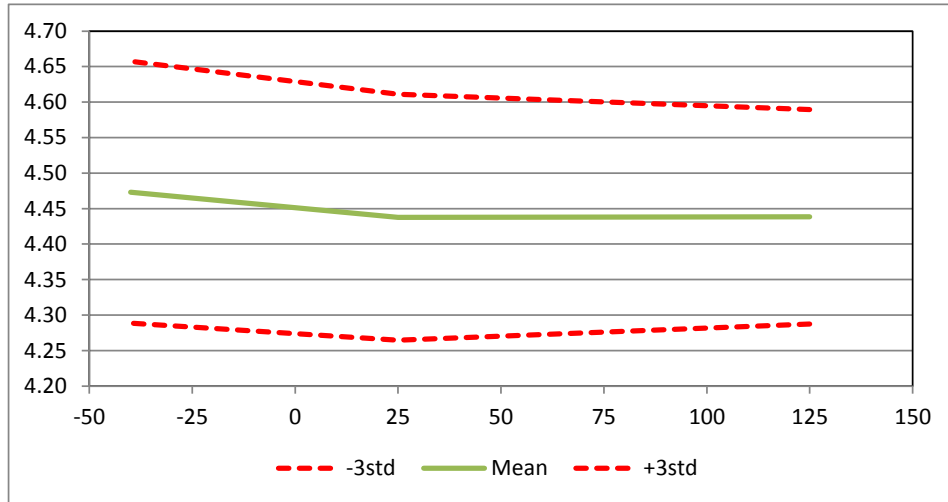


Figure 8-1: Negative going VBSUV- value vs. Temperature:

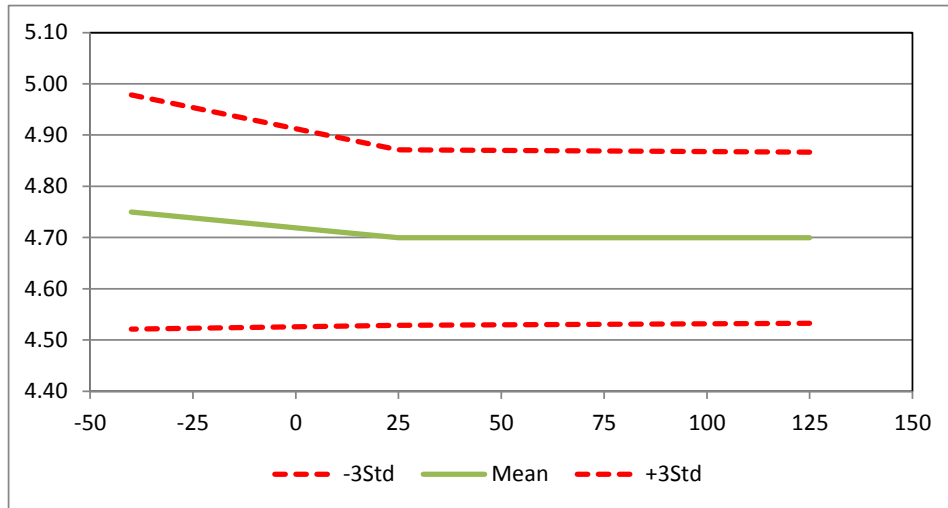


Figure 8-2: Positive going VBSUV+ Value vs. Temperature

Input and Reset Impedance

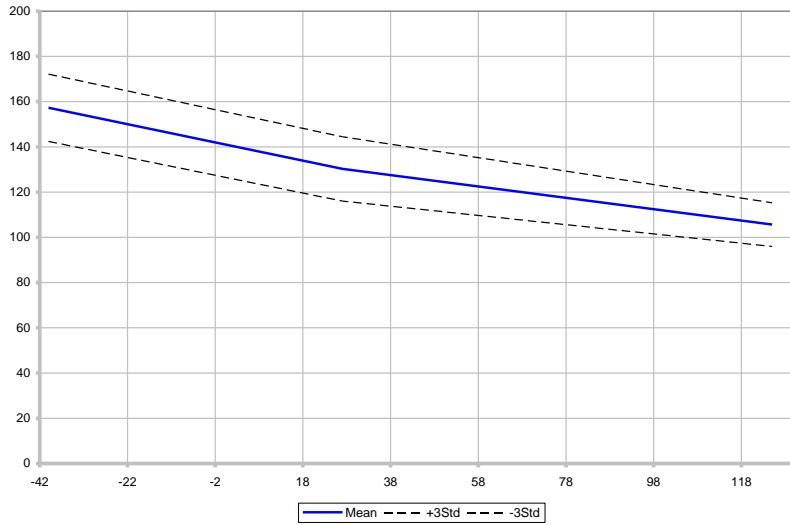


Figure 9: Input and Reset Impedance Distribution Curves vs. Temperature

Recharge FET I-V Curve

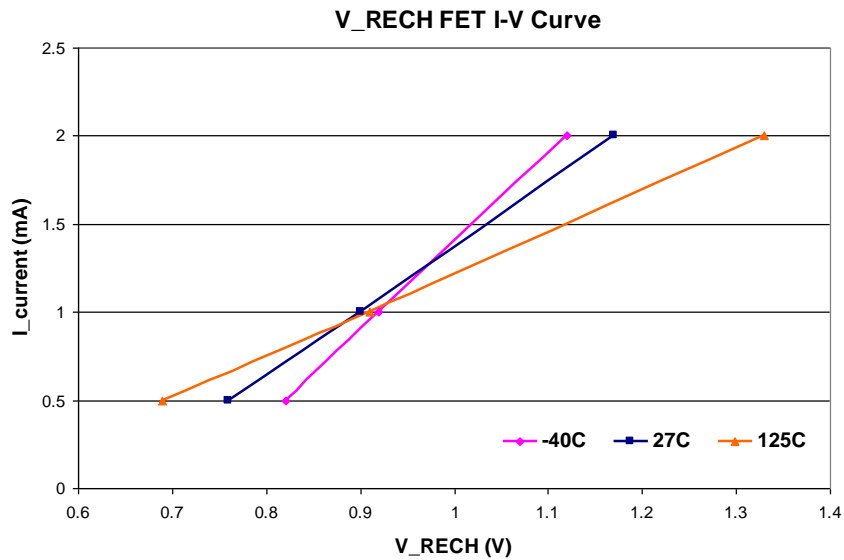


Figure 10: Recharge FET IV-Curve

## Package Details: SOIC8

**RECOMMENDED FOOTPRINT**

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0*	8*	0*	8*

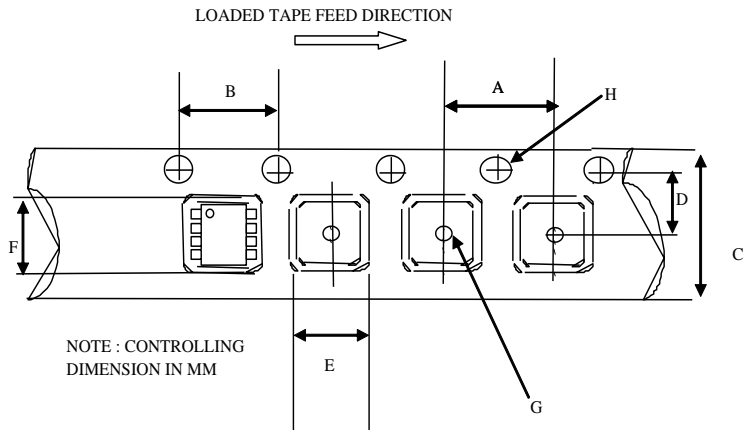
**NOTES:**

- DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
- DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**8 Lead SOIC**

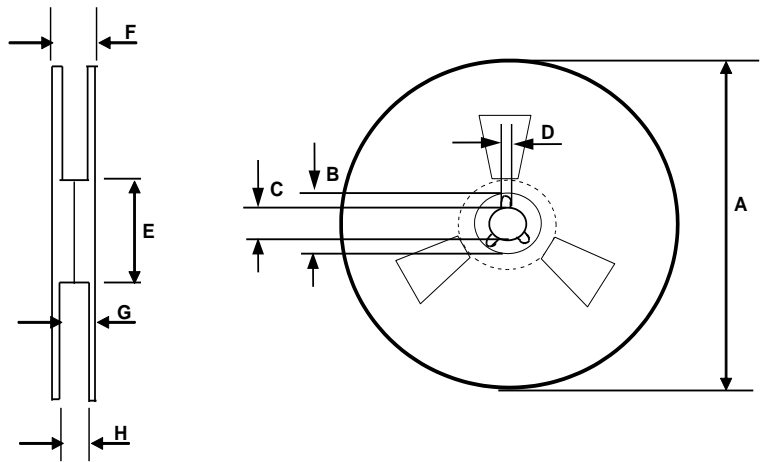


**Tape and Reel Details: SOIC8**



CARRIER TAPE DIMENSION FOR 8SOICN

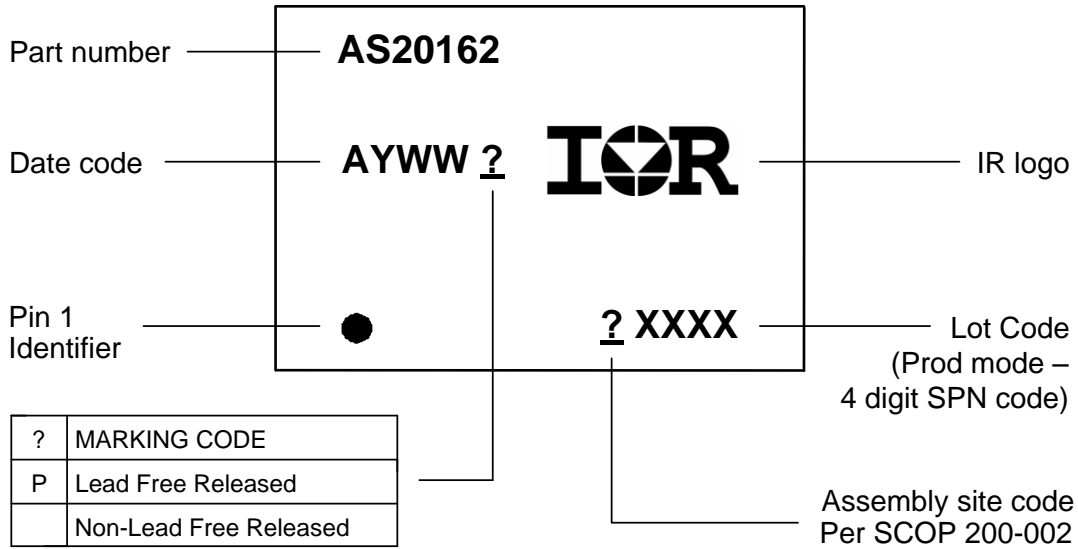
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**Part Marking Information**



**Qualification Information**<sup>(Note1)</sup>

<b>Qualification Level</b>		Automotive (per AEC-Q100)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SOIC8N	MSL3 260°C (Note2) (per IPC/JEDEC J-STD-020)
<b>ESD</b>	Machine Model	Class M1 (Pass +/-200 V) (per AEC-Q100-003)	
	Human Body Model	Class H1C (+/-2000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
<b>IC Latch-Up Test</b>		Class II, Level A (per AEC-Q100-004)	
<b>RoHS Compliant</b>		Yes	

Note 1 Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

Note 2 Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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