

Features

- High-performance, Low-power AVR[®] 8-bit Microcontroller
- RISC Architecture
 - 118 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 16 MIPS Throughput at 16 MHz
- Data and Non-volatile Program Memory
 - 2K Bytes of In-System Programmable Program Memory Flash
Endurance: 10,000 Write/Erase Cycles
 - 128 Bytes of In-System Programmable EEPROM
Endurance: 100,000 Write/Erase Cycles
 - 128 Bytes Internal SRAM
 - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
 - 8-bit Timer/Counter with Separate Prescaler
 - 8-bit High-speed Timer with Separate Prescaler
 - 2 High Frequency PWM Outputs with Separate Output Compare Registers
 - Non-overlapping Inverted PWM Output Pins
 - Universal Serial Interface with Start Condition Detector
 - 10-bit ADC
 - 11 Single Ended Channels
 - 8 Differential ADC Channels
 - 7 Differential ADC Channel Pairs with Programmable Gain (1x, 20x)
 - On-chip Analog Comparator
 - External Interrupt
 - Pin Change Interrupt on 11 Pins
 - Programmable Watchdog Timer with Separate On-chip Oscillator
- Special Microcontroller Features
 - Low Power Idle, Noise Reduction, and Power-down Modes
 - Power-on Reset and Programmable Brown-out Detection
 - External and Internal Interrupt Sources
 - In-System Programmable via SPI Port
 - Internal Calibrated RC Oscillator
- I/O and Packages
 - 20-lead PDIP/SOIC: 16 Programmable I/O Lines
 - 32-lead QFN/MLF: 16 programmable I/O Lines
- Operating Voltages
 - 2.7V - 5.5V for ATtiny26L
 - 4.5V - 5.5V for ATtiny26
- Speed Grades
 - 0 - 8 MHz for ATtiny26L
 - 0 - 16 MHz for ATtiny26
- Power Consumption at 1 MHz, 3V and 25°C for ATtiny26L
 - Active 16 MHz, 5V and 25°C: Typ 15 mA
 - Active 1 MHz, 3V and 25°C: 0.70 mA
 - Idle Mode 1 MHz, 3V and 25°C: 0.18 mA
 - Power-down Mode: < 1 µA



8-bit AVR[®] Microcontroller with 2K Bytes Flash

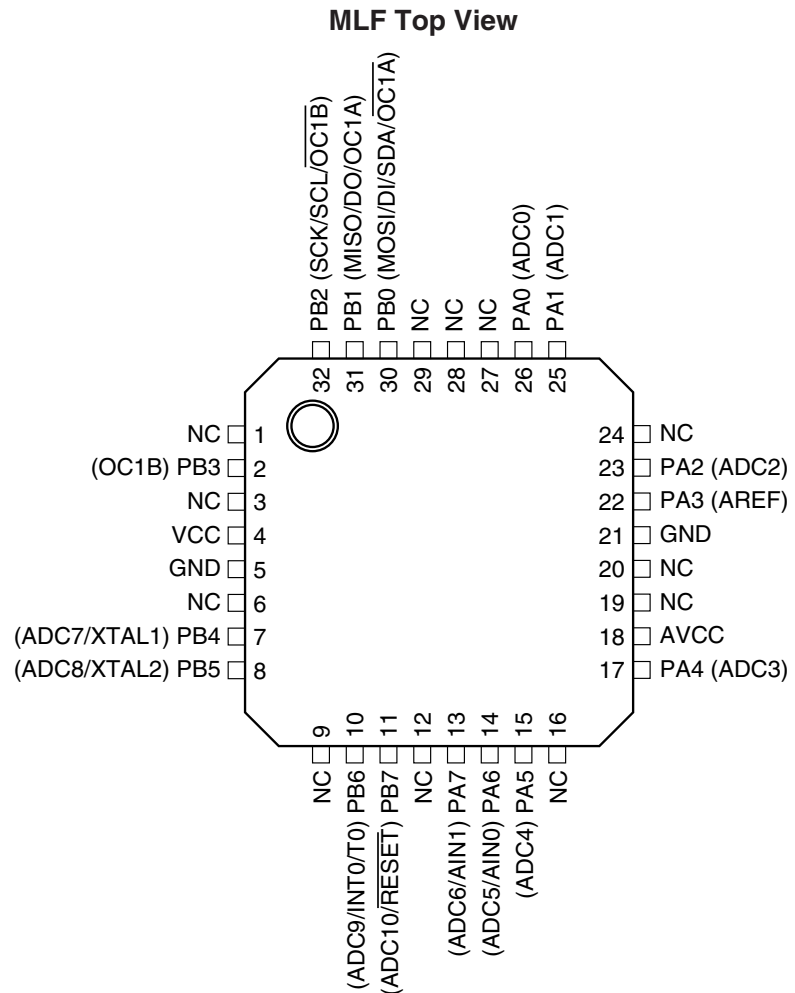
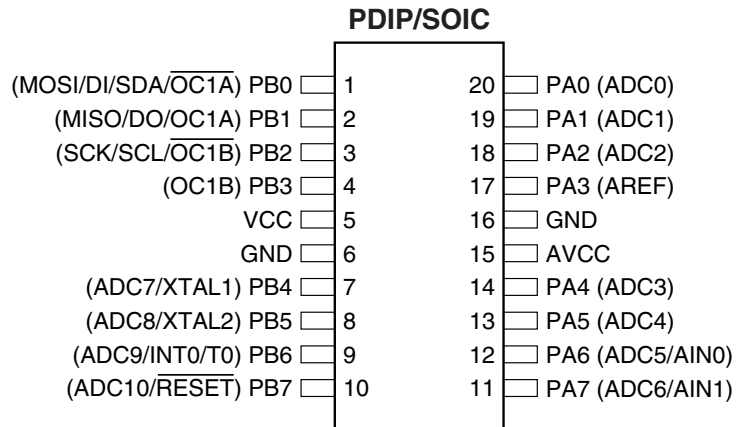
ATtiny26 ATtiny26L Summary

Not recommended for new
design

1477J-AVR-06/07



Pin Configuration



Note: The bottom pad under the QFN/MLF package should be soldered to ground.

Description

The ATtiny26(L) is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny26(L) achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers. The ATtiny26(L) has a high precision ADC with up to 11 single ended channels and 8 differential channels. Seven differential channels have an optional gain of 20x. Four out of the seven differential channels, which have the optional gain, can be used at the same time. The ATtiny26(L) also has a high frequency 8-bit PWM module with two independent outputs. Two of the PWM outputs have inverted non-overlapping output pins ideal for synchronous rectification. The Universal Serial Interface of the ATtiny26(L) allows efficient software implementation of TWI (Two-wire Serial Interface) or SM-bus interface. These features allow for highly integrated battery charger and lighting ballast applications, low-end thermostats, and fire detectors, among other applications.

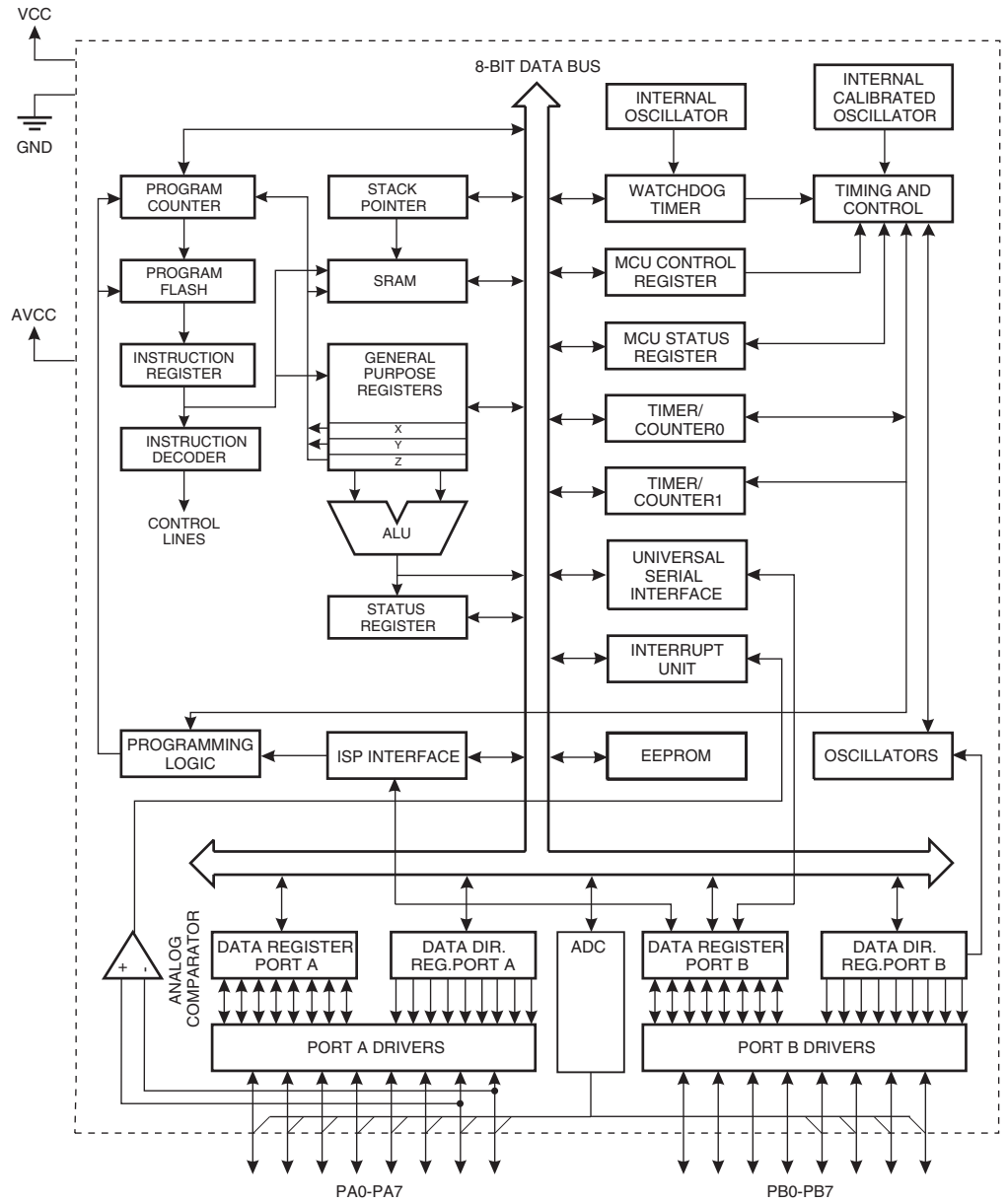
The ATtiny26(L) provides 2K bytes of Flash, 128 bytes EEPROM, 128 bytes SRAM, up to 16 general purpose I/O lines, 32 general purpose working registers, two 8-bit Timer/Counters, one with PWM outputs, internal and external Oscillators, internal and external interrupts, programmable Watchdog Timer, 11-channel, 10-bit Analog to Digital Converter with two differential voltage input gain stages, and four software selectable power saving modes. The Idle mode stops the CPU while allowing the Timer/Counters and interrupt system to continue functioning. The ATtiny26(L) also has a dedicated ADC Noise Reduction mode for reducing the noise in ADC conversion. In this sleep mode, only the ADC is functioning. The Power-down mode saves the register contents but freezes the oscillators, disabling all other chip functions until the next interrupt or hardware reset. The Standby mode is the same as the Power-down mode, but external oscillators are enabled. The wakeup or interrupt on pin change features enable the ATtiny26(L) to be highly responsive to external events, still featuring the lowest power consumption while in the Power-down mode.

The device is manufactured using Atmel's high density non-volatile memory technology. By combining an enhanced RISC 8-bit CPU with Flash on a monolithic chip, the ATtiny26(L) is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny26(L) AVR is supported with a full suite of program and system development tools including: Macro assemblers, program debugger/simulators, In-circuit emulators, and evaluation kits.

Block Diagram

Figure 1. The ATtiny26(L) Block Diagram



Pin Descriptions

| | |
|--------------------------|---|
| VCC | Digital supply voltage pin. |
| GND | Digital ground pin. |
| AVCC | AVCC is the supply voltage pin for Port A and the A/D Converter (ADC). It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. See page 96 for details on operating of the ADC. |
| Port A (PA7..PA0) | Port A is an 8-bit general purpose I/O port. PA7..PA0 are all I/O pins that can provide internal pull-ups (selected for each bit). Port A has alternate functions as analog inputs for the ADC and analog comparator and pin change interrupt as described in “Alternate Port Functions” on page 48. |
| Port B (PB7..PB0) | <p>Port B is an 8-bit general purpose I/O port. PB6..0 are all I/O pins that can provide internal pull-ups (selected for each bit). PB7 is an I/O pin if not used as the reset. To use pin PB7 as an I/O pin, instead of RESET pin, program (“0”) RSTDISBL Fuse. Port B has alternate functions for the ADC, clocking, timer counters, USI, SPI programming, and pin change interrupt as described in “Alternate Port Functions” on page 48.</p> <p>An External Reset is generated by a low level on the PB7/$\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.</p> |
| XTAL1 | Input to the inverting oscillator amplifier and input to the internal clock operating circuit. |
| XTAL2 | Output from the inverting oscillator amplifier. |



Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

About Code Examples

This datasheet contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.



Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|-------------|----------|--|--------|--------|--------|---------|---------|---------|---------|------|
| \$3F (\$5F) | SREG | I | T | H | S | V | N | Z | C | 11 |
| \$3E (\$5E) | Reserved | | | | | | | | | |
| \$3D (\$5D) | SP | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 12 |
| \$3C (\$5C) | Reserved | | | | | | | | | |
| \$3B (\$5B) | GIMSK | - | INT0 | PCIE1 | PCIE0 | - | - | - | - | 60 |
| \$3A (\$5A) | GIFR | - | INTF0 | PCIF | - | - | - | - | - | 61 |
| \$39 (\$59) | TIMSK | - | OCIE1A | OCIE1B | - | - | TOIE1 | TOIE0 | - | 61 |
| \$38 (\$58) | TIFR | - | OCF1A | OCF1B | - | - | TOV1 | TOV0 | - | 62 |
| \$37 (\$57) | Reserved | | | | | | | | | |
| \$36 (\$56) | Reserved | | | | | | | | | |
| \$35 (\$55) | MCUCR | - | PUD | SE | SM1 | SM0 | - | ISC01 | ISC00 | 38 |
| \$34 (\$54) | MCUSR | - | - | - | - | WDRF | BORF | EXTRF | PORF | 37 |
| \$33 (\$53) | TCCR0 | - | - | - | - | PSR0 | CS02 | CS01 | CS00 | 68 |
| \$32 (\$52) | TCNT0 | Timer/Counter0 (8-Bit) | | | | | | | | 69 |
| \$31 (\$51) | OSCCAL | Oscillator Calibration Register | | | | | | | | 30 |
| \$30 (\$50) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | FOC1A | FOC1B | PWM1A | PWM1B | 72 |
| \$2F (\$4F) | TCCR1B | CTC1 | PSR1 | - | - | CS13 | CS12 | CS11 | CS10 | 73 |
| \$2E (\$4E) | TCNT1 | Timer/Counter1 (8-Bit) | | | | | | | | 74 |
| \$2D (\$4D) | OCR1A | Timer/Counter1 Output Compare Register A (8-Bit) | | | | | | | | 74 |
| \$2C (\$4C) | OCR1B | Timer/Counter1 Output Compare Register B (8-Bit) | | | | | | | | 75 |
| \$2B (\$4B) | OCR1C | Timer/Counter1 Output Compare Register C (8-Bit) | | | | | | | | 75 |
| \$2A (\$4A) | Reserved | | | | | | | | | |
| \$29 (\$49) | PLLCSR | - | - | - | - | - | PCKE | PLLE | PLOCK | |
| \$28 (\$48) | Reserved | | | | | | | | | |
| \$27 (\$47) | Reserved | | | | | | | | | |
| \$26 (\$46) | Reserved | | | | | | | | | |
| \$25 (\$45) | Reserved | | | | | | | | | |
| \$24 (\$44) | Reserved | | | | | | | | | |
| \$23 (\$43) | Reserved | | | | | | | | | |
| \$22 (\$42) | Reserved | | | | | | | | | |
| \$21 (\$41) | WDTCR | - | - | - | WDCE | WDE | WDP2 | WDP1 | WDP0 | 80 |
| \$20 (\$40) | Reserved | | | | | | | | | |
| \$1F (\$3F) | Reserved | | | | | | | | | |
| \$1E (\$3E) | EEAR | - | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | 19 |
| \$1D (\$3D) | EEDR | EEPROM Data Register (8-Bit) | | | | | | | | 20 |
| \$1C (\$3C) | EEDR | - | - | - | - | EERIE | EEMWE | EEWE | EERE | 20 |
| \$1B (\$3B) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | |
| \$1A (\$3A) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | |
| \$19 (\$39) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | |
| \$18 (\$38) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | |
| \$17 (\$37) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | |
| \$16 (\$36) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | |
| \$15 (\$35) | Reserved | | | | | | | | | |
| \$14 (\$34) | Reserved | | | | | | | | | |
| \$13 (\$33) | Reserved | | | | | | | | | |
| \$12 (\$32) | Reserved | | | | | | | | | |
| \$11 (\$31) | Reserved | | | | | | | | | |
| \$10 (\$30) | Reserved | | | | | | | | | |
| \$0F (\$2F) | USIDR | Universal Serial Interface Data Register (8-Bit) | | | | | | | | 83 |
| \$0E (\$2E) | USISR | USISIF | USIOIF | USIPF | USIDC | USICNT3 | USICNT2 | USICNT1 | USICNT0 | 83 |
| \$0D (\$2D) | USICR | USISIE | USIOIE | USIWM1 | USIWM0 | USICS1 | USICS0 | USICLK | USITC | 84 |
| \$0C (\$2C) | Reserved | | | | | | | | | |
| \$0B (\$2B) | Reserved | | | | | | | | | |
| \$0A (\$2A) | Reserved | | | | | | | | | |
| \$09 (\$29) | Reserved | | | | | | | | | |
| \$08 (\$28) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACME | ACIS1 | ACIS0 | 93 |
| \$07 (\$27) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | 103 |
| \$06 (\$26) | ADCSR | ADEN | ADSC | ADFR | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | 105 |
| \$05 (\$25) | ADCH | ADC Data Register High Byte | | | | | | | | 106 |
| \$04 (\$24) | ADCL | ADC Data Register Low Byte | | | | | | | | 106 |
| ... | Reserved | | | | | | | | | |
| \$00 (\$20) | Reserved | | | | | | | | | |

Instruction Set Summary

| Mnemonic | Operands | Description | Operation | Flags | # Clocks |
|--|----------|--|---|-----------|----------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add Two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry Two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rdl, K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract Two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry Two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rdl, K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow \text{\$FF} - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow \text{\$00} - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd, K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd, K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (\text{\$FF} - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow \text{\$FF}$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow \text{STACK}$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow \text{STACK}$ | I | 4 |
| CPSE | Rd, Rr | Compare, Skip if Equal | if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd, Rr | Compare | $Rd - Rr$ | Z,N,V,C,H | 1 |
| CPC | Rd, Rr | Compare with Carry | $Rd - Rr - C$ | Z,N,V,C,H | 1 |
| CPI | Rd, K | Compare Register with Immediate | $Rd - K$ | Z,N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if $(Z = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if $(Z = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if $(C = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if $(C = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if $(N = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if $(N = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less than Zero, Signed | if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half-carry Flag Set | if $(H = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half-carry Flag Cleared | if $(H = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T-flag Set | if $(T = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T-flag Cleared | if $(T = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if $(V = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if $(V = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if $(I = 1)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if $(I = 0)$ then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move between Registers | $Rd \leftarrow Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |

Instruction Set Summary (Continued)

| Mnemonic | Operands | Description | Operation | Flags | # Clocks |
|--------------------------------------|----------|----------------------------------|--|---------|----------|
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P, b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P, b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n = 0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit Load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Two's Complement Overflow | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Two's Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half-carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half-carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |

Ordering Information

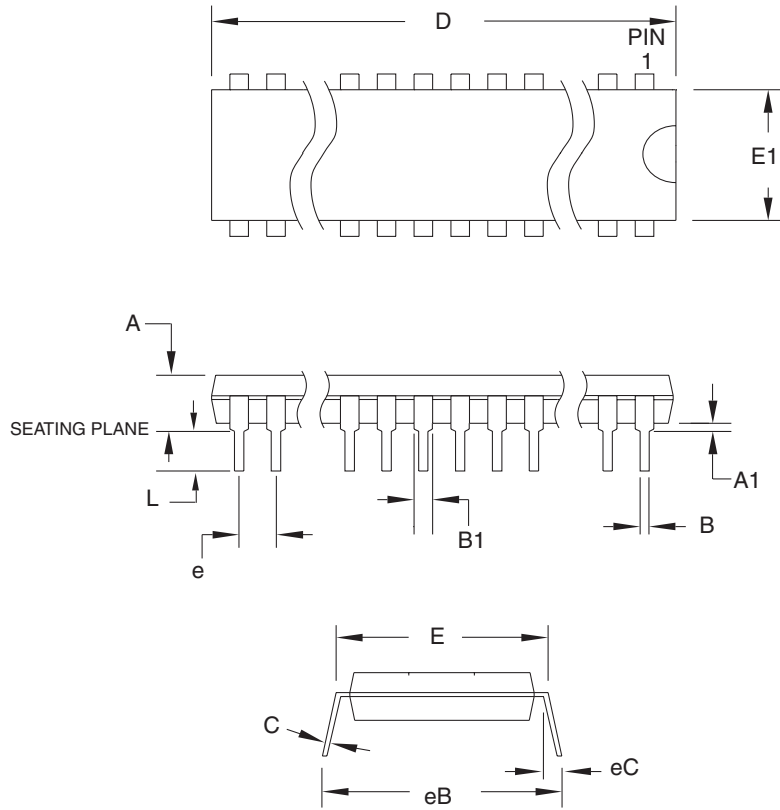
| Speed (MHz) | Power Supply | Ordering Code | Package ⁽¹⁾ | Operational Range |
|------------------------------|--------------|------------------------------|------------------------|-------------------------------|
| 8 | 2.7 - 5.5V | ATtiny26L-8PC | 20P3 | Commercial (0°C to 70°C) |
| | | ATtiny26L-8SC | 20S | |
| | | ATtiny26L-8MC | 32M1-A | |
| | | ATtiny26L-8PI | 20P3 | Industrial (-40°C to 85°C) |
| | | ATtiny26L-8SI | 20S | |
| | | ATtiny26L-8MI | 32M1-A | |
| | | ATtiny26L-8PU ⁽²⁾ | 20P3 | |
| ATtiny26L-8SU ⁽²⁾ | 20S | | | |
| ATtiny26L-8MU ⁽²⁾ | 32M1-A | | | |
| 16 | 4.5 - 5.5V | ATtiny26-16PC | 20P3 | Commercial (0°C to 70°C) |
| | | ATtiny26-16SC | 20S | |
| | | ATtiny26-16MC | 32M1-A | |
| | | ATtiny26-16PI | 20P3 | Industrial (-40°C to 85°C) |
| | | ATtiny26-16SI | 20S | |
| | | ATtiny26-16MI | 32M1-A | |
| | | ATtiny26-16PU ⁽²⁾ | 20P3 | |
| ATtiny26-16SU ⁽²⁾ | 20S | | | |
| ATtiny26-16MU ⁽²⁾ | 32M1-A | | | |

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

| Package Type | |
|---------------|---|
| 20P3 | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20S | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 32M1-A | 32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF) |

Packaging Information

20P3



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 25.493 | – | 25.984 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.270 | – | 1.551 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion.
Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

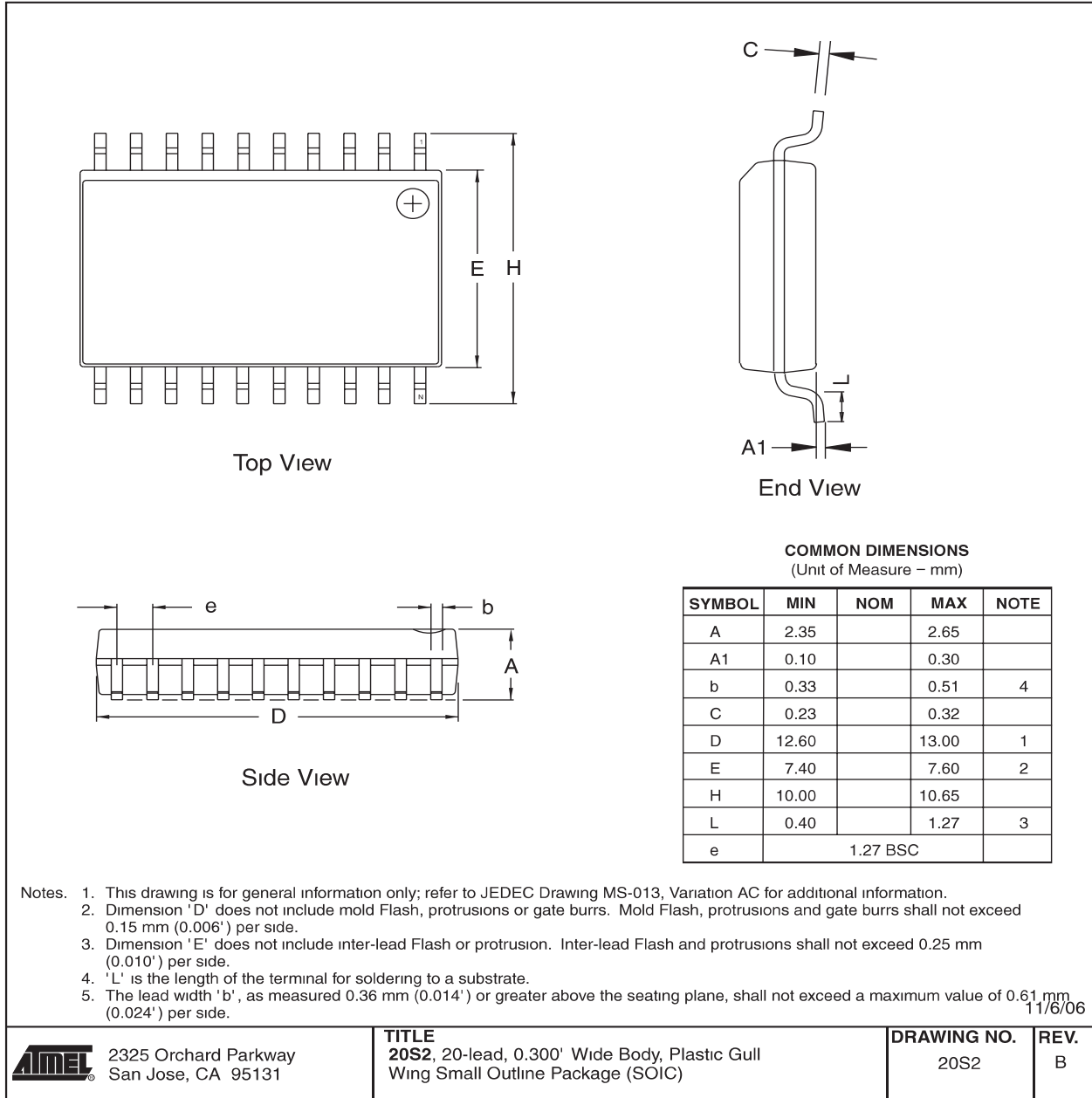
1/12/04

2325 Orchard Parkway
San Jose, CA 95131

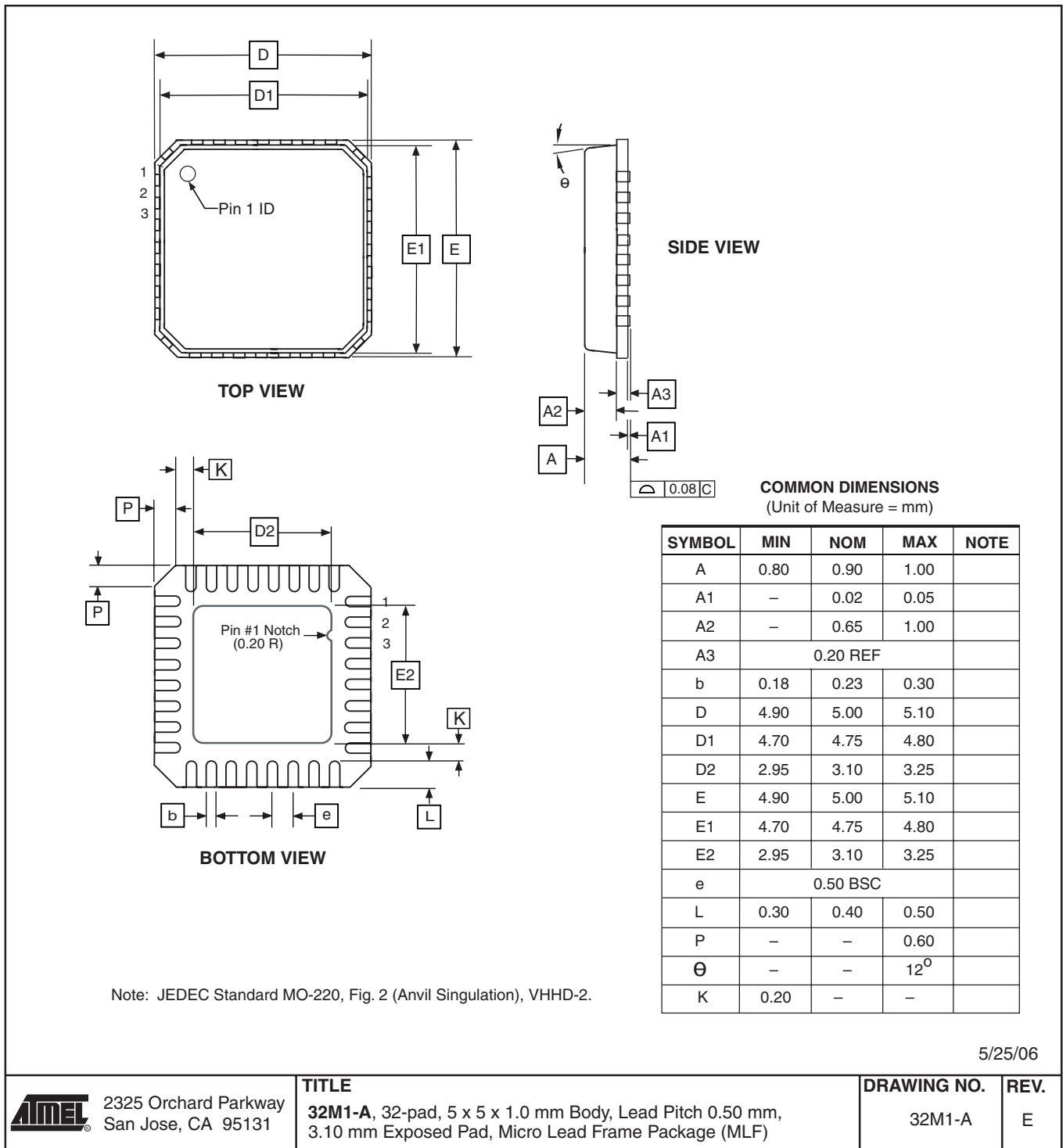
TITLE
20P3, 20-lead (0.300"/7.62 mm Wide) Plastic Dual
Inline Package (PDIP)

| | |
|--------------------|-------------|
| DRAWING NO. | REV. |
| 20P3 | C |

20S



32M1-A



Errata

The revision letter refers to the revision of the device.

ATtiny26 Rev. B/C/D

- **First Analog Comparator conversion may be delayed**

1. **First Analog Comparator conversion may be delayed**

If the device is powered by a slow rising VCC, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix/Workaround

When the device has been powered or reset, disable then enable the Analog Comparator before the first conversion.

Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

Rev. 1477J-06/07

1. “Not recommended for new design”

Rev. 1477I-10/06

1. Updated “Errata” on page 15

Rev. 1477H-04/06

1. Updated typos.
2. Added “Resources” on page 6.
3. Updated features in “System Control and Reset” on page 33.
4. Updated “Prescaling and Conversion Timing” on page 98.
5. Updated algorithm for “Enter Programming Mode” on page 114.

Rev. 1477G-03/05

1. MLF-package alternative changed to “Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF”.
2. Updated “Electrical Characteristics” on page 128
3. Updated “Ordering Information” on page 11

Rev. 1477F-12/04

1. Updated Table 16 on page 34, Table 9 on page 29, and Table 29 on page 59.
2. Added Table 20 on page 41.
3. Added “Changing Channel or Reference Selection” on page 100.
4. Updated “Offset Compensation Schemes” on page 107.
5. Updated “Electrical Characteristics” on page 128.
6. Updated package information for “20P3” on page 12.
7. Rearranged some sections in the datasheet.

Rev. 1477E-10/03

1. Removed Preliminary references.
2. Updated “Features” on page 1.
3. Removed SSOP package reference from “Pin Configuration” on page 2.
4. Updated V_{RST} and t_{RST} in Table 16 on page 34.
5. Updated “Calibrated Internal RC Oscillator” on page 30.
6. Updated DC Characteristics for V_{OL} , I_{IL} , I_{IH} , I_{CC} Power Down and V_{ACIO} in “Electrical Characteristics” on page 128.

7. Updated V_{INT} , INL and Gain Error in “ADC Characteristics” on page 131 and page 132. Fixed typo in “Absolute Accuracy” on page 132.
8. Added Figure 106 in “Pin Driver Strength” on page 148, Figure 120, Figure 121 and Figure 122 in “BOD Thresholds and Analog Comparator Offset” on page 157. Updated Figure 117 and Figure 118.
9. Removed LPM Rd, Z+ from “Instruction Set Summary” on page 9. This instruction is not supported in ATtiny26.

Rev. 1477D-05/03

1. Updated “Packaging Information” on page 12.
2. Removed ADHSM from “ADC Characteristics” on page 131.
3. Added section “EEPROM Write During Power-down Sleep Mode” on page 21.
4. Added section “Default Clock Source” on page 27.
5. Corrected PLL Lock value in the “Bit 0 – PLOCK: PLL Lock Detector” on page 76.
6. Added information about conversion time when selecting differential channels on page 99.
7. Corrected {DDxn, PORTxn} value on page 45.
8. Added section “Unconnected Pins” on page 48.
9. Added note for RSTDISBL Fuse in Table 50 on page 110.
10. Corrected DATA value in Figure 61 on page 118.
11. Added WD_FUSE period in Table 60 on page 125.
12. Updated “ADC Characteristics” on page 131 and added Table 66, “ADC Characteristics, Differential Channels, $T_A = -40^{\circ}\text{C}$ to 85°C ,” on page 132.
13. Updated “ATtiny26 Typical Characteristics” on page 133.
14. Added LPM Rd, Z and LPM Rd, Z+ in “Instruction Set Summary” on page 9.

Rev. 1477C-09/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

Rev. 1477B-04/02

1. Removed all references to Power Save sleep mode in the section “System Clock and Clock Options” on page 24.
2. Updated the section “Analog to Digital Converter” on page 96 with more details on how to read the conversion result for both differential and single-ended conversion.
3. Updated “Ordering Information” on page 11 and added QFN/MLF package information.



Rev. 1477A-03/02

1. Initial version.



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