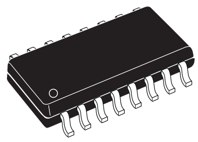
ALTAIR04-900

Off-line all-primary-sensing switching regulator

Features

- Primary side constant voltage operations with no optocoupler
- Adjustable and main-independent maximum output current for safe operations during overload/short circuit conditions
- 900 V avalanche rugged internal power section
- Quasi-resonant valley switching operation
- Low standby consumption
- Overcurrent protection against transformer saturation and secondary diode short circuit
- SO16 package



SO16N

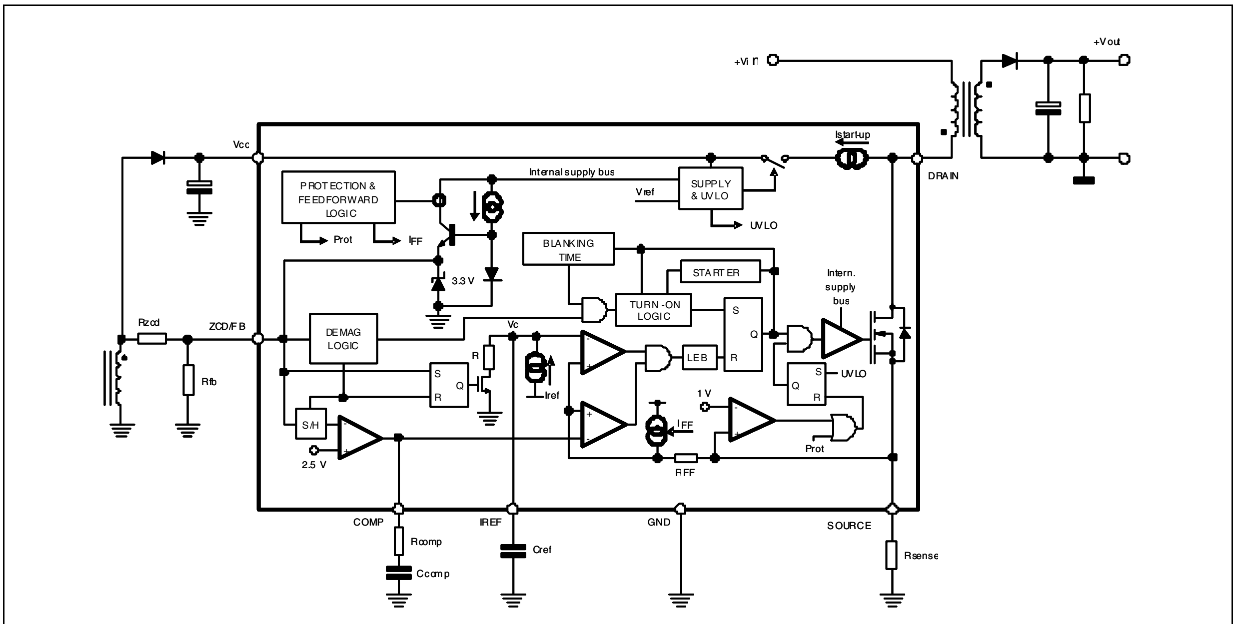
Applications

- SMPS for energy metering
- Auxiliary power supplies for 3-phases input industrial systems
- AC-DC adapters

Description

ALTAIR04-900 is a high-voltage all-primary-sensing switcher intended for operating directly from the rectified mains with minimum external parts. It combines a high-performance low-voltage PWM controller chip and a 900 V avalanche-rugged power section in the same package.

Figure 1. Block diagram



Contents

1 Device description

The device combines two silicon in the same package: a low voltage PWM controller and a 900 V avalanche rugged power section.

The controller is a current-mode specifically designed for off-line quasi-resonant flyback converters.

The device is capable of providing constant output voltage using all primary sensing feedback. This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sensor, still maintaining quite accurate regulation. Also, it is possible to set the maximum deliverable output current, thus increasing the end-product's safety and reliability during fault events.

Quasi-resonant operation is guaranteed by means of a transformer demagnetization sensing input that turns on the power section. The same input serves also the output voltage monitor, to perform CV regulation, and the input voltage monitor, to achieve mains-independent maximum deliverable output current (line voltage feedforward).

The maximum switching frequency is top-limited below 166 kHz, so that at medium-light load a special function automatically lowers the operating frequency still maintaining the valley switching operation. At very light load, the device enters a controlled burst-mode operation that, along with the built-in high-voltage start-up circuit and the low operating current, helps minimize the standby power.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is able to power itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops below UVLO threshold.

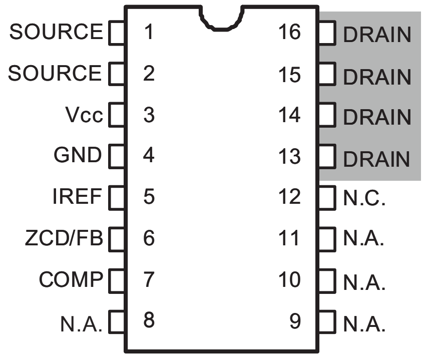
However, if ultra-low no-load input consumption is required to comply with the most stringent energy-saving recommendations, then the device needs to be powered via the auxiliary winding.

In addition to these functions that optimize power handling under different operating conditions, the device offers protection features that considerably increase end-product's safety and reliability: auxiliary winding disconnection - or brownout - detection and shorted secondary rectifier - or transformer's saturation - detection.

All of them are auto restart mode.

2 Pin connection

Figure 2. Pin connection (top view)



Note: The copper area for heat dissipation has to be designed under the drain pins

Table 1. Pin functions

N.	Name	Function
1, 2	SOURCE	Power section source and input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor connected between the pin and GND. The resulting voltage is compared with an internal reference (0.75V max.) to determine MOSFET's turn-off. The pin is equipped with 250 ns blanking time after the gate-drive output goes high for improved noise immunity. If a second comparison level located at 1V is exceeded the IC is stopped and restarted after Vcc has dropped below 5V.
3	Vcc	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high-voltage start-up generator; when the device is running the same generator keeps it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
4	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a trace going to this pin and kept separate from any pulsed current return.
5	IREF	CC regulation loop reference voltage. An external capacitor has to be connected between this pin and GND. An internal circuit develops a voltage on this capacitor that is used as the reference for the MOSFET's peak drain current during CC regulation. The voltage is automatically adjusted to keep the average output current constant.

Table 1. Pin functions (continued)

N.	Name	Function
6	ZCD/FB	Transformer's demagnetization sensing for quasi-resonant operation. Input/output voltage monitor. A negative-going edge triggers MOSFET's turn-on. The current sourced by the pin during ON-time is monitored to get an image of the input voltage to the converter, in order to compensate the internal delay of the current sensing circuit and achieve a CC regulation independent of the mains voltage. If this current does not exceed 50µA, either a floating pin or an abnormally low input voltage is assumed, the device is stopped and restarted after Vcc has dropped below 5V. Still, the pin voltage is sampled-and-held right at the end of transformer's demagnetization to get an accurate image of the output voltage to be fed to the inverting input of the internal, transconductance-type, error amplifier, whose non-inverting input is referenced to 2.5V. Please note that the maximum $I_{ZCD/FB}$ sunk/sourced current has to not exceed ±2 mA (AMR) in all the Vin range conditions. No capacitor is allowed between the pin and the auxiliary transformer.
7	COMP	Output of the internal transconductance error amplifier. The compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop.
8-11	N.A	Not available. These pins must be left not connected
12	N.C	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
13 to 16	DRAIN	Drain connection of the internal power section. The internal high-voltage start-up generator sinks current from this pin as well. Pins connected to the internal metal frame to facilitate heat dissipation.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{DS}	1,2, 13-16	Drain-to-source (ground) voltage	-1 to 900	V
I_D	1,2, 13-16	Drain current	0.7	A
Eav	1,2, 13-16	Single pulse avalanche energy (Tj = 25°C, I_D = 0.7A)	25	mJ
Vcc	3	Supply voltage (Icc < 25mA)	Self limiting	V
$I_{ZCD/FB}$	6	Zero current detector current	±2	mA
Vcomp	8	Analog input	-0.3 to 3.6	V
Ptot		Power dissipation @T_A = 50°C	0.9	W
Tj		Junction temperature range	-25 to 150	°C
Tstg		Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}pin}$	Thermal resistance, junction-to-pin	10	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient	110	

4 Electrical characteristics

(T_J = -25 to 125 °C, Vcc = 14 V; unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power section						
$V_{(BR)DSS}$	Drain-source breakdown	I_D< 100 µA; Tj = 25 °C	900			V
I_{DSS}	Off state drain current	V_{DS} = 850 V; Tj = 125 °C (See *Figure 4* and note)			80	µA
$R_{DS(on)}$	Drain-source ON-state resistance	Id=250 mA; Tj = 25 °C		16	19	W
		Id=250 mA; Tj = 125 °C			38	
C_{oss}	Effective (energy-related) output capacitance	(See *Figure 3*)				
High-voltage start-up generator						
V_{Start}	Min. Drain start voltage	I_{charge} < 100 µA	40	50	60	V
I_{charge}	Vcc startup charge current	V_{DRAIN}> V_{Start}; Vcc < Vcc_{On} Tj = 25 °C	4	5.5	7	mA
		V_{DRAIN}> V_{Start}; Vcc < Vcc_{On}	+/-10%			
$V_{CCrestart}$	Vcc restart voltage (Vcc falling)	(1)	9.5	10.5	11.5	V
		After protection tripping		5		
Supply voltage						
Vcc	Operating range	After turn-on	11.5		23	V
Vcc_{On}	Turn-on threshold	(1)	12	13	14	V
Vcc_{Off}	Turn-off threshold	(1)	9	10	11	V
V_Z	Zener voltage	Icc = 20 mA	23	25	27	V
Supply current						
$Icc_{start-up}$	Start-up current	(See *Figure 5*)		200	300	µA
Iq	Quiescent current	(See *Figure 6*)		1	1.4	mA
Icc	Operating supply current @ 50 kHz	(See *Figure 7*)		1.4	1.7	mA
$Iq_{(fault)}$	Fault quiescent current	During hiccup and brownout (See *Figure 8*)		250	350	µA
Start-up timer						
T_{START}	Start timer period		100	125	175	µs
$T_{RESTART}$	Restart timer period during burst mode		400	500	700	µs
Zero current detector						
I_{ZCDb}	Input bias current	V_{ZCD} = 0.1 to 3 V		0.1	1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA	3.0	3.3	3.6	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 1 mA	-90	-60	-30	mV
V_{ZCDA}	Arming voltage	positive-going edge	100	110	120	mV
V_{ZCDT}	Triggering voltage	negative-going edge	50	60	70	mV
I_{ZCDON}	Min. source current during MOSFET ON-time		-25	-50	-75	µA
T_{BLANK}	Trigger blanking time after MOSFET's turn-off	$V_{COMP} \geq 1.3V$		6		µs
		$V_{COMP} = 0.9V$		30		
Line feedforward						
R_{FF}	Equivalent feedforward resistor	I_{ZCD} = 1mA		45		Ω
Transconductance error amplifier						
V_{REF}	Voltage reference	Tj = 25°C (1)	2.46	2.5	2.54	V
		Tj = -25 to 125°C and Vcc=12V to 23V (1)	2.42		2.58	
gm	Transconductance	$\Delta I_{COMP} = \pm 10$ µA, V_{COMP} = 1.65 V	1.3	2.2	3.2	mS
Gv	Voltage gain	Open loop		73		dB
GB	Gain-bandwidth product			500		KHz
I_{COMP}	Source current	V_{ZCD} = 2.3V, V_{COMP} = 1.65V	70	100		µA
	Sink current	V_{ZCD} = 2.7V, V_{COMP} = 1.65V	400	750		µA
V_{COMPH}	Upper COMP voltage	V_{ZCD} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP voltage	V_{ZCD} = 2.7 V		0.7		V
V_{COMPBM}	Burst-mode threshold			1		V
Hys	Burst-mode hysteresis			65		mV
Current reference						
V_{IREFx}	Maximum value	$V_{COMP} = V_{COMPL}$ (1)	1.5	1.6	1.7	V
G_I	Current loop gain	$V_{COMP} = V_{COMPH}$	0.5	0.6	0.7	
V_{CREF}	Current reference voltage		0.38	0.4	0.42	V
Current sense						
t_{LEB}	Leading-edge blanking		200	250	300	ns
td(H-L)	Delay-to-output			300		ns
V_{CSx}	Max. clamp value	dVcs/dt = 200 mV/µs (1)	0.7	0.75	0.8	V
V_{CSdis}	Hiccup-mode OCP level	(1)	0.92	1	1.08	V

1. Parameters tracking each other

Figure 3. C_{OSS} Output capacitance variation

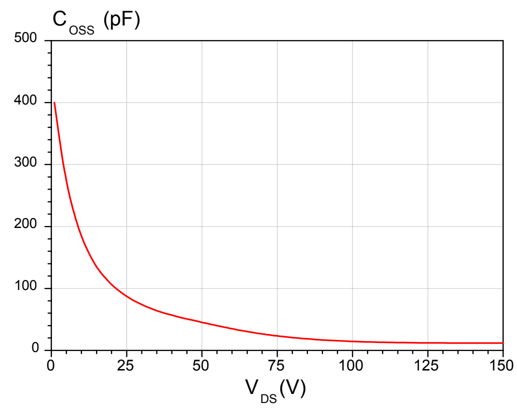
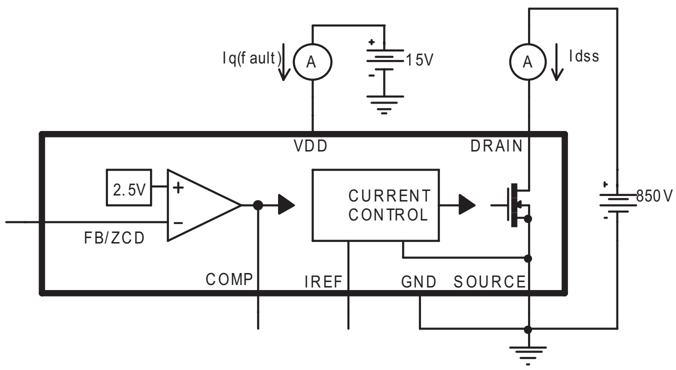


Figure 4. Off state drain and source current test circuit



Note: The measured I_{DSS} is the sum between the current across the start-up resistor and the effective MOSFET's off state drain current

Figure 5. Start-up current test circuit

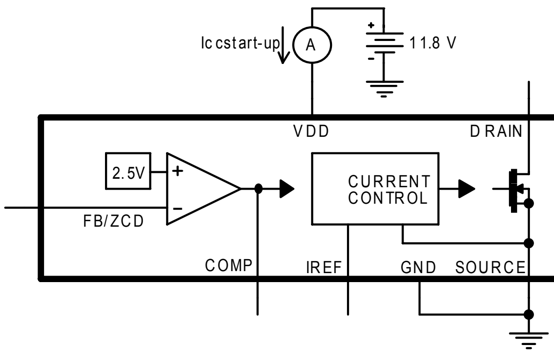


Figure 6. Quiescent current test circuit

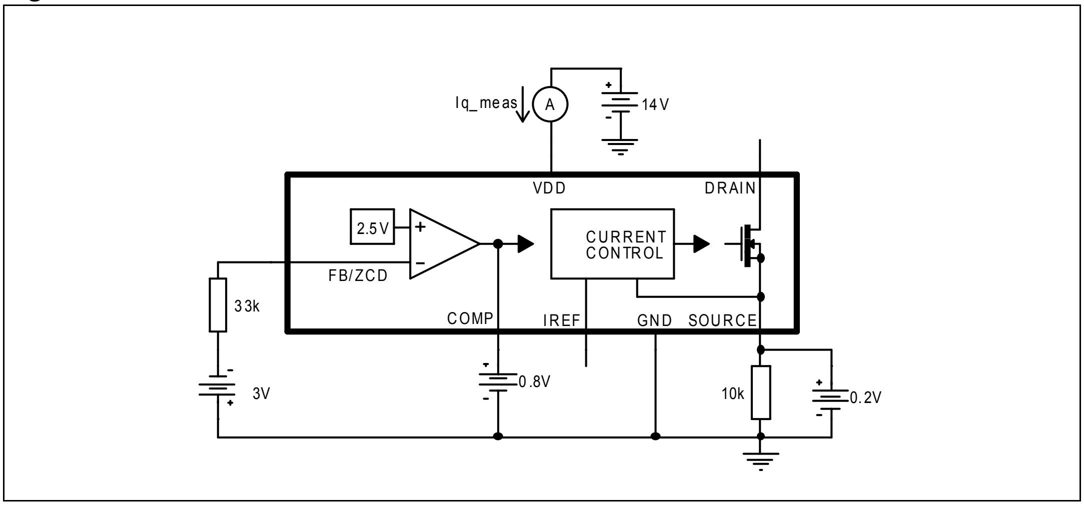
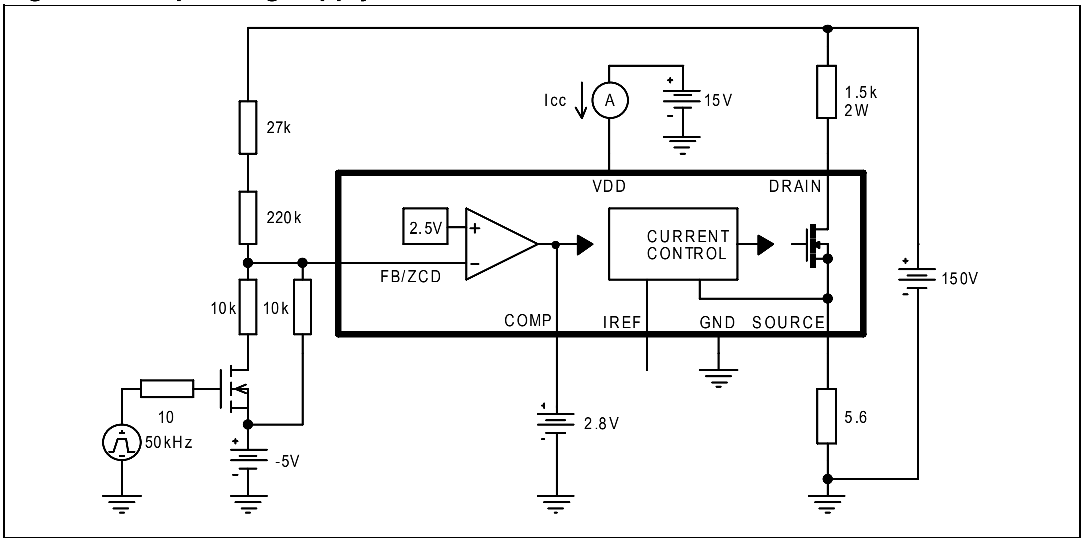
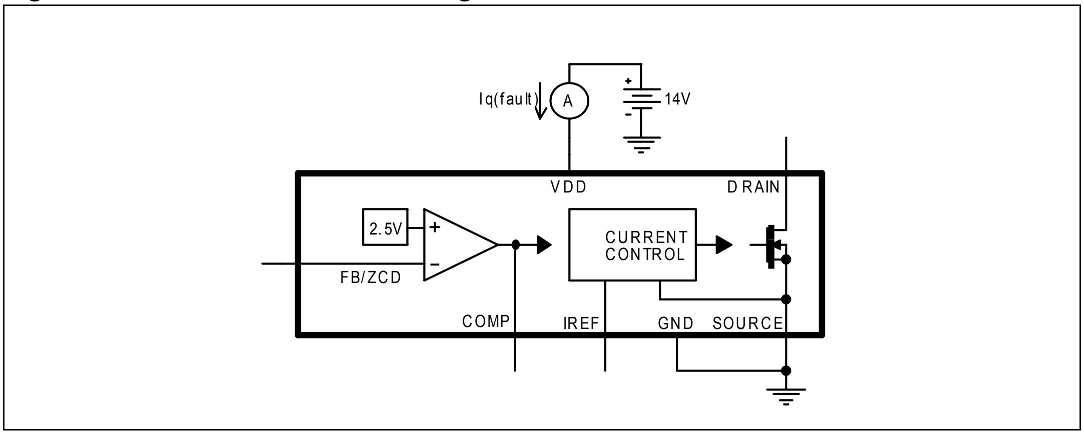


Figure 7. Operating supply current test circuit



Note: The circuit across the ZCD pin is used for switch-on synchronization

Figure 8. Quiescent current during fault test circuit



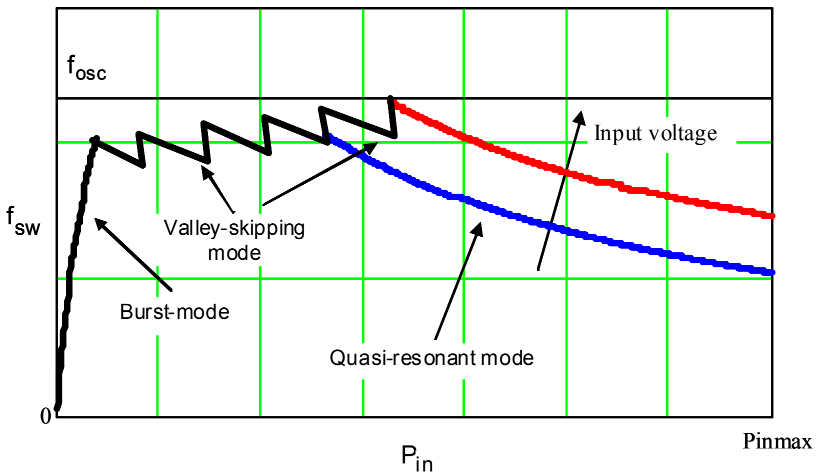
5 Application information

The device is an all-primary sensing switching regulator, based on quasi-resonant flyback topology.

Depending on converter's load condition, the device is able to work in different modes (see *Figure 9*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency is different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 9*). Minimum turn-on losses, low EMI emission and safe behavior in short circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. Depending on voltage on COMP pin, the device defines the maximum operating frequency of the converter. As the load is reduced MOSFET's turn-on does not any more occur on the first valley but on the second one, the third one and so on. In this way the switching frequency is no longer increased (piecewise linear portion in *Figure 9*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter enters a controlled on/off operation with constant peak current. Decreasing the load results in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 9. Multi-mode operation of ALTAIR04-900



5.1 Power section and gate driver

The power section guarantees safe avalanche operation within the specified energy rating as well as high dv/dt capability. The Power MOSFET has a $V_{(BR)DSS}$ of 900 V min. and a typical $R_{DS(on)}$ of 16 Ω.

The gate driver is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally.

5.2 High voltage startup generator

Figure 10 shows the internal schematic of the high-voltage start-up generator (HV generator). The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than Vstart threshold, 50 V_{DC} typically. When the HV current generator is ON, the Icharge current (5.5 mA typical value) is delivered to the capacitor on the V_{CC} pin.

With reference to the timing diagram of *Figure 10*, when power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it draws about 5.5 mA (typical) from the bulk capacitor. Most of this current charges the bypass capacitor connected between the Vcc pin and ground and make its voltage rise linearly.

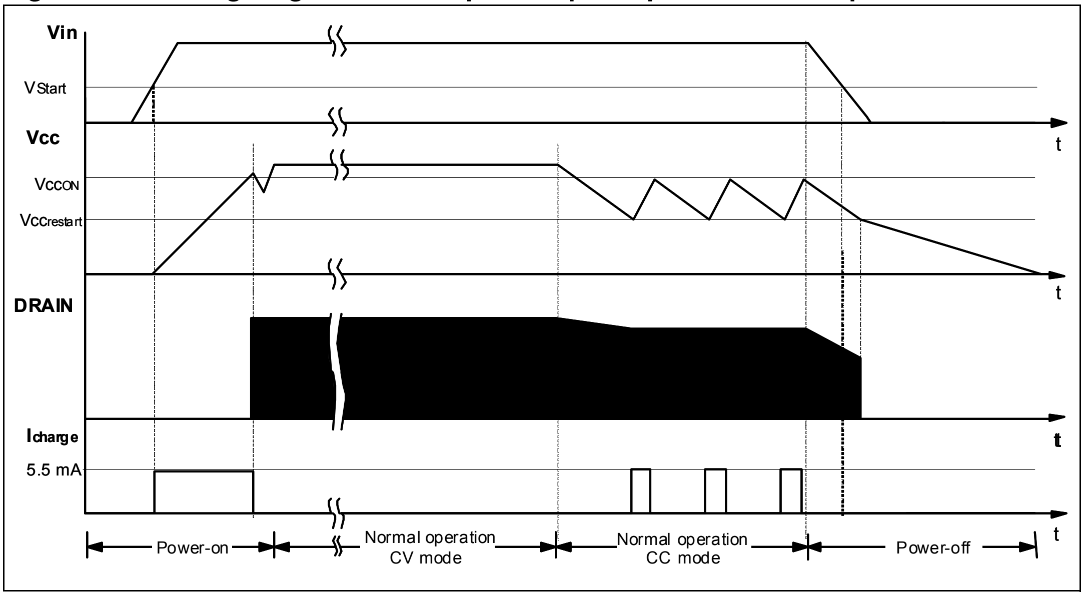
As the Vcc voltage reaches the start-up threshold (13 V typ.) the chip starts operating, the internal power MOSFET is enabled to switch and the HV generator is cut off by the Vcc_OK signal asserted high. The IC is powered by the energy stored in the Vcc capacitor.

The chip is able to power itself directly from the rectified mains: when the voltage on the V_{CC} pin falls below $Vcc_{restart}$ (10.5V typ.), during each MOSFET's off-time the HV current generator is turned on and charges the supply capacitor until it reaches the V_{CCOn} threshold.

In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during CC regulation, when the flyback voltage generated by the auxiliary winding alone may not be able to keep Vcc above VCCrestart.

At converter power-down the system loses regulation as soon as the input voltage falls below V_{Start}. This prevents converter's restart attempts and ensures monotonic output voltage decay at system power-down.

Figure 10. Timing diagram: normal power-up and power-down sequences

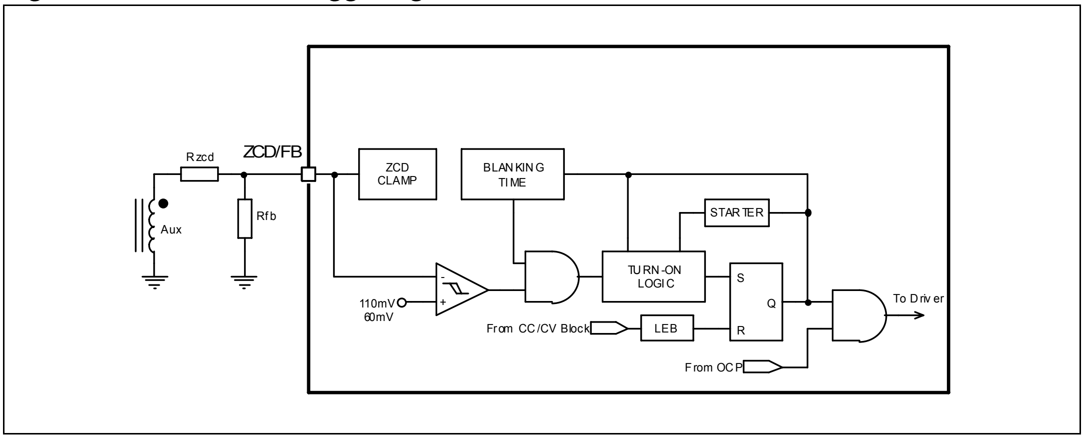


5.3 Zero current detection and triggering block

The zero current detection (ZCD) and triggering blocks switch on the power MOSFET if a negative-going edge falling below 50 mV is applied to the ZCD/FB pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is used to detect transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the IC.

Figure 11. ZCD block, triggering block



The triggering block is blanked after MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

This blanking time is dependent on the voltage on COMP pin: it is T_{BLANK} = 30 µs for V_{COMP} = 0.9 V, and decreases almost linearly down to T_{BLANK} = 6 µs for V_{COMP} = 1.3 V

The voltage on the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block of *Figure 11*. The upper clamp is typically at 3.3 V, while the lower clamp is located at -60mV. The interface between the pin and the auxiliary winding is a resistor divider. Its resistance ratio as well as the individual resistance values has to be properly chosen (see "*Section 5.4: Constant voltage operation*" and "*Section 5.6: Voltage feedforward block*".

Please note that the maximum $I_{ZCD/FB}$ sunk/sourced current has to not exceed ±2 mA (AMR) in all the Vin range conditions. No capacitor is allowed between ZCD pin and the auxiliary transformer.

The switching frequency is top-limited below 166 kHz, as the converter's operating frequency tends to increase excessively at light load and high input voltage.

A Starter block is also used to start-up the system, that is, to turn on the MOSFET during converter power-up, when no or a too small signal is available on the ZCD pin.

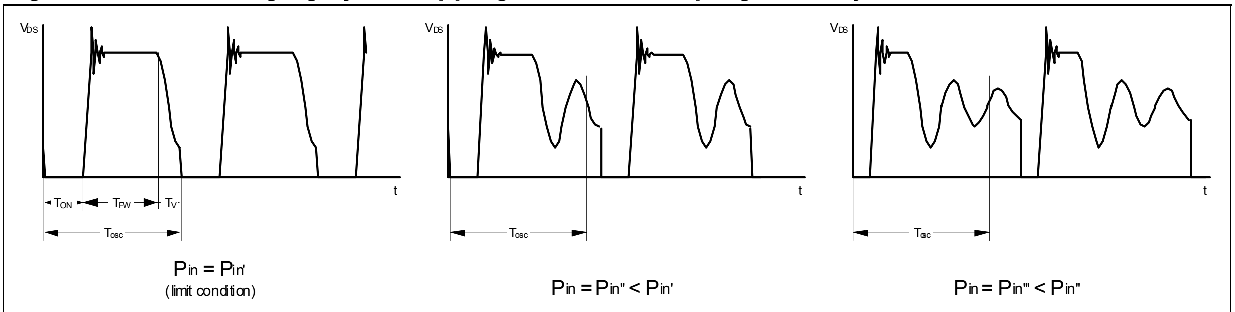
The starter frequency is 2 kHz if COMP pin below burst mode threshold, i.e. 1 V, while it becomes 8 kHz if this voltage exceed this value.

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the ZCD circuit, MOSFET's turn-on starts to be locked to transformer demagnetization, hence setting up QR operation.

The starter is activated also when the IC is in CC regulation and the output voltage is not high enough to allow the ZCD triggering.

If the demagnetization completes – hence a negative-going edge appears on the ZCD pin – after a time exceeding time T_{BLANK} from the previous turn-on, the MOSFET is turned on again, with some delay to ensure minimum voltage at turn-on. If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it is ignored and only the first negative-going edge after T_{BLANK} turns-on the MOSFET. In this way one or more drain ringing cycles is skipped ("valley-skipping mode", *Figure 12*) and the switching frequency is prevented from exceeding $1/T_{BLANK}$.

Figure 12. Drain ringing cycle skipping as the load is progressively reduced



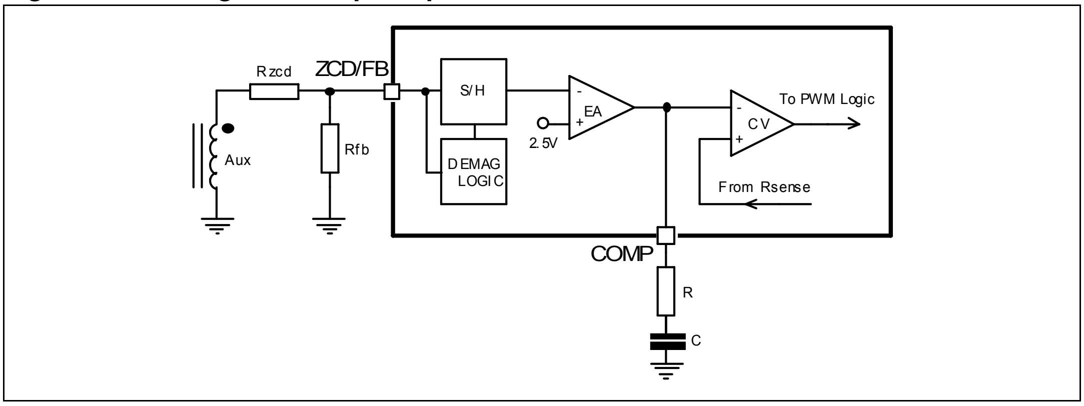
Note that when the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles is compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

5.4 Constant voltage operation

The IC is specifically designed to work in primary regulation and the output voltage is sensed through a voltage partition of the auxiliary winding, just before the auxiliary rectifier diode.

Figure 13 shows the internal schematic of the constant voltage mode and the external connections.

Figure 13. Voltage control principle: internal schematic



Due to the parasitic wires resistance, the auxiliary voltage is representative of the output just when the secondary current becomes zero. For this purpose, the signal on ZCD/FB pin is sampled-and-held at the end of transformer's demagnetization to get an accurate image of the output voltage and it is compared with the error amplifier internal reference.

The COMP pin is used for the frequency compensation: usually, an RC network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

The output voltage can be defined according the formula:

$$R_{FB} = \frac{V_{REF}}{\frac{N_{AUX}}{N_{SEC}} \cdot V_{OUT} - V_{REF}} \cdot R_{ZCD} \quad (1)$$

Where N_{SEC} and N_{AUX} are the secondary and auxiliary turn's number respectively.

The R_{ZCD} value can be defined depending on the application parameters (see "*Section 5.6: Voltage feedforward block*").

5.5 Constant current operation

Figure 14 presents the principle used for controlling the average output current of the flyback converter.

The output voltage of the auxiliary winding is used by the demagnetization block to generate the control signal for the mosfet switch Q1. A resistor R in series with it absorbs a current V_C/R, where V_C is the voltage developed across the capacitor Cref.

The flip-flop's output is high as long as the transformer delivers current on secondary side. This is shown in *Figure 15*.

The capacitor Cref has to be chosen so that its voltage V_C can be considered as a constant. Since it is charged and discharge by currents in the range of some ten µA (I_{CREF} is typically 20 µA) at the switching frequency rate, a capacitance value in the range 4.7-10 nF is suited for switching frequencies in the ten kHz.

The average output current can be expressed as:

$$I_{OUT} = \frac{N_{PRI}}{N_{SEC}} \cdot \frac{G_I \cdot V_{CREF}}{(2 \cdot R_{SENSE})} \quad (2)$$

where N_{PRI} is the primary turn's number.

This formula shows that the average output current does not depend anymore on the input or the output voltage, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio n and the sense resistor R_{SENSE}.

Current loop gain G_I and current reference voltage V_{CREF} are internally defined.

Figure 14. Current control principle

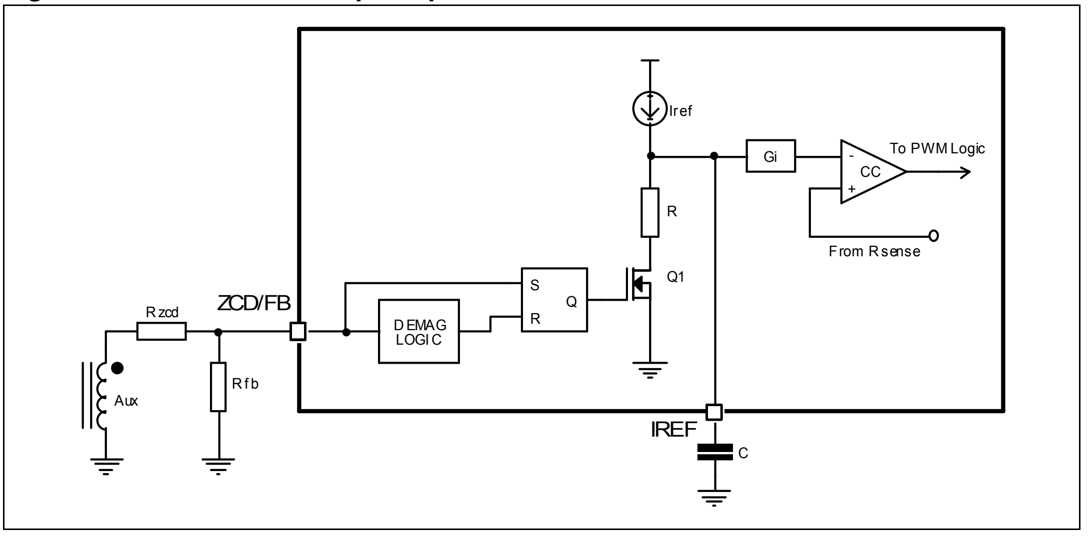
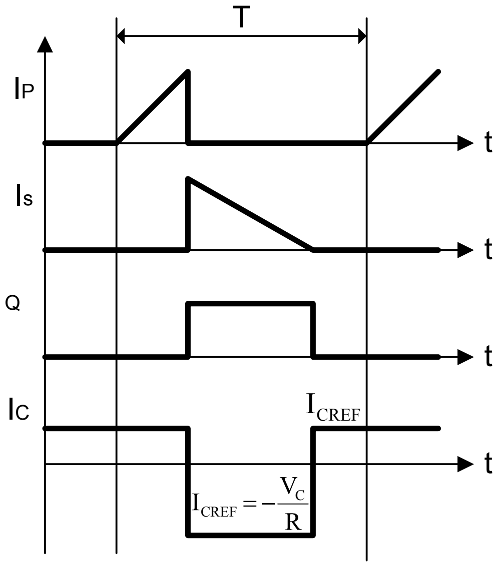


Figure 15. Constant current operation: Switching cycle waveforms



5.6 Voltage feedforward block

The current control structure uses the voltage V_C to define the output current, according to (2). Actually, the CC comparator is affected by an internal propagation delay Td, which switches off the MOSFET with a peak current than higher the foreseen value.

This current overshoot is equal to:

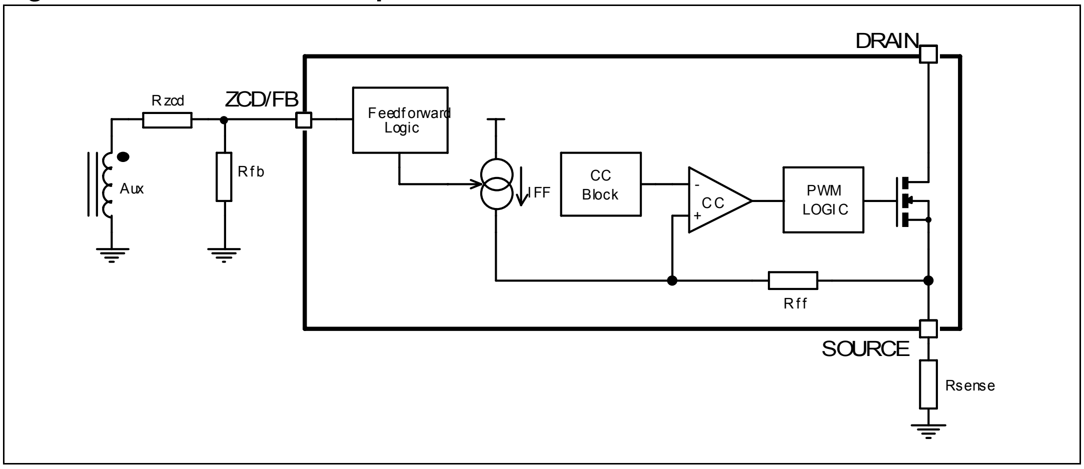
$$\Delta I_P = \frac{V_{IN} \cdot T_d}{L_P} \quad (3)$$

where Lp is the primary inductance and it introduces an error on the calculated CC setpoint, depending on the input voltage.

The device implements a line feedforward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The internal schematic is shown in *Figure 16*.

Figure 16. Feedforward compensation: internal schematic



The R_{ZCD} resistor can be calculated as follows:

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{L_P \cdot R_{FF}}{T_d \cdot R_{SENSE}} \tag{4}$$

In this case the peak drain current does not depend on input voltage anymore.

One more consideration concerns the R_{ZCD} value: during MOSFET's ON-time, the current sourced by the ZCD/FB pin, I_{ZCD}, is compared with an internal reference current I_{ZCDON} (-50 µA typical).

If $I_{ZCD} < I_{ZCDON}$, the brownout function is activated and the IC is shut-down.

This feature is especially important when the auxiliary winding is accidentally disconnected and considerably increases the end-product's safety and reliability.

5.7 Burst-mode operation at no load or very light load

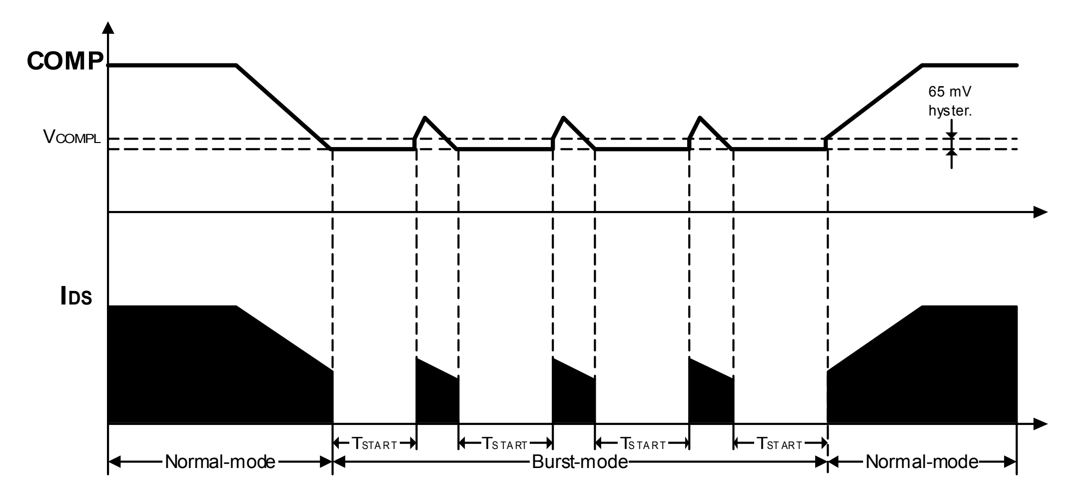
When the voltage at the COMP pin falls 65 mV below a threshold fixed internally at a value, V_{COMPBM}, the IC is disabled with the MOSFET kept in OFF state and its consumption reduced at a lower value to minimize Vcc capacitor discharge.

In this condition the converter operates in burst-mode (one pulse train every T_{START}=500 µs), with minimum energy transfer.

As a result of the energy delivery stop, the output voltage decreases: after 500 µs the controller switches-on the MOSFET again and the sampled voltage on the ZCD pin is compared with the internal reference. If the voltage on the EA output, as a result of the comparison, exceeds the V_{COMPL} threshold, the device restarts switching, otherwise it stays OFF for another 500 µs period.

In this way the converter works in burst-mode with a nearly constant peak current defined by the internal disable level. Then a load decrease causes a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 17* along with the others previously described, is noise-free since the peak current is low

Figure 17. Load-dependent operating modes: timing diagrams



5.8 Soft-start and starter block

The soft start feature is automatically implemented by the constant current block, as the primary peak current is limited from the voltage on the C_{REF} capacitor.

During start-up, as the output voltage is zero, the IC starts in CC mode with no high peak current operations. In this way the voltage on the output capacitor increases slowly and the soft-start feature is ensured.

Actually the CREF value is not important to define the soft-start time, as its duration depends on others circuit parameters, like transformer ratio, sense resistor, output capacitors and load. The user can define the best appropriate value by experiments.

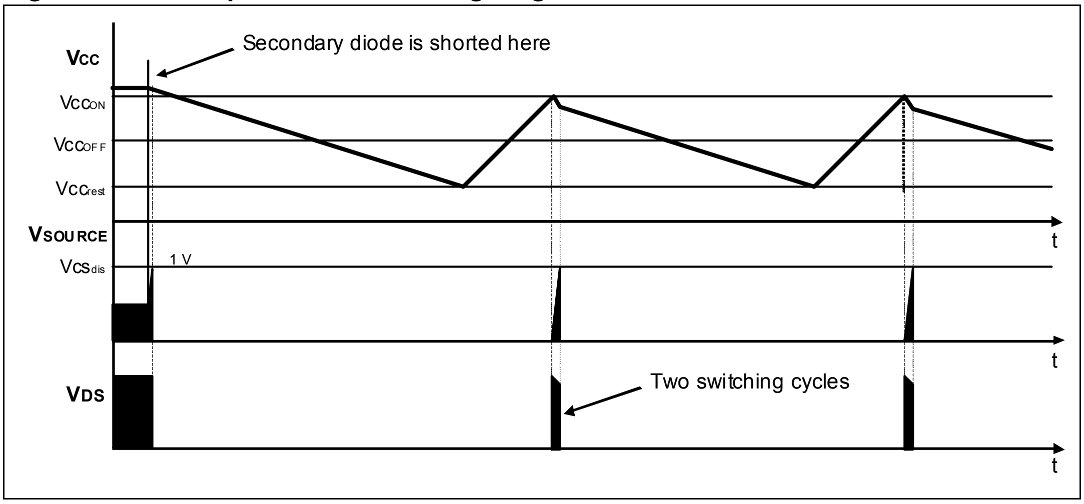
5.9 Hiccup mode OCP

The device is also protected against short circuit of the secondary rectifier, short circuit on the secondary winding or a hard-saturated flyback transformer. A comparator monitors continuously the voltage on the R_{SENSE} and activates a protection circuitry if this voltage exceeds 1 V.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator is tripped again a real malfunction is assumed and the device is stopped.

This condition is latched as long as the device is supplied. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the V_{CC} capacitor decays and cross the UVLO threshold after some time, which clears the latch. The internal start-up generator is still off, then the V_{CC} voltage still needs to go below its restart voltage before the V_{CC} capacitor is charged again and the device restarted. Ultimately, this results in a low-frequency intermittent operation (Hiccup-mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 18*.

Figure 18. Hiccup-mode OCP: timing diagram

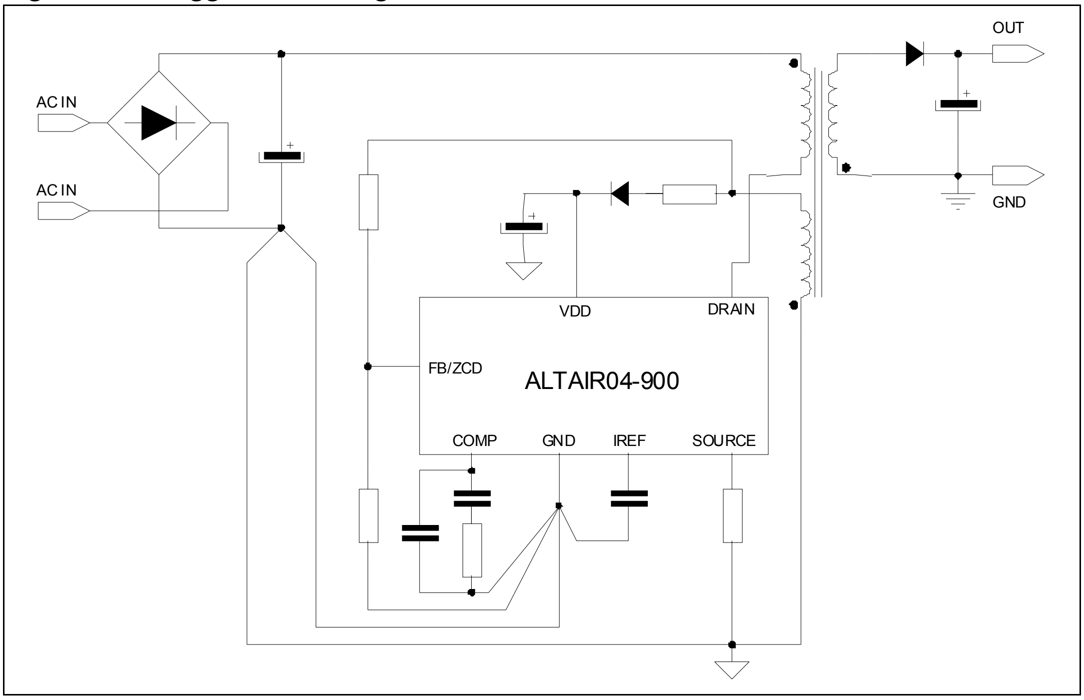


5.10 Layout recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the ALTAIR04-900 as well. Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues. In particular:

- The compensation network should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible
- Signal Ground should be routed separately from power ground, as well from the sense resistor trace.

Figure 19. Suggested routing for converter



6 Typical application

Figure 20. Test board schematic: 4.5 W (9 V - 500 mA) wide range mains adapter

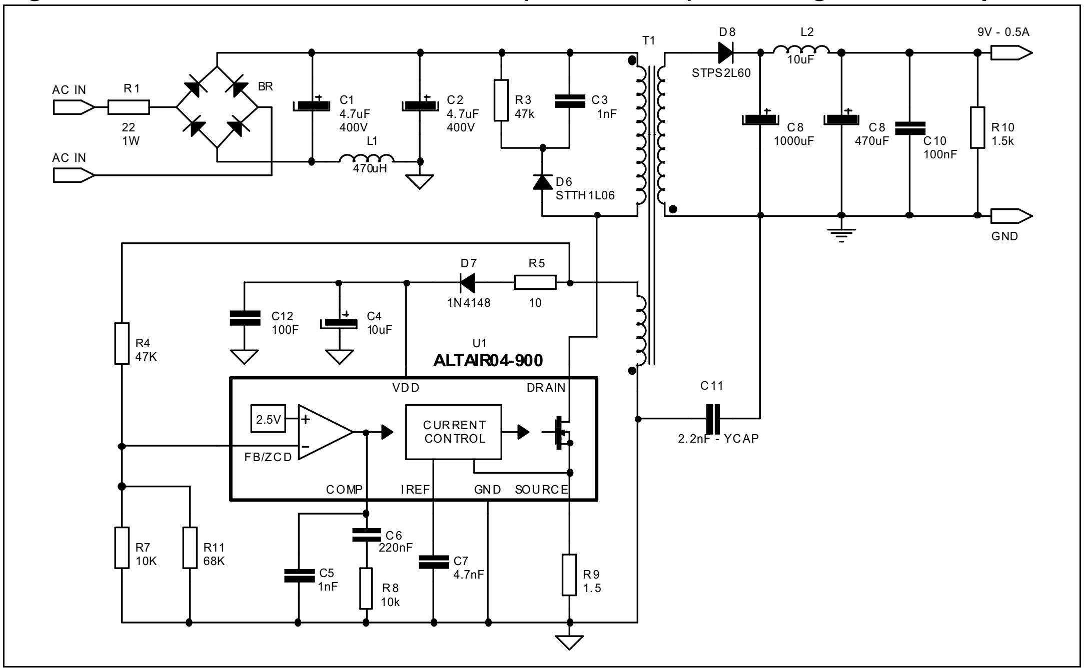
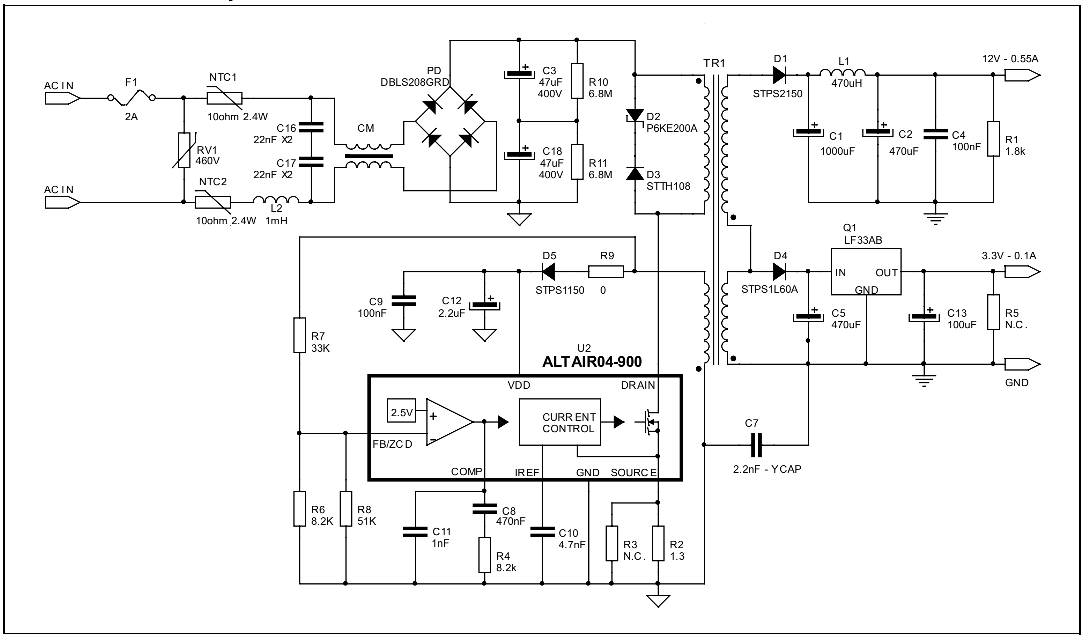


Figure 21. Electrical schematic for 440 Vac input voltage option thanks to the 900 V rated power section of Altair04-900



6.1 Test board: evaluation data

Figure 22. No-load consumption

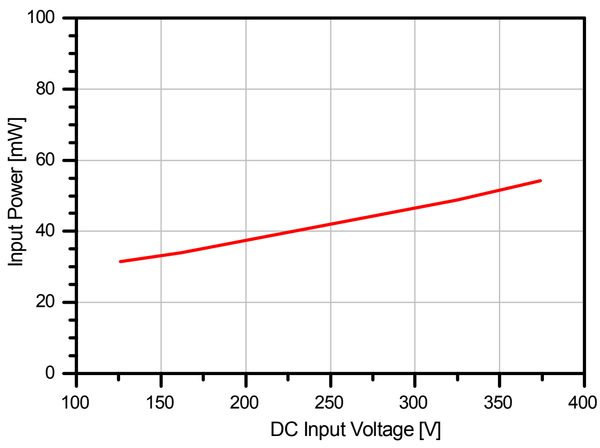


Figure 23. Efficiency at full load

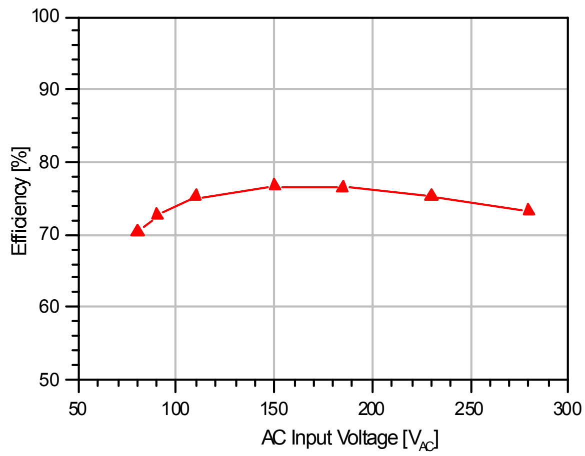


Figure 24. VI Curve @ 110 V_{AC}

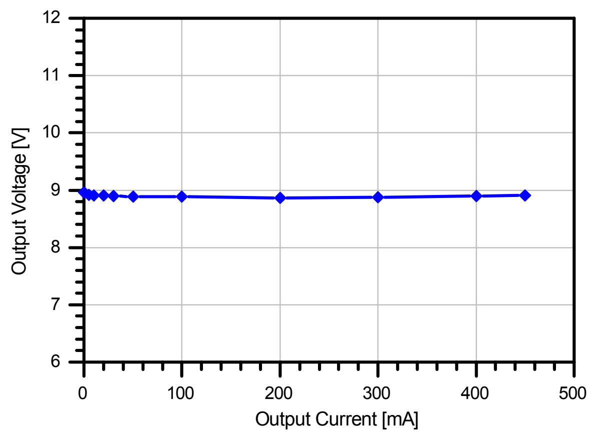
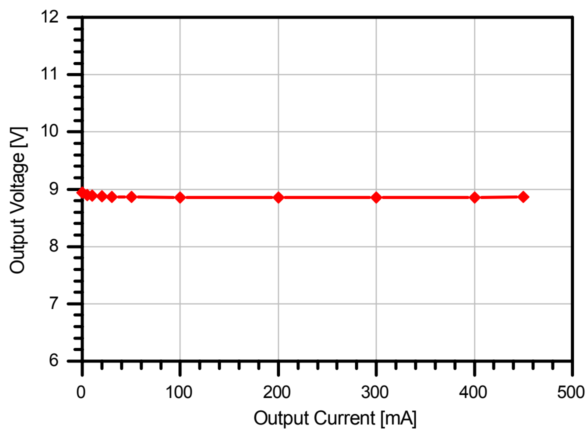
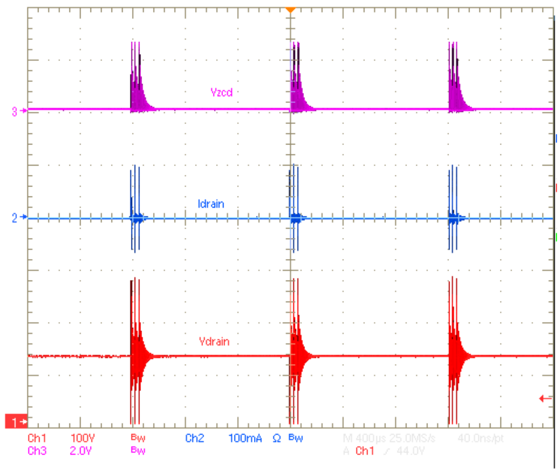


Figure 25. VI Curve @ 264 V_{AC}



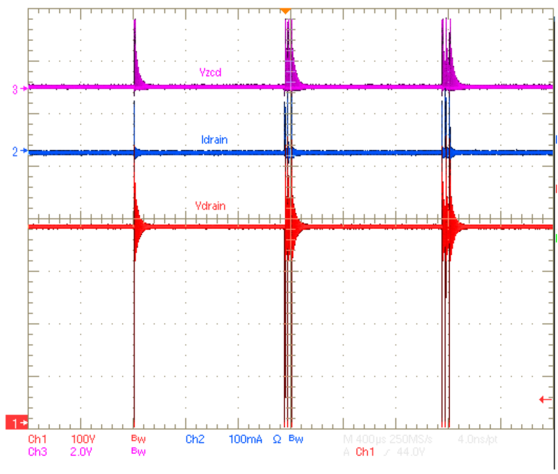
6.2 Test board: main waveforms

Figure 26. 110 V_{AC}, No-load



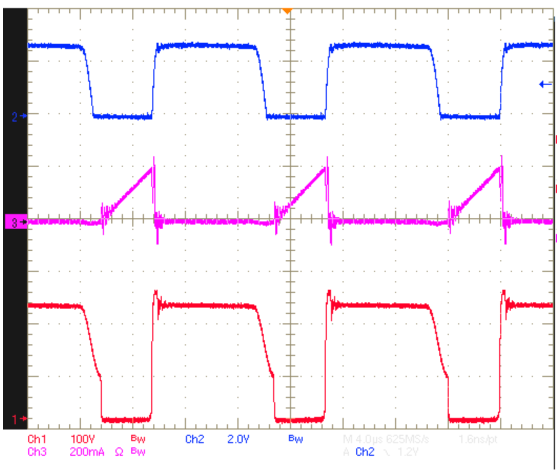
M: 400 s/div

Figure 27. 264 V_{AC}, No-load



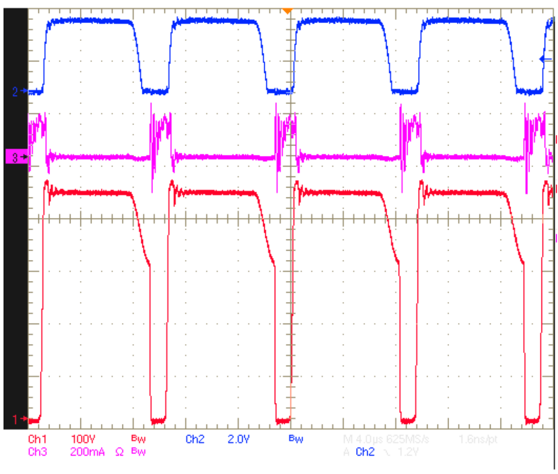
M: 400 s/div

Figure 28. 110 V_{AC}, Full load



M: 400 s/div

Figure 29. 234 V_{AC}, Full load



M: 400 s/div

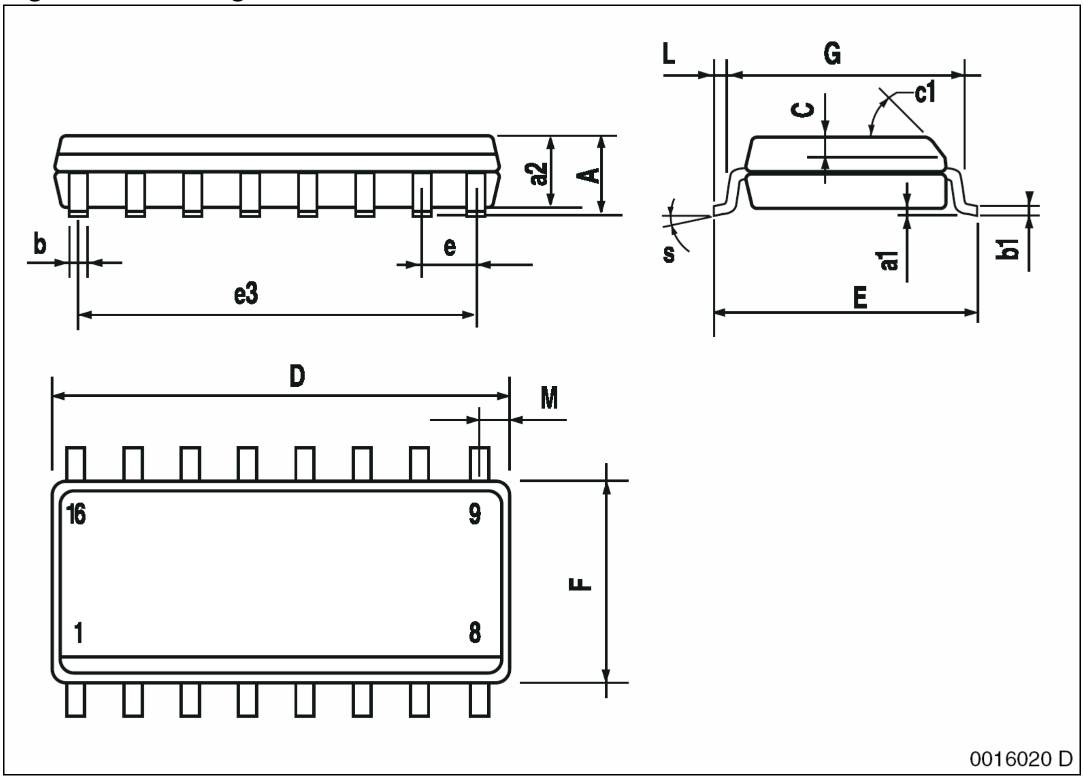
7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 5. SO16N mechanical data

Dim.	Mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1			45°	(typ.)		
D (1)	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F(1)	3.8		4.0	0.150		0.157
G	4.60		5.30	0.181		0.208
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8 °(max.)					

Figure 30. Package dimensions



8 Order codes

Table 6. Ordering information

Order code	Package	Packaging
ALTAIR04-900	SO16N	Tube
ALTAIR04-900TR		Tape and reel

9 Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Nov-2010	1	Initial release
25-Jan-2011	2	Updated *Chapter Table 4. on page 7*