

# AFE5401-Q1 Quad-Channel, Analog Front-End for Automotive Radar Baseband Receiver

## 1 Features

- Integrated Analog Front-End Includes:
  - Quad LNA, Equalizer, PGA, Antialiasing Filter, and ADC
- PGA Input-Referred Noise:  $3.0 \text{ nV}/\sqrt{\text{Hz}}$
- Simultaneous Sampling Across Channels
- Programmable LNA Gain
- Optional Equalizer Mode
- Programmable-Gain Amplifiers (PGAs)
- Programmable, Third-Order, Antialiasing Filter:
  - 7 MHz, 8 MHz, 10.5 MHz, and 12 MHz
- Parallel CMOS Outputs
- 64-mW Total Core Power per Channel
- Supplies: 1.8 V and 3.3 V

## 2 Applications

- Automotive Radar
- Data Acquisition
- SONAR™

## 3 Description

The AFE5401-Q1 includes four channels, with each channel comprising a low-noise amplifier (LNA), an optional equalizer (EQ), a programmable gain amplifier (PGA), and an antialias filter followed by a high-speed, 12-bit, analog-to-digital converter (ADC) at 25 MSPS per channel.

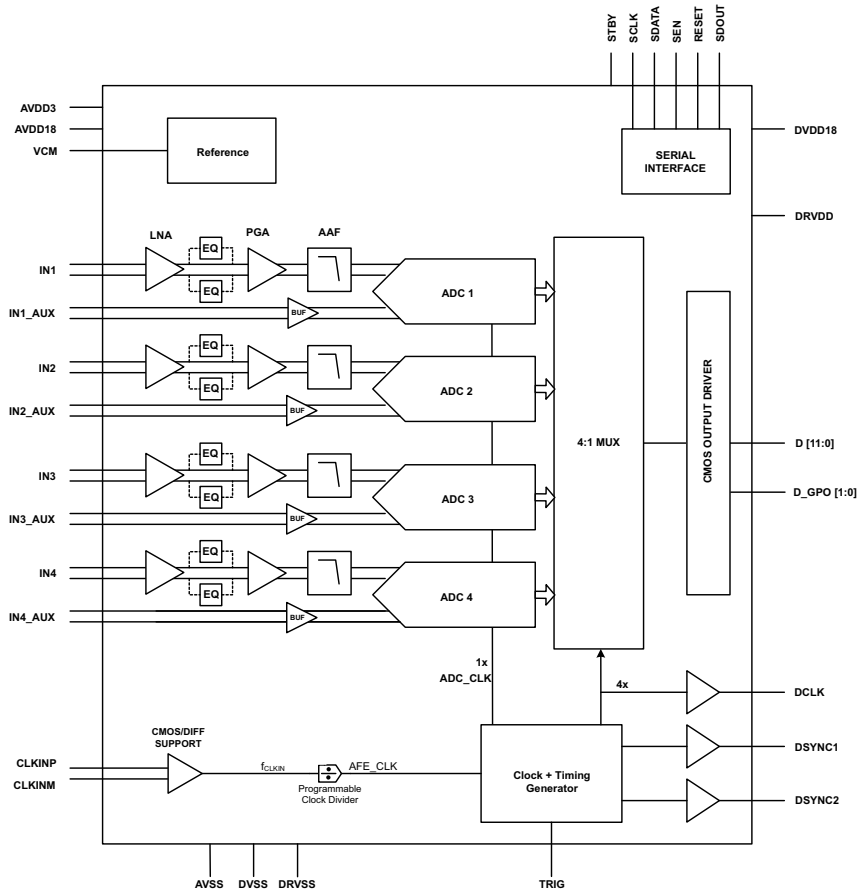
The four ADC outputs are multiplexed on a 12-bit, parallel, CMOS-compatible output bus.

To request a full data sheet or other design resources: [request AFE5401-Q1](#)

### Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
AFE5401TRGCRQ1	VQFN (64)	9 mm x 9 mm
AFE5401TRGCTQ1	VQFN (64)	9 mm x 9 mm

**Functional Block Diagram**



## 4 Revision History

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**Changes from Revision B (March 2014) to Revision C** **Page**

- Added link to request full data sheet ..... 1
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**Changes from Revision A (February 2014) to Revision B** **Page**

- Changed device status from Product Preview to Production Data ..... 1
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**Changes from Original (December 2013) to Revision A** **Page**

- Changed data sheet title ..... 1
  - Added Applications section ..... 1
  - Added the Device Information table ..... 1
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## 5 Device and Documentation Support

### 5.1 Trademarks

SONAR is a trademark of Cakewalk, Inc.  
All other trademarks are the property of their respective owners.

### 5.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 5.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE5401TRGCRQ1	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AFE5401	<a href="#">Samples</a>
AFE5401TRGCTQ1	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AFE5401	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE5401TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
AFE5401TRGCTQ1	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

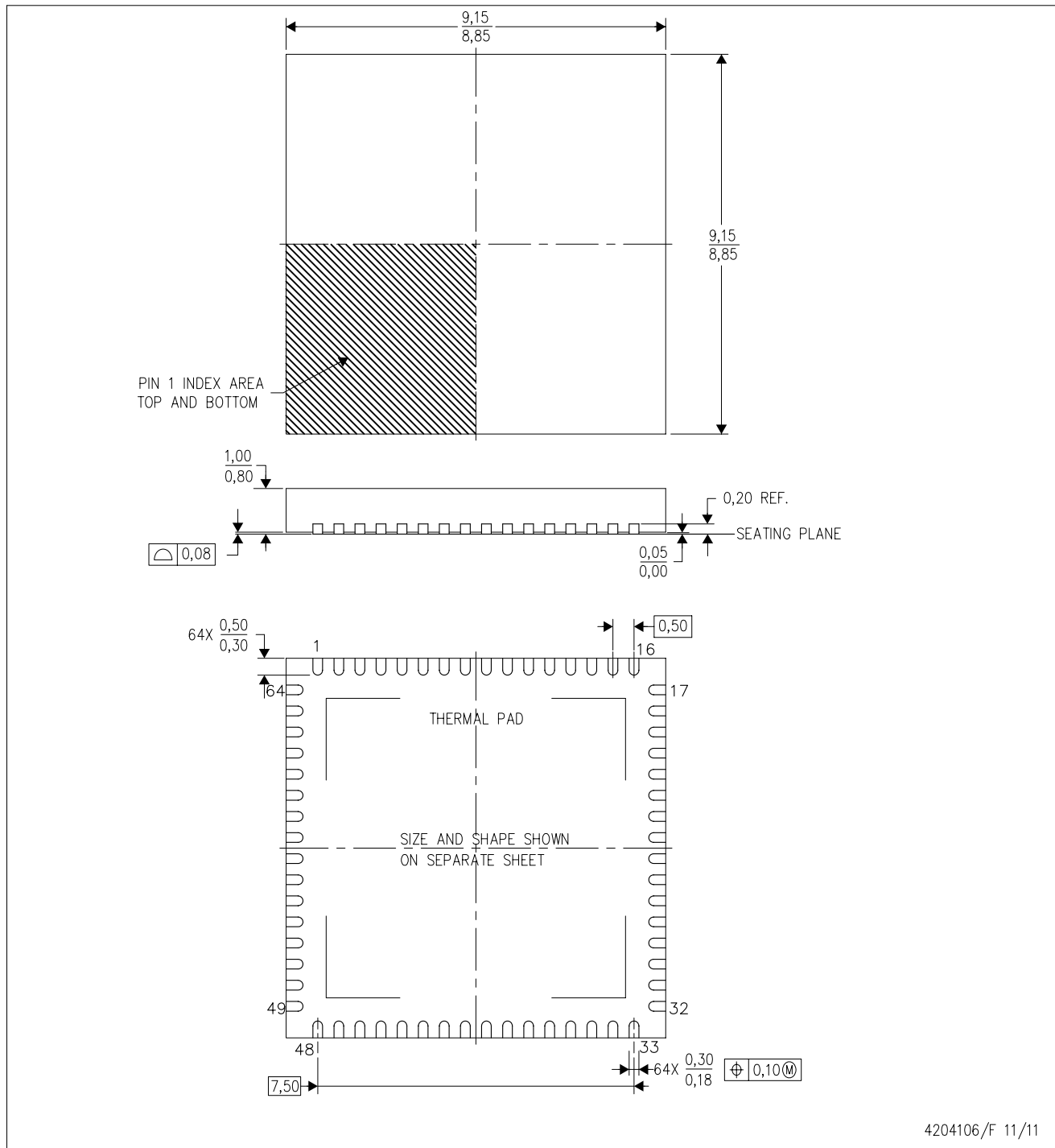
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE5401TRGCRQ1	VQFN	RGC	64	2000	336.6	336.6	28.6
AFE5401TRGCTQ1	VQFN	RGC	64	250	213.0	191.0	55.0

# MECHANICAL DATA

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



# THERMAL PAD MECHANICAL DATA

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD

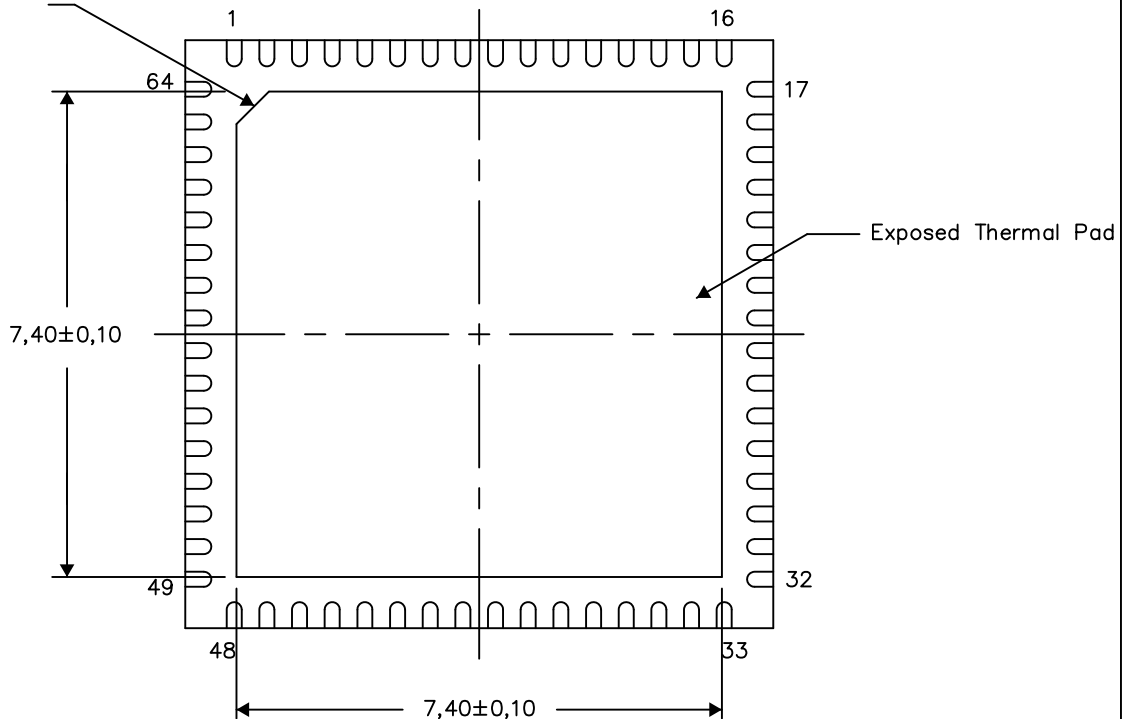
## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR  
CO,35



Bottom View

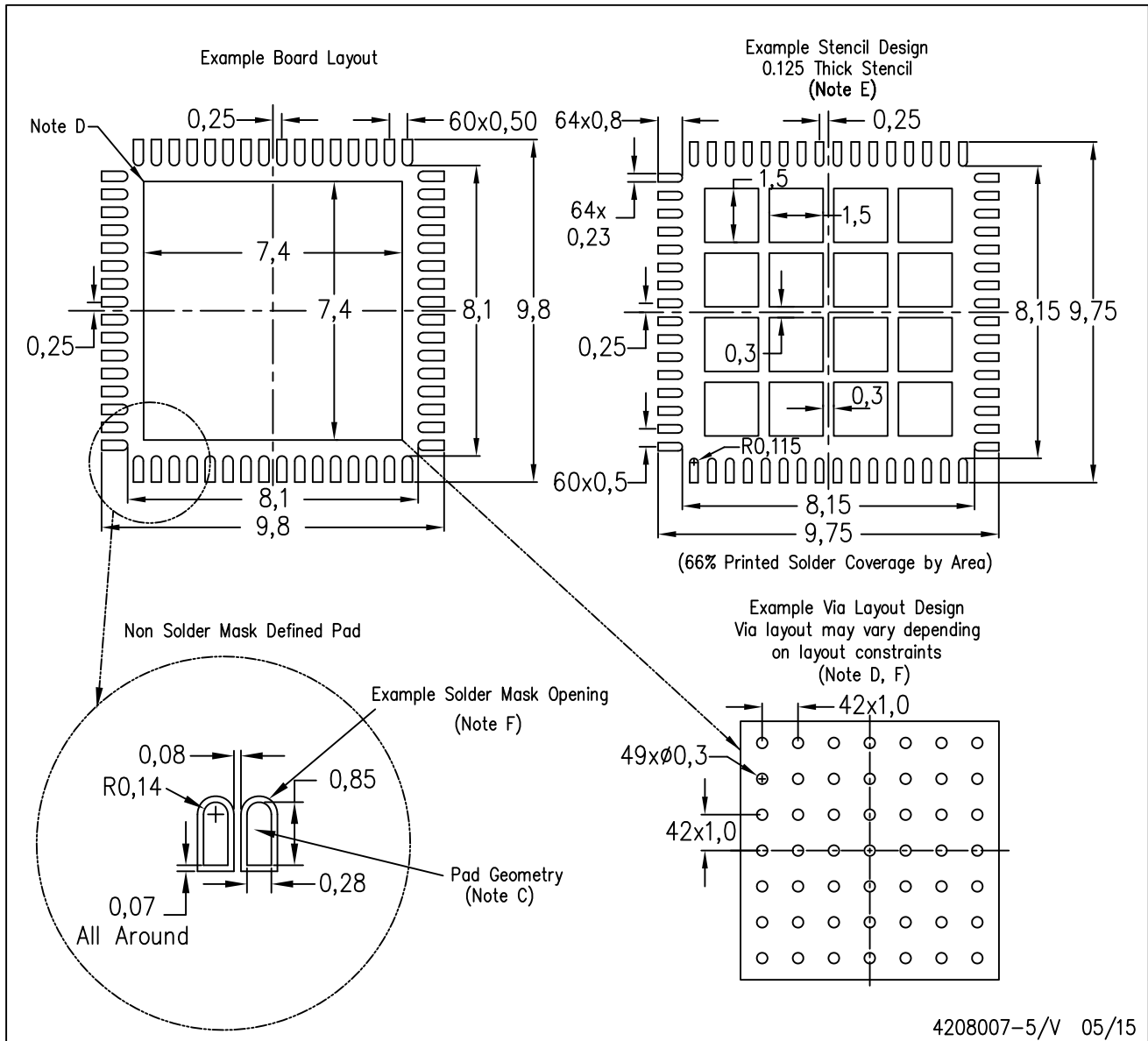
Exposed Thermal Pad Dimensions

4206192-4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S-PVQFN-N64)

PLASTIC QUAD FLATPACK NO-LEAD



4208007-5/V 05/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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