ADS131E08S Eight-Channel, 24-Bit, Analog Front-End with Fast Power-Up Time

1 Features

- Power-Up Time: 3 ms
- Eight Differential Simultaneous Sampling Inputs
- High Performance:
  - Dynamic Range at 1 kSPS: 118 dB
  - Crosstalk: –125 dB
  - THD: –100 dB at 50 Hz and 60 Hz
- Low Power Consumption: 2 mW/Channel
- Data Rates: 1, 2, 4, 8, 16, 32, and 64 kSPS
- Gain Options: 1, 2, 4, 8, and 12
- Internal Voltage Reference: 8 ppm/°C Drift
- Supply Range:
  - Analog:
    - 2.7 V to 5.25 V (Unipolar)
    - ±2.5 V (Bipolar)
  - Digital: 1.7 V to 3.6 V
- Fault Detection and Device Self-Testing Capability
- SPI™ Compatible Data Interface and Four GPIOs
- Package: 64-Pin TQFP
- Operating Temperature Range: –40°C to +105°C

2 Applications

- Industrial Power Applications:
  - Circuit Breakers, Protection Relays, Power Monitoring
- Data Acquisition Systems

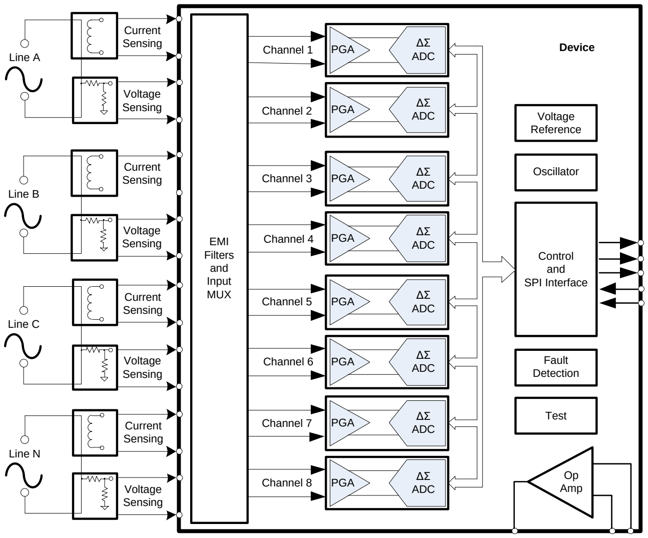
3 Description

The ADS131E08S is a multichannel, simultaneous sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with built-in programmable gain amplifiers (PGAs), an internal reference, and an internal oscillator. The ADC wide dynamic range, scalable data rates, and internal fault detect monitors make the ADS131E08S very attractive in industrial power monitoring, control, and protection applications. Fast power-up time allows data to be available within 3 ms of power being applied to the device for line-powered power applications. True high-impedance inputs enable the ADS131E08S to directly interface with a resistor-divider network or a voltage transformer to measure line voltage, or a current transformer or Rogowski coil to measure line current. With high integration levels and exceptional performance, the ADS131E08S enables the creation of scalable industrial power systems at a significantly reduced size, power, and overall cost.

The ADS131E08S has an individual input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and fault detection. Fault detection can be implemented internal to the device, using the integrated comparators with digital-to-analog converter (DAC)-controlled trigger levels. The ADS131E08S can operate at data rates as high as 64 kSPS.

The complete analog front-end (AFE) solution is available in a 64-pin TQFP package and is specified over the industrial temperature range of –40°C to +105°C.

Power Application: Three-Phase Voltage and Current Connection



Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS131E08S	TQFP (64)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Changes from Original (October 2015) to Revision A — **Page**

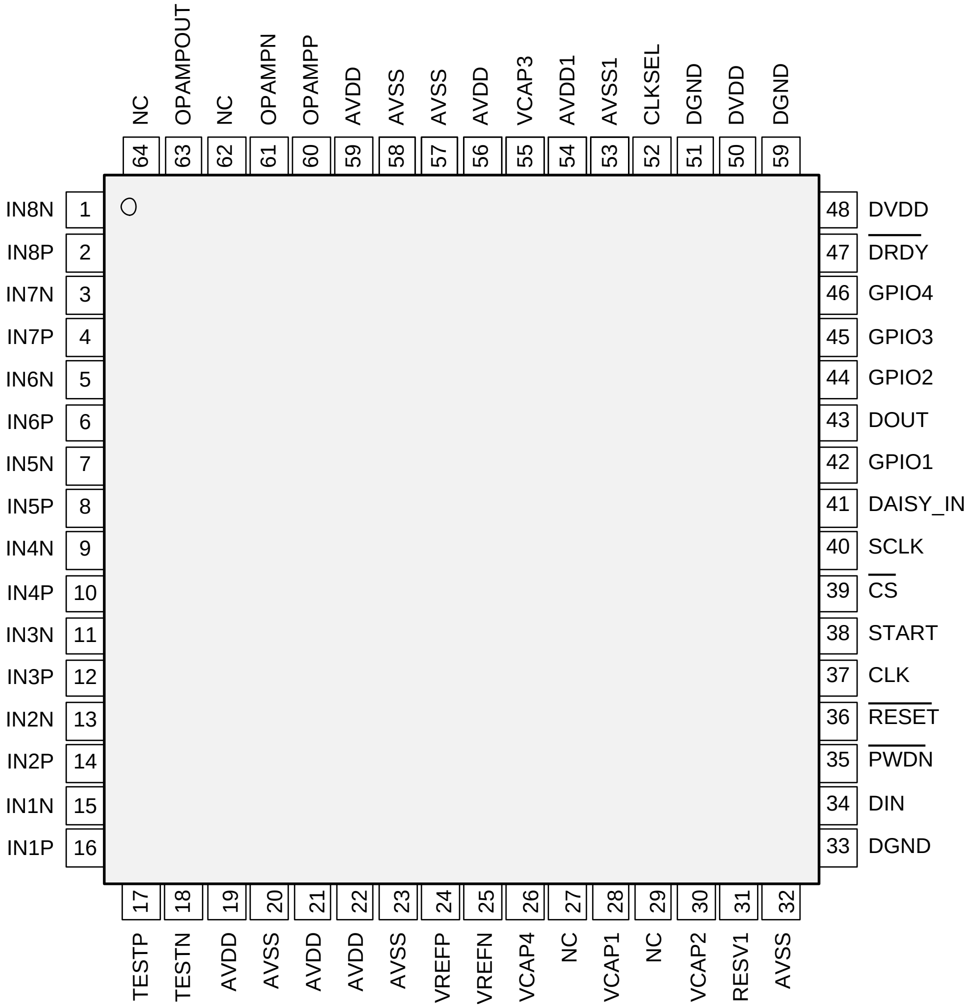
- Released to production 1

5 Device Comparison

PRODUCT	# OF INPUTS	REFERENCE OPTIONS	RESOLUTION (Bits)	POWER-UP TIME (ms)
ADS130E08	8	Internal, external	16	128
ADS131E04	4	Internal, external	24	128
ADS131E06	6	Internal, external	24	128
ADS131E08	8	Internal, external	24	128
ADS131E08S	8	Internal only	24	3

6 Pin Configuration and Functions

PAG Package
64-Pin TQFP
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AVDD	19, 21, 22, 56, 59	Supply	Analog supply; decouple each AVDD pin to AVSS with a 1-µF capacitor
AVDD1	54	Supply	Charge pump analog supply; decouple AVDD1 to AVSS1 with a 1-µF capacitor
AVSS	20, 23, 32, 57, 58	Supply	Analog ground
AVSS1	53	Supply	Charge pump analog ground; decouple AVDD1 to AVSS1 with a 1-µF capacitor
$\overline{\text{CS}}$	39	Digital input	Serial peripheral interface (SPI) chip select; active low
CLK	37	Digital input	Master clock input; connect to DGND if unused
CLKSEL	52	Digital input	Master clock select
DAISY_IN	41	Digital input	Daisy-chain input; connect to DGND if unused
DGND	33, 49, 51	Supply	Digital ground
DIN	34	Digital input	SPI data input
DOUT	43	Digital output	SPI data output
$\overline{\text{DRDY}}$	47	Digital output	Data ready; active low; connect to DGND with a 10-kΩ resistor if unused
DVDD	48, 50	Supply	Digital power supply; decouple each DVDD pin to DGND with a 1-µF capacitor
GPIO1	42	Digital input/output	General-purpose input/output pin 1; connect to DGND with a 10-kΩ resistor if unused
GPIO2	44	Digital input/output	General-purpose input/output pin 2; connect to DGND with a 10-kΩ resistor if unused
GPIO3	45	Digital input/output	General-purpose input/output pin 3; connect to DGND with a 10-kΩ resistor if unused
GPIO4	46	Digital input/output	General-purpose input/output pin 4; connect to DGND with a 10-kΩ resistor if unused
IN1N(1)	15	Analog input	Negative analog input 1
IN1P(1)	16	Analog input	Positive analog input 1
IN2N(1)	13	Analog input	Negative analog input 2
IN2P(1)	14	Analog input	Positive analog input 2
IN3N(1)	11	Analog input	Negative analog input 3
IN3P(1)	12	Analog input	Positive analog input 3
IN4N(1)	9	Analog input	Negative analog input 4
IN4P(1)	10	Analog input	Positive analog input 4
IN5N(1)	7	Analog input	Negative analog input 5
IN5P(1)	8	Analog input	Positive analog input 5
IN6N(1)	5	Analog input	Negative analog input 6
IN6P(1)	6	Analog input	Positive analog input 6
IN7N(1)	3	Analog input	Negative analog input 7
IN7P(1)	4	Analog input	Positive analog input 7
IN8N(1)	1	Analog input	Negative analog input 8
IN8P(1)	2	Analog input	Positive analog input 8
NC	27, 29, 62, 64	—	No connection, leave floating; can be connected to AVDD or AVSS with a 10-kΩ or higher resistor
OPAMPN	61	Analog input	Op amp inverting input; leave floating if unused and power-down the op amp
OPAMPOUT	63	Analog output	Op amp output; leave floating if unused and power-down the op amp
OPAMPP	60	Analog input	Op amp noninverting input; leave floating if unused and power-down the op amp
$\overline{\text{PWDN}}$	35	Digital input	Power-down; active low
$\overline{\text{RESET}}$	36	Digital input	System reset; active low
RESV1	31	Digital input	Reserved for future use; must tie to logic low; connect to DGND
SCLK	40	Digital input	SPI clock

(1) Connect any unused or powered down analog input pins to AVDD.

Pin Functions (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
START	38	Digital input	Start conversion
TESTN (1)	18	Analog input/output	Test signal, negative pin; connect to DGND with a 10-kΩ resistor if unused
TESTP (1)	17	Analog input/output	Test signal, positive pin; connect to DGND with a 10-kΩ resistor if unused
VCAP1	28	Analog output	Analog bypass capacitor; connect a 470-pF capacitor to AVSS
VCAP2	30	Analog output	Analog bypass capacitor; connect a 270-nF capacitor to AVSS
VCAP3	55	Analog output	Analog bypass capacitor; connect a 270-nF capacitor to AVSS
VCAP4	26	Analog output	Analog bypass capacitor; connect a 270-nF capacitor to AVSS
VREFN	25	Analog input	Negative reference voltage; connect to AVSS
VREFP	24	Analog output	Positive reference voltage output; connect a 330-nF capacitor to VREFN

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	5.5	V
DVDD to DGND	–0.3	3.9	V
AVSS to DGND	–3.0	0.2	V
Analog input voltage	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	DGND – 0.3	DVDD + 0.3	V
Digital output voltage	DGND – 0.3	DVDD + 0.3	V
Continuous input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing beyond the supply rails must be current limited to 10 mA or less.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to AVSS	2.7	5.0	5.25	V
DVDD	Digital power supply	DVDD to DGND	1.7	1.8	3.6	V
	Analog to digital supply	AVDD to DVDD	–2.1		3.6	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} – V_{(AINN)}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
V_{CM}	Common-mode input voltage	$V_{CM} = (V_{(AINP)} – V_{(AINN)}) / 2$	See the *Input Common-Mode Range* section			V
VOLTAGE REFERENCE INPUTS						
REFN	Negative reference input		AVSS			V
EXTERNAL CLOCK SOURCE						
f_{CLK}	Master clock rate	CLKSEL pin = 0, (AVDD – AVSS) = 3 V	1.7	2.048	2.25	MHz
		CLKSEL pin = 0, (AVDD – AVSS) = 5 V	1.0	2.048	2.25	
DIGITAL INPUTS						
	Input voltage		DGND – 0.1		DVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		105	°C

7.4 Thermal Information

THERMAL METRIC (1)		ADS131E08S	UNIT
		PAG (TQFP)	
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +105°C. Typical specifications are at T_A = 25°C. All specifications are at DVDD = 1.8 V, AVDD = 5 V, AVSS = 0 V, V_{REF} = 4.0 V, external f_{CLK} = 2.048 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_i	Input capacitance			20		pF
I_{IB}	Input bias current	PGA output in normal range		5		nA
	DC input impedance			200		MΩ
PGA PERFORMANCE						
	Gain settings			1, 2, 4, 8, 12		V/V
BW	Bandwidth			See Table 3		
ADC PERFORMANCE						
DR	Data rate	f_{CLK} = 2.048 MHz	1	4	64	kSPS
	Resolution	DR = 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, and 16 kSPS	24			Bits
		DR = 32 kSPS and 64 kSPS	16			
CHANNEL PERFORMANCE (DC Performance)						
INL	Integral nonlinearity	Full-scale, best fit		10		ppm
	Dynamic range	Data rate = 4 kSPS, gain = 1		116		dB
		Gain settings other than 1		See the *Noise Measurements* section		
E_O	Offset error(1)	Gain = 1	–100	–450	–800	µV
	Offset error drift(1)			0.2	2.5	µV/°C
E_G	Gain error	Excluding voltage reference error		0.1%		
	Gain drift	Excluding voltage reference drift		3		ppm/°C
	Gain match between channels			0.2		% of FS
CHANNEL PERFORMANCE (AC Performance)						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz or 60 Hz(2)		–110		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz or 60 Hz		–80		dB
	Crosstalk	f_{IN} = 50 Hz or 60 Hz		–125	–113	dB
SNR	Signal-to-noise ratio	f_{IN} = 50 Hz or 60 Hz, amplitude = –0.5 dBFS, normalized		108		dB
		f_{IN} = 50 Hz or 60 Hz, amplitude = –15 dBFS, normalized		115		
THD	Total harmonic distortion	f_{IN} = 50 Hz or 60 Hz, amplitude = –0.5 dBFS		–102		dBc
		f_{IN} = 50 Hz or 60 Hz, amplitude = –15 dBFS		–107		
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Output voltage(1)	T_A = 25°C, V_{REF} = 2.4 V, VREF_4V = 0		2.4		V
		T_A = 25°C, V_{REF} = 4 V, VREF_4V = 1	3.88	4	4.12	
	Accuracy	T_A = 25°C		±0.2%		
	Temperature drift	T_A = –40°C ≤ T_A ≤ 105°C		8		ppm/°C
	Power-up time	VCAP1 = 470 pF, VREFP = 330 nF, settled to 0.2%		1		ms
INTERNAL OSCILLATOR						
	Internal oscillator clock frequency			2.048		MHz
	Internal oscillator accuracy(1)	T_A = 25°C			±1%	
		–40°C ≤ T_A ≤ +105°C			±3%	
	Power-up time			20		µs
	Internal oscillator power consumption			120		µW

(1) Minimum and maximum values are specified by design and characterization data.
(2) CMRR is measured with a common-mode signal of (AVSS + 0.3 V) to (AVDD – 0.3 V). The values indicated are the minimum of the eight channels.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +105°C. Typical specifications are at T_A = 25°C. All specifications are at DVDD = 1.8 V, AVDD = 5 V, AVSS = 0 V, V_{REF} = 4.0 V, external f_{CLK} = 2.048 MHz, data rate = 4 kSPS, and gain = 1 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATIONAL AMPLIFIER						
	Integrated noise	0.1 Hz to 250 Hz		9		μV_{RMS}
	Noise density	2 kHz		120		nV/√Hz
GBP	Gain bandwidth product	50-kΩ || 10-pF load		100		kHz
SR	Slew rate	50-kΩ || 10-pF load		0.25		V/µs
	Load current			50		µA
THD	Total harmonic distortion	f_{IN} = 100 Hz		70		dB
V_{CM}	Common-mode input range		AVSS + 0.7		AVDD – 0.3	V
	Quiescent current consumption			20		µA
FAULT DETECT AND ALARM						
	Comparator threshold accuracy			±30		mV
SYSTEM MONITORS						
	Analog supply reading error			2%		
	Digital supply reading error			2%		
	Device wake-up	From standby mode		31.25		µs
TEMPERATURE SENSOR						
	Offset voltage	T_A = 25°C(3)		144		mV
	Temperature coefficient(3)			400		µV/°C
SELF-TEST SIGNAL						
	Signal frequency			$f_{CLK} / 2^{21}$		Hz
				$f_{CLK} / 2^{20}$		
	Signal voltage			±1		mV
				±2		
	Accuracy			±2%		
DIGITAL INPUTS AND OUTPUTS						
V_{IH}	High-level input voltage(1)	DVDD = 1.7 V to 1.8 V	DVDD – 0.2 V			V
		DVDD = 1.8 V to 3.6 V	0.8 DVDD		DVDD + 0.1	V
V_{IL}	Low-level input voltage(1)	DVDD = 1.7 V to 1.8 V			DGND + 0.2	V
		DVDD = 1.8 V to 3.6 V	DGND – 0.1		0.2 DVDD	V
V_{OH}	High-level output voltage(1)	I_{OH} = –500 µA	0.9 DVDD			V
V_{OL}	Low-level output voltage(1)	I_{OL} = 500 µA			0.1 DVDD	V
I_{IN}	Input current	0 V < $V_{DigitalInput}$ < DVDD	–10		10	µA
SUPPLY CURRENT (Operational Amplifier Turned Off)						
I_{AVDD}	Analog supply current	AVDD – AVSS = 3 V		5.1		mA
		AVDD – AVSS = 5 V		5.8		
I_{DVDD}	Digital supply current	DVDD = 3.3 V		1		mA
		DVDD = 1.8 V		0.4		
POWER DISSIPATION (8 Channels Powered Up)						
	Power dissipation	Normal mode, AVDD – AVSS = 3 V		16		mW
		Standby mode, AVDD – AVSS = 3 V		2		
		Power-down mode, AVDD – AVSS = 3 V		10		µW
		Normal mode, AVDD – AVSS = 5 V(1)		29.7	32.9	mW
		Standby mode, AVDD – AVSS = 5 V		4.2		
		Power-down mode, AVDD – AVSS = 5 V		20		µW

(3) See the *Temperature Sensor (TempP, TempN)* section for more information.

7.6 Timing Requirements

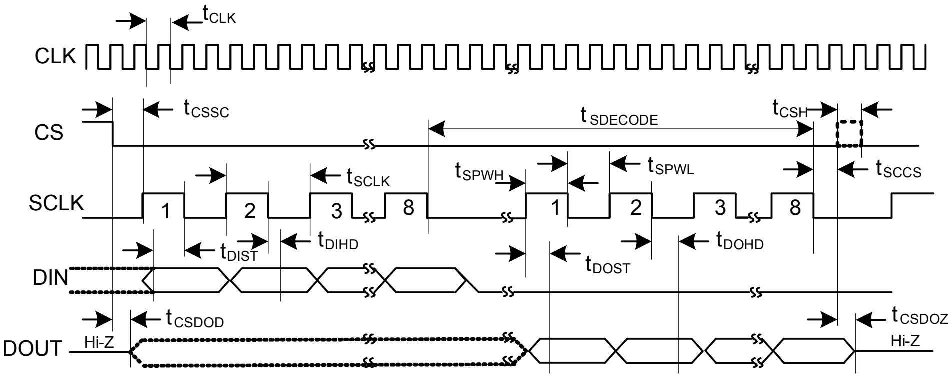
over operating ambient temperature range and DVDD = 1.7 V to 3.6 V (unless otherwise noted)

		2.7 V ≤ DVDD ≤ 3.6 V		1.7 V ≤ DVDD ≤ 2.0 V		UNIT
		MIN	MAX	MIN	MAX	
t_{CLK}	Master clock period	444	588	444	588	ns
t_{CSSC}	Delay time, first SCLK rising edge after $\overline{\text{CS}}$ falling edge	6		17		ns
t_{SCLK}	SCLK period	50		66.6		ns
$t_{SPWH, L}$	Pulse duration, SCLK high or low	15		25		ns
t_{DIST}	Setup time, DIN valid before SCLK falling edge	10		10		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	10		11		ns
t_{CSH}	Pulse duration, $\overline{\text{CS}}$ high	2		2		t_{CLK}
t_{SCCS}	Delay time, $\overline{\text{CS}}$ rising edge after final SCLK falling edge	4		4		t_{CLK}
$t_{SDECODE}$	Command decode time	4		4		t_{CLK}
$t_{DISCK2ST}$	Setup time, DAISY_IN valid before SCLK falling edge	10		10		ns
$t_{DISCK2HT}$	Hold time, DAISY_IN valid after SCLK falling edge	10		10		ns

7.7 Switching Characteristics

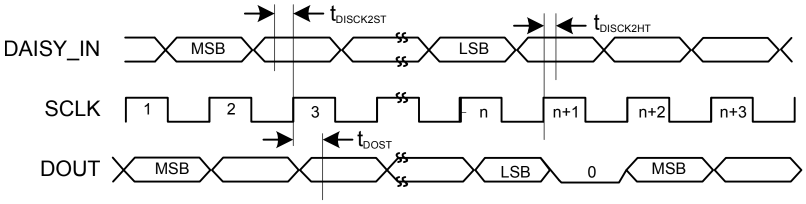
over operating ambient temperature range, DVDD = 1.7 V to 3.6 V, and load on DOUT = 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		2.7 V ≤ DVDD ≤ 3.6 V		1.7 V ≤ DVDD ≤ 2.0 V		UNIT
		MIN	MAX	MIN	MAX	
t_{CSDOD}	Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT driven	10		20		ns
t_{DOST}	Propagation delay time, SCLK rising edge to valid new DOUT		17		32	ns
t_{DOHD}	Hold time, SCLK falling edge to invalid DOUT	10		10		ns
t_{CSDOZ}	Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT high impedance		10		20	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

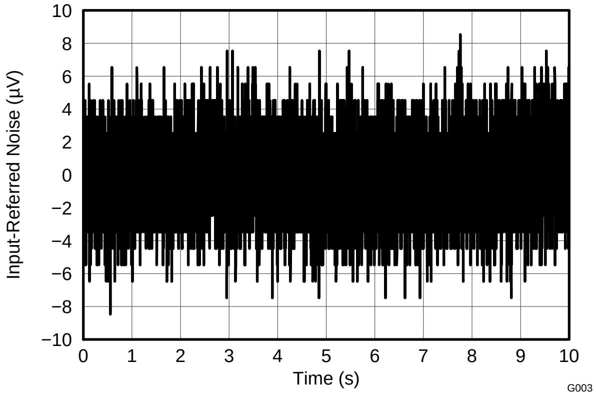


(1) n = Number of channels × resolution + 24 bits. Number of channels is 8; resolution is 24-bit.

Figure 2. Daisy-Chain Interface Timing

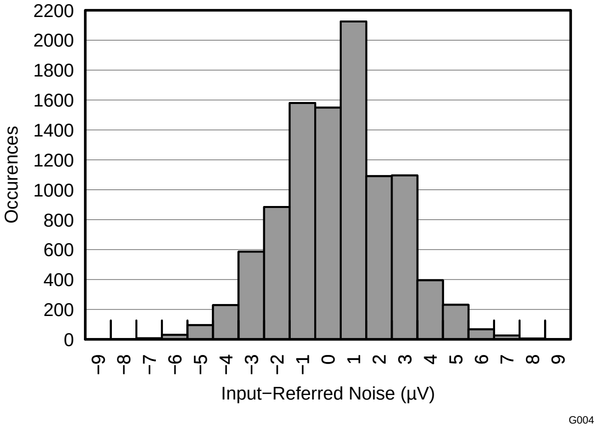
7.8 Typical Characteristics

at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted)



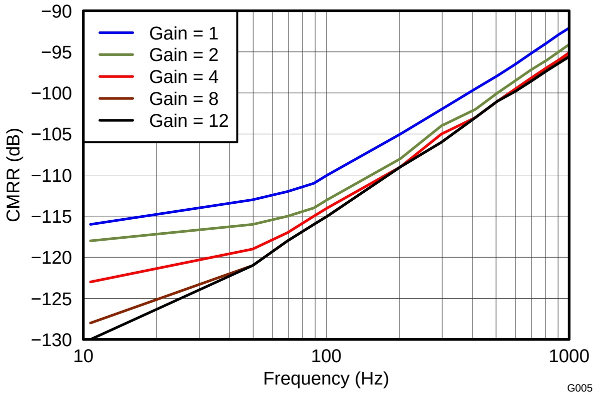
Data rate = 1 kSPS, gain = 1

Figure 3. Input-Referred Noise



Data rate = 1 kSPS, gain = 1

Figure 4. Noise Histogram



Data rate = 4 kSPS, V_{IN} = AVDD – 0.3 V to AVSS + 0.3 V

Figure 5. Common-Mode Rejection Ratio vs Frequency

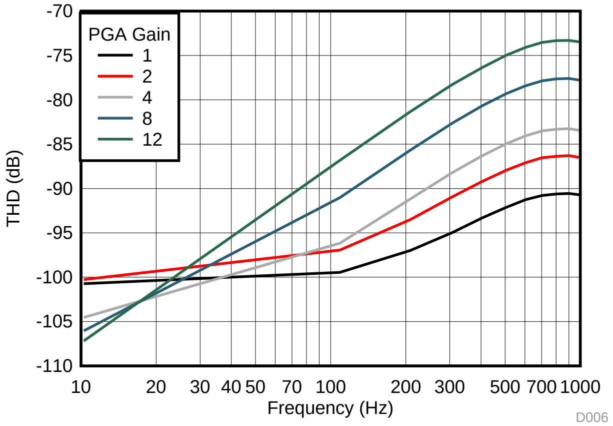


Figure 6. Total Harmonic Distortion vs Frequency

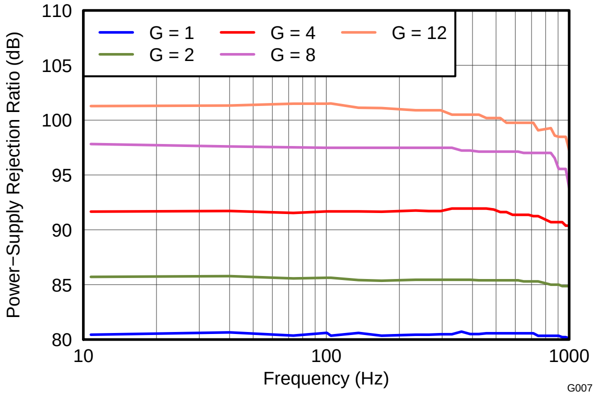


Figure 7. PSRR vs Frequency

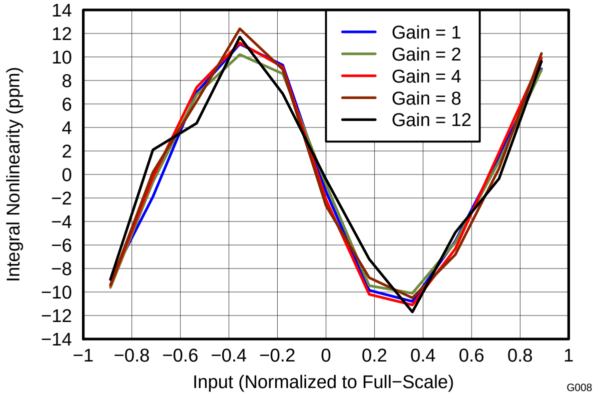


Figure 8. INL vs PGA Gain

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted)

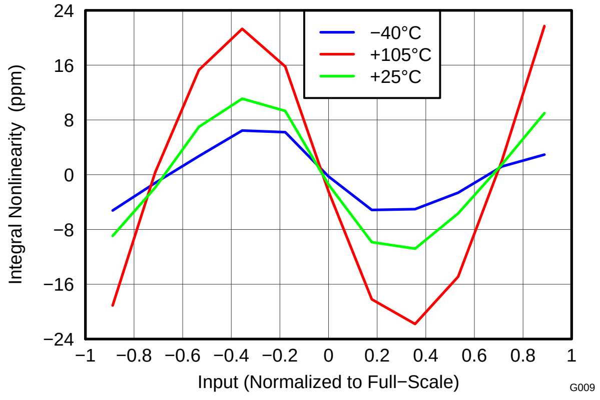
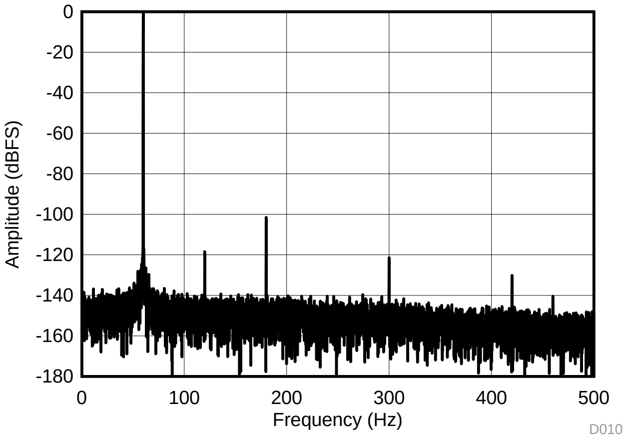
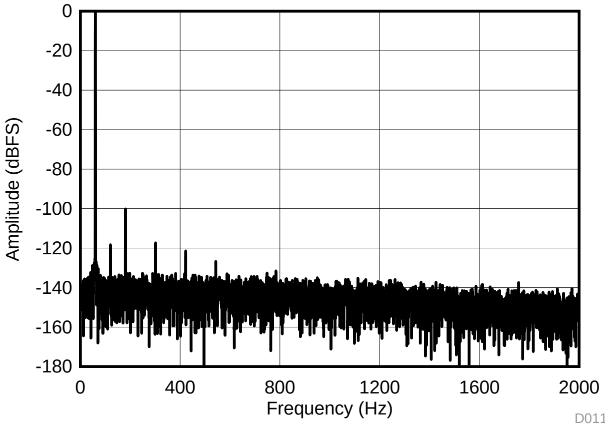


Figure 9. INL vs Temperature



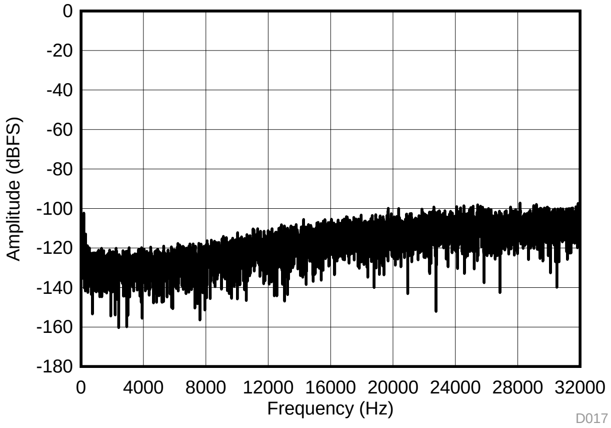
Gain = 1, THD = –101.5 dB, SNR = 111 dB,
data rate = 1 kSPS, 16384 points

Figure 10. THD FFT Plot



Gain = 1, THD = –100 dB, SNR = 107 dB,
data rate = 4 kSPS, 16384 points

Figure 11. THD FFT Plot



Gain = 1, THD = –100 dB, SNR = 76 dB,
data rate = 64 kSPS, 16384 points

Figure 12. FFT Plot

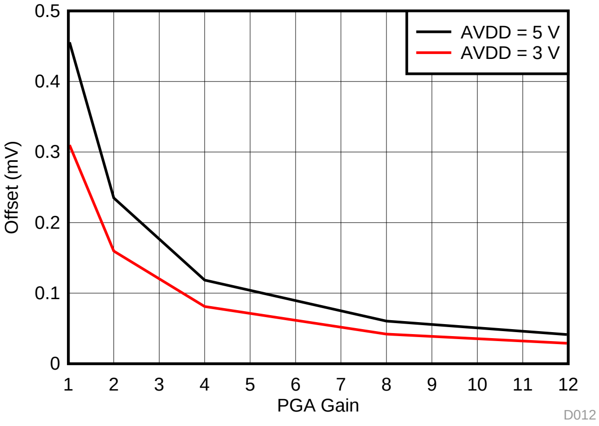


Figure 13. Offset vs PGA Gain (Absolute Value)

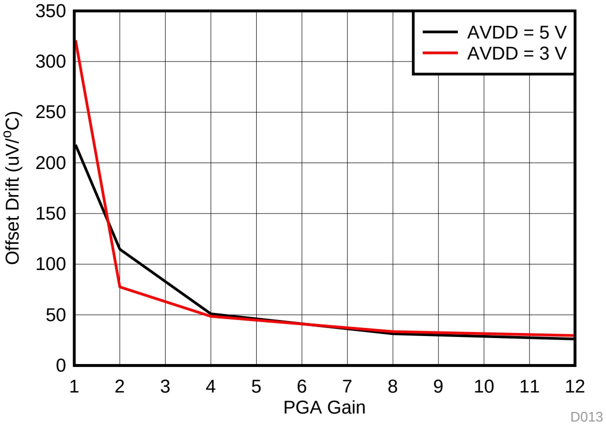


Figure 14. Offset Drift vs PGA Gain

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external f_{CLK} = 2.048 MHz, data rate = 8 kSPS, and gain = 1 (unless otherwise noted)

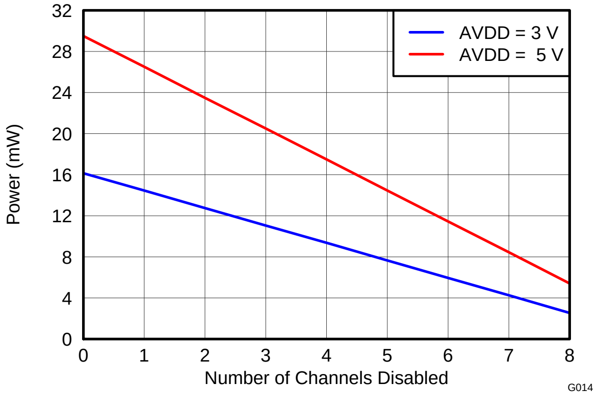
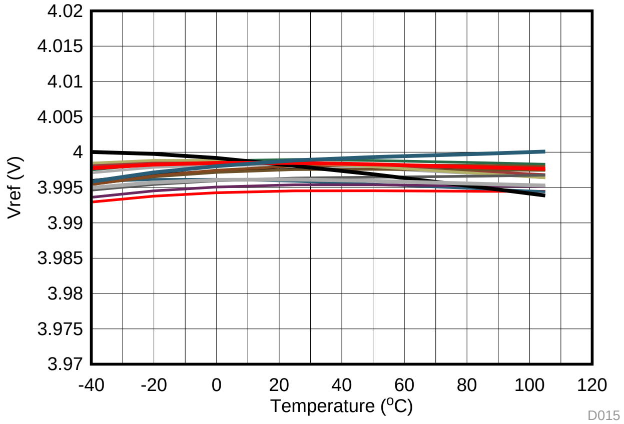


Figure 15. Channel Power



AVDD = 5 V, AVSS = 0 V, V_{REF} = 4 V

Figure 16. Internal V_{REF} vs Temperature

8 Parameter Measurement Information

8.1 Noise Measurements

Adjust the data rate and PGA gain to optimize the ADS131E08S noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Increasing the PGA gain reduces the input-referred noise, which is particularly useful when measuring low-level signals. Table 1 summarizes the ADS131E08S noise performance with a 3-V analog power supply. Table 2 summarizes the ADS131E08S noise performance with a 5-V analog power supply. Data are representative of typical noise performance at $T_A = 25°C$. Data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. A minimum of 1000 consecutive readings are used to calculate the RMS noise for each reading. For the two highest data rates, noise is limited by the ADC quantization noise and does not have a Gaussian distribution. Table 1 and Table 2 show measurements taken with an internal reference. Data are representative of the ADS131E08S noise performance shown in both effective number of bits (ENOB) and dynamic range when using a low-noise external reference (such as the REF5025). ENOB data in Table 1 and Table 2 are calculated using Equation 1 and dynamic range data in Table 1 and Table 2 are calculated using Equation 2.

$$\text{ENOB} = \text{Log}_2 \times \left| \frac{0.7071 \times V_{REF}}{V_{RMS\_Noise} \times \text{Gain}} \right| \tag{1}$$

$$\text{Dynamic Range} = 20 \times \text{Log}_{10} \times \left| \frac{0.7071 \times V_{REF}}{V_{RMS\_Noise} \times \text{Gain}} \right| \tag{2}$$

Table 1. Input-Referred Noise, 3-V Analog Supply, and 2.4-V Reference

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.1	12.31	74.1	12.30	74.0	12.29	74.0	12.29	73.9	12.27
001	32	8384	89.6	14.89	89.6	14.88	89.4	14.85	88.6	14.71	87.6	14.55
010	16	4192	102.8	17.07	102.3	16.99	100.6	16.72	97.1	16.12	94.2	15.65
011	8	2096	108.2	18.0	107.4	17.9	105.2	17.5	101.6	16.9	98.9	16.5
100	4	1048	111.4	18.6	109.4	18.4	107.4	18.1	103.5	17.4	100.5	17.0
101	2	524	114.6	19.1	113.7	19.0	111.4	18.6	107.7	18.0	104.9	17.5
110	1	262	117.7	19.6	116.8	19.5	114.5	19.1	110.7	18.5	108.0	18.0

Table 2. Input-Referred Noise, 5-V Analog Supply, and 4-V Reference

DR BITS (CONFIG1 Register)	OUTPUT DATA RATE (kSPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN									
			x1		x2		x4		x8		x12	
			DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB	DYNAMIC RANGE (dB)	ENOB
000	64	16768	74.7	12.41	74.7	12.41	74.7	12.41	74.7	12.41	74.6	12.39
001	32	8384	90.3	15.01	90.3	15.00	90.2	14.99	89.9	14.93	89.4	14.85
010	16	4192	104.3	17.33	104.0	17.28	103.1	17.12	100.5	16.70	98.1	16.30
011	8	2096	112.3	18.7	111.6	18.6	109.7	18.3	106.3	17.7	103.8	17.3
100	4	1048	116.0	19.3	115.2	19.2	113.1	18.8	109.5	18.3	106.9	17.8
101	2	524	119.1	19.8	118.2	19.7	116.2	19.4	112.6	18.8	109.9	18.3
110	1	262	122.1	20.4	121.3	20.2	119.1	19.9	115.6	19.3	112.9	18.8

9 Detailed Description

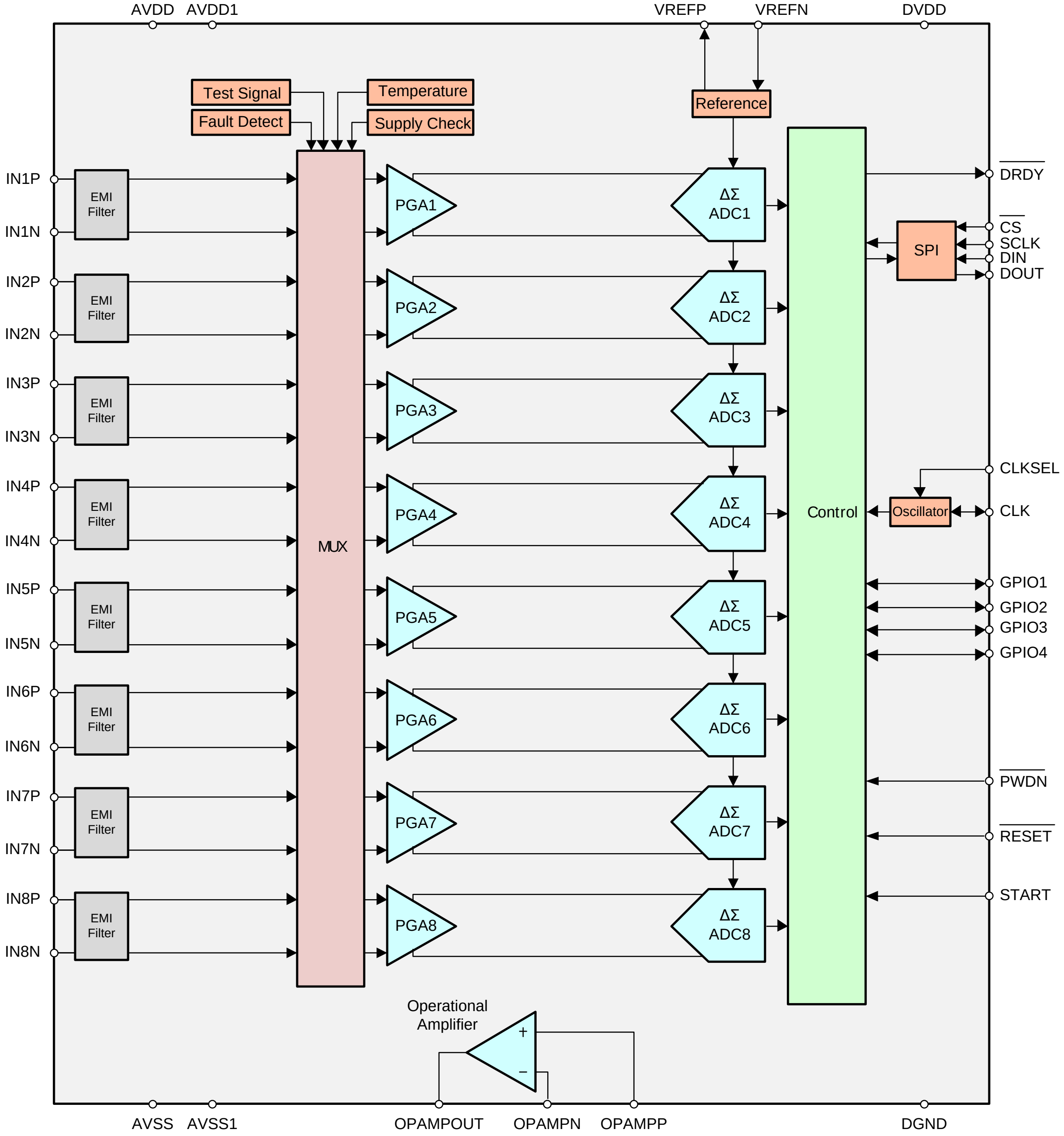
9.1 Overview

The ADS131E08S is a low-power, 8-channel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with an integrated programmable gain amplifier (PGA) and short start-up time. The analog device performance across a scalable data rate makes the device well-suited for smart-grid and other industrial power monitor, control, and protection applications.

The ADS131E08S has a programmable multiplexer that allows for various internal monitoring signal measurements including temperature, supply, and input short for device noise testing. The PGA gain can be chosen from one of five settings: 1, 2, 4, 8, or 12. The ADCs in the device offer data rates of 1 kSPS, 2 kSPS, 4 kSPS, 8 kSPS, 16 kSPS, 32 kSPS, and 64 kSPS. The device communicates using a serial peripheral interface (SPI)-compatible interface. The device provides four general-purpose I/O (GPIO) pins for general use. Use multiple devices to easily add channels to the system and synchronize them with the START pins.

Program the internal reference to either 2.4 V or 4 V. The internal oscillator generates a 2.048-MHz clock. Use the integrated comparators, with programmable trigger-points, for input overrange or underrange detection. A detailed diagram of the ADS131E08S is provided in the *Functional Block Diagram* section.

9.2 Functional Block Diagram



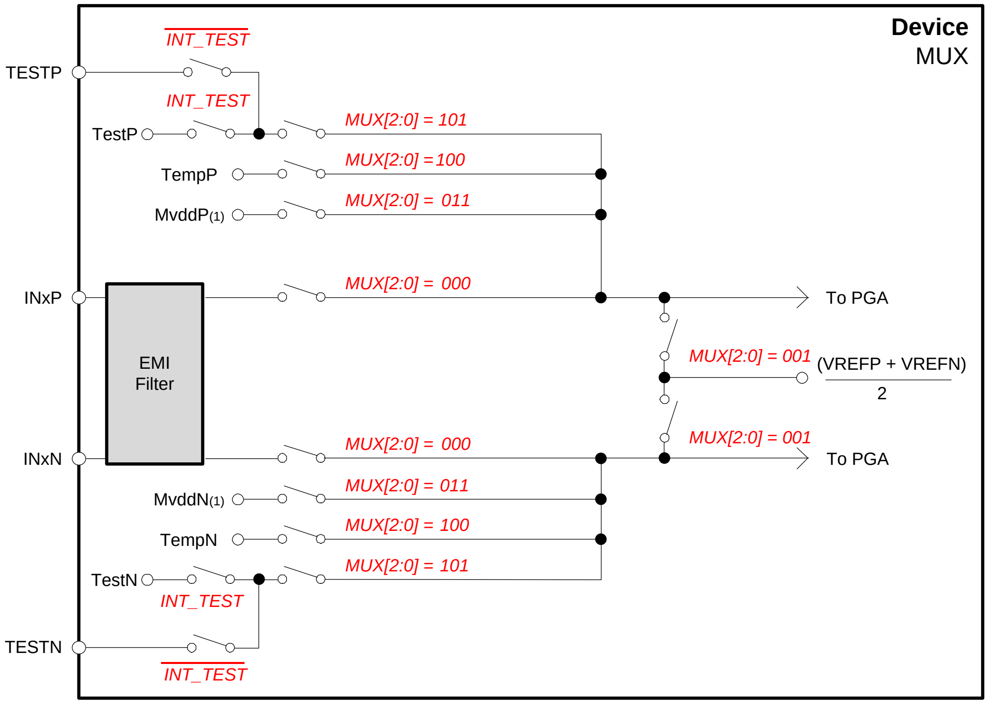
9.3 Feature Description

9.3.1 Electromagnetic Interference (EMI) Filter

An RC filter at the input functions as an EMI filter on all channels. The –3-dB filter bandwidth is approximately 3 MHz.

9.3.2 Input Multiplexer

The ADS131E08S input multiplexers are very flexible and provide many configurable signal-switching options. Figure 17 shows a diagram of the multiplexer on a single channel of the device. INxP and INxN are separate for each of the eight blocks. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CHnSET registers (see the *CHnSET* registers in the *Register Map* section for details). The output of each multiplexer is connected to the individual channel PGA.



(1) MVDD monitor voltage supply depends on channel number; see the *Power-Supply Measurements (MVDDP, MVDDN)* section.

Figure 17. Input Multiplexer Block for One Channel

Feature Description (continued)

9.3.2.1 Device Noise Measurements

Setting CHnSET[2:0] = 001 sets the common-mode voltage of [($V_{(VREFP)}$ + $V_{(VREFN)}$) / 2] to both channel inputs. Use this setting to test inherent device noise in the user system.

9.3.2.2 Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. The test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls the switching frequency of the test signal. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. The INT_TEST register bit (in the *CONFIG2: Configuration Register 2* section) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the test or calibration of multiple devices with the same signal.

9.3.2.3 Temperature Sensor (TempP, TempN)

Setting CHnSET[2:0] = 100 sets the channel input to the temperature sensor. This sensor uses two internal diodes with one diode having a current density 16 times that of the other, as shown in Figure 18. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

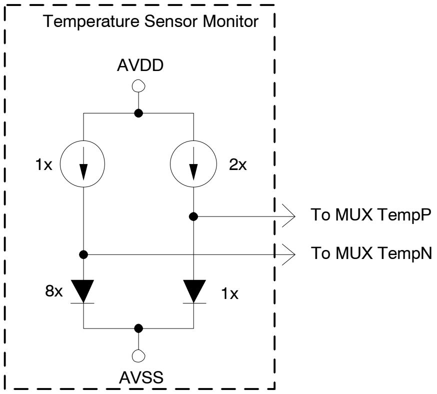


Figure 18. Temperature Sensor Implementation

The internal device temperature tracks the PCB temperature closely because of the low thermal resistance of the package to the PCB. Self-heating of the ADS131E08S causes a higher reading than the temperature of the surrounding PCB. Setting the channel gain to 1 is recommended when the temperature measurement is taken.

The scale factor of Equation 3 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to µV.

$$\text{Temperature}\ (^\circ\text{C}) = \left(\frac{V_{\text{Temperature}}\ (\mu\text{V}) - 144{,}000\ \mu\text{V}}{400\ \mu\text{V} / ^\circ\text{C}} \right) \quad (3)$$

9.3.2.4 Power-Supply Measurements (MVDDP, MVDDN)

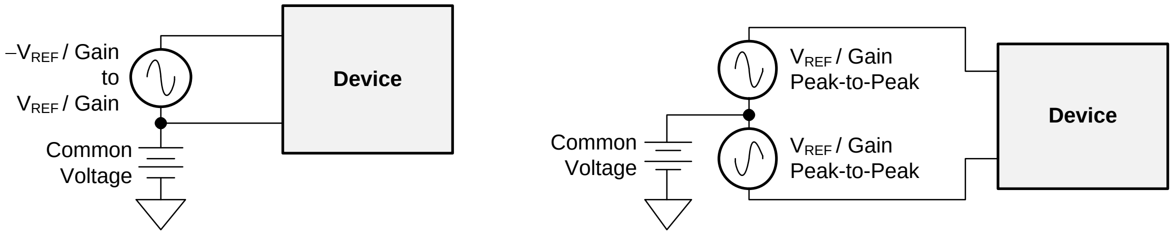
Setting CHnSET[2:0] = 011 sets the channel inputs to different device supply voltages. For channels 1, 2, 5, 6, 7, and 8 (MVDDP – MVDDN) is [0.5 × (AVDD – AVSS)]; for channels 3 and 4 (MVDDP – MVDDN) is DVDD / 4. Set the gain to 1 to avoid saturating the PGA when measuring power supplies.

Feature Description (continued)

9.3.3 Analog Input

The analog inputs to the device connect directly to an integrated low-noise, low-drift, high input impedance, programmable gain amplifier. The amplifier is located following the individual channel multiplexer.

The ADS131E08S analog inputs are fully differential. The differential input voltage (V_{INxP} – V_{INxN}) can span from –V_{REF} / gain to V_{REF} / gain. See the *Data Format* section for an explanation of the correlation between the analog input and digital codes. There are two general methods of driving the ADS131E08S analog inputs: pseudo-differential or fully-differential, as shown in Figure 19, Figure 20, and Figure 21.



a) Psuedo-Differential Input

b) Differential Input

Figure 19. Methods of Driving the ADS131E08S: Pseudo-Differential or Fully Differential

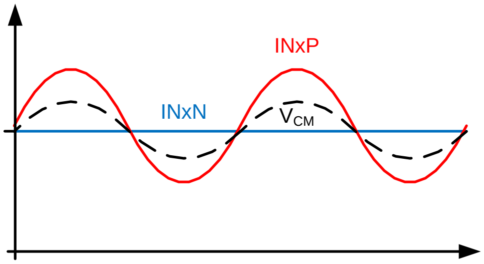


Figure 20. Pseudo-Differential Input Mode

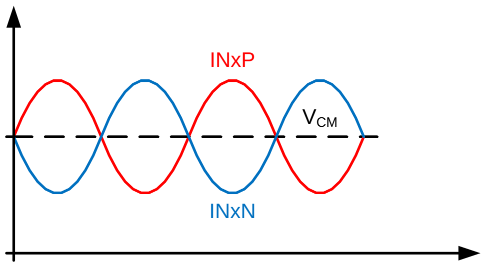


Figure 21. Fully-Differential Input Mode

Hold the INxN pin at a common voltage, preferably at mid supply, to configure the fully differential input for a pseudo-differential signal. Swing the INxP pin around the common voltage –V_{REF} / gain to V_{REF} / gain and remain within the absolute maximum specifications. Verify that the differential signal at the minimum and maximum points meets the common-mode input specification discussed in the *Input Common-Mode Range* section.

Configure the signals at INxP and INxN to be 180° out-of-phase centered around a common voltage to use a fully-differential input method. Both the INxP and INxN inputs swing from the common voltage + ½ V_{REF} / gain to the common voltage – ½ V_{REF} / gain. The differential voltage at the maximum and minimum points is equal to –V_{REF} / gain to V_{REF} / gain. Use the ADS131E08S in a differential configuration to maximize the dynamic range of the data converter. For optimal performance, the common voltage is recommended to be set at the midpoint of the analog supplies [(AVDD + AVSS) / 2].

If any of the analog input channels are not used, then power-down these pins using register bits to conserve power. See the *SPI Command Definitions* section for more information on how to power-down individual channels. Tie any unused or powered down analog input pins directly to AVDD.

9.3.4 PGA Settings and Input Range

Each channel has its own configurable programmable gain amplifier (PGA) following its multiplexer. The PGA is designed using two operational amplifiers in a differential configuration, as shown in Figure 22. Set the gain to one of five settings (1, 2, 4, 8, and 12) using the CHnSET registers for each individual channel (see the *CHnSET* registers in the *Register Map* section for details). The ADS131E08S has CMOS inputs and therefore has negligible current noise. Table 3 shows the typical small-signal bandwidth values for various gain settings.

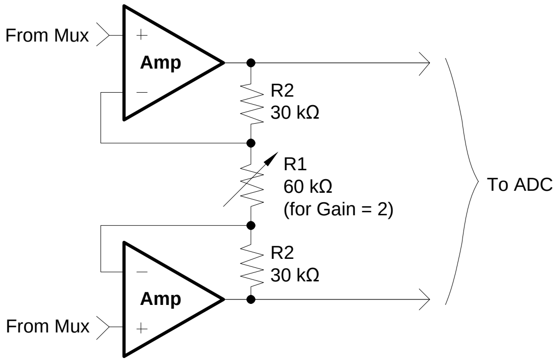


Figure 22. PGA Implementation

Table 3. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT T_A = 25°C (kHz)
1	237
2	146
4	96
8	48
12	32

The PGA resistor string that implements the gain has 120 kΩ of resistance for a gain of 2. This resistance provides a current path across the PGA outputs in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input.

9.3.4.1 Input Common-Mode Range

The usable input common-mode range of the analog front-end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. The common-mode range, V_{CM}, is defined in Equation 4:

$$\text{AVDD} - 0.3\ \text{V} - \left(\frac{\text{Gain} \times V_{MAX\_DIFF}}{2} \right) > V_{CM} > \text{AVSS} + 0.3\ \text{V} + \left(\frac{\text{Gain} \times V_{MAX\_DIFF}}{2} \right)$$

where:

- V_{MAX_DIFF} = maximum differential signal at the PGA input and
- V_{CM} = common-mode voltage (4)

For example:

If AVDD – AVSS = 3.3 V, gain = 2, and V_{MAX_DIFF} = 1000 mV,
Then 1.3 V < V_{CM} < 2.0 V

9.3.5 ΔΣ Modulator

Each ADS131E08S channel has its own delta-sigma (ΔΣ) ADC. The ΔΣ converters use second-order modulators optimized for low-power applications. The modulator samples the input signal at the modulator rate of (f_{MOD} = f_{CLK} / 2). As with any ΔΣ modulator, the ADS131E08S noise is shaped until f_{MOD} / 2, as shown in Figure 23.

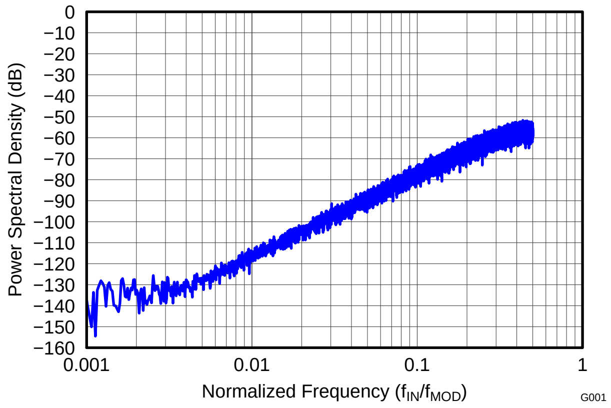


Figure 23. Modulator Noise Spectrum Up to 0.5 × f_{MOD}

9.3.6 Clock

The ADS131E08S provides two different device clocking methods: internal and external. Internal clocking using the internal oscillator is ideally-suited for non-synchronized, low-power systems. The internal oscillator is trimmed for accuracy at room temperature. The accuracy of the internal oscillator varies over the specified temperature range; see the *Electrical Characteristics* table for details. External clocking is recommended when synchronizing multiple ADS131E08S devices or when synchronizing to an external event because the internal oscillator clock performance can vary over temperature. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit. Provide the external clock any time after the analog and digital supplies are present.

The CLKSEL pin selects either the internal oscillator or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output on the CLK pin. A truth table for the CLKSEL pin and the CLK_EN bit is shown in Table 4. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. During power-down, the external clock is recommended to be shut down to save power.

Table 4. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal oscillator	3-state
1	1	Internal oscillator	Output: internal oscillator

9.3.7 Digital Decimation Filter

The digital filter receives the modulator output bit stream and decimates the data stream. The decimation ratio determines the number of samples taken to create the output data word, and is set by the modulator rate divided by the data rate (f_{MOD} / f_{DR}). By adjusting the decimation ratio, a tradeoff can be made between resolution and data rate: higher decimation allows for higher resolution (thus creating lower data rates) and lower decimation decreases resolution but enables wider bandwidths with higher data rates. Higher data rates are typically used in power applications that implement software re-sampling techniques to help with channel-to-channel phase adjustment for voltage and current.

The digital filter on each channel consists of a third-order sinc filter. An input step change takes three conversion cycles for the filter to settle. Adjust the decimation ratio of the sinc^3 filters using the DR[2:0] bits in the CONFIG1 register (see the *Register Map* section for details). The data rate setting is a global setting that sets all channels to the same data rate.

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc^3 filter attenuates the high-frequency modulator noise, then decimates the data stream into parallel data. The decimation rate affects the overall converter data rate.

Equation 5 shows the scaled sinc^3 filter Z-domain transfer function.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^{3} \quad (5)$$

The sinc^3 filter frequency domain transfer function is shown in Equation 6.

$$\left|H(f)\right| = \left|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^{3}$$

where:

- N = decimation ratio (6)

The sinc^3 filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 24 illustrates the sinc filter frequency response and Figure 25 illustrates the sinc filter roll-off. Figure 26 and Figure 27 illustrate the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 28 illustrates the transfer function extended until 4 f_{MOD}. Figure 28 illustrates that the ADS131E08S passband repeats itself at every f_{MOD}. Note that the digital filter response and filter notches are proportional to the master clock frequency.

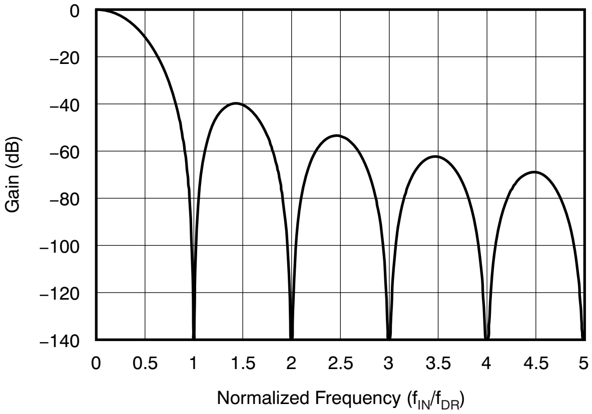


Figure 24. Sinc Filter Frequency Response

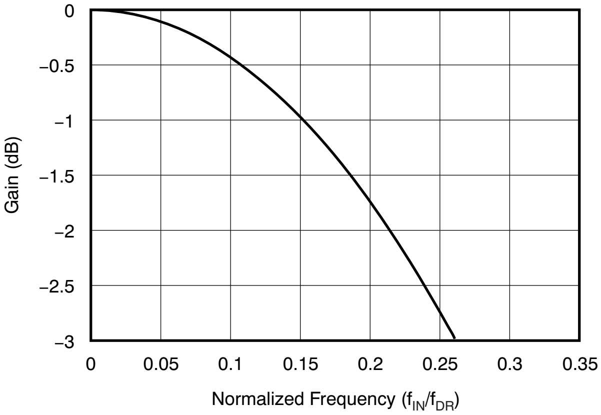


Figure 25. Sinc Filter Roll-Off

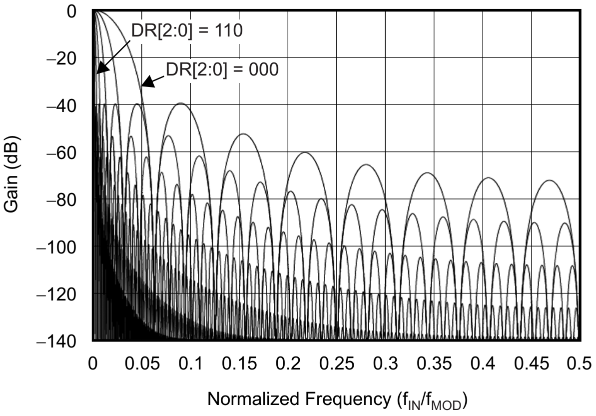


Figure 26. Transfer Function of Decimation Filters Until f_{MOD} / 2

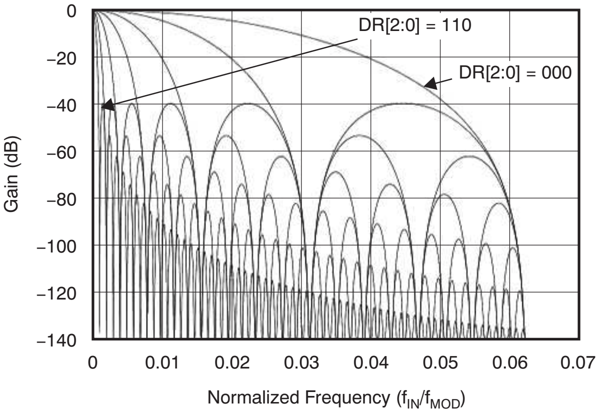


Figure 27. Transfer Function of Decimation Filters Until f_{MOD} / 16

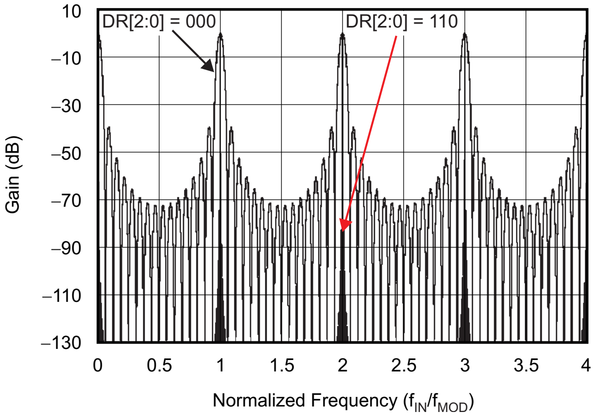
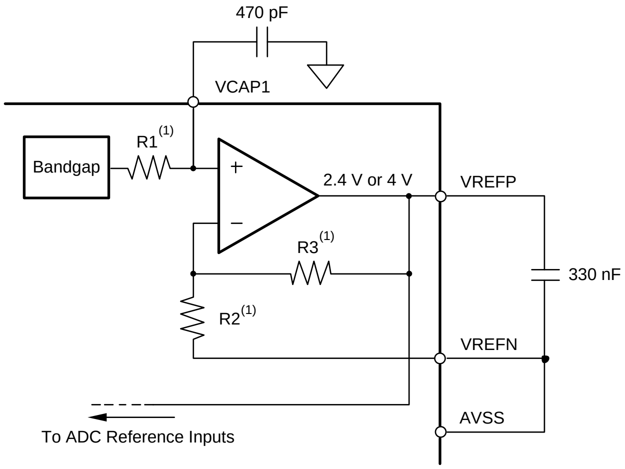


Figure 28. Transfer Function of Decimation Filters Until 4 f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

9.3.8 Voltage Reference

The ADS131E08S uses an internal voltage reference and does not provide the option of connecting an external reference voltage. Figure 29 shows a simplified block diagram of the internal reference. There are two internal reference voltage options generated with respect to AVSS: 2.4 V and 4 V. Connect VREFN to AVSS.



(1) For V_{REF} = 2.4 V: R1 = 12.5 kΩ, R2 = 25 kΩ, and R3 = 25 kΩ.
For V_{REF} = 4 V: R1 = 10.5 kΩ, R2 = 15 kΩ, and R3 = 35 kΩ.

Figure 29. Internal Reference Implementation

The external band-limiting capacitors, connected to VCAP1 and between the VREFP and VREFN nodes, determine the amount of reference noise contribution. Although limiting the bandwidth through larger capacitor sizes helps keep noise at a minimum, using large capacitors increases the power-up time of the ADC. Using the capacitor values shown in Figure 29 is recommended to optimize the power-up time of the device.

The internal band gap (VCAP1 pin) used to create the internal reference voltage requires a capacitor to filter noise. As a result of limited drive strength, the size of the capacitor on VCAP1 sets the power-up time of the device. Figure 30 shows the accuracy of the first 200 conversion samples with different capacitors on VCAP1 following power-up. Larger capacitors on VCAP1 help filter broadband noise but add to the power-up time. To generate the plot of Figure 30, the ADC input voltage is fixed at 1 V during power-up and the ADC output conversion result is tracked to show the VCAP1 power-up time.

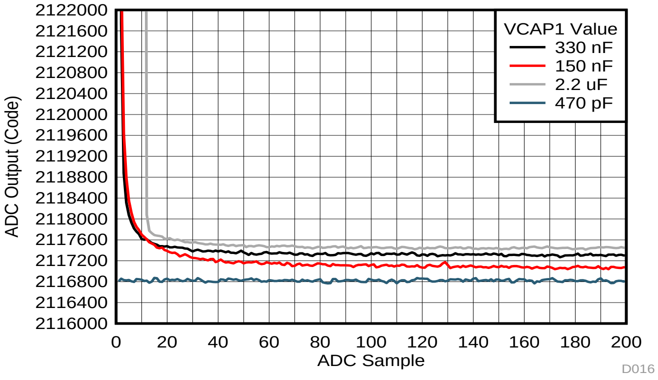


Figure 30. VCAP1 Power-Up Time versus External Capacitor Value

Use the VREF_4V bit in the CONFIG2 register to set the internal reference to either 4 V or 2.4 V. By default, the reference powers up as 4 V for a 5-V system (or ±2.5-V supplies). In a 3-V system (or ±1.5-V supplies), configure the internal reference to 2.4 V immediately following power-up. No damage occurs to the device when the ADS131E08S is set to a 4-V reference when using a 3-V supply system. The internal reference saturates until programmed to 2.4 V.

9.3.9 Input Out-of-Range Detection

The ADS131E08S has integrated comparators to detect out-of-range conditions on the input signals. The basic principle is to compare the input voltage against a threshold voltage set by a 3-bit digital-to-analog converter (DAC) based off the analog power supply. The comparator trigger threshold level is set by the COMP_TH[2:0] bits in the FAULT register.

If the ADS131E08S is powered from a ±2.5-V supply and COMP_TH[2:0] = 000 (95% and 5%), the high-side trigger threshold is set at 2.25 V [equal to AVSS + (AVDD – AVSS) × 95%] and the low-side threshold is set at –2.25 V [equal to AVSS + (AVDD – AVSS) × 5%]. The threshold calculation formula applies to unipolar as well as to bipolar supplies.

A fault condition can be detected by setting the appropriate threshold level using the COMP_TH[2:0] bits. To determine which of the inputs is out of range, read the FAULT_STATP and FAULT_STATN registers individually or read the FAULT_STATx bits as part of the output data stream; see the *Data Output (DOUT)* section.

9.3.10 General-Purpose Digital I/O (GPIO)

The ADS131E08S has a total of four general-purpose digital I/O (GPIO) pins available. Configure the digital I/O pins as either inputs or outputs through the GPIOC bits. The GPIOD bits in the GPIO register indicate the level of the pins. The GPIO logic high voltage level is set by the voltage level of DVDD. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output level.

If configured as inputs, the GPIO pins must be driven to a defined state. The GPIO pins are set as inputs after power-up or after a reset. Figure 31 shows the GPIO pin structure. Connect unused GPIO pins directly to DGND through 10-kΩ resistors.

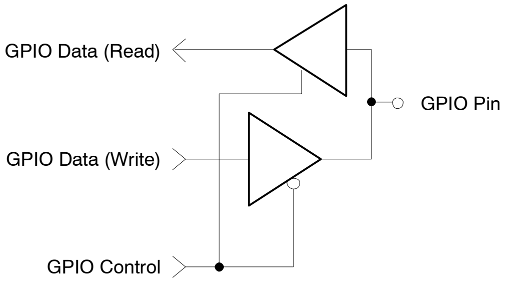


Figure 31. GPIO Pin Implementation

9.4 Device Functional Modes

9.4.1 Power-Down

Power-down all on-chip circuitry by pulling the $\overline{\text{PWDN}}$ pin low. To exit power-down mode, take the $\overline{\text{PWDN}}$ pin high. The internal oscillator and reference require time to come out of power-down mode. During power-down, the external clock is recommended to be shut down to save power.

9.4.2 Reset

There are two methods to reset the ADS131E08S: pull the $\overline{\text{RESET}}$ pin low, or send the RESET command. When using the $\overline{\text{RESET}}$ pin, driving the pin low forces the device into reset. Follow the minimum pulse duration timing specifications before taking the $\overline{\text{RESET}}$ pin back high. The RESET command takes effect on the eighth SCLK falling edge. After the device is reset, 18 t_{CLK} cycles are required to complete initialization of the configuration registers to the default states and start the conversion cycle.

9.4.3 Conversion Mode

Set the START pin high (for a minimum of 2 t_{CLK}) or send the START command to begin conversions. When the START pin is held low, or if the START command is not sent, conversions are halted and the new data-ready indicator (the $\overline{\text{DRDY}}$ signal) does not issue.

When using the START command to control conversions, hold the START pin low.

In multiple device configurations, the START pin is used to synchronize devices (see the *Multiple Device Configuration* section for more details).

9.4.3.1 START Pin Low-to-High Transition or START Command Sent

When the START pin is pulled high or when the START command is sent, the device ADCs begin converting the input signals and the data ready indicator, $\overline{\text{DRDY}}$, is pulled high. The next $\overline{\text{DRDY}}$ falling edge indicates that data are ready. The settling time (t_{SETTLE}) is the time required for the converter to output fully-settled data when the START signal is pulled high or the START command is issued. Figure 32 shows the timing diagram and Table 5 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Table 5 lists the settling time as a function of t_{CLK}.

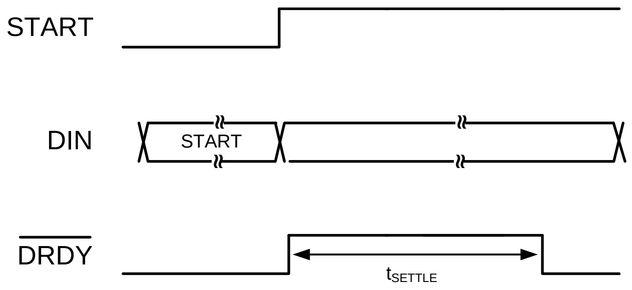


Figure 32. Settling Time for the Initial Conversion

Table 5. Settling Time for Different Data Rates

DR[2:0]	SETTLING TIME	UNIT
000	152	t_{CLK}
001	296	t_{CLK}
010	584	t_{CLK}
011	1160	t_{CLK}
100	2312	t_{CLK}
101	4616	t_{CLK}
110	9224	t_{CLK}

9.4.3.2 Input Signal Step

When the device is converting and there is a step change on the input signal, a delay of 3 t_{DR} is required for the output data to settle. Settled data are available on the fourth $\overline{\text{DRDY}}$ pulse. Data are available to read at each $\overline{\text{DRDY}}$ low transition prior to the 4th $\overline{\text{DRDY}}$ pulse, but are recommended to be ignored. Figure 33 shows the required wait time for complete settling for an input step or input transient event on the analog input.

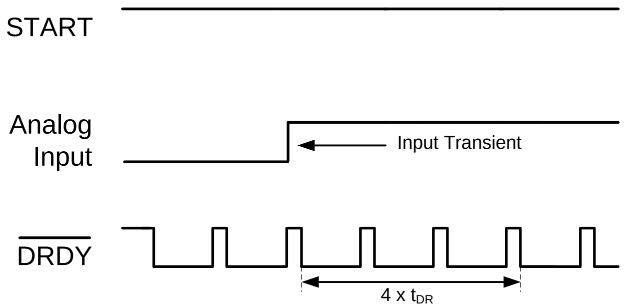
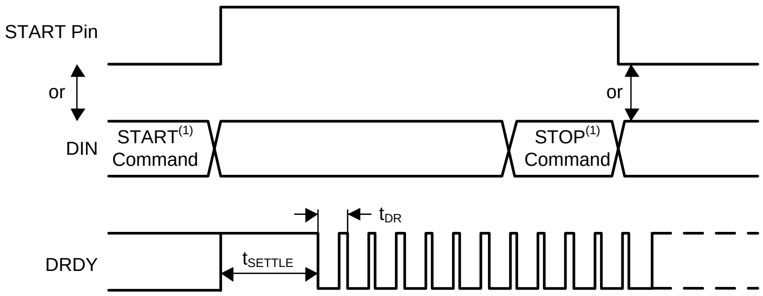


Figure 33. Settling Time for the Input Transient

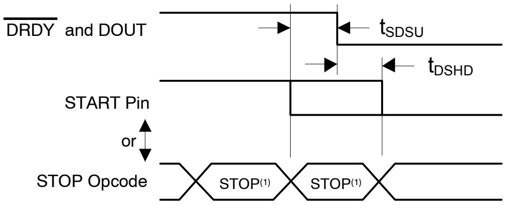
9.4.3.3 Continuous Conversion Mode

When the START pin is pulled high or the START command is issued, conversions continue indefinitely until the START pin is taken low or the STOP command is transmitted, as shown in Figure 34. When the START pin is pulled low or the STOP command is issued, the conversion in progress completes and the $\overline{\text{DRDY}}$ output transitions from high to low indicating that the latest data are available. Figure 35 and Table 6 illustrate the timing of where the START pin can be brought low or the STOP command can be sent relative to a completed conversion to halt further conversions. If the START pin is pulled low or if the STOP command is sent after the t_{DSHD} time, then an additional conversion takes place and completes before further conversions are halted. To continuously run the converter without commands, tie the START pin high.



(1) START and STOP commands take effect on the seventh SCLK falling edge.

Figure 34. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the transmission.

Figure 35. START to $\overline{\text{DRDY}}$ Timing

Table 6. Timing Characteristics for Figure 35[1]

		MIN	UNIT
t_{SDSU}	Setup time; set the START pin low or send the STOP command before the $\overline{\text{DRDY}}$ falling edge to halt further conversions	16	t_{CLK}
t_{DSHD}	Delay time; set the START pin low or send the STOP command to complete the current conversion and halt further conversions	16	t_{CLK}

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the transmission.

9.5 Programming

9.5.1 SPI Interface

The SPI-compatible serial interface consists of four signals: $\overline{\text{CS}}$, SCLK, DIN, and DOUT. The interface is used to read conversion data, read and write registers, and control the ADS131E08S operation. The $\overline{\text{DRDY}}$ output is used as a status signal to indicate when ADC data are ready for readback. $\overline{\text{DRDY}}$ goes low when new data are available.

9.5.1.1 Chip Select ($\overline{\text{CS}}$)

Chip select ($\overline{\text{CS}}$) selects the ADS131E08S for SPI communication. $\overline{\text{CS}}$ must remain low for the duration of the serial communication. After the serial communication is finished, wait four or more t_{CLK} cycles before taking $\overline{\text{CS}}$ high; see the *Timing Requirements* section. When $\overline{\text{CS}}$ is taken high, the serial interface is reset, SCLK and DIN are ignored (SCLK clears $\overline{\text{DRDY}}$ even when $\overline{\text{CS}}$ is high; see Figure 38 for more details), and DOUT enters a high-impedance state. $\overline{\text{DRDY}}$ asserts when data conversion is complete, regardless of whether $\overline{\text{CS}}$ is high or low.

9.5.1.2 Serial Clock (SCLK)

Use SCLK as the SPI serial clock to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS131E08S.

Care must be taken to prevent glitches on SCLK when $\overline{\text{CS}}$ is low. Glitches as small as 1 ns in duration can be interpreted as a valid serial clock. An instruction on DIN is decoded every eight serial clocks. If instructions are suspected of being interrupted erroneously, toggle $\overline{\text{CS}}$ high and back low to reset the SPI interface, placing the device in normal operation.

For a single device, the minimum speed needed for SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Standard Configuration* section.) The SCLK rate limitation, as described by Equation 7, applies to RDATAC mode.

$$t_{SCLK} < (t_{DR} - 4\ t_{CLK}) / (N_{BITS} \times 8 + 24)$$

where

- N_{BITS} = resolution of data for the current data rate; 16 or 24 (7)

For example, if the ADS131E08S is used with an 8-kSPS mode (24-bit resolution), the minimum SCLK speed is 1.755 MHz to shift out all the data.

Data retrieval can be done either by putting the device in read data continuous mode (RDATAC mode) or reading on demand using the read data command (RDATA). The SCLK rate limitation, as described by Equation 7, applies to RDATAC mode. When using the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{\text{DRDY}}$ signals. This calculation assumes that there are no other commands issued in between data captures.

There are two methods for transmitting SCLKs to the ADS131E08S to meet the decode timing specification ($t_{SDECODE}$) illustrated in Figure 1 for multiple byte commands:

1. SCLK can be transmitted in 8-bit bursts with a gap between bursts to maintain the $t_{SDECODE}$ timing specification. The maximum SCLK frequency is specified in Figure 1.
2. A continuous SCLK stream can be sent when $\overline{\text{CS}}$ is low. Verify that the SCLK speed meets the $t_{SDECODE}$ timing requirement. This method is not to be confused with a free-running SCLK where SCLK also operates when $\overline{\text{CS}}$ is high. A free-running SCLK operation is not supported by this device.

Programming (continued)

9.5.1.3 Data Input (DIN)

Use the data input pin (DIN) along with SCLK to send commands and register data to the ADS131E08S. The device latches data on DIN on the SCLK falling edge.

9.5.1.4 Data Output (DOUT)

Use the data output pin (DOUT) with SCLK to read conversions and register data from the ADS131E08S. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{\text{CS}}$ is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line can also be used to indicate when new data are available. If $\overline{\text{CS}}$ is low when new data are ready, a high-to-low transition on the DOUT line occurs synchronously with a high-to-low transition on $\overline{\text{DRDY}}$, as shown in Figure 36. This feature can be used to minimize the number of connections between the device and system controller.

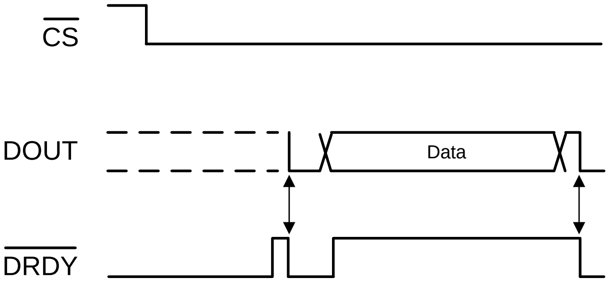


Figure 36. Using DOUT as $\overline{\text{DRDY}}$

9.5.1.5 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output signal that transitions from high to low to indicate that new conversion data are ready. $\overline{\text{DRDY}}$ behavior is determined by whether the device is in RDATAC mode or if the RDATA command is being used to read data on demand. See the *RDATAC: Start Read Data Continuous Mode* and *RDATA: Read Data* sections for further details. The $\overline{\text{CS}}$ signal has no effect on the data-ready signal.

When reading data with the RDATA command, the read operation can overlap the next $\overline{\text{DRDY}}$ occurrence without data corruption.

Figure 37 shows the relationship between $\overline{\text{DRDY}}$, DOUT, and SCLK during data retrieval. DOUT transitions on the SCLK rising edge. $\overline{\text{DRDY}}$ goes high on the first SCLK falling edge regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin. Data starts with the MSB of the status word and then proceeds to the ADC channel data in sequential order (channel 1, channel 2, and so forth). Data for powered down channels appear in the data stream as 0s and are to be ignored.

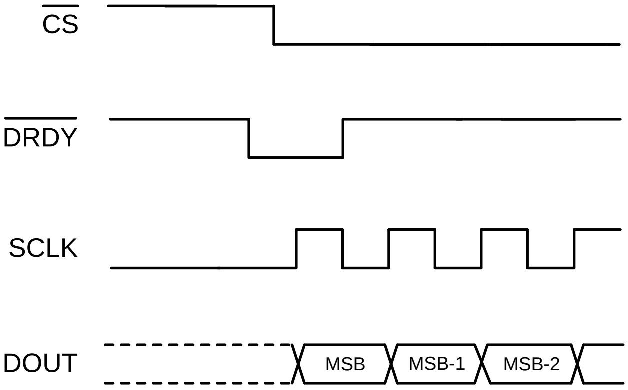


Figure 37. $\overline{\text{DRDY}}$ Behavior with Data Retrieval

Programming (continued)

The $\overline{\text{DRDY}}$ signal is cleared on the first SCLK falling edge regardless of the state of $\overline{\text{CS}}$. This condition must be taken into consideration if the SPI bus is used to communicate with other devices on the same bus. Figure 38 shows a behavior diagram for $\overline{\text{DRDY}}$ when SCLKs are sent with $\overline{\text{CS}}$ high. Figure 38 shows that no data are clocked out, but the $\overline{\text{DRDY}}$ signal is cleared.

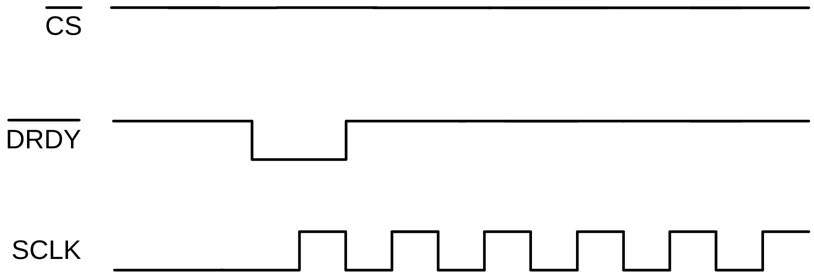


Figure 38. $\overline{\text{DRDY}}$ and SCLK Behavior when $\overline{\text{CS}}$ is High

9.5.2 Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Start Read Data Continuous Mode* section) can be used to set the device in a mode to read the data continuously without having to send a command. The read data command (see the *RDATA: Read Data* section) can be used to read only one data output from the device (see the *SPI Command Definitions* section for more details). Conversion data are read out serially on DOUT. The MSB of the status word is clocked out on the first SCLK rising edge, followed by the ADC channel data. $\overline{\text{DRDY}}$ returns to high on the first SCLK falling edge. DIN remains low for the entire read operation.

9.5.2.1 Status Word

A status word precedes data readback and provides information on the state of the ADS131E08S. The status word is 24 bits long and contains the values for FAULT_STATP, FAULT_STATN, and the GPIO data bits. The content alignment is shown in Figure 39.

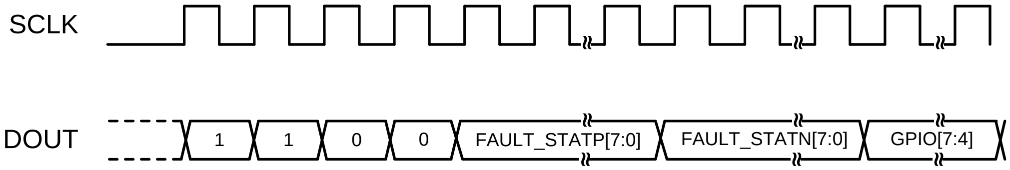


Figure 39. Status Word Content

NOTE

The status word length is always 24 bits. The length does not change for 32-kSPS and 64-kSPS data rates.

9.5.2.2 Readback Length

The number of bits in the data output depends on the number of channels and the number of bits per channel. The data format for each channel data are twos complement and MSB first.

For the ADS131E08S with 32-kSPS and 64-kSPS data rates, the number of data bits is: 24 status bits + 16 bits per channel × 8 channels = 152 bits.

For all other data rates, the number of data bits is: 24 status bits + 24 bits per channel × 8 channels = 216 bits.

When channels are powered down using the user register setting, the corresponding channel output is set to 0. However, the sequence of channel outputs remains the same.

Programming (continued)

The ADS131E08S also provides a multiple data readback feature. Data can be read out multiple times by simply providing more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY_IN bit in the CONFIG1 register must be set to 1 for multiple read backs.

9.5.2.3 Data Format

The DR[2:0] bits in the CONFIG1 register sets the output resolution for the ADS131E08S. When DR[2:0] = 000 or 001, the 16 bits of data per channel are sent in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 8.

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{16} = \text{FS} / 2^{15} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

Table 7 summarizes the ideal output codes for different input signals.

Table 7. 16-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} $V_{(INxP)} - V_{(INxN)}$	IDEAL OUTPUT CODE(1)
$\geq$ FS $(2^{15} - 1) / 2^{15}$	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
$\leq$ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

When DR[2:0] = 010, 011, 100, 101, or 110, the ADS131E08S outputs 24 bits of data per channel in binary twos complement format, MSB first. The size of one code (LSB) is calculated using Equation 9.

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{24} = \text{FS} / 2^{23} \quad (9)$$

A positive full-scale input [$V_{IN} \geq (\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 8 summarizes the ideal output codes for different input signals.

Table 8. 24-Bit Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} $V_{(INxP)} - V_{(INxN)}$	IDEAL OUTPUT CODE(1)
$\geq$ FS $(2^{23} - 1) / 2^{23}$	7FFFFFh
FS / 2^{23}	000001h
0	000000h
–FS / 2^{23}	FFFFFFh
$\leq$ –FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

9.5.3 SPI Command Definitions

The ADS131E08S provides flexible configuration control. The commands, summarized in Table 9, control and configure device operation. The commands are stand-alone, except for the register read and register write operations that require a second command byte to include additional data. $\overline{CS}$ can be taken high or held low between commands but must stay low for the entire command operation (including multibyte commands). System commands and the RDATA command are decoded by the ADS131E08S on the seventh SCLK falling edge. The register read and write commands are decoded on the eighth SCLK falling edge. Make sure to follow the SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 9. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
SYSTEM COMMANDS			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start or restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversions	0000 1010 (0Ah)	
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	
DATA READ COMMANDS			
RDATAC	Enable read data continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop read data continuous mode	0001 0001 (11h)	
RDATA	Read data by command	0001 0010 (12h)	
REGISTER READ COMMANDS			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = the starting register address for read and write commands.

9.5.3.1 WAKEUP: Exit STANDBY Mode

The WAKEUP command exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* section. Be sure to allow enough time for all circuits in STANDBY mode to power-up (see the *Electrical Characteristics* table for details). There are no SCLK rate restrictions for this command and it can be issued at any time. Following the WAKEUP command, wait 4 t_{CLK} cycles before sending another command.

9.5.3.2 STANDBY: Enter STANDBY Mode

The STANDBY command enters low-power standby mode. All circuits in the device are powered down except for the reference section. The standby mode power consumption is specified in the *Electrical Characteristics* table. There are no SCLK rate restrictions for this command and it can be issued at any time. Do not send any other command other than the WAKEUP command after the device enters standby mode.

9.5.3.3 RESET: Reset Registers to Default Values

The RESET command resets the digital filter and returns all register settings to their default values; see the *Reset* section for more details. There are no SCLK rate restrictions for this command and it can be issued at any time. 18 t_{CLK} cycles are required to execute the RESET command. Do not send any commands during this time.

9.5.3.4 START: Start Conversions

The START command starts data conversions. Tie the START pin low to control conversions by the START and STOP commands. If conversions are in progress, this command has no effect. The STOP command is used to stop conversions. If the START command is immediately followed by a STOP command, then there must be a gap of 4 t_{CLK} cycles between the commands. The current conversion completes before further conversions are halted. There are no SCLK rate restrictions for this command and it can be issued at any time.

9.5.3.5 STOP: Stop Conversions

The STOP command stops conversions. Tie the START pin low to control conversions by the START and STOP commands. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect.

9.5.3.6 OFFSETCAL: Channel Offset Calibration

The OFFSETCAL command is used to cancel the offset of each channel. The OFFSETCAL command is recommended to be issued every time there is a change in PGA gain settings.

When the OFFSETCAL command is issued, the device configures itself to the lowest data rate (DR = 110, 1 kSPS) and performs the following steps for each channel:

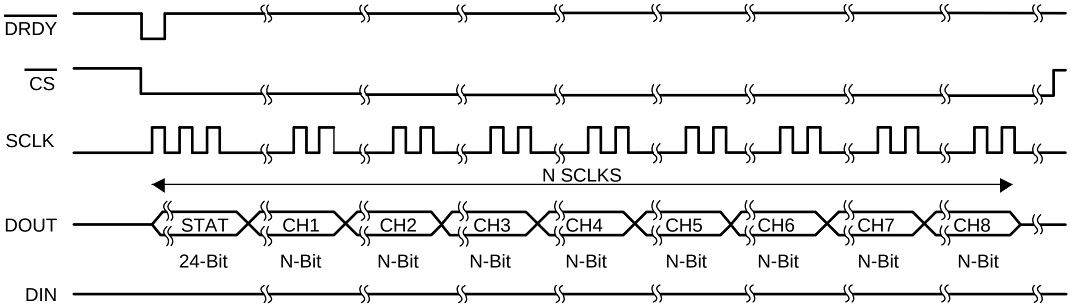
- Short the analog inputs of each channel together and connect them to mid-supply [(AVDD + AVSS) / 2)
- Reset the digital filter (requires a filter settling time = 4 t_{DR})
- Collect 16 data points for calibration = 15 t_{DR}

Total calibration time = (19 t_{DR} × 8) + 1 ms = 153 ms.

9.5.3.7 RDATAC: Start Read Data Continuous Mode

The RDATAC command enables read data continuous mode. In this mode, conversion data are retrieved from the device without the need to issue subsequent RDATA commands. This mode places the conversion data in the output register with every $\overline{\text{DRDY}}$ falling edge so that the data can be shifted out directly. Shift out all data from the device before data are updated with a new $\overline{\text{DRDY}}$ falling edge to avoid losing data. The read data continuous mode is the default mode of the device.

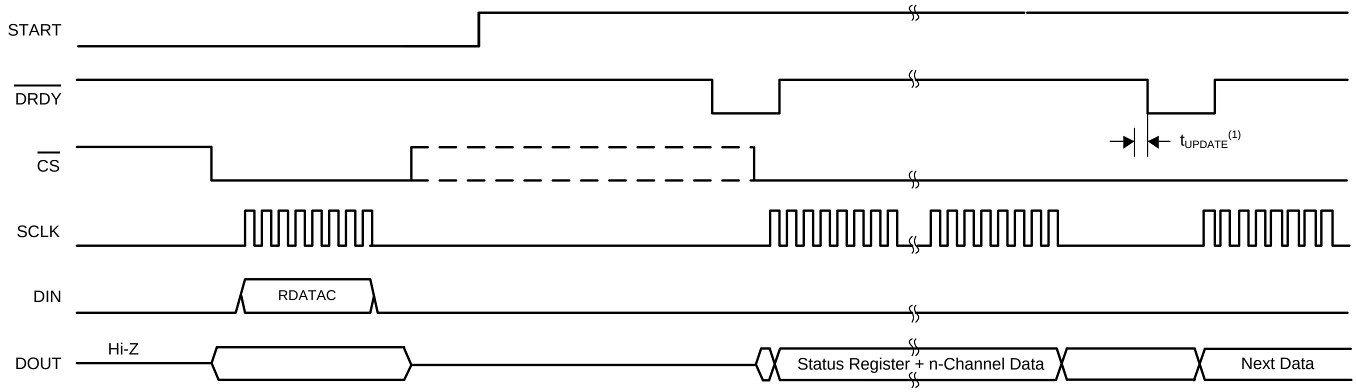
Figure 40 shows the ADS131E08S data output protocol when using RDATAC mode.



NOTE: X SCLKs = (N bits)(8 channels) + 24 bits. N-bit is dependent upon the DR[2:0] registry bit settings (N = 16 or 24).

Figure 40. ADS131E08S SPI Bus Data Output (Eight Channels)

RDATAC mode is stopped by the stop read data continuous (SDATAC) command. If the device is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the device. There are no SCLK rate restrictions for this command. However, subsequent data retrieval SCLKs or the SDATAC command must wait at least 4 t_{CLK} cycles for the command to execute. RDATAC timing is shown in Figure 41. There is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{\text{DRDY}}$ pulse where this command cannot be issued in. If no data are retrieved from the device and $\overline{\text{CS}}$ is held low, a high-to-low DOUT transition occurs synchronously with $\overline{\text{DRDY}}$. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 41 shows the recommended way to use the RDATAC command. Read data continuous mode is ideally-suited for applications such as data loggers or recorders where registers are set one time and do not need to be reconfigured.



(1) $t_{UPDATE} = 4 / f_{CLK}$. Do not read data during this time.

Figure 41. Reading Data in RDATAC Mode

9.5.3.8 SDATAC: Stop Read Data Continuous Mode

The SDATAC command stops the read data continuous mode. There are no SCLK rate restrictions for this command, but wait at least 4 t_{CLK} cycles before issuing any further commands. Use the read data (RDATA) command to read data when in SDATAC mode.

9.5.3.9 RDATA: Read Data

Use the RDATA command to read conversion data when not in read data continuous mode. Issue this command after $\overline{\text{DRDY}}$ goes low to read the conversion result (in stop read data continuous mode). There are no SCLK rate restrictions for this command, and there is no wait time needed for subsequent commands or data retrieval SCLKs. To use the RDATA command, the device must be actively converting (the START pin must be held high or the START command must be issued). When reading data with the RDATA command, the read operation can overlap the next $\overline{\text{DRDY}}$ occurrence without data corruption. RDATA can be sent multiple times after new data are available, thus supporting multiple data readback. Figure 42 illustrates the recommended way to use the RDATA command. RDATA is best suited for systems where register settings must be read or the user does not have precise control over timing. Reading data using the RDATA command is recommended to avoid data corruption when the $\overline{\text{DRDY}}$ signal is not monitored.

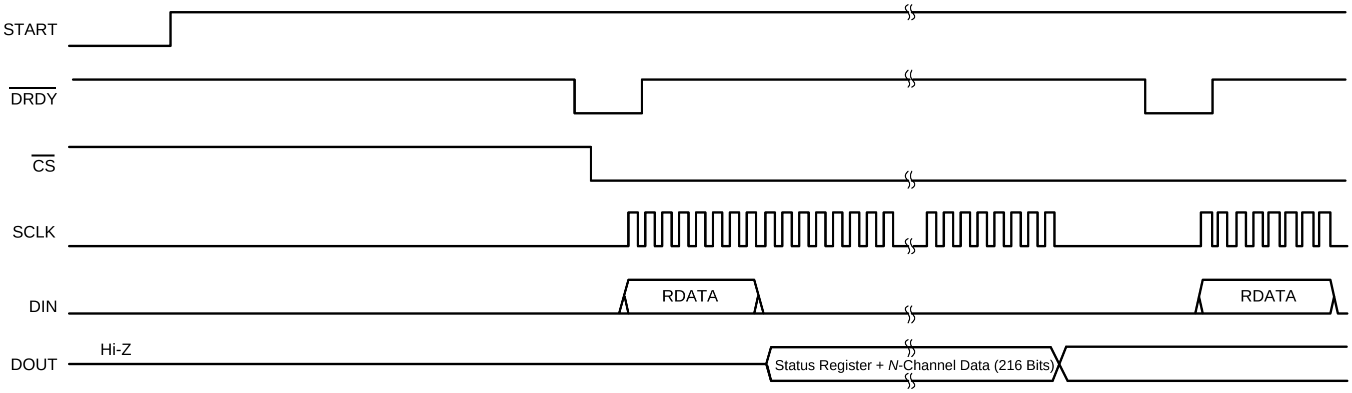


Figure 42. RDATA Usage

9.5.3.10 RREG: Read from Register

The RREG command reads the contents of one or more device configuration registers. When the device is in read data continuous mode, an SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued at any time. The RREG command is a two-byte command on DIN followed by the register data output on DOUT. The command is constructed as follows:

First byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 43. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued; see Figure 1. CS must be low for the entire command.

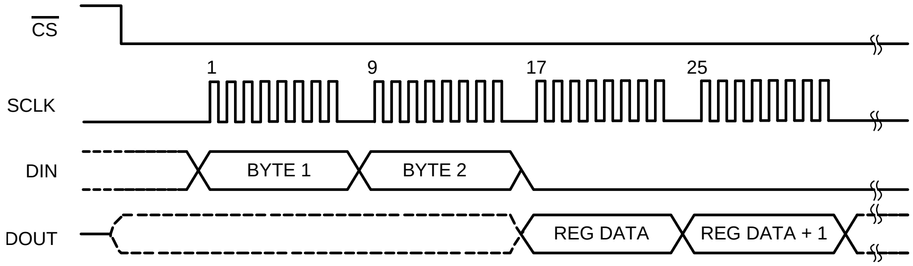


Figure 43. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (BYTE 1 = 0010 0000, BYTE 2 = 0000 0001)

9.5.3.11 WREG: Write to Register

The WREG command writes data to one or more device configuration registers. The WREG command is a two-byte command followed by the register data input. The command is constructed as follows:

First byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the two command bytes, the register data follows (in MSB-first format), as shown in Figure 44. For multiple register writes across reserved registers (0Dh–11h), these registers must be included in the register count and the default setting of the reserved register must be written. The WREG command can be issued at any time. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued; see Figure 1. $\overline{CS}$ must be low for the entire command.

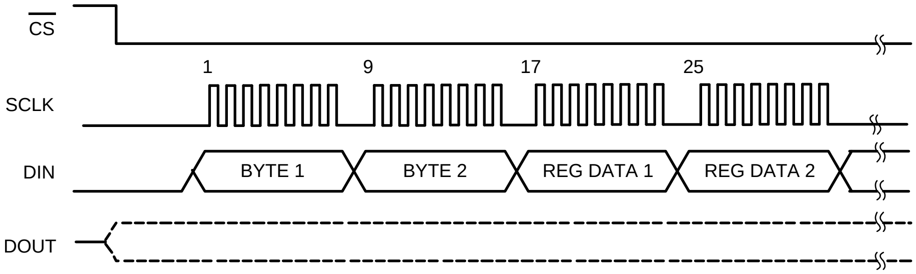


Figure 44. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (BYTE 1 = 0100 0000, BYTE 2 = 0000 0001)

9.5.3.12 Sending Multibyte Commands

The ADS131E08S serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute each command. This timing requirement can place restrictions on the SCLK speed and operational modes. For example:

Assuming CLK is 2.048 MHz, then $t_{SDECODE}$ (4 t_{CLK}) is 1.96 µs. When SCLK is 16 MHz, one byte can be transferred in 0.5 µs. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay of 1.46 µs (1.96 µs – 0.5 µs) must be inserted after the first byte and before the second byte. If SCLK is 4 MHz, one byte is transferred in 2 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification (2 µs > 1.96 µs), the processor can send subsequent bytes without delay.

9.6 Register Map

Table 10 describes the various ADS131E08S registers.

Table 10. Register Map(1)

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (Read-Only Registers)										
00h	ID	D2	1	1	REV_ID	1	0	0	1	0
GLOBAL SETTINGS ACROSS CHANNELS										
01h	CONFIG1	D4	1	DAISY_IN	CLK_EN	1	0	DR[2:0]		
02h	CONFIG2	E0	1	1	1	INT_TEST	0	TEST_AMP0	TEST_FREQ[1:0]	
03h	CONFIG3	E8	1	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
04h	FAULT	00	COMP_TH[2:0]			0	0	0	0	0
CHANNEL-SPECIFIC SETTINGS										
05h	CH1SET	10	PD1	GAIN1[2:0]			0	MUX1[2:0]		
06h	CH2SET	10	PD2	GAIN2[2:0]			0	MUX2[2:0]		
07h	CH3SET	10	PD3	GAIN3[2:0]			0	MUX3[2:0]		
08h	CH4SET	10	PD4	GAIN4[2:0]			0	MUX4[2:0]		
09h	CH5SET	10	PD5	GAIN5[2:0]			0	MUX5[2:0]		
0Ah	CH6SET	10	PD6	GAIN6[2:0]			0	MUX6[2:0]		
0Bh	CH7SET	10	PD7	GAIN7[2:0]			0	MUX7[2:0]		
0Ch	CH8SET	10	PD8	GAIN8[2:0]			0	MUX8[2:0]		
FAULT DETECT STATUS REGISTERS (Read-Only Registers)										
12h	FAULT_STATP	00	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
13h	FAULT_STATN	00	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO SETTINGS										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

(1) When using multiple register write commands, registers 0Dh, 0Eh, 0Fh, 10h, and 11h must be written to 00h.

9.6.1 Register Descriptions

9.6.1.1 ID: ID Control Register (Factory-Programmed, Read-Only) (address = 00h) [reset = D2h]

This register is programmed during device manufacture to indicate device characteristics.

Figure 45. ID: ID Control Register

7	6	5	4	3	2	1	0
1	1	REV_ID	1	0	0	1	0
R-1h	R-1h	R-1h	R-1h	R-0h	R-0h	R-1h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 11. ID: ID Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	3h	**Reserved.** Always reads 1.
5	REV_ID	R	0h	**Device family identification.** This bit indicates the device family. 0 = ADS131E08S 1 = Reserved
4	Reserved	R	1h	**Reserved.** Always reads 1.
3-2	Reserved	R	0h	**Reserved.** Always reads 0.
1	Reserved	R	1h	**Reserved.** Always reads 1.
0	Reserved	R	0h	**Reserved.** Always reads 0.

9.6.1.2 CONFIG1: Configuration Register 1 (address = 01h) [reset = D4h]

This register configures each ADC channel sample rate.

Figure 46. CONFIG1: Configuration Register 1

7	6	5	4	3	2	1	0
1	DAISY_IN	CLK_EN	1	0	DR[2:0]		
R/W-1h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-4h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 12. CONFIG1: Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
6	DAISY_IN	R/W	1h	**Daisy-chain and multiple data readback mode.** This bit determines which mode is enabled. 0 = Daisy-chain mode 1 = Multiple data readback mode
5	CLK_EN	R/W	0h	**CLK connection**(1). This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1. 0 = Oscillator clock output disabled 1 = Oscillator clock output enabled
4	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2-0	DR[2:0]	R/W	4h	**Output data rate.** These bits determine the output data rate and resolution; see Table 13 for details.

(1) Additional power is consumed when driving external devices.

Table 13. Data Rate Settings

DR[2:0]	RESOLUTION	DATA RATE (kSPS)(1)
000	16-bit output	64
001	16-bit output	32
010	24-bit output	16
011	24-bit output	8
100	24-bit output	4
101	24-bit output	2
110	24-bit output	1
111	Do not use	NA

(1) Where f_{CLK} = 2.048 MHz. Data rates scale with master clock frequency.

9.6.1.3 CONFIG2: Configuration Register 2 (address = 02h) [reset = 00h]

This register configures the test signal generation; see the *Input Multiplexer* section for more details.

Figure 47. CONFIG2: Configuration Register 2

7	6	5	4	3	2	1	0
1	1	1	INT_TEST	0	TEST_AMP	TEST_FREQ[1:0]	
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 14. CONFIG2: Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
4	INT_TEST	R/W	0h	**Test signal source.** This bit determines the source for the test signal. 0 = Test signals are driven externally 1 = Test signals are generated internally
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2	TEST_AMP	R/W	0h	**Test signal amplitude.** These bits determine the calibration signal amplitude. 0 = $1 \times -(V_{(VREFP)} - V_{(VREFN)}) / 2400$ 1 = $2 \times -(V_{(VREFP)} - V_{(VREFN)}) / 2400$
1-0	TEST_FREQ[1:0]	R/W	0h	**Test signal frequency.** These bits determine the test signal frequency. 00 = Pulsed at $f_{CLK} / 2^{21}$ 01 = Pulsed at $f_{CLK} / 2^{20}$ 10 = Not used 11 = At dc

9.6.1.4 CONFIG3: Configuration Register 3 (address = 03h) [reset = E8]

This register configures the reference and internal amplifier operation.

Figure 48. CONFIG3: Configuration Register 3

7	6	5	4	3	2	1	0
1	1	VREF_4V	0	OPAMP_REF	PDB_OPAMP	0	0
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. CONFIG3: Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	1h	**Reserved.** Must be set to 1. This bit reads high.
5	VREF_4V	R/W	1h	**Internal reference voltage.** This bit determines the reference voltage, VREFP. 0 = VREFP is set to 2.4 V 1 = VREFP is set to 4 V
4	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
3	OPAMP_REF	R/W	0h	**Op amp reference.** This bit determines whether the op amp noninverting input connects to the OPAMPP pin or to the internally-derived supply (AVDD + AVSS) / 2. 0 = Noninverting input connected to the OPAMPP pin 1 = Noninverting input connected to (AVDD + AVSS) / 2
2	PDB_OPAMP	R/W	0h	**Op amp power-down.** This bit powers down the op amp. 0 = Power-down op amp 1 = Enable op amp
1	Reserved	R/W	0h	**Reserved.** Must be set to 0. Reads back as 0.
0	Reserved	R	0h	**Reserved.** Reads back as either 1 or 0.

9.6.1.5 FAULT: Fault Detect Control Register (address = 04h) [reset = 00h]

This register configures the fault detection operation.

Figure 49. FAULT: Fault Detect Control Register

7	6	5	4	3	2	1	0
COMP_TH[2:0]			0	0	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. FAULT: Fault Detect Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	COMP_TH[2:0]	R/W	0h	**Fault detect comparator threshold.** These bits determine the fault detect comparator threshold level setting. See the *Input Out-of-Range Detection* section for a detailed description. **Comparator high-side threshold.** 000 = 95% 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% **Comparator low-side threshold.** 000 = 5% 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4-0	Reserved	R/W	00h	**Reserved.** Must be set to 0. This bit reads low.

9.6.1.6 CHnSET: Individual Channel Settings (address = 05h to 0Ch) [reset = 10h]

This register configures the power mode, PGA gain, and multiplexer settings for the channels; see the *Input Multiplexer* section for details. CHnSET are similar to CH1SET, corresponding to the respective channels (see Table 10).

Figure 50. CHnSET(1): Individual Channel Settings

7	6	5	4	3	2	1	0
PDn	GAINn[2:0]			0	MUXn[2:0]		
R/W-0h	R/W-1h			R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

(1) n = 1 to 8.

Table 17. CHnSET: Individual Channel Settings Field Descriptions

Bit	Field	Type	Reset	Description
7	PDn	R/W	0h	**Power-down (n = individual channel number).** This bit determines the channel power mode for the corresponding channel. 0 = Normal operation 1 = Channel power-down
6-4	GAINn[2:0]	R/W	1h	**PGA gain (n = individual channel number).** These bits determine the PGA gain setting. 000 = Do not use 001 = 1 010 = 2 011 = Do not use 100 = 4 101 = 8 110 = 12 111 = Do not use
3	Reserved	R/W	0h	**Reserved.** Must be set to 0. This bit reads low.
2-0	MUXn[2:0]	R/W	0h	**Channel input (n = individual channel number).** These bits determine the channel input selection. 000 = Normal input 001 = Input shorted to (AVDD + AVSS) / 2 (for offset or noise measurements) 010 = Do not use 011 = MVDD for supply measurement 100 = Temperature sensor 101 = Test signal 110 = Do not use 111 = Do not use

9.6.1.7 FAULT_STATP: Fault Detect Positive Input Status (address = 12h) [reset = 00h]

This register stores the status of whether the positive input on each channel has a fault or not. Faults are determined by comparing the input pin to a threshold set by Table 16; see the *Input Out-of-Range Detection* section for details.

Figure 51. FAULT_STATP: Fault Detect Positive Input Status

7	6	5	4	3	2	1	0
IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 18. FAULT_STATP: Fault Detect Positive Input Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8P_FAULT	R	0h	**IN8P threshold detect.** 0 = Channel 8 positive input pin does not exceed threshold set 1 = Channel 8 positive input pin exceeds threshold set
6	IN7P_FAULT	R	0h	**IN7P threshold detect.** 0 = Channel 7 positive input pin does not exceed threshold set 1 = Channel 7 positive input pin exceeds threshold set
5	IN6P_FAULT	R	0h	**IN6P threshold detect.** 0 = Channel 6 positive input pin does not exceed threshold set 1 = Channel 6 positive input pin exceeds threshold set
4	IN5P_FAULT	R	0h	**IN5P threshold detect.** 0 = Channel 5 positive input pin does not exceed threshold set 1 = Channel 5 positive input pin exceeds threshold set
3	IN4P_FAULT	R	0h	**IN4P threshold detect.** 0 = Channel 4 positive input pin does not exceed threshold set 1 = Channel 4 positive input pin exceeds threshold set
2	IN3P_FAULT	R	0h	**IN3P threshold detect.** 0 = Channel 3 positive input pin does not exceed threshold set 1 = Channel 3 positive input pin exceeds threshold set
1	IN2P_FAULT	R	0h	**IN2P threshold detect.** 0 = Channel 2 positive input pin does not exceed threshold set 1 = Channel 2 positive input pin exceeds threshold set
0	IN1P_FAULT	R	0h	**IN1P threshold detect.** 0 = Channel 1 positive input pin does not exceed threshold set 1 = Channel 1 positive input pin exceeds threshold set

9.6.1.8 FAULT_STATN: Fault Detect Negative Input Status (address = 13h) [reset = 00h]

This register stores the status of whether the negative input on each channel has a fault or not. Faults are determined by comparing the input pin to a threshold set by Table 16; see the *Input Out-of-Range Detection* section for details.

Figure 52. FAULT_STATN: Fault Detect Negative Input Status

7	6	5	4	3	2	1	0
IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read only; -n = value after reset

Table 19. FAULT_STATN: Fault Detect Negative Input Status Field Descriptions

Bit	Field	Type	Reset	Description
7	IN8N_FAULT	R	0h	**IN8N threshold detect.** 0 = Channel 8 negative input pin does not exceed threshold set 1 = Channel 8 negative input pin exceeds threshold set
6	IN7N_FAULT	R	0h	**IN7N threshold detect.** 0 = Channel 7 negative input pin does not exceed threshold set 1 = Channel 7 negative input pin exceeds threshold set
5	IN6N_FAULT	R	0h	**IN6N threshold detect.** 0 = Channel 6 negative input pin does not exceed threshold set 1 = Channel 6 negative input pin exceeds threshold set
4	IN5N_FAULT	R	0h	**IN5N threshold detect.** 0 = Channel 5 negative input pin does not exceed threshold set 1 = Channel 5 negative input pin exceeds threshold set
3	IN4N_FAULT	R	0h	**IN4N threshold detect.** 0 = Channel 4 negative input pin does not exceed threshold set 1 = Channel 4 negative input pin exceeds threshold set
2	IN3N_FAULT	R	0h	**IN3N threshold detect.** 0 = Channel 3 negative input pin does not exceed threshold set 1 = Channel 3 negative input pin exceeds threshold set
1	IN2N_FAULT	R	0h	**IN2N threshold detect.** 0 = Channel 2 negative input pin does not exceed threshold set 1 = Channel 2 negative input pin exceeds threshold set
0	IN1N_FAULT	R	0h	**IN1N threshold detect.** 0 = Channel 1 negative input pin does not exceed threshold set 1 = Channel 1 negative input pin exceeds threshold set

9.6.1.9 GPIO: General-Purpose IO Register (address = 14h) [reset = 0Fh]

This register controls the format and state of the four GPIO pins.

Figure 53. GPIO: General-Purpose IO Register

7	6	5	4	3	2	1	0
GPIOD[4:1]				GPIOC[4:1]			
R/W-0h				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. GPIO: General-Purpose IO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIOD[4:1]	R/W	0h	**GPIO data.** These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.
3-0	GPIOC[4:1]	R/W	Fh	**GPIO control (corresponding to GPIOD).** These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Multiple Device Configuration

The ADS131E08S provides configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{\text{CS}}$. With one additional chip select signal per device, multiple devices can be operated on the same SPI bus. The number of signals needed to interface to *N* devices is 3 + *N*.

10.1.1.1 Synchronizing Multiple Devices

When using multiple devices, the devices can be synchronized using the START signal. The delay time from the rising edge of the START signal to the falling edge of the $\overline{\text{DRDY}}$ signal is fixed for a given data rate (see the *Conversion Mode* section for more details on the settling times). Figure 54 shows the behavior of two devices when synchronized with the START signal.

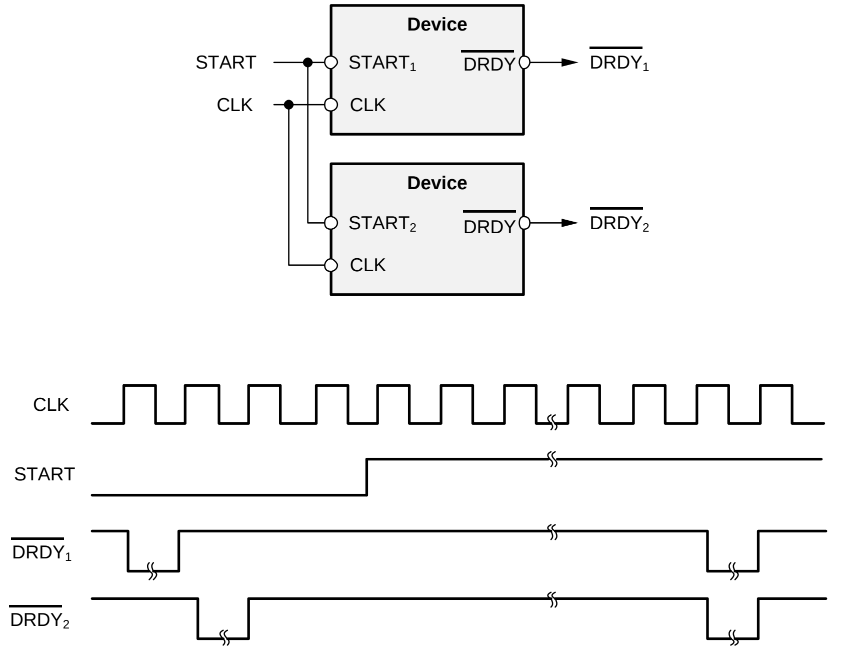


Figure 54. Synchronizing Multiple Converters

To use the internal oscillator in a daisy-chain configuration, one device must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock must be brought out of the device by setting the $\overline{\text{CLK\_EN}}$ register bit to 1. The master device clock is used as the external clock source for the other devices.

There are two ways to connect multiple devices with an optimal number of interface pins: standard configuration and daisy-chain configuration.

Application Information (continued)

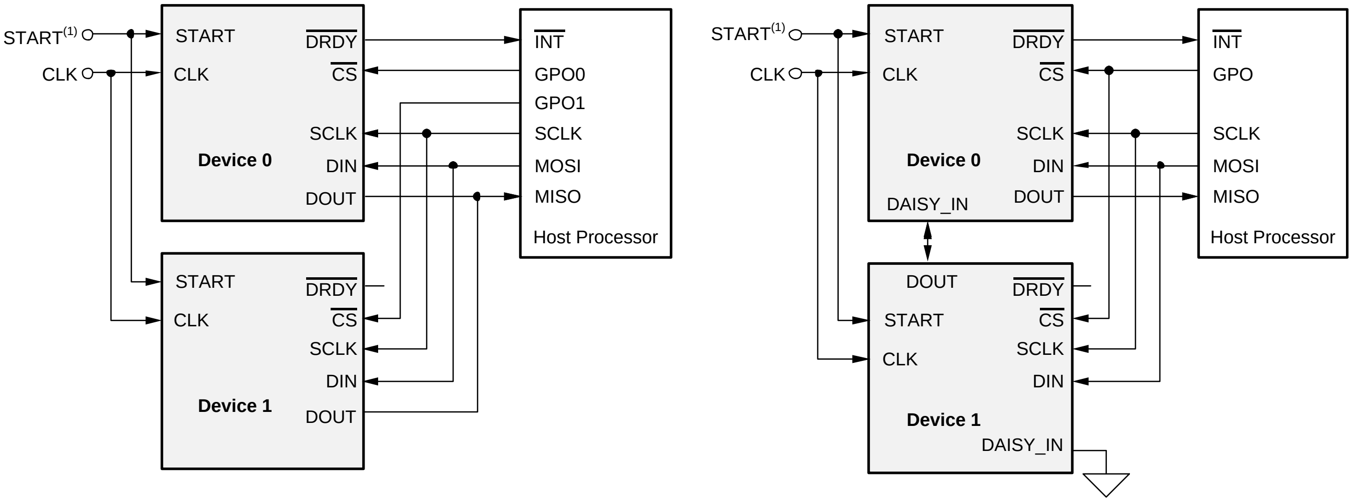
10.1.1.2 Standard Configuration

Figure 55a shows a configuration with two ADS131E08s devices cascaded. Together, the devices create a system with 16 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{\text{CS}}$ being driven to logic 1, the DOUT pin of this device is high-impedance. This structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications where extra I/O pins are available.

10.1.1.3 Daisy-Chain Configuration

Daisy-chain mode is enabled by setting the DAISY_IN bit in the CONFIG1 register. Figure 55b shows the daisy-chain configuration. In this mode SCLK, DIN, and $\overline{\text{CS}}$ are shared across multiple devices. The DOUT pin of device 1 is connected to the DAISY_IN pin of device 0, thereby creating a daisy-chain for the data. Connect the DAISY_IN pin of device 1 to DGND if not used. The daisy-chain timing requirements for the SPI interface are illustrated in Figure 2. Data from the ADS131E08S device 0 appear first on DOUT, followed by a *don't care* bit, and then the status and data words from the ADS131E08S device 1.

The internal oscillator output cannot be enabled because all devices in the chain operate by sharing the same DIN pin, thus an external clock must be used.



a) Standard Configuration

b) Daisy-Chain Configuration

(1) To reduce pin count, set the START pin low and use the START command to synchronize and start conversions.

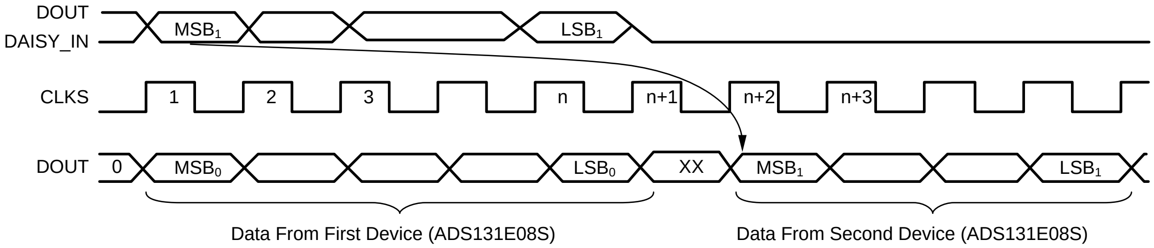
Figure 55. Multiple Device Configurations

There are several items to be aware of when using daisy-chain mode:

1. One extra SCLK must be issued between each data set (see Figure 56)
2. All devices are configured to the same register values because the $\overline{\text{CS}}$ signal is shared
3. Device register readback is only valid for device 0 in the daisy-chain. Only ADC conversion data can be read back from device 1 through device *N*, where *N* is the last device in the chain.

Application Information (continued)

The more devices in the chain, the more challenging adhering to setup and hold times becomes. A star-pattern connection of SCLK to all devices, minimizing the trace length of DOUT, and other printed circuit board (PCB) layout techniques helps to mitigate this challenge with signal delays. Placing delay circuits (such as buffers) between DOUT and DAISY_IN are options to help reduce signal delays. One other option is to insert a *D* flip-flop between DOUT and DAISY_IN clocked on an inverted SCLK. Figure 56 shows a timing diagram for daisy-chain mode.



NOTE: n = (number of channels) × (resolution) + 24 bits. The number of channels is 8. Resolution is 16 bits or 24 bits.

Figure 56. Daisy-Chain Data Word

The maximum number of devices that can be daisy-chained depends on the data rate that the devices are operated at. The maximum number of devices can be calculated with Equation 10.

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24} \tag{10}$$

where:

- N_{BITS} = device resolution (depends on DR[2:0] setting)
- $N_{CHANNELS}$ = number of channels powered up in the device (10)

For example, when the ADS131E08S is operated in 24-bit, 8-kSPS data rate with f_{SCLK} = 10 MHz, up to six devices can be daisy-chained together.

10.1.2 Power Monitoring Specific Applications

All channels of the ADS131E08S are exactly identical, yet independently configurable, thus giving the user the flexibility of selecting any channel for voltage or current monitoring. An overview of a system configured to monitor voltage and current is illustrated in Figure 57. Also, the simultaneously sampling capability of the device allows the user to monitor both the current and the voltage at the same time. The full-scale differential input voltage of each channel is determined by the PGA gain setting (see the *CHnSET: Individual Channel Settings* section) for the respective channel and V_{REF} (see the *CONFIG3: Configuration Register 3* section).

Application Information (continued)

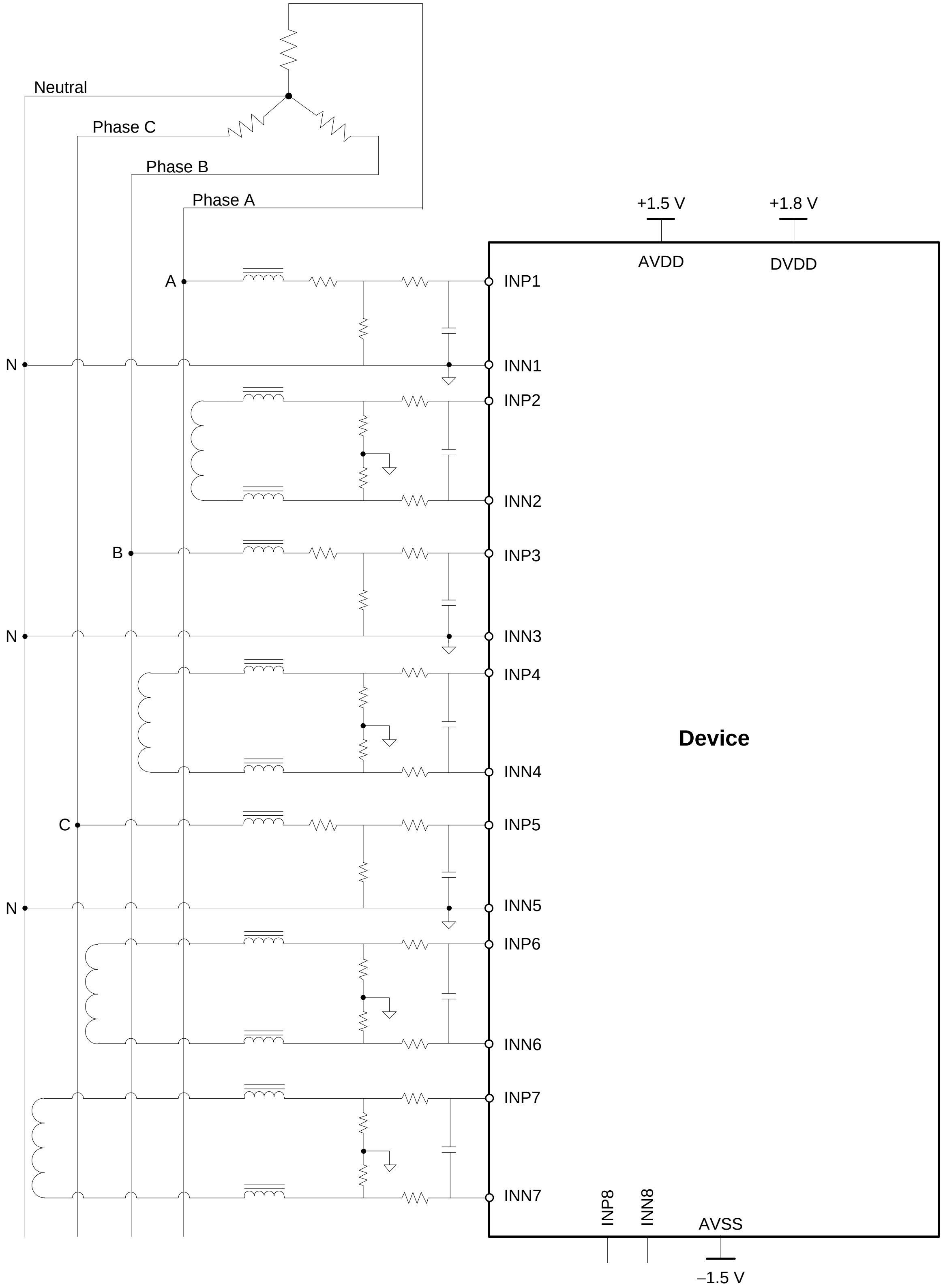


Figure 57. Overview of a Power-Monitoring System

Application Information (continued)

10.1.3 Current Sensing

Figure 58 illustrates a simplified diagram of typical configurations used for current sensing with a Rogowski coil, current transformer (CT), or an air coil that outputs a current or voltage. In the case of a current output transformer, the burden resistors (R1) are used for current-to-voltage conversion. The output of the burden resistors is connected to the ADS131E08S INxP and INxN inputs through an antialiasing RC filter for current sensing. In the case of a voltage output transformer for current sensing (such as certain types of Rogowski coils), the output terminals of the transformer are directly connected to the ADS131E08S INxP and INxN inputs through an antialiasing RC filter. The input network must be biased to mid-supply if using a unipolar-supply analog configuration (AVSS = 0 V, AVDD = 2.7 V to 5.5 V). The common-mode bias voltage [(AVDD + AVSS) / 2] can be obtained from the ADS131E08S by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting the OPAMP_REF bit of the CONFIG3 register to 1, or generated externally with a resistor divider network between the positive and negative supplies.

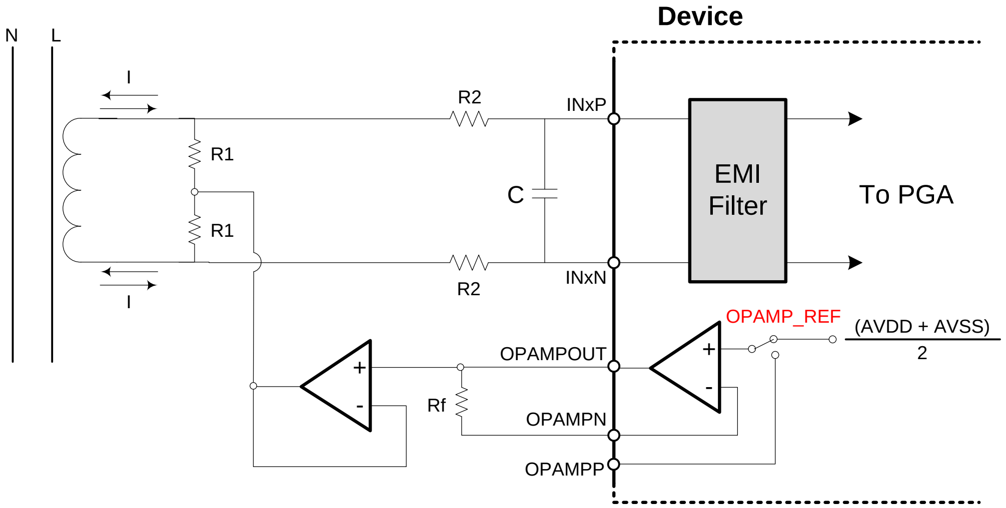
Select the value of resistor R1 for the current output transformer and turns ratio of the transformer such that the ADS131E08S full-scale differential input voltage range is not exceeded. Likewise, select the output voltage for the voltage output transformer to not exceed the full-scale differential input voltage range. In addition, the selection of the resistors (R1 and R2) and turns ratio must not saturate the transformer over the full operating dynamic range. Figure 58a illustrates differential input current sensing and Figure 58b illustrates single-ended input voltage sensing. Use separate external op amps to source and sink current because the internal op amp has very limited current sink and source capability. Additionally, separate op amps for each channel help isolate individual phases from one another to limit crosstalk.

10.1.4 Voltage Sensing

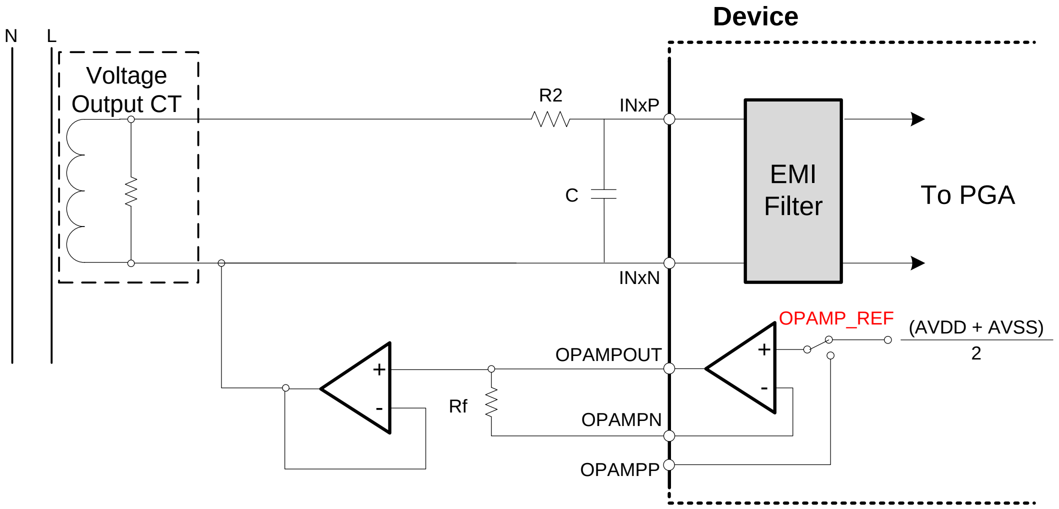
Figure 59 illustrates a simplified diagram of commonly-used differential and single-ended methods of voltage sensing. A resistor divider network is used to step down the line voltage to within the acceptable ADS131E08S input range and then connect to the inputs (INxP and INxN) through an antialiasing RC filter formed by resistor R3 and capacitor C. The common-mode bias voltage [(AVDD + AVSS) / 2] can be obtained from the ADS131E08S by either configuring the internal op amp in a unity-gain configuration using the R_F resistor and setting the OPAMP_REF bit of the CONFIG3 register, or generated externally by using a resistor divider network between the positive and negative supplies.

In either of the cases illustrated in Figure 59 (Figure 59a for a differential input and Figure 59b for a single-ended input), the line voltage is divided down by a factor of [R2 / (R1 + R2)]. Values of R1 and R2 must be carefully chosen so that the voltage across the ADS131E08S inputs (INxP and INxN) does not exceed the range of the ADS131E08S over the full operating dynamic range. Use separate external op amps to source and sink current because the internal op amp has very limited current sink and source capability. Additionally, separate op amps for each channel help isolate individual phases from one another to limit crosstalk.

Application Information (continued)



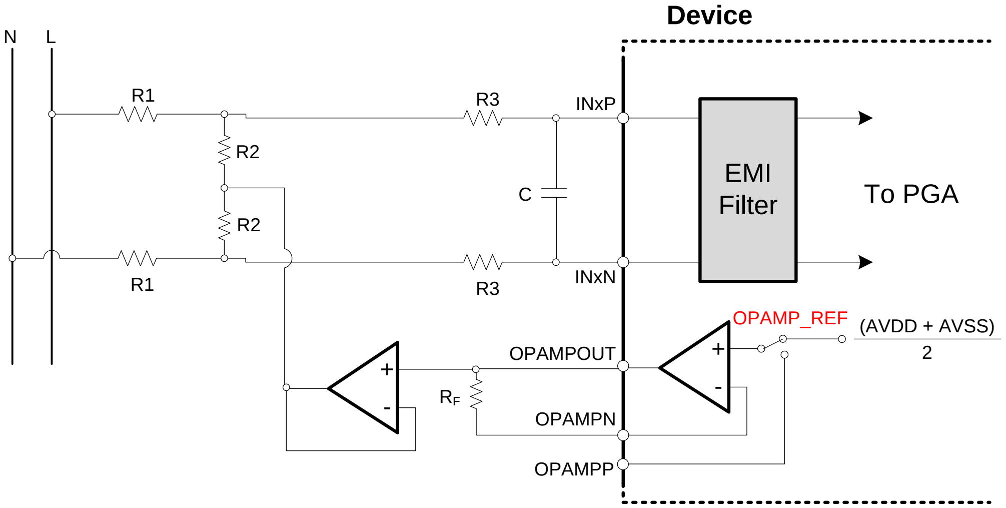
(a) Current Output CT with Differential Input



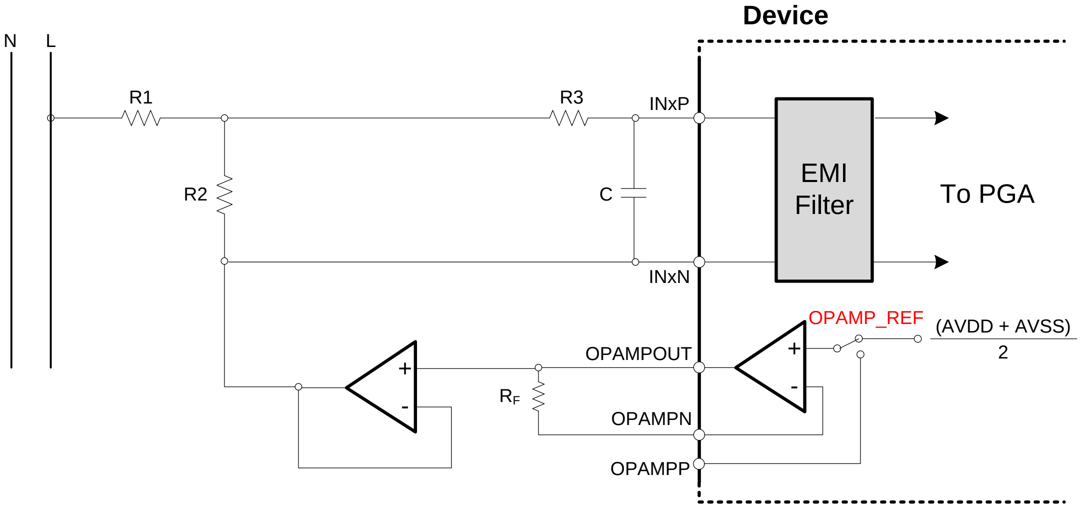
(b) Voltage Output CT with Single-Ended Input

Figure 58. Simplified Current-Sensing Connections

Application Information (continued)



(a) Voltage Sensing with Differential Input



(b) Voltage Sensing with Single-Ended Input

Figure 59. Simplified Voltage-Sensing Connections

10.2 Typical Application

Figure 60 shows the ADS131E08S being used as part of an electronic trip unit (ETU) in a circuit breaker or protection relay. Delta-sigma (ΔΣ), analog-to-digital converters (ADCs), such as the ADS131E08S, are ideal for this application because these devices provide a wide dynamic range. The fast power-up time of the ADS131E08S makes the device an ideal candidate for line-powered circuit breaker applications.

The system measures voltages and currents output from a breaker enclosure. In this example, the first three inputs measure line voltage and the remaining five inputs measure line current from the secondary winding of a current transformer (CT). A voltage divider steps down the voltage from the output of the breaker. Several resistors are used to break up power consumption and are used as a form of fault protection against any potential resistor short-circuit. After the voltage step down, RC filters are used for antialiasing and diodes protect the inputs from overrange.

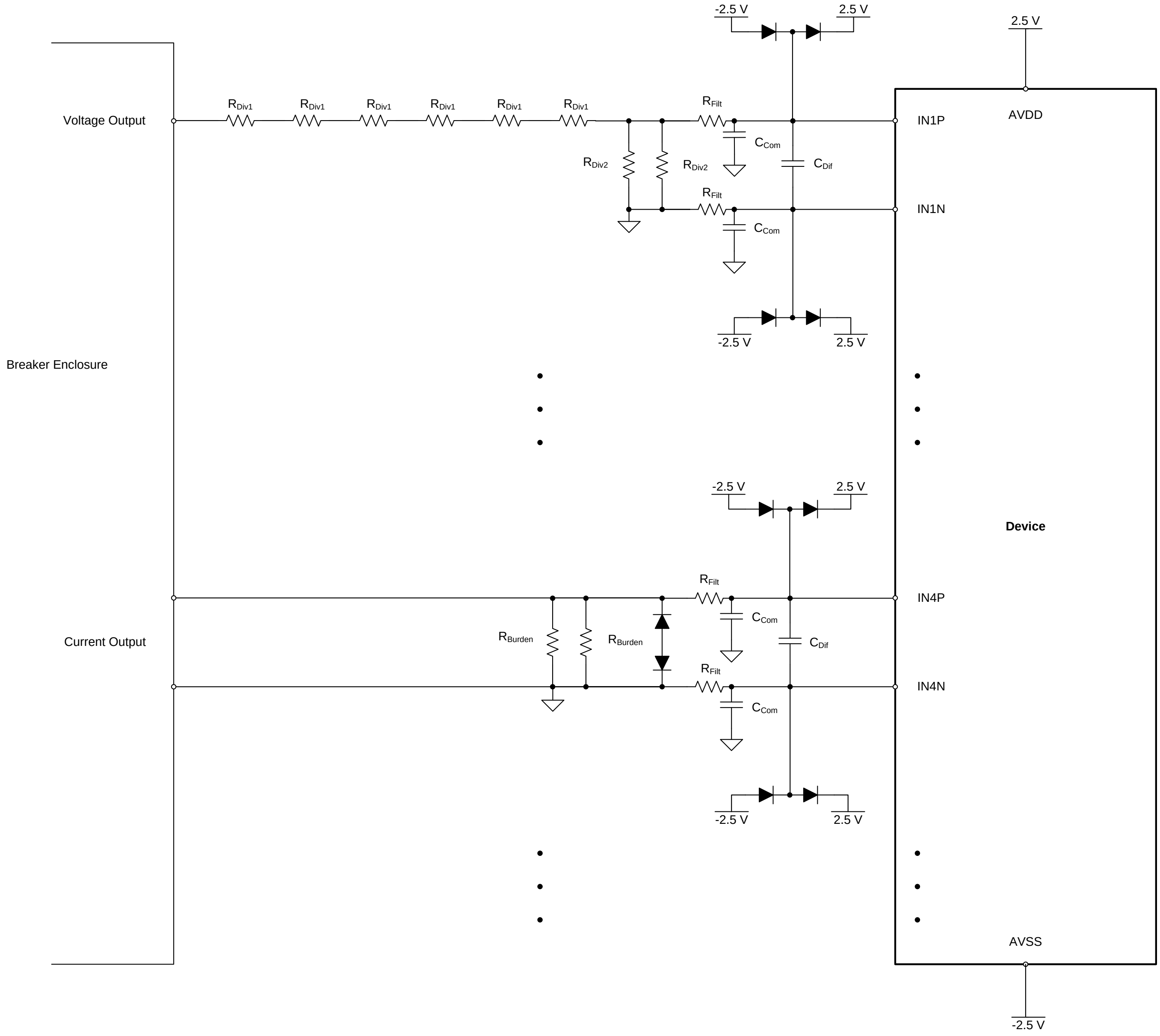


Figure 60. ETU Block Diagram: High-Resolution and Fast Power-Up Analog Front-End for Air Circuit Breaker or Molded Case Circuit Breaker and Protection Relay

Typical Application (continued)

10.2.1 Design Requirements

Table 21 summarizes the design requirements for the circuit breaker front-end application.

Table 21. ETU Circuit Breaker Design Requirements

DESIGN PARAMETER	VALUE
ADC power-up	< 3 ms
Number of voltage inputs	3
Voltage input range	10 V to 750 V
Number of current inputs	5
Current input range	50 mA to 25 A
Dynamic range with fixed gain	> 500
Accuracy	±1%

10.2.2 Detailed Design Procedure

The line voltage is stepped down to a voltage range within the measurable range of the ADC. The reference voltage determines the range in which the ADC can measure signals. The ADS131E08S has two integrated low-drift reference voltage options: 2.4 V and 4 V.

Equation 11 describes the transfer function for the voltage divider at the input in Figure 60. Using multiple series resistors, R_{DIV1}, and multiple parallel resistors, R_{DIV2}, allows for power and heat to be dissipated among several circuit elements and serves as protection against a potential short-circuit across a single resistor. The number of resistors trade off with nominal accuracy because each additional element introduces an additional source of tolerance.

$$V_{IN} = V_{Phase} \times \left(\frac{0.5 \times R_{Div2}}{6 \times R_{Div1} + 0.5 \times R_{Div2}} \right) \tag{11}$$

The step-down resistor, R_{Div2}, dominates the measurement error produced by the resistor network. Using input PGAs on the ADS131E08S helps to mitigate this error source by allowing R_{Div2} to be made smaller and then amplifying the signal to near full-scale using the ADS131E08S PGA.

For this design, R_{Div1} is set to 200 kΩ and R_{Div2} is set to 2.4 kΩ to provide proper signal attenuation at a sufficient power level across each resistor. The input saturates at values greater than ±750 V when using the ADS131E08S internal 2.4-V reference and a PGA gain of 2.

The ADS131E08S measures the line current by creating a voltage across the burden resistance (R_{Burden} in Figure 60) in parallel with the secondary winding of a CT. As with the voltage measurement front-end, multiple resistors (R_{Div1}) that are used to step down a voltage share the duty of dissipating power. In this design, R_{BURDEN} is set to 33 Ω. Used with a 1:500 turns ratio CT, the ADC input saturates with a line current over 25 A when the ADC is configured using the internal 2.4-V reference and a PGA gain of 2.

Diodes protect the ADS131E08S inputs from overvoltage and current. Diodes on each input shunt to either supply if the input voltage exceeds the safe range for the device. On current inputs, a diode shunts the inputs if current on the secondary winding of the CT threatens to damage the device.

The combination of R_{Filt}, C_{Com}, and C_{Dif} form the antialiasing filters for each of the inputs. The differential capacitor C_{Dif} improves the common-mode rejection of the system by sharing its tolerance between the positive and negative input. The antialiasing filter requirement is not strict because the nature of a ΔΣ converter (with oversampling and digital filter) attenuates a significant proportion of out-of-band noise. In addition, the input PGAs have intentionally low bandwidth to provide additional antialiasing. The component values used in this design are R_{Filt} = 1 kΩ, C_{Com} = 47 pF, and C_{Dif} = 0.015 µF. This first-order filter produces a relatively flat frequency response beyond 2 kHz, capable of measuring greater than 30 harmonics at a 50-Hz or 60-Hz fundamental frequency. The 3-dB cutoff frequency of the filter is 5.3 kHz for each input channel.

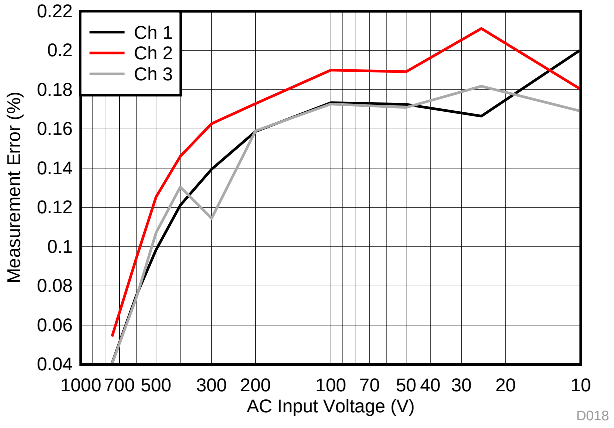
The ETU in a circuit breaker or protection relay can be powered from the line. In this case, fast power-up is required to allow the ADC to begin making measurements shortly after power is restored. The ADS131E08S is designed to fully power-up and collect data in less than 3 ms.

Each analog system block introduces errors from input to output. Protection CTs in the 5P accuracy class can introduce as much as ±1% current error from input to output. CTs in the 10P accuracy class can introduce as much as ±3% error. The burden resistor also introduces errors in the form of resistor tolerance and temperature drift. For the voltage input, error comes from the divider network in the form of resistor tolerance and temperature drift. Finally, the converter introduces errors in the form of offset error, gain error, and reference error. All of these specifications can drift over temperature.

10.2.3 Application Curves

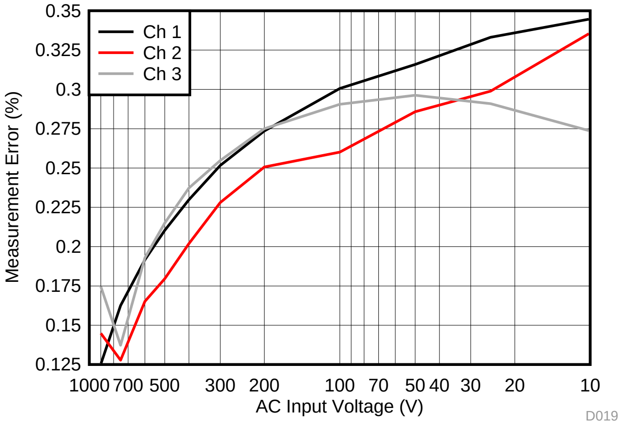
Accuracy is measured using a system designed in a similar way to that illustrated in Figure 60. The CT used for the current input is CT1231 (a 0.3 class, solid core, 5:2500 turns transformer). In each case, data are taken for three channels over one cycle of the measured waveform and the RMS input-referred signal is compared to the output to calculate the error. The equation used to derive the measurement error is shown in Equation 12. Data are taken using both the 2.4-V and 4-V internal reference voltages. In all cases, measured accuracy is within ±1%.

$$\text{Measurement Accuracy(\%)} = \left(\frac{\text{Measured} - \text{Actual}}{\text{Actual}}\right) \times 100 \tag{12}$$



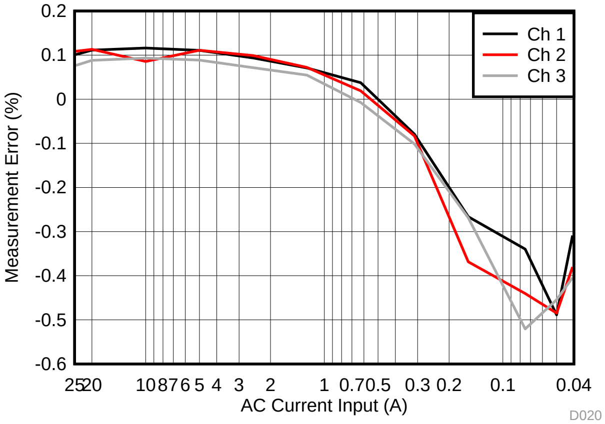
One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 2.4 V, measurement accuracy is absolute value

Figure 61. Input Voltage vs ADC Measurement Error: 2.4-V Reference



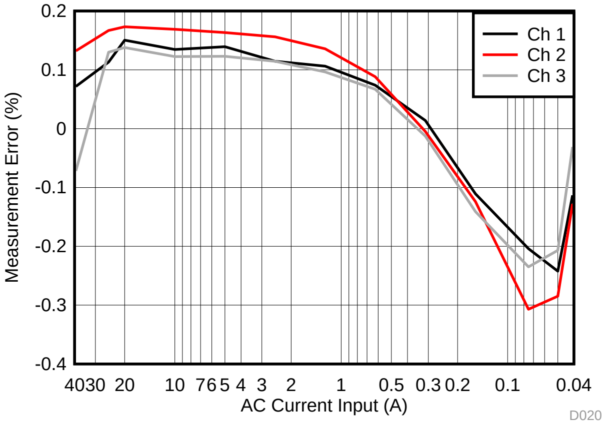
One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 4 V, measurement accuracy is absolute value

Figure 62. Input Voltage vs ADC Measurement Error: 4-V Reference



One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 2.4 V

Figure 63. Input Current vs ADC Measurement Error: 2.4-V Reference



One 50-Hz line cycle , 4-kSPS data rate, 80 samples, gain = 2, V_{REF} = 4 V

Figure 64. Input Current vs ADC measurement Error: 4-V Reference

For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see *High Resolution, Fast Startup Analog Front End for Air Circuit Breaker Design Guide* (TIDUB80).

10.3 Initialization Set Up

10.3.1 Setting the Device Up for Basic Data Capture

This section outlines the procedure to configure the device to capture data. Follow the steps shown in Figure 65 to put the ADS131E08S in a configured state to acquire data within the specified 3-ms power-up time. For details on the timings for commands, see the appropriate sections in this document. The flow chart of Figure 65 details the initial ADS131E08S configuration and setup.

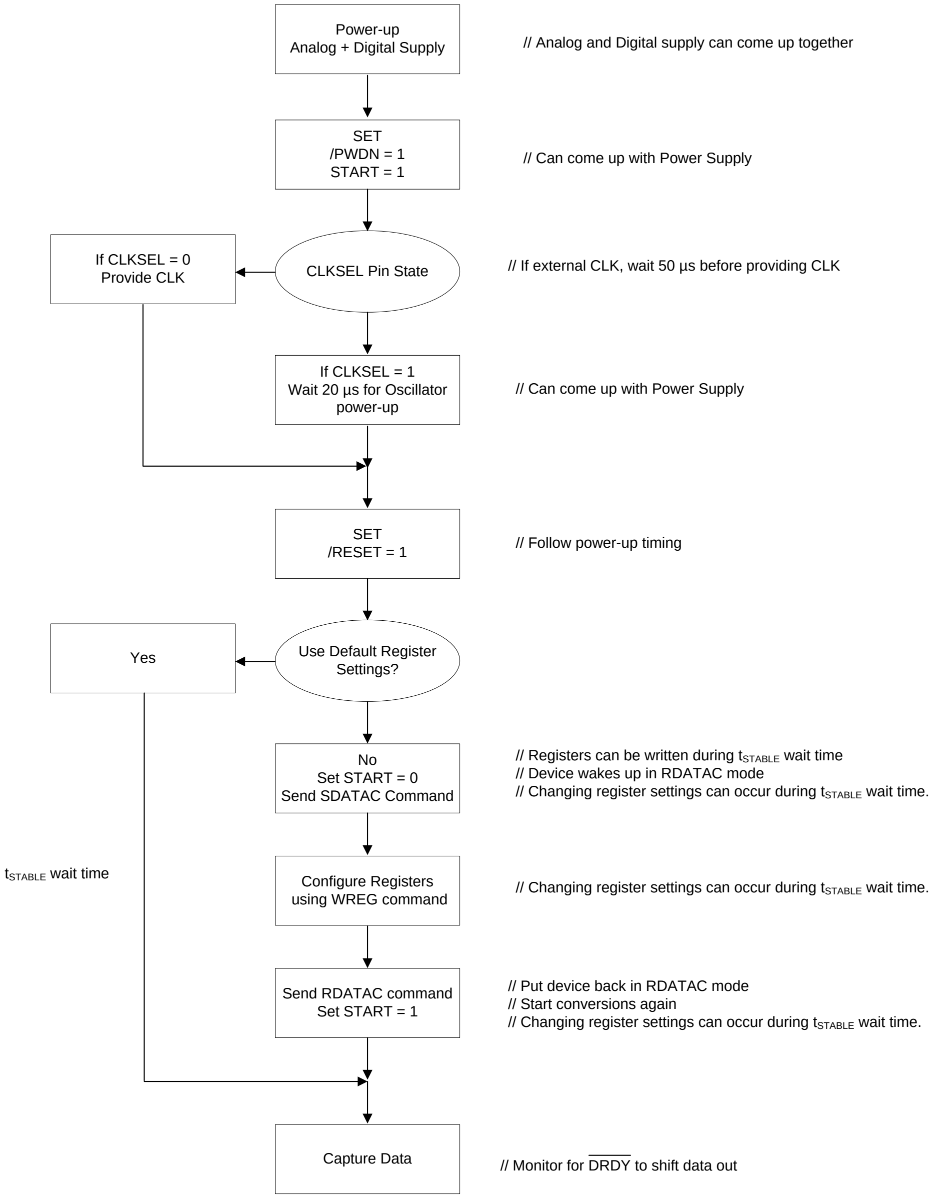


Figure 65. Initial Flow at Power-Up

11 Power Supply Recommendations

11.1 Power-Up Timing

Settled data from the ADS131E08S are available within 3 ms of power-up if a strict timing sequence is followed. Before device power-up, all digital and analog inputs must be held low. Provide the master clock 50 µs after the analog and digital supplies reach 90% of their nominal values, shown as t_{PCLK} in Figure 66. Pull the $\overline{\text{RESET}}$ pin high following the t_{PRST} timing to bring the ADC digital filters out of a reset state and to begin the conversion process.

Settled data are available at the first $\overline{\text{DRDY}}$ falling edge, shown as t_{SETTLE} in Figure 66. These data are from the settled digital filter; however, the first data set may not be a settled representation of the input because additional time is required for the reference and critical voltage nodes to settle to their final values. The t_{STABLE} timing adds the recommended wait time for settled data to be available at the ADC output. When the t_{STABLE} time has passed, the next $\overline{\text{DRDY}}$ falling edge indicates a valid conversion result of the input signal where both the digital filter and node voltages are settled.

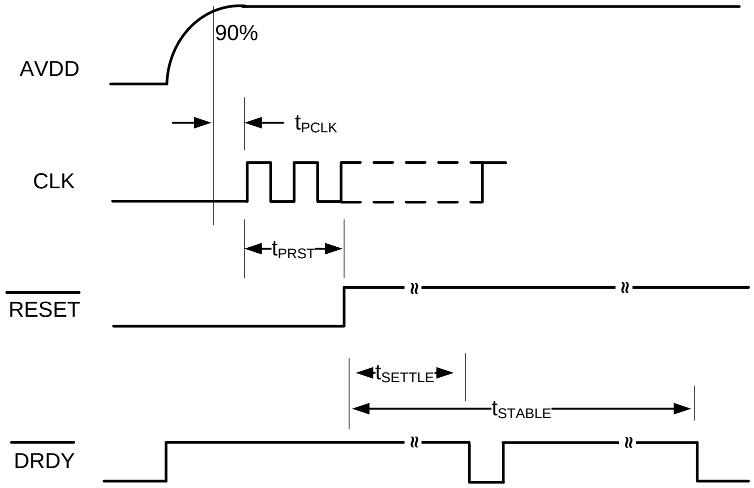


Figure 66. Power-Up Timing Diagram

Table 22. Power-Up Sequence Timing

		MIN	TYP	MAX	UNIT
t_{PCLK}	Delay time, first external CLK rising edge after AVDD reaches 90%	50			µs
	Delay time, internal oscillator start-up after AVDD reaches 90%	20			
t_{PRST}	Delay time, $\overline{\text{RESET}}$ rising edge after first CLK rising edge	2			t_{CLK}
t_{SETTLE}	Settling time, first settled data after $\overline{\text{RESET}}$ rising edge(1)	2312			t_{CLK}
t_{STABLE}	Settling time, valid data after $\overline{\text{RESET}}$ rising edge	2.2			ms

(1) Timing is for the 4-kSPS data rate; see Table 5 for digital filter settling times for different data rates.

To deviate from the default register settings, write to the ADS131E08S registers after pulling the $\overline{\text{RESET}}$ pin high. Changes to any of the registers delay the t_{SETTLE} start point until the register write is complete. If the data rate is changed following the $\overline{\text{RESET}}$ pin going high, the t_{SETTLE} timing takes on the settling characteristics of Table 5 relative to the completion of the command.

11.2 Recommended External Capacitor Values

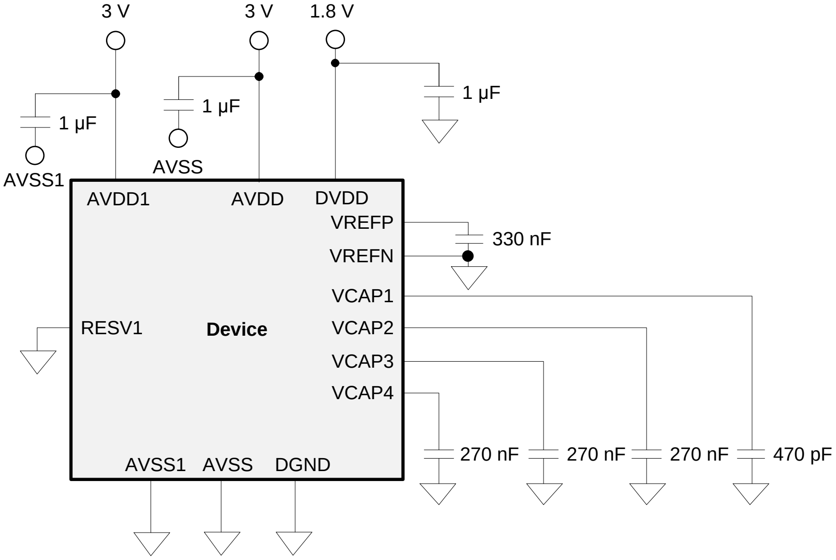
The ADS131E08S power-up time is set by the time required for the critical voltage nodes to settle to their final values. The analog supplies (AVDD and AVSS), digital supply (DVDD), and internal node voltages (VCAPx pins) must be up and stable when the data converter samples are taken to ensure performance. The combined current sourcing capability of the supplies and size of the bypass capacitors dictate the ramp rate of AVDD, AVSS, and DVDD. The VCAPx voltages are charged internally using the supply voltages. Table 23 lists the internal node voltages, their function, and recommended capacitor values to optimize the power-up time.

Table 23. Recommended External Capacitor Values

PIN		FUNCTION	RECOMMENDED CAPACITOR VALUE
NAME	NO.		
VCAP1	28	Band-gap voltage for the ADC	470 pF to AVSS
VCAP2	30	Modulator common-mode	270 nF to AVSS
VCAP3	55	PGA charge pump	270 nF to AVSS
VCAP4	26	Reference common-mode	270 nF to AVSS
VREFP	24	Reference voltage after the internal buffer	330 nF to AVSS
AVDD	19, 21, 22, 56, 59	Analog supply	1 µF each to AVSS
AVDD1	54	Internal PGA charge pump analog supply	1 µF to AVSS1
AVSS	20, 23, 32, 57, 58	Analog supply	1 µF each to AVDD
AVSS1	53	Internal PGA charge pump analog supply	1 µF to AVDD1
DVDD	48, 50	Digital supply	1 µF each to DGND

11.3 Device Connections for Unipolar Power Supplies

Figure 67 shows the ADS131E08S connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to the analog ground (AVSS) and the digital supply (DVDD) is referenced to the digital ground (DGND). The ADS131E08S supports an analog supply range of AVDD = 2.7 V to 5.25 V when operated in unipolar supply mode.

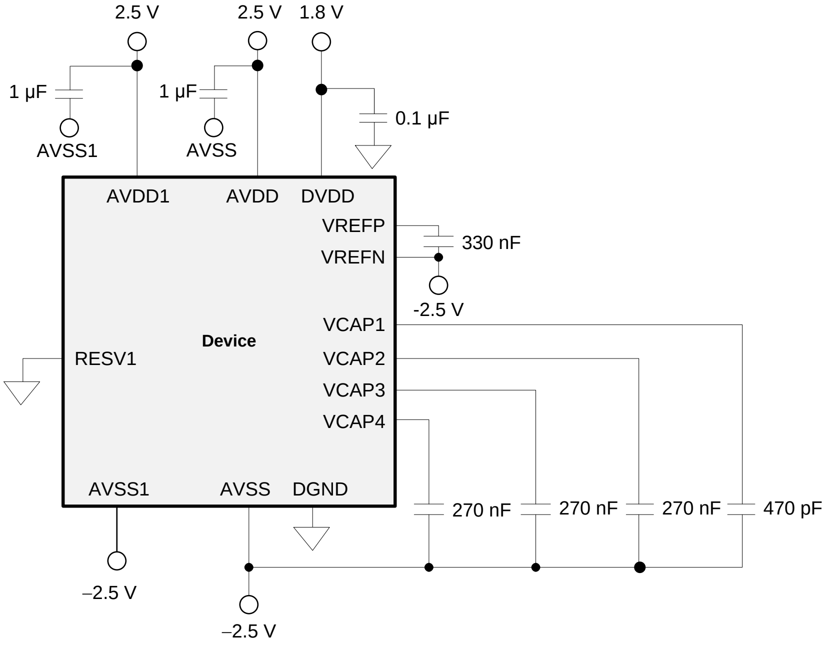


NOTE: Place the supply, reference, and VCAP1 to VCAP4 capacitors as close to the package as possible.

Figure 67. Unipolar Power Supply Operation

11.4 Device Connections for Bipolar Power Supplies

Figure 68 shows the ADS131E08S connected to a bipolar supply. In this example, the analog supply (AVDD) is referenced to the analog ground (AVSS) and the digital supply (DVDD) is referenced to the digital ground (DGND). The ADS131E08S supports an analog supply range of AVDD and AVSS = ±1.5 V to ±2.5 V when operated in bipolar supply mode.



NOTE: Place the supply, reference, and VCAP1 to VCAP4 capacitors as close to the package as possible.

Figure 68. Bipolar Power Supply Operation

12 Layout

12.1 Layout Guidelines

Use a low-impedance connection for ground so that return currents flow undisturbed back to their respective sources. For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. Keep connections to the ground plane as short and direct as possible. When using vias to connect to the ground layer, use multiple vias in parallel to reduce impedance to ground.

A mixed-signal layout sometimes incorporates separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital, and power-supply components are properly placed. Proper placement of components partitions the analog, digital, and power-supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. If ground plane separation is necessary, then make the connection at the ADC. Connecting individual ground planes at multiple locations creates ground loops, and is not recommended. A single ground plane for analog and digital avoids ground loops.

Bypass supply pins with a low-equivalent series resistance (ESR) ceramic capacitor. The placement of the bypass capacitors must be as close as possible to the supply pins using short, direct traces. For optimum performance, the ground-side connections of the bypass capacitors must also be low-impedance connections. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective (also known as a Kelvin connection). If multiple ADCs are on the same PCB, use wide power-supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs.

If external filtering is used for the analog inputs, use C0G-type ceramic capacitors when possible. C0G capacitors have stable properties and low-noise characteristics. Ideally, route differential signals as pairs to minimize the loop area between the traces. Route digital circuit traces (such as clock signals) away from all analog pins. The internal reference output return shares the same pin as the AVSS power supply. To minimize coupling between the power-supply trace and reference return trace, route the two traces separately; ideally, as a star connection at the AVSS pin.

Short, direct interconnections must be made on analog input lines and stray wiring capacitance must be avoided, particularly between the analog input pins and AVSS. These analog input pins are high-impedance and are extremely sensitive to extraneous noise. Treat the AVSS pin as a sensitive analog signal and connect directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS131E08S if shielding is not implemented. Keep digital signals as far as possible from the analog input signals on the PCB.

The SCLK input of the serial interface must be free from noise and glitches. Even with relatively slow SCLK frequencies, short digital signal rise and fall times can cause excessive ringing and noise. For best performance, keep the digital signal traces short, using termination resistors as needed, and make sure all digital signals are routed directly above the ground plane with minimal use of vias. Figure 69 shows the ideal placement of system components.

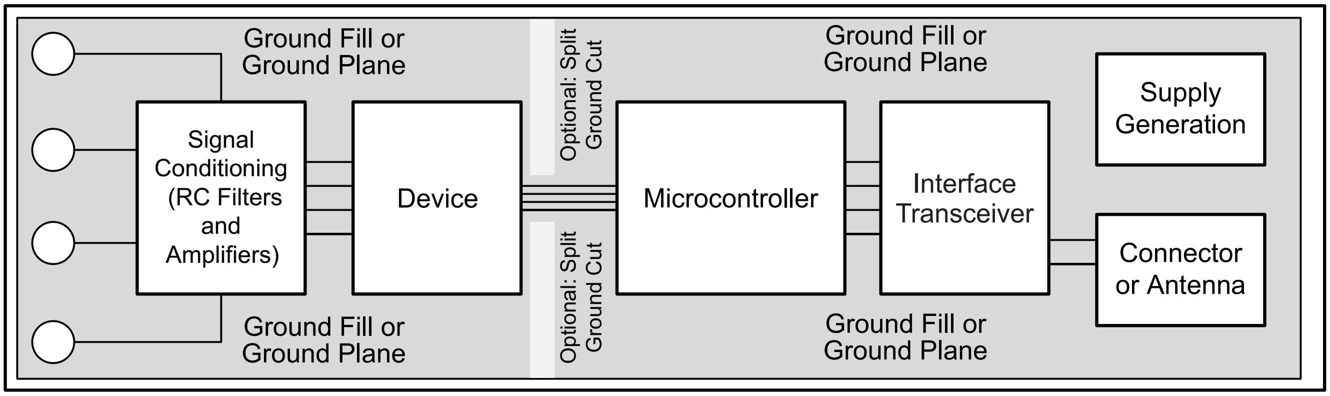


Figure 69. System Component Placement

12.2 Layout Example

Figure 70 shows an example layout of the ADS131E08S requiring a minimum of two PCB layers. The example circuit is shown for either a unipolar analog supply connection or a bipolar analog supply connection. In this example, polygon pours are used as supply connections around the device. If a three- or four-layer PCB is used, the additional inner layers can be dedicated to route power traces. The PCB is partitioned with analog signals routed from the left, digital signals routed to the right, and power routed above and below the device.

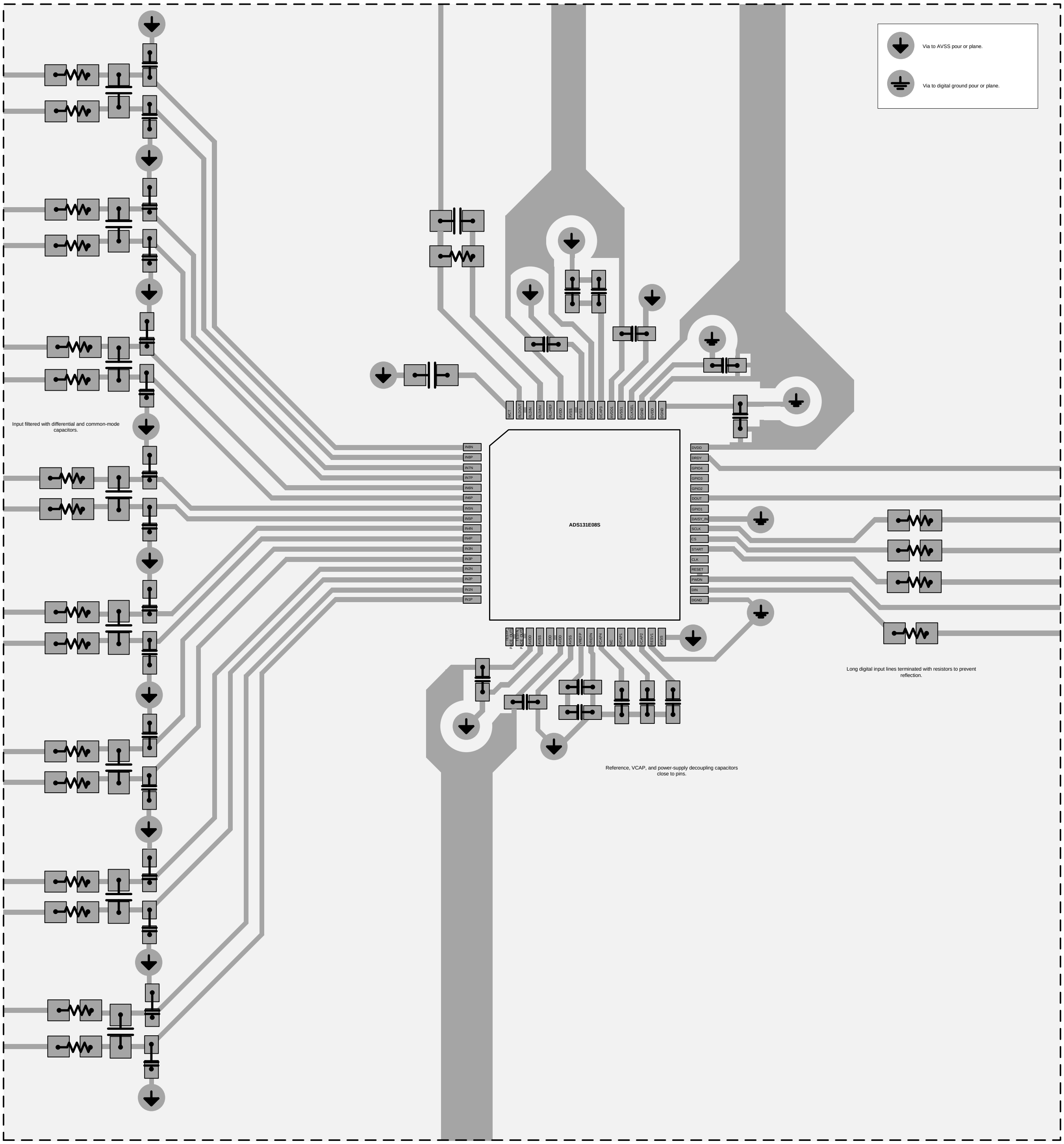


Figure 70. ADS131E08S Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

ADS131E04, ADS131E06, ADS131E08 Data Sheet, SBAS561

REF5025 Data Sheet,

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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13.3 Trademarks

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13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS131E08SPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08S	Samples
ADS131E08SPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS131E08S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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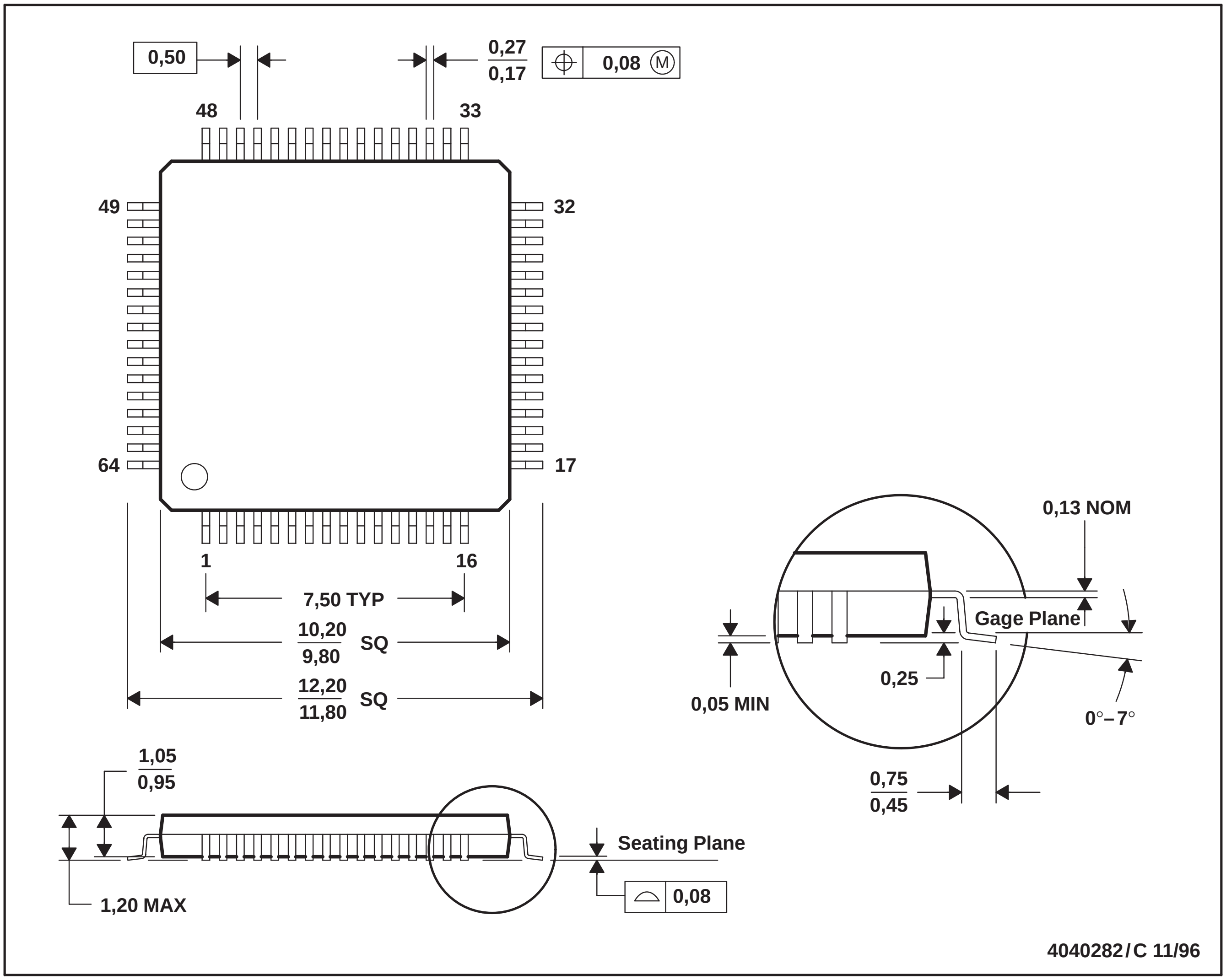

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B. This drawing is subject to change without notice.
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DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
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