Integrated, Quad RF Transceiver with Observation Path

Data Sheet

ADRV9010

FEATURES

4 differential transmitters
4 differential receivers
2 observation receivers with 2 inputs each
Center frequency
- **650 MHz to 3800 MHz (ADRV9010BBCZ)**
- **650 MHz to 6000 MHz (ADRV9010BBCZ-A)**

Maximum receiver bandwidth: 200 MHz
Maximum transmitter bandwidth: 200 MHz
Maximum transmitter synthesis bandwidth: 450 MHz
Maximum observation receiver bandwidth: 450 MHz
Fully integrated independent fractional-N radio frequency synthesizers
Fully integrated clock synthesizer
Multichip phase synchronization for all local oscillators and baseband clocks
JESD204B/JESD204C digital interface

APPLICATIONS

3G/4G/5G TDD macro and small cell base stations
TDD active antenna systems for advanced LTE and 5G

GENERAL DESCRIPTION

The ADRV9010 is a highly integrated, radio frequency (RF) agile transceiver that offers four independently controlled transmitters, dedicated observation receiver inputs for monitoring each transmitter channel, four independently controlled receivers, integrated synthesizers, and digital signal processing functions to provide a complete transceiver solution. The device provides the high radio performance and low power consumption demanded by cellular infrastructure applications such as TDD-based small cell base station radios, macro 3G/4G/5G TDD systems, and TDD based massive multiple in/multiple out (MIMO) base stations. The ADRV9010BBCZ operates from 650 MHz to 3800 MHz, covering most of the licensed and unlicensed cellular bands. The ADRV9010BBCZ-A operates from 650 MHz to 6000 MHz.

The receiver subsystem consists of four independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The four independent transmitters use an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise. The ADRV9010 device also includes two wide bandwidth, time shared observation path receivers with two inputs each for monitoring transmitter outputs.

The complete transceiver subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, eliminating the need for these functions in the digital baseband. Other auxiliary functions such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose input/outputs (GPIOs) that provide an array of digital control options are also integrated.

To achieve a high level of RF performance, the transceiver includes five fully integrated phase-locked loops (PLLs). Two PLLs provide high performance, low power fractional-N RF synthesis for the transmitter and receiver signal paths. One fully integrated PLL also supports an independent local oscillator (LO) mode for the observation receiver. Another PLL generates the clocks needed for the converters and digital circuits and a fifth PLL provides the clock for the serial data interface. A multichip synchronization mechanism synchronizes the phases of all LOs and baseband clocks between multiple ADRV9010 chips. All voltage controlled oscillators (VCOs) and loop filter components are integrated and adjustable through the digital control interface.

The serial data interface consists of eight serializer lanes and eight deserializer lanes. The interface supports both the JESD204B and JESD204C standards, operating at data rates up to 16.22016 Gbps. The interface also supports interleaved mode for lower bandwidths, thus reducing the number of high speed data interface lanes to one. Both fixed and floating-point data formats are supported. The floating-point format allows internal automatic gain control (AGC) to be invisible to the demodulator device.

The ADRV9010 is powered directly from 1.0 V, 1.3 V, and 1.8 V regulators and is controlled via a standard serial peripheral interface (SPI). Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9010 is packaged in a 14 mm × 14 mm, 289-ball chip scale ball grid array (CSP_BGA).

Rev. E **Document Feedback**

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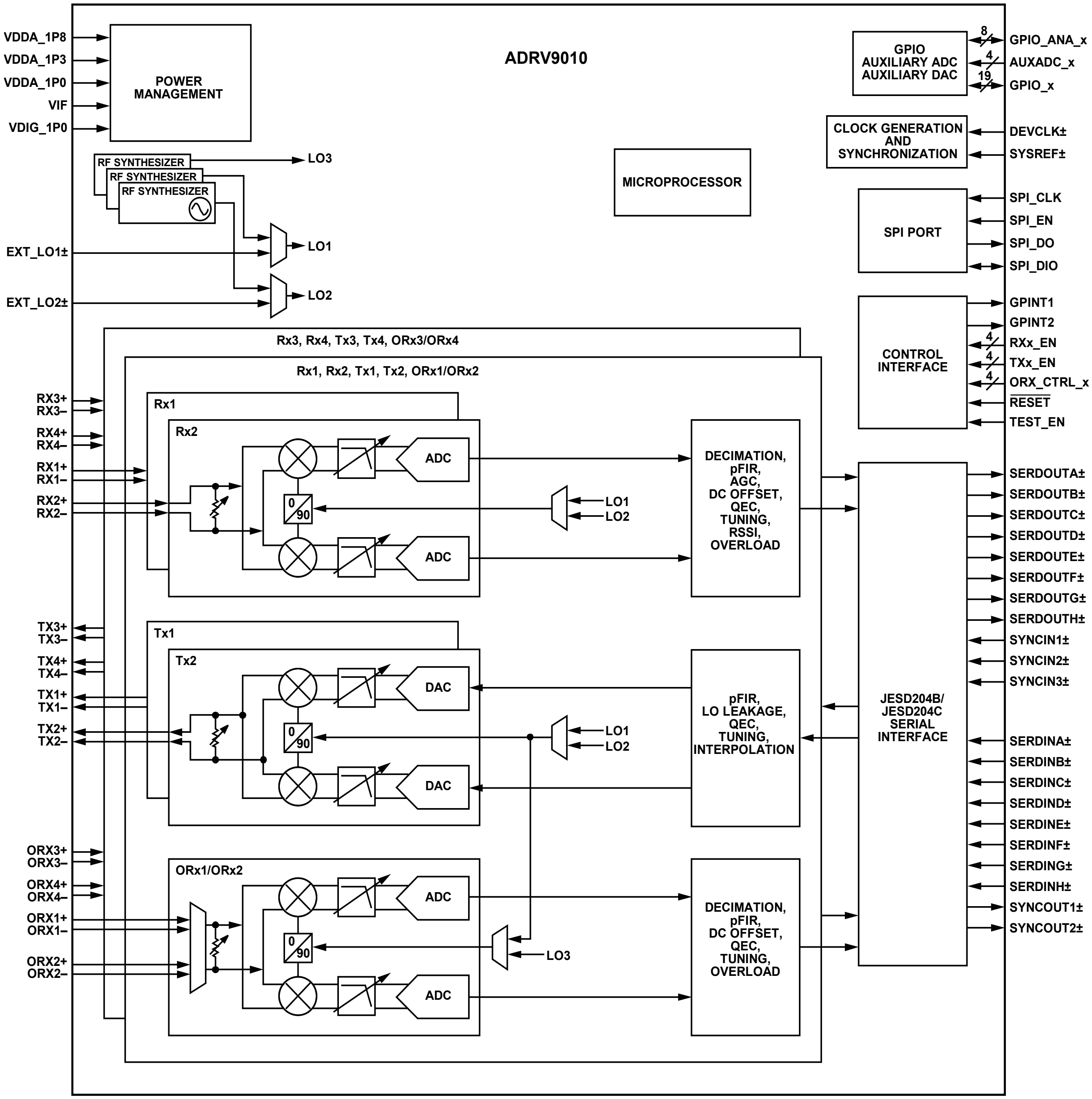
REVISION HISTORY

1/2021—Revision E: Initial Version

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. VDDA_1P8 REPRESENTS VCONV1_1P8, VCONV2_1P8, VANA1_1P8, VANA2_1P8, VANA3_1P8, VANA4_1P8, AND VJVCO_1P8.
VDDA_1P3 REPRESENTS VANA1_1P3, VANA2_1P3, VCONV1_1P3, VCONV2_1P3, VRFVCO1_1P3, VRFVCO2_1P3, VAUXVCO_1P3, VCLKVCO_1P3, VRFSYN1_1P3, VRFSYN2_1P3, VCLKSYN_1P3, VAUXSYN_1P3, VRXLO_1P3, AND VTXLO_1P3.
VDDA_1P0 REPRESENTS VJSYN_1P0, VDES_1P0, VTT_DES, AND VSER_1P0.

20043-001

Figure 1.

SPECIFICATIONS

All specifications are verified using a Wenzel Associates Model 500-23867, 245.76 MHz voltage controlled crystal oscillator (VCXO) as the device clock, unless otherwise noted. Specifications are applicable over the lifetime of the device. Power supplies are as follows: VDDA_1P8 = 1.8 V, VIF = 1.8 V, VDDA_1P3 = 1.3 V, VDDA_1P0 = 1.0 V, and VDIG_1P0 = 1.0 V. VDDA_1P8 represents VCONV1_1P8, VCONV2_1P8, VANA1_1P8, VANA2_1P8, VANA3_1P8, VANA4_1P8, and VJVCO_1P8. VDDA_1P3 represents VANA1_1P3, VANA2_1P3, VCONV1_1P3, VCONV2_1P3, VRFVCO1_1P3, VRFVCO2_1P3, VAUXVCO_1P3, VCLKVCO_1P3, VRFSYN1_1P3, VRFSYN2_1P3, VCLKSYN_1P3, VAUXSYN_1P3, VRXLO_1P3, and VTXLO_1P3. VDDA_1P0 represents VJSYN_1P0, VDES_1P0, VTT_DES, and VSER_1P0. All RF specifications are based on measurements that include printed circuit board (PCB) and matching circuit losses, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMITTERS (Tx)						
Center Frequency						
		650		3800	MHz	ADRV9010BBCZ
		650		6000	MHz	ADRV9010BBCZ-A
Tx Synthesis Bandwidth				450	MHz	Wider bandwidth for use in digital processing algorithms
Tx Large Signal Bandwidth				200	MHz	Zero-IF mode
Peak-to-Peak Gain Deviation			1.0		dB	450 MHz bandwidth, includes compensation by programmable finite impulse response (pFIR) filter
			0.1		dB	Any 20 MHz bandwidth span within the large signal bandwidth, includes compensation by pFIR filter
Deviation from Linear Phase			1		Degrees	450 MHz bandwidth
Maximum Output Power						0 dBFS, 1 MHz signal input, 50 Ω load, 0 dB Tx attenuation
800 MHz			6.4		dBm	
1800 MHz			6.0		dBm	
2600 MHz			6.1		dBm	
3800 MHz			6.5		dBm	
4800 MHz			6.0		dBm	
5700 MHz			5.7		dBm	
Power Control Range			32		dB	
Power Control Resolution			0.05		dB	
Attenuation Accuracy						
Integral Nonlinearity (Gain)	INL		0.1		dB	Valid over full power control range for any 4 dB step
Differential Nonlinearity (Gain)	DNL		±0.04		dB	Monotonic
Output Power Temperature Slope			−4.5		mdB/°C	Valid over full power control range
LO Delay Temperature Slope			1.05		ps/°C	Valid over full power control range

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Adjacent Channel Leakage Power Ratio (ACLR) Long Term Evolution (LTE)						20 MHz LTE at −12 dBFS
800 MHz			−67		dB	
1800 MHz			−67		dB	
2600 MHz			−67		dB	
3800 MHz			−67		dB	
4800 MHz			−65		dB	
5700 MHz			−65		dB	
Inband Noise Floor			−154.5		dBFS/Hz	0 dB attenuation, inband noise falls 1 dB for each decibel of attenuation for attenuation settings between 0 dB and 20 dB
Interpolation Images			−76		dBc	
Tx to Tx Isolation: All Tx Output Effects on All Other Tx Outputs						
800 MHz			80		dB	
1800 MHz			76		dB	
2600 MHz			74		dB	
3800 MHz			70		dB	
4800 MHz			70		dB	
5700 MHz			64		dB	
Image Rejection						
Within Large Signal Bandwidth						QEC active up to 20 dB of attenuation, continuous wave (CW) tone swept across the large signal bandwidth
800 MHz			75		dB	
1800 MHz			75		dB	
2600 MHz			76		dB	
3800 MHz			65		dB	
4800 MHz			65		dB	
5700 MHz			61		dB	
Beyond Large Signal Bandwidth						Assumes that distortion power density is 25 dB less than the desired power density
800 MHz			40		dB	
1800 MHz			38		dB	
2600 MHz			34		dB	
3800 MHz			37		dB	
4800 MHz			37		dB	
5700 MHz			37		dB	
Output Impedance	Z_{OUT}		50		Ω	Differential and nominal
Maximum Output Load Voltage Standing Wave Ratio (VSWR)				3		Maximum value to ensure adequate calibration
Output Return Loss			10		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Third-Order Intercept Point	OIP3					0 dB Tx attenuation, 90 MHz and 95 MHz tones
800 MHz			30		dBm	
1800 MHz			30		dBm	
2600 MHz			29		dBm	
3800 MHz			27		dBm	
4800 MHz			27		dBm	
5700 MHz			27		dBm	
Carrier Leakage						With LO leakage correction active, 0 dB Tx attenuation; scales dB for dB with attenuation
Carrier Offset from LO			−82		dBFS/MHz	
Carrier on the LO			−71		dBFS/MHz	Measured using an LTE 20 MHz signal
Error Vector Magnitude	EVM					PLL optimized for narrow-band noise, measured using LTE 20 MHz signal
800 MHz			0.36		%	50 kHz PLL bandwidth
1800 MHz			0.60		%	50 kHz PLL bandwidth
2600 MHz			0.42		%	500 kHz PLL bandwidth
3800 MHz			0.50		%	200 kHz PLL bandwidth
4800 MHz			0.67		%	400 kHz PLL bandwidth
5700 MHz			0.84		%	500 kHz PLL bandwidth
Transmitter TDD Parameters						
Time from SPI_EN Going High to Change in Tx Attenuation	t_{SCH}		12		ns	
Time Between Consecutive Microattenuation Steps	t_{ACH}		20		ns	A large change in attenuation may be broken up into a series of smaller attenuation changes
Attenuation Overshoot During Transition			0.1		dB	
Change in Attenuation per Microstep			0.1		dB	
RECEIVERS (Rx)						
Center Frequency						
		650		3800	MHz	ADRV9010BBCZ
		650		6000	MHz	ADRV9010BBCZ-A
Gain Range			30		dB	
Attenuation Accuracy						
Analog Gain Step			0.5		dB	Attenuator steps from 0 dB to 6 dB
			1		dB	Attenuator steps from 6 dB to 30 dB
Residual Gain Step Error			0.1		dB	
Gain Temperature Slope			−6.4		mdB/°C	
Internal LO Delay Temperature Slope			1.0		ps/°C	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Frequency Response						
Peak-to-Peak Gain Deviation			1		dB	200 MHz bandwidth, includes compensation by pFIR filter
			0.2		dB	Any 20 MHz span, includes compensation by pFIR filter
Rx Bandwidth				200	MHz	
Rx Alias Band Rejection		80			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					This CW signal level corresponds to the signal level seen at the matching circuit input that produces −2 dBFS at the digital output with 0 dB channel attenuation
800 MHz			−12.7		dBm	
1800 MHz			−12.2		dBm	
2600 MHz			−12		dBm	
3800 MHz			−12		dBm	
4800 MHz			−11.3		dBm	
5700 MHz			−10.3		dBm	
Maximum Source VSWR				3		
Input Impedance	Z_{IN}		100		Ω	Differential
Input Port Return Loss			10		dB	
Noise Figure						0 dB attenuation at Rx port
800 MHz			11		dB	
1800 MHz			11.5		dB	
2600 MHz			11.9		dB	
3800 MHz			12		dB	
4800 MHz			12.5		dB	
5700 MHz			14.5		dB	
Noise Figure Ripple			1.5		dB	At band edge
Second-Order Input Intermodulation Intercept Point	IIP2					0 dB attenuation, complex
800 MHz			65		dBm	
1800 MHz			65		dBm	
2600 MHz			68		dBm	
3800 MHz			62		dBm	
4800 MHz			58		dBm	
5700 MHz			58		dBm	
Third-Order Input Intermodulation Intercept Point, Difference Product						
Wideband	$WB\text{-}IIP3_{DIFF}$					Two tones near the band edge; P_{HIGH} − 9 dB per tone
800 MHz			14.5		dBm	
1800 MHz			17		dBm	
2600 MHz			17		dBm	
3800 MHz			16.5		dBm	
4800 MHz			17		dBm	
5700 MHz			18		dBm	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Midband	$MB\text{-}IIP3_{DIFF}$					Two tones near middle of the band; P_{HIGH} − 9 dB per tone
800 MHz			18.8		dBm	
1800 MHz			27		dBm	
2600 MHz			22		dBm	
3800 MHz			22		dBm	
4800 MHz			22		dBm	
5700 MHz			20		dBm	
Wideband	$WB\text{-}IIP3_{SUM}$					Two tones approximately bandwidth/6 offset from the LO; P_{HIGH} − 9 dB per tone
800 MHz			18		dBm	
1800 MHz			20		dBm	
2600 MHz			21		dBm	
3800 MHz			23		dBm	
4800 MHz			22		dBm	
5700 MHz			22		dBm	
Second-Order Harmonic Distortion						
Maximum Input	$HD2_{MAX}$		−72		dBc	P_{HIGH} CW signal, harmonic distortion tones falling within 100 MHz of the LO
Recommended Input	HD2		−75		dBc	P_{HIGH} − 3 dB CW signal, harmonic distortion tones falling within 100 MHz of the LO
Third-Order Harmonic Distortion						
Maximum Input	$HD3_{MAX}$		−66		dBc	P_{HIGH} CW signal, harmonic distortion tones falling within 100 MHz of the LO
Recommended Input	HD3		−72		dBc	P_{HIGH} − 3 dB CW signal, harmonic distortion tones falling within 100 MHz of the LO
Fourth-Order Harmonic Distortion						
Maximum Input	$HD4_{MAX}$		−90		dBc	P_{HIGH} CW signal, harmonic distortion tones falling within 100 MHz of the LO
Recommended Input	HD4		−90		dBc	P_{HIGH} − 3 dB CW signal, harmonic distortion tones falling within 100 MHz of the LO
Fifth-Order Harmonic Distortion						
Maximum Input	$HD5_{MAX}$		−87		dBc	P_{HIGH} CW signal, harmonic distortion tones falling within 100 MHz of the LO
Recommended Input	HD5		−90		dBc	P_{HIGH} − 3 dB CW signal, harmonic distortion tones falling within 100 MHz of the LO
Image Rejection			75		dB	QEC active, within 200 MHz Rx bandwith
Rx to Rx Signal Isolation						
800 MHz			75		dB	
1800 MHz			69		dB	
2600 MHz			69		dB	
3800 MHz			64		dB	
4800 MHz			61		dB	
5700 MHz			58		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rx Band Spurs Referenced to RF Input at Maximum Gain			−95		dBm	No more than one spur at this level per 10 MHz of Rx bandwidth; excludes converter clock spurs; no input signal applied
Spurious-Free Dynamic Range	SFDR		81		dBc	P_{HIGH} CW signal anywhere inside the band ±20 MHz, excludes harmonic distortion products
Rx Input LO Leakage at Maximum Gain						Leakage decreased dB for dB with attenuation for first 12 dB
800 MHz			−65		dBm	
1800 MHz			−63		dBm	
2600 MHz			−65		dBm	
3800 MHz			−59		dBm	
4800 MHz			−53		dBm	
5700 MHz			−55		dBm	
Tx to Rx Signal Isolation						All Tx output effects on all Rx inputs
800 MHz			80		dB	
1800 MHz			73		dB	
2600 MHz			73		dB	
3800 MHz			72		dB	
4800 MHz			68		dB	
5700 MHz			66		dB	
OBSERVATION RECEIVER (ORx)						
Center Frequency						
		650		3800	MHz	ADRV9010BBCZ
		650		6000	MHz	ADRV9010BBCZ-A
Gain Range			30		dB	
Analog Gain Step			0.5		dB	For attenuator steps from 0 dB to 6 dB
Peak-to-Peak Gain Deviation			1		dB	450 MHz RF bandwidth, compensation by pFIR filter
			0.1		dB	Any 20 MHz bandwidth span, compensation by pFIR filter
Deviation from Linear Phase			1		Degrees	450 MHz RF bandwidth
ORx Bandwidth				450	MHz	
ORx Alias Band Rejection		60			dB	Due to digital filters
Maximum Useable Input Level	P_{HIGH}					This CW signal level corresponds to the signal level seen at the matching circuit input that produces −2 dBFS at the digital output with 0 dB channel attenuation
800 MHz			−12.7		dBm	
1800 MHz			−12.2		dBm	
2600 MHz			−10.6		dBm	
3800 MHz			−12.0		dBm	
4800 MHz			−11.3		dBm	
5700 MHz			−9.0		dBm	
Input Impedance	Z_{IN}		100		Ω	Differential
Input Source VSWR				3		
Input Port Return Loss			10		dB	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Integrated Noise						
450 MHz Bandwidth			−58.5		dBFS	Sample rate at maximum value integrated from 500 kHz to 225 MHz, no input signal
491.52 MHz Bandwidth (Nyquist)			−57.5		dBFS	Sample rate at maximum value integrated from 500 kHz to 245.76 MHz, no input signal
Second-Order Input Intermodulation Intercept Point	IIP2					Maximum ORx gain; P_{HIGH} − 11 dB per tone
800 MHz			53		dBm	
1800 MHz			53		dBm	
2600 MHz			65		dBm	
3800 MHz			48		dBm	
4800 MHz			45		dBm	
5700 MHz			55		dBm	
Third-Order Input Intermodulation Intercept Point						Maximum ORx gain; P_{HIGH} − 11 dB per tone
Narrow Band	$IIP3_{NB}$					IM3 product < 130 MHz at baseband; P_{HIGH} − 11 dB per tone, 491.52 MSPS
800 MHz			12		dBm	
1800 MHz			15		dBm	
2600 MHz			18		dBm	
3800 MHz			17		dBm	
4800 MHz			17		dBm	
5700 MHz			18		dBm	
Wide Band	$IIP3_{WB}$					IM3 products > 130 MHz at baseband; P_{HIGH} − 11 dB per tone, 491.52 MSPS
800 MHz			9		dBm	
1800 MHz			12		dBm	
2600 MHz			12		dBm	
3800 MHz			11		dBm	
4800 MHz			11		dBm	
5700 MHz			13		dBm	
Third-Order Intermodulation Product						
Narrow Band	$IM3_{NB}$					IM3 product < 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−71.5		dBc	
1800 MHz			−76.5		dBc	
2600 MHz			−80		dBc	
3800 MHz			−80		dBc	
4800 MHz			−77		dBc	
5700 MHz			−76		dBc	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Wide Band	$IM3_{WB}$					IM3 product > 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−65.5		dBc	
1800 MHz			−70.5		dBc	
2600 MHz			−67		dBc	
3800 MHz			−68		dBc	
4800 MHz			−65		dBc	
5700 MHz			−66		dBc	
Fifth-Order Intermodulation Product						
Narrow Band	$IM5_{NB}$					IM5 product < 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−91		dBc	
1800 MHz			−96		dBc	
2600 MHz			−85		dBc	
3800 MHz			−82		dBc	
4800 MHz			−82		dBc	
5700 MHz			−78		dBc	
Wide Band	$IM5_{WB}$					IM5 product > 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−87		dBc	
1800 MHz			−85		dBc	
2600 MHz			−85		dBc	
3800 MHz			−73		dBc	
4800 MHz			−73		dBc	
5700 MHz			−78		dBc	
Seventh-Order Intermodulation Product						
Narrow Band	$IM7_{NB}$					IM7 product < 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−74		dBc	
1800 MHz			−79		dBc	
2600 MHz			−77		dBc	
3800 MHz			−71		dBc	
4800 MHz			−71		dBc	
5700 MHz			−74		dBc	
Wide Band	$IM7_{WB}$					IM7 product > 130 MHz at baseband; two tones, each at P_{HIGH} − 11 dB, 491.52 MSPS
800 MHz			−79		dBc	
1800 MHz			−79		dBc	
2600 MHz			−80		dBc	
3800 MHz			−71		dBc	
4800 MHz			−71		dBc	
5700 MHz			−84		dBc	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Spurious-Free Dynamic Range	SFDR		64		dB	Nonintermodulation related spurs; does not include harmonic distortion; input set at P_{HIGH} − 8 dB
Second-Order Harmonic Distortion	HD2					Input set at P_{HIGH} − 8 dB
Inband			−80		dBc	Inband harmonic distortion falls within ±100 MHz
Out of Band			−73		dBc	Out of band harmonic distortion falls within ±225 MHz
Third-Order Harmonic Distortion	HD3					Input set at P_{HIGH} − 8 dB
Inband			−70		dBc	Harmonic distortion falls within ±100 MHz
Out of Band			−65		dBc	Harmonic distortion falls within ±225 MHz
Image Rejection						After online tone calibration, QEC active
Within Large Signal Bandwidth			75		dB	
Outside Large Signal Bandwidth			75		dB	
Tx to ORx Signal Isolation						All Tx output effects on all ORx inputs
800 MHz			90		dB	
1800 MHz			85		dB	
2600 MHz			88		dB	
3800 MHz			88		dB	
4800 MHz			77		dB	
5700 MHz			76		dB	
LO SYNTHESIZER	LO1, LO2					
LO Frequency Step			7.3		Hz	1.6 GHz to 3.2 GHz, 245.76 MHz phase frequency detector (PFD) frequency
LO Spectral Purity			−80		dBc	
Integrated Phase Noise						Integrated from 1 kHz to 100 MHz
Narrow Bandwidth Optimized						PLL optimized to minimize phase noise at offsets > 200 kHz
800 MHz LO			0.12		°rms	
1800 MHz LO			0.27		°rms	
2600 MHz LO			0.66		°rms	
3800 MHz LO			0.53		°rms	
4800 MHz LO			0.91		°rms	
5700 MHz LO			1.57		°rms	
Wide Bandwidth Optimized						PLL bandwidth optimized for integrated phase noise and phase noise at offsets > 1 MHz
800 MHz LO			0.07		°rms	
1800 MHz LO			0.11		°rms	
2600 MHz LO			0.17		°rms	
3800 MHz LO			0.26		°rms	
4800 MHz LO			0.30		°rms	
5700 MHz LO			0.42		°rms	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Spot Phase Noise, Narrow Band						PLL optimized to minimize phase noise at offsets > 200 kHz
800 MHz LO						
100 kHz Offset			−115		dBc/Hz	
1 MHz Offset			−141		dBc/Hz	
10 MHz Offset			−162		dBc/Hz	
1800 MHz LO						
100 kHz Offset			−107		dBc/Hz	
200 kHz Offset			−115		dBc/Hz	
400 kHz Offset			−123		dBc/Hz	
600 kHz Offset			−128		dBc/Hz	
800 kHz Offset			−131		dBc/Hz	
1.2 MHz Offset			−136		dBc/Hz	
1.8 MHz Offset			−140		dBc/Hz	
6 MHz Offset			−151		dBc/Hz	
10 MHz Offset			−156		dBc/Hz	
2600 MHz LO						
100 kHz Offset			−97		dBc/Hz	
1 MHz Offset			−124		dBc/Hz	
10 MHz Offset			−150		dBc/Hz	
3800 MHz LO						
100 kHz Offset			−100		dBc/Hz	
1 MHz Offset			−126		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	
4800 MHz LO						
100 kHz Offset			−94		dBc/Hz	
1 MHz Offset			−120		dBc/Hz	
10 MHz Offset			−145		dBc/Hz	
5700 MHz LO						
100 kHz Offset			−89		dBc/Hz	
1 MHz Offset			−115		dBc/Hz	
10 MHz Offset			−141		dBc/Hz	
Spot Phase Noise, Wide Band						PLL bandwidth optimized for integrated phase noise and phase noise at offsets > 1 MHz
800 MHz LO						
100 kHz Offset			−114		dBc/Hz	
1 MHz Offset			−141		dBc/Hz	
10 MHz Offset			−162		dBc/Hz	
1800 MHz LO						
100 kHz Offset			−112		dBc/Hz	
1 MHz Offset			−133		dBc/Hz	
10 MHz Offset			−156		dBc/Hz	
2600 MHz LO						
100 kHz Offset			−112		dBc/Hz	
1 MHz Offset			−120		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	
3800 MHz LO						
100 kHz Offset			−104		dBc/Hz	
1 MHz Offset			−125		dBc/Hz	
10 MHz Offset			−149		dBc/Hz	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
4800 MHz LO						
100 kHz Offset			−106		dBc/Hz	
1 MHz Offset			−117		dBc/Hz	
10 MHz Offset			−144		dBc/Hz	
5700 MHz LO						
100 kHz Offset			−104		dBc/Hz	
1 MHz Offset			−112		dBc/Hz	
10 MHz Offset			−140		dBc/Hz	
AUXILIARY SYNTHESIZER	LO3					
LO Frequency Step			1.8		Hz	1.625 GHz to 3.25 GHz, 61.44 MHz PFD frequency
LO Spectral Purity			−65		dBc	$\|f_{RFLO} - f_{AUXLO}\|$[1] > 15 MHz
Integrated Phase Noise						Integrated from 1 kHz to 100 MHz, PLL bandwidth optimized for integrated phase noise
800 MHz LO			0.18		°rms	
1800 MHz LO			0.22		°rms	
2600 MHz LO			0.46		°rms	
3800 MHz LO			0.43		°rms	
4800 MHz LO			0.70		°rms	
5700 MHz LO			1.12		°rms	
Spot Phase Noise						
800 MHz LO						
100 kHz Offset			−112		dBc/Hz	
1 MHz Offset			−121		dBc/Hz	
10 MHz Offset			−141		dBc/Hz	
1800 MHz LO						
100 kHz Offset			−110		dBc/Hz	
1 MHz Offset			−120		dBc/Hz	
10 MHz Offset			−134		dBc/Hz	
2600 MHz LO						
100 kHz Offset			−103		dBc/Hz	
1 MHz Offset			−114		dBc/Hz	
10 MHz Offset			−132		dBc/Hz	
3800 MHz LO						
100 kHz Offset			−104		dBc/Hz	
1 MHz Offset			−114		dBc/Hz	
10 MHz Offset			−128		dBc/Hz	
4800 MHz LO						
100 kHz Offset			−100		dBc/Hz	
1 MHz Offset			−110		dBc/Hz	
10 MHz Offset			−127		dBc/Hz	
5700 MHz LO						
100 kHz Offset			−95		dBc/Hz	
1 MHz Offset			−106		dBc/Hz	
10 MHz Offset			−126		dBc/Hz	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LO PHASE SYNCHRONIZATION						
Initial Phase Synchronization Accuracy			0.9		ps	
EXTERNAL LO INPUT						
Input Frequency	f_{EXTLO}	1600		12000	MHz	Input frequency must be 2× the desired frequency for LO frequency (f_{LO})[2] ≥ 1 GHz and 4× the desired f_{LO} for f_{LO} < 1 GHz
Input Signal Power		−6	0	+6	dBm	50 Ω matching at the source
Input Signal Differential Phase Balance				15	Degrees	To ensure adequate quadrature error correction
Input Signal Differential Amplitude Balance				2	dB	
Input Signal Duty Cycle Error				2	%	
CLOCK SYNTHESIZER						
4915.2 MHz Sample Clock						
Integrated Phase Noise			0.69		°rms	1 kHz to 10 MHz, PLL bandwidth optimized for low jitter
Spot Phase Noise						PLL bandwidth optimized for integrated phase noise
100 kHz Offset			−96		dBc/Hz	
1 MHz Offset			−113		dBc/Hz	
10 MHz Offset			−140		dBc/Hz	
3932.16 MHz Sample Clock						
Integrated Phase Noise			0.89		°rms	1 kHz to 10 MHz, PLL bandwidth optimized to minimize phase noise at offsets > 200 kHz
Spot Phase Noise						PLL bandwidth optimized to minimize phase noise at offsets > 200 kHz
100 kHz Offset			−92		dBc/Hz	
1 MHz Offset			−120		dBc/Hz	
10 MHz Offset			−143		dBc/Hz	
REFERENCE CLOCK (DEVCLK± SIGNAL)						
Frequency Range		15		1000	MHz	
Signal Level (Differential)		0.2		1.0	V p-p	AC-coupled, common-mode voltage internally supplied; for best spurious performance and to meet the specified PLL performance parameters, use a 1 V p-p input clock
SYSTEM REFERENCE INPUTS	SYSREF+, SYSREF−					
Logic Compliance			LVDS/LVPECL			
Differential Input Voltage		400	800	1800	mV p-p	External 100 Ω termination
Input Common-Mode Voltage			0.675	2.0	V	
Input Resistance (Differential)			18		kΩ	
Input Capacitance (Differential)			1		pF	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AUXILIARY CONVERTERS						
ADC						
Resolution			10		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			0.95		V	
DAC						
Resolution			12		Bits	
Output Voltage: AUXDAC_0						
Minimum			0.2		V	
Maximum			VDDA_1P8 − 0.25		V	
Output Voltage: AUXDAC_1 to AUXDAC_7						
Minimum			0.1		V	
Maximum			VDDA_1P8 − 0.1		V	
Drive Capability			10		mA	
DIGITAL SPECIFICATIONS: SINGLE-ENDED SIGNALS						Applies to the following pins: GPIO_x, GPINTx, TXx_EN, RXx_EN, ORX_CTRL_x, TEST_EN, RESET, SPI_EN, SPI_CLK, SPI_DO, and SPI_DIO
Logic Inputs						
Input Voltage						
High Level		VIF × 0.65		VIF + 0.18	V	
Low Level		−0.30		VIF × 0.35	V	
Input Current						
High Level		−10		+10	μA	
Low Level		−10		+10	μA	
Logic Outputs						
Output Voltage						
High Level		VIF − 0.45			V	
Low Level				0.45	V	
Drive Capability			10		mA	
DIGITAL SPECIFICATIONS: DIFFERENTIAL SIGNALS						Applies to the SYNCINx± and SYNCOUTx± pins
Logic Inputs						
Input Voltage Range		825		1675	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	
Receiver Differential Input Impedance			100		Ω	Internal termination enabled

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Outputs						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Differential			225		mV	
Offset			1200		mV	
DIGITAL SPECIFICATIONS: VDDA_1P8 REFERENCED SIGNALS						Applies to the GPIO_ANA_x pin
Logic Inputs						
Input Voltage						
High Level		VDDA_1P8 × 0.65		VDDA_1P8 + 0.18	V	
Low Level		−0.30		VDDA_1P8 × 0.35	V	
Input Current						
High Level		−10		+10	µA	
Low Level		−10		+10	µA	
Logic Outputs						
Output Voltage						
High Level		VDDA_1P8 − 0.45			V	
Low Level				0.45	V	
Drive Capability			10		mA	

[1] f_{RFLO} is the frequency of the RF LO synthesizer and f_{AUXLO} is the frequency of the auxiliary synthesizer.
[2] f_{LO} is the frequency of the internal local oscillator generator.

POWER SUPPLY SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CHARACTERISTICS					Voltage range requirements must be met at each ball input for the respective voltage supply rail
VDDA_1P0 Supply	0.95	1.0	1.05	V	
VDIG_1P0 Supply	0.95	1.0	1.05	V	
VDDA_1P3 Supply	1.235	1.3	1.365	V	
VDDA_1P8 Supply	1.71	1.8	1.89	V	
VIF Supply	1.71	1.8	1.89	V	

CURRENT CONSUMPTION

TDD Operation (Typical Values)

Table 3. TDD Mode: 4 Rx Channels Enabled, Maximum Gain

Profile Conditions[1]	Supply (A)			Total Average Power (W)	75% Tx, 25% Rx Average Power (W)
	1.0 V	1.3 V	1.8 V		
USE CASE 26 NONLINK SHARING (16 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.750	2.197	0.241	5.048	5.456
USE CASE 14 LINK SHARING (12 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.570	2.184	0.271	4.907	5.491
USE CASE 47 LINK SHARING (16 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.409	2.210	0.245	4.731	5.134

[1] All current measurements made at room temperature without a heat sink.

Table 4. TDD Mode: 4 Tx and 1 ORx Channels Enabled, 0 dB Attenuation, Maximum Gain

Profile Conditions[1]	Supply (A)			Total Average Power (W)	75% Tx, 25% Rx Average Power (W)
	1.0 V	1.3 V	1.8 V		
USE CASE 26 NONLINK SHARING (16 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.731	2.088	0.633	5.592	5.456
USE CASE 14 LINK SHARING (12 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.796	2.061	0.668	5.686	5.491
USE CASE 47 LINK SHARING (16 BITS) 491.52 MSPS Tx/ORx Data Rate 245.76 MSPS Rx Data Rate 245.76 MHz Device Clock	1.419	2.081	0.631	5.269	5.134

[1] All current measurements made at room temperature without a heatsink.

DIGITAL INTERFACE AND TIMING SPECIFICATIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SPI TIMING						
Write SPI_CLK Period	t_{CP}	40		100	ns	
SPI_CLK High Pulse Width	t_{MP}	10			ns	
SPI_EN Setup to First SPI_CLK Rising Edge	t_{SC}	4			ns	
Last SPI_CLK Falling Edge to SPI_EN Hold	t_{HC}	0			ns	
SPI_DIO Data Input Setup to SPI_CLK	t_S	4			ns	
SPI_DIO Data Input Hold to SPI_CLK	t_H	0			ns	
SPI_CLK Falling Edge to Output Data Delay (3- or 4-Wire Mode)	t_{CO}	10		16	ns	
Bus Turnaround Time After Baseband Processor Drives Last Address Bit	t_{HZM}	t_H		t_{CO}	ns	
Bus Turnaround Time After ADRV9010 Drives Last Address Bit	t_{HZS}	0		t_{CO}	ns	
Byte to Byte Delay Time	t_{INT}			400	ns	Pause duration between any two bytes of the 3-byte operation (write or read)
DIGITAL TIMING						
TXx_EN Pulse Width[1]		10			µs	
RXx_EN Pulse Width[1]		10			µs	
ORX_CTRL_x Pulse Width[2]		10			µs	
TXx_EN to Valid Data[1]			2		µs	
RXx_EN to Valid Data[1]			2		µs	
ORX_CTRL_x to Valid Data[2]			3		µs	
JESD204B/JESD204C DATA OUTPUT INTERFACE						
Unit Interval	UI	61.65		1000	ps	
Data Rate per Channel (Nonreturn to Zero (NRZ))		1000		16220	Mbps	
Rise Time	t_R	17	26		ps	20% to 80% in 100 Ω load
Fall Time	t_F	17	26		ps	20% to 80% in 100 Ω load
Output Common-Mode Voltage	V_{CM}	0		1.8	V	AC-coupled
Termination Voltage = 1.0 V	V_{TT}	735		1135	mV	DC-coupled
Differential Output Voltage	V_{DIFF}	360	466	770	mV	
Short-Circuit Current	I_{DSHORT}	−100		+100	mA	
Differential Termination Impedance	Z_{RDIFF}	80	100	120	Ω	
SYSREF_IN Signal Setup Time to DEVCLK± Signal	t_S	200			ps	
SYSREF_IN Signal Hold Time to DEVCLK± Signal	t_H	200			ps	
JESD204B/JES204C DATA INPUT INTERFACE						
Unit Interval	UI	61.65		1000	ps	
Data Rate per Channel (NRZ)		1000		16220	Mbps	
Input Common-Mode Voltage	V_{CM}	0.05		1.65	V	AC-coupled
V_{TT} = 1.0 V		720		1200	mV	DC-coupled (not recommended)
Differential Input Voltage	V_{DIFF}	125		750	mV	
V_{TT} Source Impedance	Z_{TT}		1.2	30	Ω	
Differential Termination Impedance	Z_{RDIFF}	80	106	120	Ω	
V_{TT}						
AC-Coupled		1.27		1.33	V	
DC-Coupled		1.14		1.26	V	

[1] Where x represents the channel number.
[2] Where x represents A, B, C, or D.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VDDA_1P8 to VSSA	−0.3 V to +2.2 V
VDDA_1P3 to VSSA	−0.2 V to +1.5 V
VDDA_1P0, VDIG_1P0 to VSSD, VSSA	−0.2 V to +1.2 V
VIF Referenced Logic Inputs and Outputs to VSSD	−0.3 V to VIF + 0.3 V
JESD204B Logic Outputs to VSSA	−0.3 V to VSER_1P0
JESD204B Logic Inputs to VSSA	−0.3 V to VDES_1P0
Input Current to Any Pin Except Supplies	±10 mA
Maximum Input Power into RF Ports	See Table 8 for limits vs. survival time
Junction Temperature Range[1]	−40°C to +110°C
Storage Temperature Range	−65°C to +150°C

[1] The maximum junction temperature for continuous operation is 110°C. See the Junction Temperature section for more details.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

JUNCTION TEMPERATURE

The maximum junction temperature for continuous operation is 110°C. Although operation up to 125°C is supported, specification compliance is only guaranteed up to 110°C. To avoid a reduction in operating lifetime by operating above 110°C, the device must operate at a temperature less than 110°C for a period (t_{UNITS}) determined by the following equation:

$$t_{UNITS < 110} = (AF_{T > 110} - 1)/(1 - AF_{T < 110})$$

where $AF_{T > 110}$ and $AF_{T < 110}$ are acceleration factors obtained from Table 7.

For example, if the device operates at 125°C for 1 hour, expected device lifetime is maintained if the device operates at 100°C for 4.5 hours to offset the time operating above 110°C.

Table 7. Acceleration Factors for High Temperature Operation

Operating Junction Temperature (°C)	Acceleration Factor (AF)
125	3.75
120	2.44
115	1.57
110	1.00
105	0.63
100	0.39
95	0.24
90	0.14

Table 8. Maximum Input Power into RF Ports vs. Lifetime

RF Port Input Power, CW Signal (dBm)	Lifetime	
	Gain = −30 dB	Gain = 0 dB
7	>10 years	>10 years
10	>10 years	20,000 hours
20	>10 years	14 hours
23	>10 years	110 minutes
25	>7 years	60 minutes

REFLOW PROFILE

The ADRV9010 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal resistance values specified in Table 9 are calculated based on JEDEC specifications (unless specified otherwise) and should be used in compliance with JESD51-12. Note that using enhanced heat removal techniques (PCB, heat sink, air flow, and so forth) improves thermal resistance.

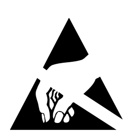
θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 9. Thermal Resistance Values

Package Type	θ_{JA}	θ_{JC}	Unit
BC-289-3	14.8	0.03	(°C/W)

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

ADRV9010
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSSA	VSSA	VSSA	TX3+	TX3–	VSSA	VTXLO_1P3	VSSA	VRXLO_1P3	VSSA	VSSA	VSSA	TX2+	TX2–	VSSA	VSSA	VSSA
B	RX3–	VSSA	VSSA	VANA3_1P8	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VAUXVCO_1P0	VSSA	VSSA	VANA2_1P8	VSSA	VSSA	RX2+
C	RX3+	VSSA	NIC	GPIO_ANA_7	GPIO_ANA_6	VAUXSYN_1P3	VSSA	DEVCLK+	DEVCLK–	VSSA	VAUXVCO_1P3	GPIO_ANA_1	GPIO_ANA_0	VSSA	RBIAS	VSSA	RX2–
D	VSSA	VSSA	VANA2_1P3	VSSA	VSSA	VSSA	VSSA	SYSREF+	SYSREF–	VSSA	VSSA	VSSA	VSSA	VSSA	VANA1_1P3	VSSA	VSSA
E	AUXADC_3	EXT_LO2–	VSSA	ORX3+	ORX3–	VSSA	TX3_EN	GPIO_11	GPIO_9	GPIO_3	TX2_EN	VSSA	ORX1+	ORX1–	VSSA	EXT_LO1+	AUXADC_1
F	AUXADC_2	EXT_LO2+	VSSA	VSSA	VSSA	VSSA	ORX_CTRL_C	GPIO_12	GPIO_10	GPIO_4	ORX_CTRL_B	VSSA	VSSA	VSSA	VSSA	EXT_LO1–	AUXADC_0
G	VSSA	VSSA	VRFVCO2_1P3	VSSA	VRFVCO2_1P0	VSSA	RX3_EN	GPIO_13	VDIG_1P0	GPIO_5	RX2_EN	VSSA	VRFVCO1_1P0	VSSA	VRFVCO1_1P3	VSSA	VSSA
H	RX4–	VSSA	VCONV2_1P8	VSSA	VSSA	VSSA	GPIO_17	GPIO_14	VSSD	GPIO_6	GPIO_0	VSSA	VSSA	VSSA	VCONV1_1P8	VSSA	RX1+
J	RX4+	VSSA	VCONV2_1P3	VSSA	VRFSYN2_1P3	VSSA	RX4_EN	GPIO_15	VDIG_1P0	GPIO_7	RX1_EN	VSSA	VRFSYN1_1P3	VSSA	VCONV1_1P3	VSSA	RX1–
K	VSSA	VSSA	VCONV2_1P0	VSSA	VSSA	VSSA	GPIO_18	GPIO_16	VSSD	GPIO_8	GPIO_1	VSSA	VSSA	VSSA	VCONV1_1P0	VSSA	VSSA
L	GPIO_ANA_5	GPIO_ANA_4	VSSA	ORX4+	ORX4–	VSSA	ORX_CTRL_D	SPI_DIO	VDIG_1P0	SPI_EN	ORX_CTRL_A	VSSA	ORX2+	ORX2–	VSSA	GPIO_ANA_2	GPIO_ANA_3
M	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	TX4_EN	SPI_DO	VSSD	SPI_CLK	TX1_EN	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
N	TX4–	VANA4_1P8	VSSA	VSSA	VCLKVCO_1P3	SYNCIN3+	GPINT2	GPINT1	VIF	$\overline{\text{RESET}}$	GPIO_2	SYNCIN1+	SYNCIN1–	SYNCOUT2+	SYNCOUT2–	VANA1_1P8	TX1+
P	TX4+	VSSA	VSSA	VSSA	VCLKVCO_1P0	SYNCIN3–	SYNCIN2+	SYNCIN2–	VSSA	TEST_EN	VJVCO_1P8	VDES_1P0	VDES_1P0	VTT_DES	SYNCOUT1+	VSSA	TX1–
R	VSSA	VSSA	VSER_1P0	VSER_1P0	VSSA	VSSA	VCLKSYN_1P3	VSSA	VJSYN_1P0	VSSA	NIC	VSSA	VSSA	VSSA	SYNCOUT1–	VSSA	VSSA
T	SERDOUTD+	SERDOUTD–	SERDOUTC+	SERDOUTC–	SERDOUTB+	SERDOUTB–	SERDOUTA+	SERDOUTA–	VSSA	SERDIND–	SERDIND+	SERDINC+	SERDINC–	SERDINB–	SERDINB+	SERDINA+	SERDINA–
U	SERDOUTH+	SERDOUTH–	SERDOUTG+	SERDOUTG–	SERDOUTF+	SERDOUTF–	SERDOUTE+	SERDOUTE–	VSSA	SERDINH–	SERDINH+	SERDING+	SERDING–	SERDINF–	SERDINF+	SERDINE+	SERDINE–

- ANALOG GROUND
- DIGITAL GROUND
- ANALOG POWER
- DIGITAL POWER
- ANALOG INPUTS/OUTPUTS
- ANALOG GPIO
- AUXILIARY ADC INPUTS
- DIGITAL INPUTS/OUTPUTS
- SPI BUS
- LVDS SERDES CONTROLS
- SERDES INPUTS/OUTPUTS
- DIFFERENTIAL SYSREF SIGNAL
- NOT INTERNALLY CONNECTED

20043-002

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Ball No.	Type[1]	Mnemonic	Description
A1 to A3, A6, A8, A10 to A12, A15 to A17, B2, B3, B5 to B10, B12, B13, B15, B16, C2, C7, C10, C14, C16, D1, D2, D4 to D7, D10 to D14, D16, D17, E3, E6, E12, E15, F3 to F6, F12 to F15, G1, G2, G4, G6, G12, G14, G16, G17, H2, H4 to H6, H12 to H14, H16, J2, J4, J6, J12, J14, J16, K1, K2, K4 to K6, K12 to K14, K16, K17, L3, L6, L12, L15, M1 to M6, M12 to M17, N3, N4, P2 to P4, P9, P16, R1, R2, R5, R6, R8, R10, R12 to R14, R16, R17, T9, U9	I	VSSA	Analog Grounds.
A4, A5	O	TX3+, TX3−	Differential Outputs for Transmitter Channel 3. Do not connect if unused.
A7	I	VTXLO_1P3	1.3 V Supply Input.
A9	I	VRXLO_1P3	1.3 V Supply Input.
A13, A14	O	TX2+, TX2−	Differential Outputs for Transmitter Channel 2. Do not connect if unused.
B1, C1	I	RX3−, RX3+	Differential Inputs for Receiver Channel 3. Connect to VSSA if unused.
B4	I	VANA3_1P8	1.8 V Supply Input.
B11	O	VAUXVCO_1P0	1.0 V Internal Supply Node. Bypass Pin B11 with a 4.7 µF capacitor.
B14	I	VANA2_1P8	1.8 V Supply Input.
B17, C17	I	RX2+, RX2−	Differential Inputs for Receiver Channel 2. Connect to VSSA if unused.
C3, R11	N/A	NIC	Not Internally Connected. Pin C3 and R11 must remain disconnected.
C4, C5, C12, C13, L1, L2, L17, L16	I/O	GPIO_ANA_7 to GPIO_ANA_0	General-Purpose Inputs and Outputs. The GPIO pins are referenced to 1.8 V but can also function as auxiliary DAC outputs. If unused, these pins can be connected to VSSA with a 10 kΩ resistor or configured as outputs, driven low, and left disconnected.
C6	I	VAUXSYN_1P3	1.3 V Supply Input.
C8, C9	I	DEVCLK+, DEVCLK−	Device Clock Differential Inputs.
C11	I	VAUXVCO_1P3	1.3 V Supply Input.
C15	I	RBIAS	Bias Resistor Connection. Pin C15 generates an internal current based on an external 1% resistor. Connect a 4.99 kΩ resistor between C15 and analog ground (VSSA).
D3	I	VANA2_1P3	1.3 V Supply Input.
D8, D9	I	SYSREF+, SYSREF−	LVDS System Reference Clock Inputs for the Serializer/Deserializer (SERDES) Interface. Connect a 100 Ω termination between these pins.
D15	I	VANA1_1P3	1.3 V Supply Input.
E1	I	AUXADC_3	Auxiliary ADC 3 Input. Do not connect if unused.
E2, F2	I/O	EXT_LO2−, EXT_LO2+	Differential External LO Input/Output 2. If used for the external LO input, the input frequency must be 2× the desired carrier frequency. Do not connect if unused.
E4, E5	I	ORX3+, ORX3−	Differential Inputs for Observation Receiver Channel 3. Connect to VSSA if unused.
E7	I	TX3_EN	Enable Input for Transmitter Channel 3. Connect to VSSA if unused.

Ball No.	Type[1]	Mnemonic	Description
E8 to E10, F8 to F10, G8, G10, H7, H8, H10, H11, J8, J10, K7, K8, K10, K11, N11	I/O	GPIO_0 to GPIO_18	General-Purpose Digital Inputs and Outputs. See Figure 2 to match the ball location to the GPIO_x signal name. If unused, these pins can be connected to VSSA with a 10 kΩ resistor or configured as outputs, driven low, and left disconnected.
E11	I	TX2_EN	Enable Input for Transmitter Channel 2. Connect to VSSA if unused.
E13, E14	I	ORX1+, ORX1−	Differential Inputs for Observation Receiver Channel 1. Connect to VSSA if unused.
E16, F16	I/O	EXT_LO1+, EXT_LO1−	Differential External LO Input/Output 1. If used for the external LO input, the input frequency must be 2× the desired carrier frequency. Do not connect if unused.
E17	I	AUXADC_1	Auxiliary ADC 1 Input. Do not connect if unused.
F1	I	AUXADC_2	Auxiliary ADC2 Input. Do not connect if unused.
F7, F11, L7, L11	I	ORX_CTRL_C, ORX_CTRL_B, ORX_CTRL_D, ORX_CTRL_A	These pins determines the active ORX_x path. Connect to VSSA directly or with a pull-down resistor if unused.
F17	I	AUXADC_0	Auxiliary ADC0 Input. Do not connect if unused.
G3	I	VRFVCO2_1P3	1.3 V Supply Input.
G5	O	VRFVCO2_1P0	1.0 V Internal Supply Node. Bypass this pin with a 4.7 μF capacitor.
G7	I	RX3_EN	Enable Input for Receiver Channel 3. Connect to VSSA if unused.
G9, J9, L9	I	VDIG_1P0	1.0 V Digital Supply Input.
G11	I	RX2_EN	Enable Input for Receiver Channel 2. Connect to VSSA if unused.
G13	O	VRFVCO1_1P0	1.0 V Internal Supply Node. Bypass this pin with a 4.7 μF capacitor.
G15	I	VRFVCO1_1P3	1.3 V Supply Input.
H1, J1	I	RX4−, RX4+	Differential Inputs for Receiver Channel 4. Connect to VSSA if unused.
H3	I	VCONV2_1P8	1.8 V Supply Input.
H9, K9, M9	I	VSSD	Digital Ground.
H15	I	VCONV1_1P8	1.8 V Supply Input.
H17, J17	I	RX1+, RX1−	Differential Inputs for Receiver Channel 1. Connect to VSSA if unused.
J3	I	VCONV2_1P3	1.3 V Supply Input.
J5	I	VRFSYN2_1P3	1.3 V Supply Input.
J7	I	RX4_EN	Enable Input for Receiver Channel 4. Connect to VSSA if unused.
J11	I	RX1_EN	Enable Input for Receiver Channel 1. Connect to VSSA if unused.
J13	I	VRFSYN1_1P3	1.3 V Supply Input.
J15	I	VCONV1_1P3	1.3 V Supply Input.
K3	O	VCONV2_1P0	1.0 V Internal Supply Node. Bypass this pin with a 4.7 μF capacitor.
K15	O	VCONV1_1P0	1.0 V Internal Supply Node. Bypass this pin with a 4.7 μF capacitor.

Ball No.	Type[1]	Mnemonic	Description
L4, L5	I	ORX4+, ORX4−	Differential Inputs for Observation Receiver Channel 4. Connect to VSSA if unused.
L8	I/O	SPI_DIO	Serial Data Input/Output. Pin L8 is a serial data input only when in 4-wire mode. When L8 is in 3-wire mode, it is a serial data input/output.
L10	I	SPI_EN	Serial Data Bus Chip Select. Active low.
L13, L14	I	ORX2+, ORX2−	Differential Inputs for Observation Receiver Channel 2. Connect to VSSA if unused.
M7	I	TX4_EN	Enable Input for Transmitter Channel 4. Connect to VSSA if unused.
M8	O	SPI_DO	Serial Data Output.
M10	I	SPI_CLK	Serial Data Bus Clock Input.
M11	I	TX1_EN	Enable Input for Transmitter Channel 1. Connect to VSSA if unused.
N1, P1	O	TX4−, TX4+	Differential Outputs for Transmitter Channel 4. Do not connect if unused.
N2	I	VANA4_1P8	1.8 V Supply Input.
N5	I	VCLKVCO_1P3	1.3 V Supply Input.
N6, P6	I	SYNCIN3+, SYNCIN3−	Low Voltage Differential Signal (LVDS) Synchronization Signal Input 3. Connect to VSSA if unused.
N7	O	GPINT2	General-Purpose Interrupt Output 2. Do not connect if unused.
N8	O	GPINT1	General-Purpose Interrupt Output 1. Do not connect if unused.
N9	I	VIF	1.8 V Interface Supply Input.
N10	I	$\overline{\text{RESET}}$	Active Low Chip Reset.
N12, N13	I	SYNCIN1+, SYNCIN1−	LVDS Synchronization Signal Input 1. Connect to VSSA if unused.
N14, N15	O	SYNCOUT2+, SYNCOUT2−	LVDS Synchronization Signal Output 2. Do not connect if unused.
N16	I	VANA1_1P8	1.8 V Supply Input.
N17, P17	O	TX1+, TX1−	Differential Outputs for Transmitter Channel 1. Do not connect if unused.
P5	O	VCLKVCO_1P0	1.0 V Internal Supply Node. Bypass this pin with a 4.7 μF capacitor.
P7, P8	I	SYNCIN2+, SYNCIN2−	LVDS Synchronization Signal Input 2. Connect to VSSA if unused.
P10	I	TEST_EN	Test Input for JTAG Boundary Scan. Pull high to enable boundary scan, and tie to VSSA if unused.
P11	I	VJVCO_1P8	1.8 V Supply Input.
P12, P13	I	VDES_1P0	1.0 V Analog Supply Input.
P14	I	VTT_DES	1.0 V Analog Supply Input.
P15, R15	O	SYNCOUT1+, SYNCOUT1−	LVDS Synchronization Signal Output 1. Do not connect if unused.
R3, R4	I	VSER_1P0	1.0 V Analog Supply Input.
R7	I	VCLKSYN_1P3	1.3 V Supply Input.
R9	I	VJSYN_1P0	1.0 V Analog Supply Input.

Ball No.	Type[1]	Mnemonic	Description
T1, T2	O	SERDOUTD+, SERDOUTD−	SERDES Differential Output D. Do not connect if unused.
T3, T4	O	SERDOUTC+, SERDOUTC−	SERDES Differential Output C. Do not connect if unused.
T5, T6	O	SERDOUTB+, SERDOUTB−	SERDES Differential Output B. Do not connect if unused.
T7, T8	O	SERDOUTA+, SERDOUTA−	SERDES Differential Output A. Do not connect if unused.
T10, T11	I	SERDIND−, SERDIND+	SERDES Differential Input D. Do not connect if unused.
T12, T13	I	SERDINC+, SERDINC−	SERDES Differential Input C. Do not connect if unused.
T14, T15	I	SERDINB−, SERDINB+	SERDES Differential Input B. Do not connect if unused.
T16, T17	I	SERDINA+, SERDINA−	SERDES Differential Input A. Do not connect if unused.
U1, U2	O	SERDOUTH+, SERDOUTH−	SERDES Differential Output H. Do not connect if unused.
U3, U4	O	SERDOUTG+, SERDOUTG−	SERDES Differential Output G. Do not connect if unused.
U5, U6	O	SERDOUTF+, SERDOUTF−	SERDES Differential Output F. Do not connect if unused.
U7, U8	O	SERDOUTE+, SERDOUTE−	SERDES Differential Output E. Do not connect if unused.
U10, U11	I	SERDINH−, SERDINH+	SERDES Differential Input H. Do not connect if unused.
U12, U13	I	SERDING+, SERDING−	SERDES Differential Input G. Do not connect if unused.
U14, U15	I	SERDINF−, SERDINF+	SERDES Differential Input F. Do not connect if unused.
U16, U17	I	SERDINE+, SERDINE−	SERDES Differential Input E. Do not connect if unused.

[1] I is input, O is output, N/A is not applicable, and I/O is input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 800 MHz, unless otherwise noted.

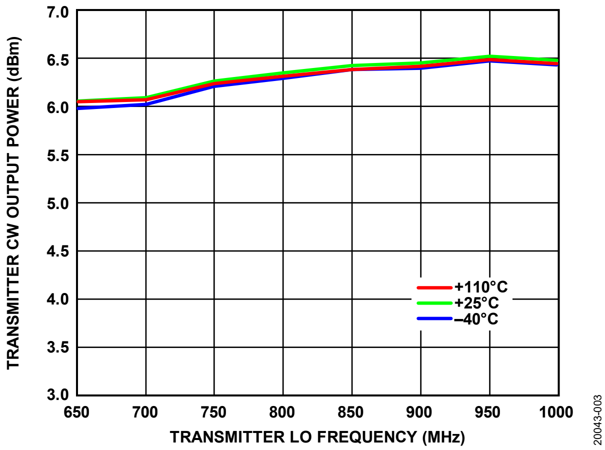


Figure 3. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

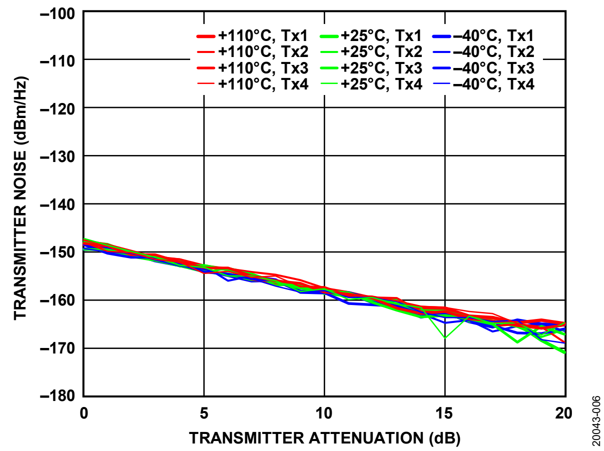


Figure 6. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset

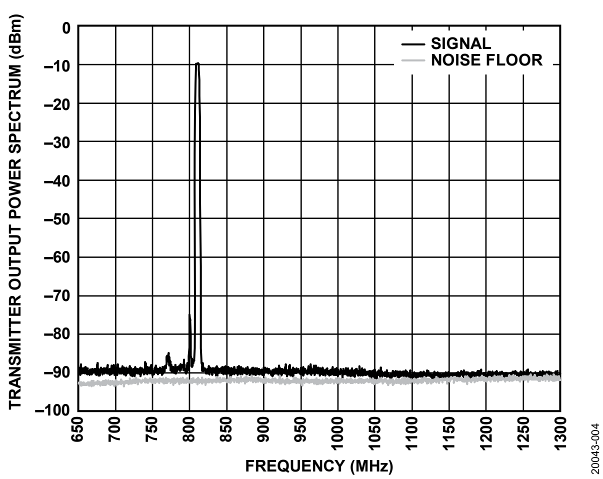


Figure 4. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

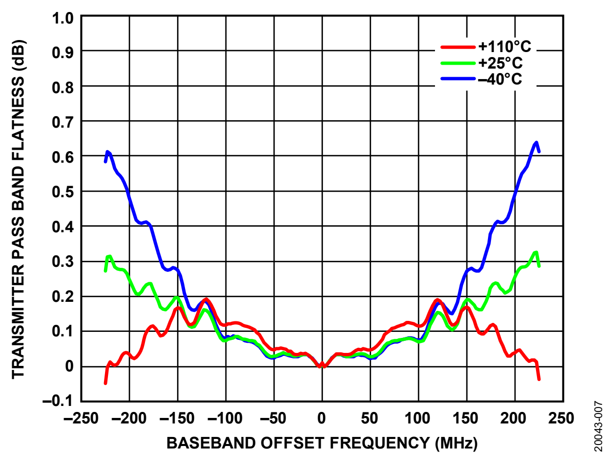


Figure 7. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

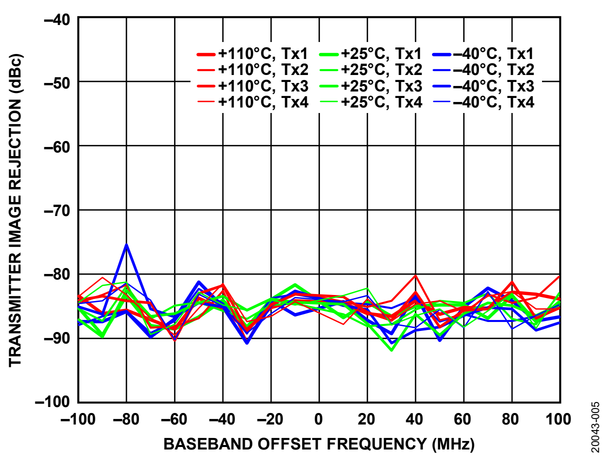


Figure 5. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

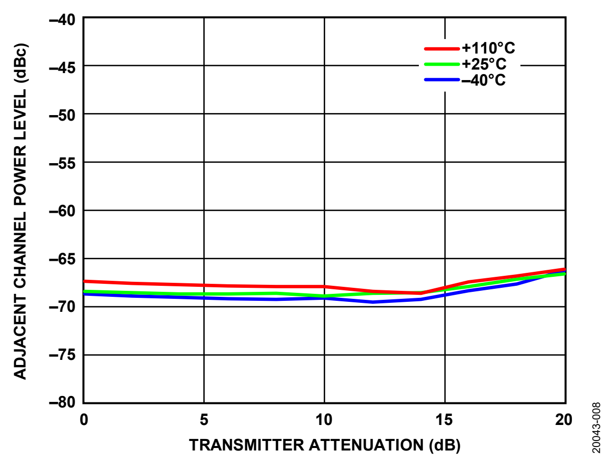


Figure 8. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

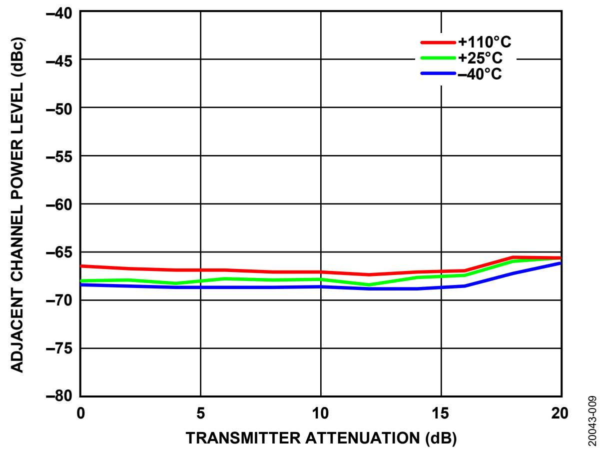


Figure 9. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

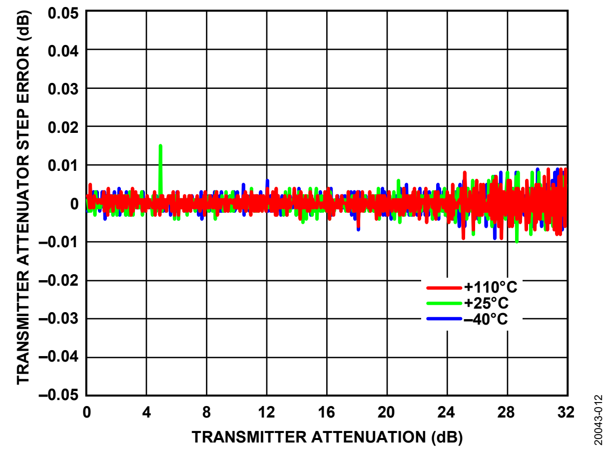


Figure 12. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

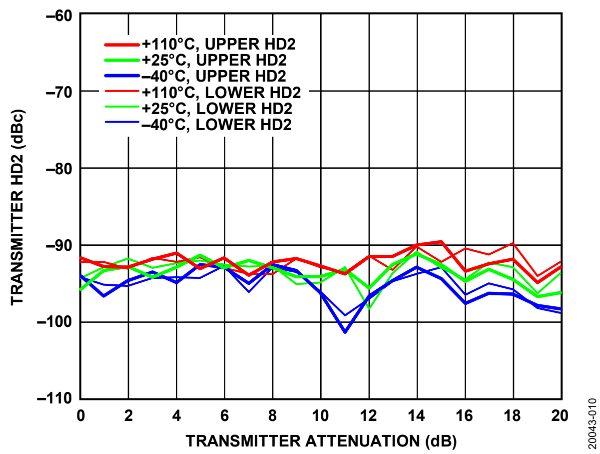


Figure 10. Transmitter Second Harmonic Distortion (HD2) vs. Transmitter Attenuation, 10 MHz Offset

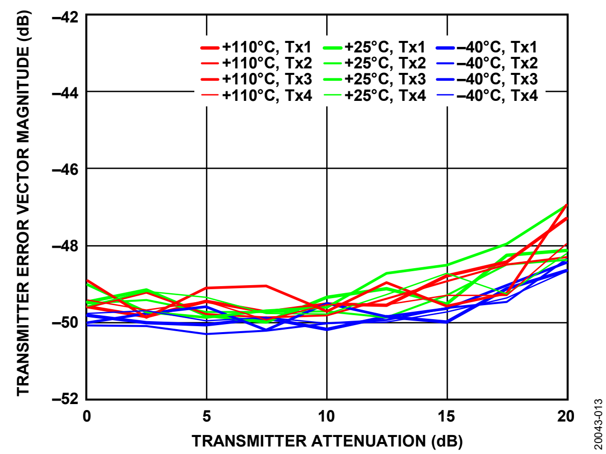


Figure 13. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

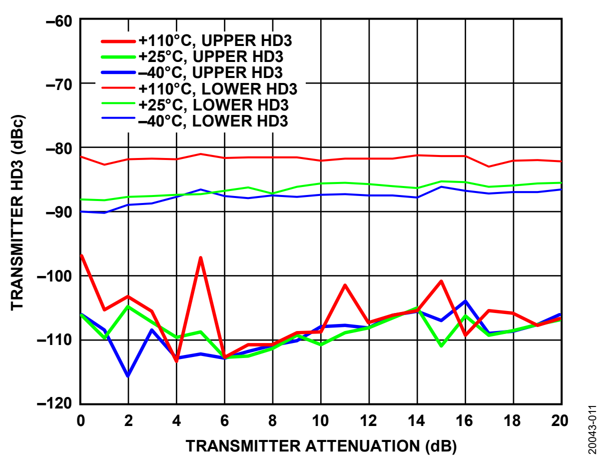


Figure 11. Transmitter Third Harmonic Distortion (HD3) vs. Transmitter Attenuation, 10 MHz Offset

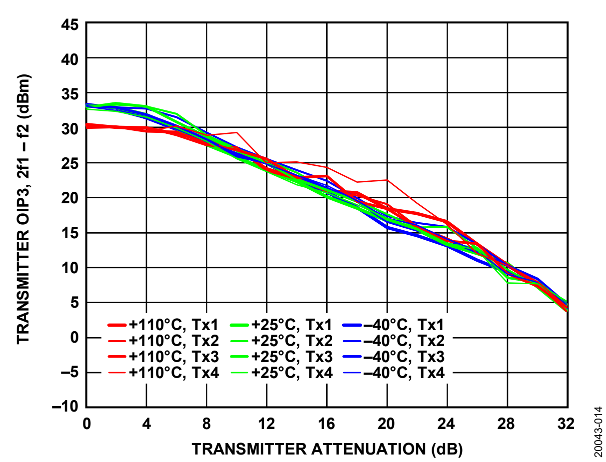


Figure 14. Transmitter OIP3, 2f1 – f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

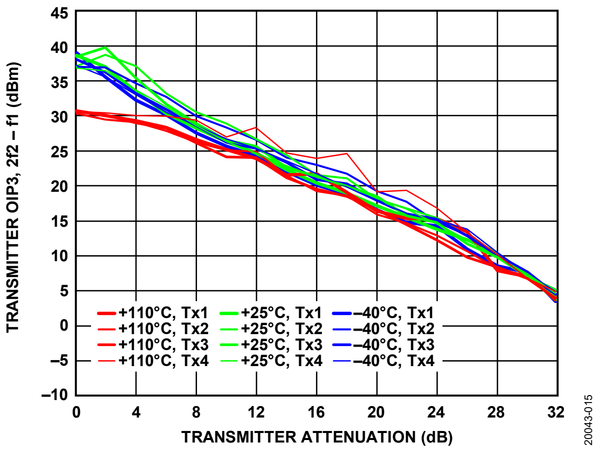


Figure 15. Transmitter OIP3, 2f2 − f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

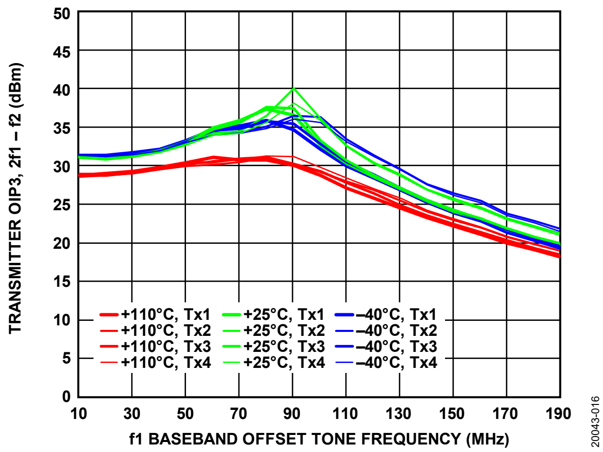


Figure 16. Transmitter OIP3, 2f1 − f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

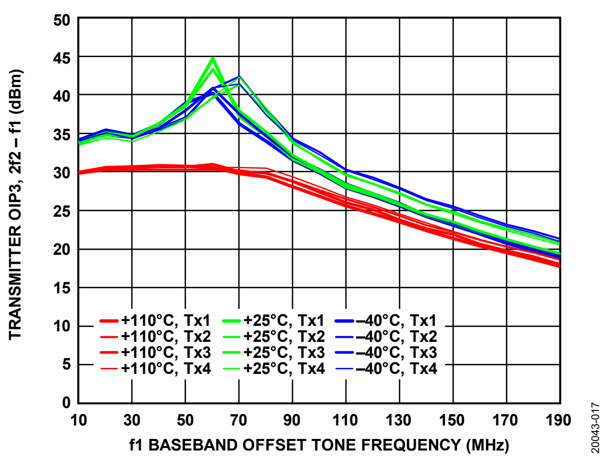


Figure 17. Transmitter OIP3, 2f2 − f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

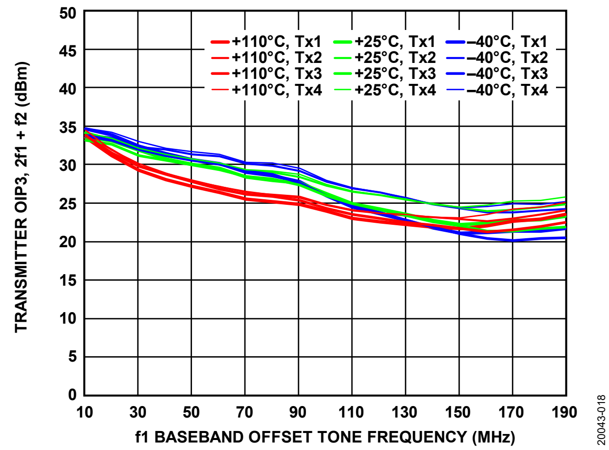


Figure 18. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

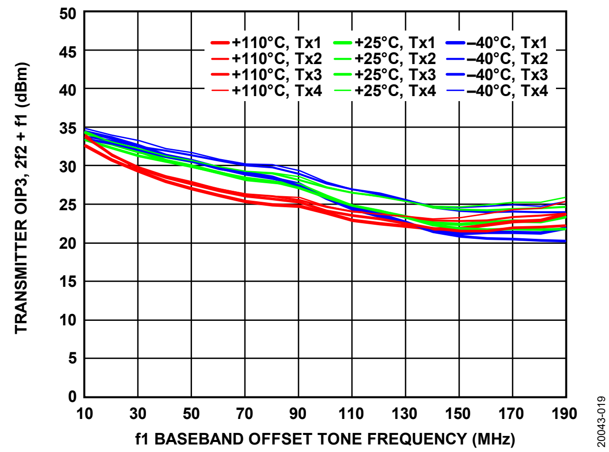


Figure 19. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

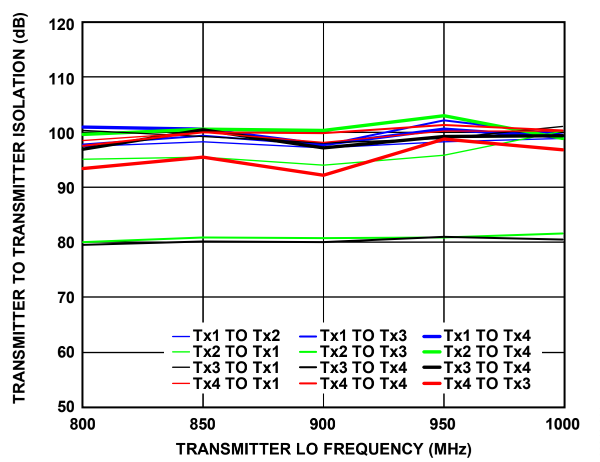


Figure 20. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

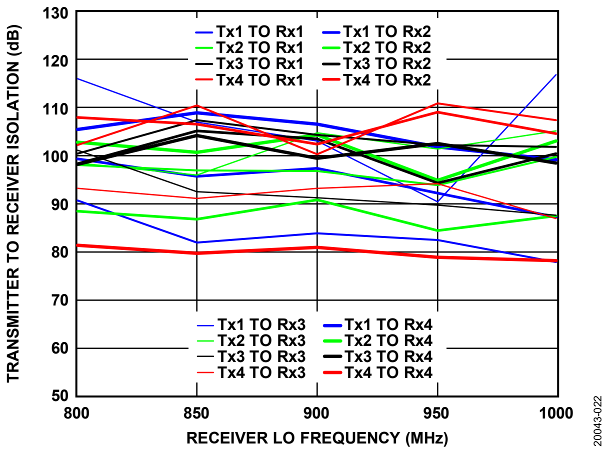


Figure 21. Transmitter to Receiver Isolation vs. Receiver LO Frequency

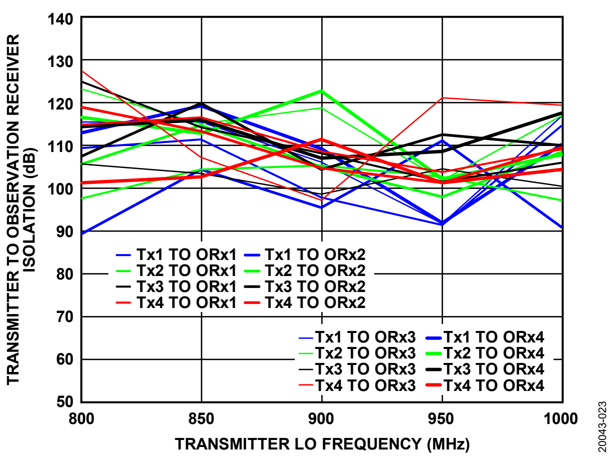


Figure 22. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

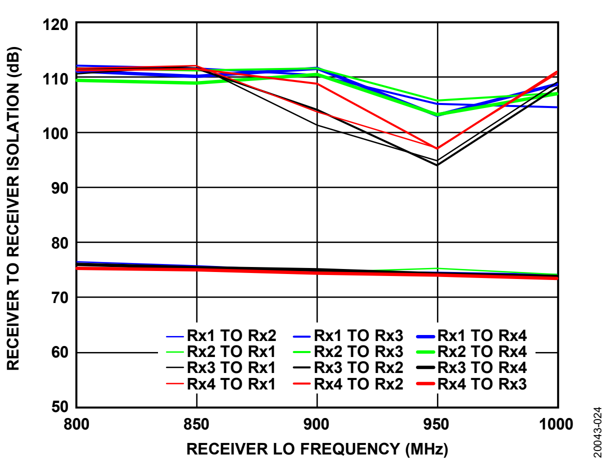


Figure 23. Receiver to Receiver Isolation vs. Receiver LO Frequency

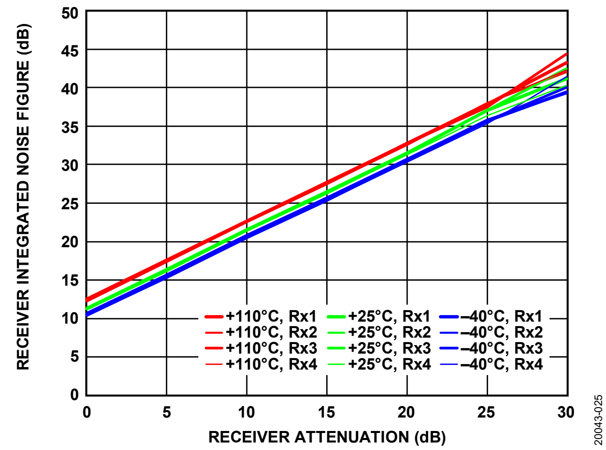


Figure 24. Receiver Integrated Noise Figure vs. Receiver Attenuation, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

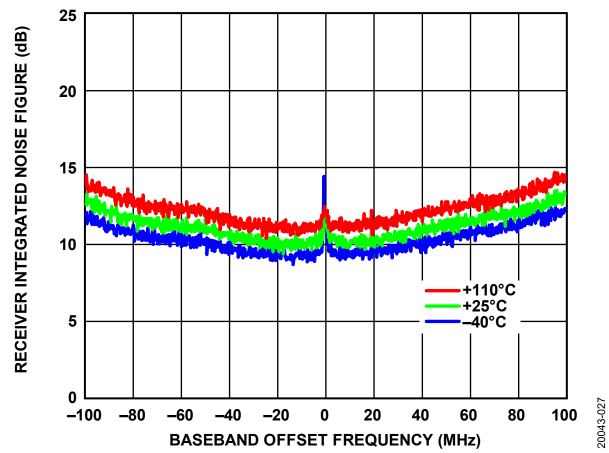


Figure 25. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

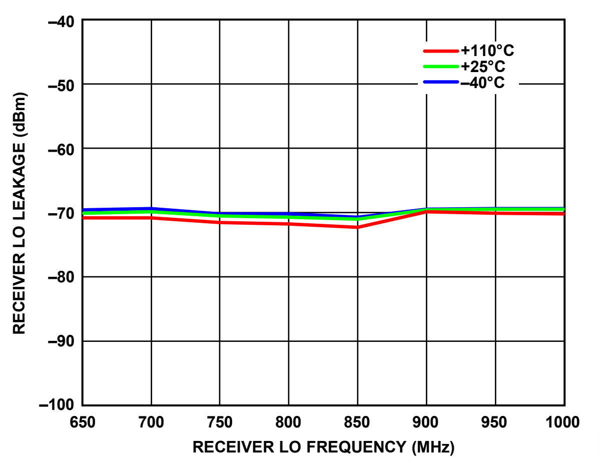


Figure 26. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

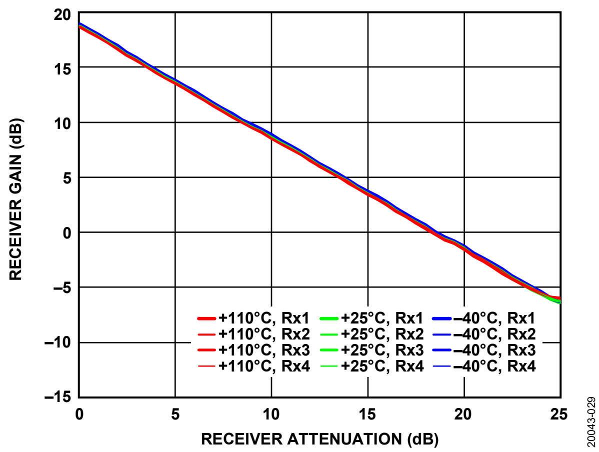


Figure 27. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

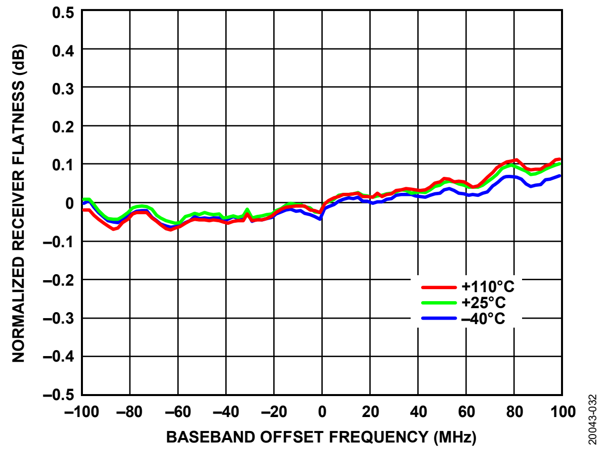


Figure 30. Normalized Receiver Flatness vs. Baseband Offset Frequency, −5 dBFS Input Signal, 0 dB Attenuation

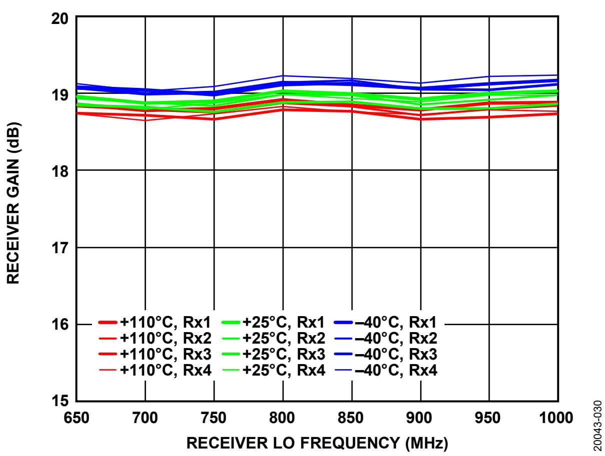


Figure 28. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

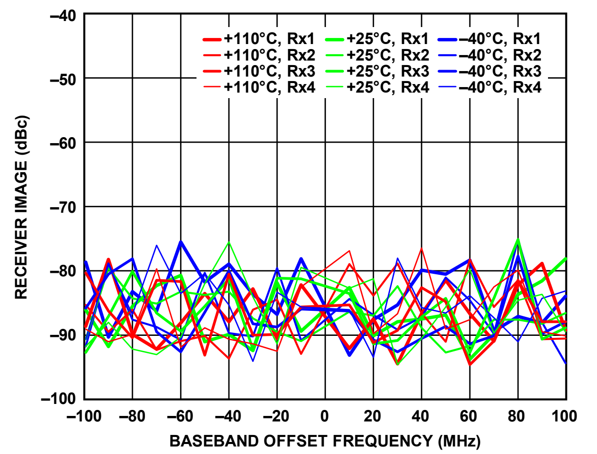


Figure 31. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

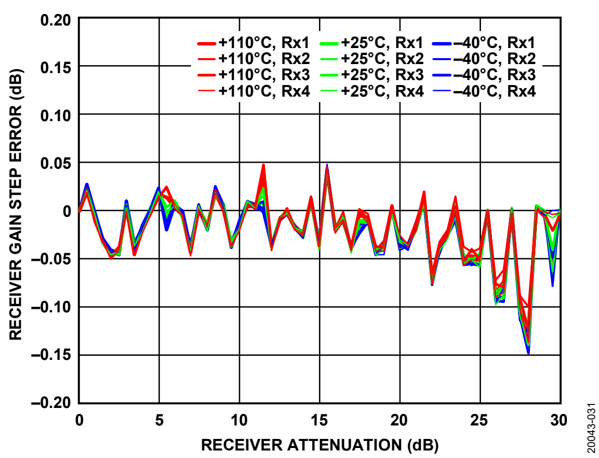


Figure 29. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

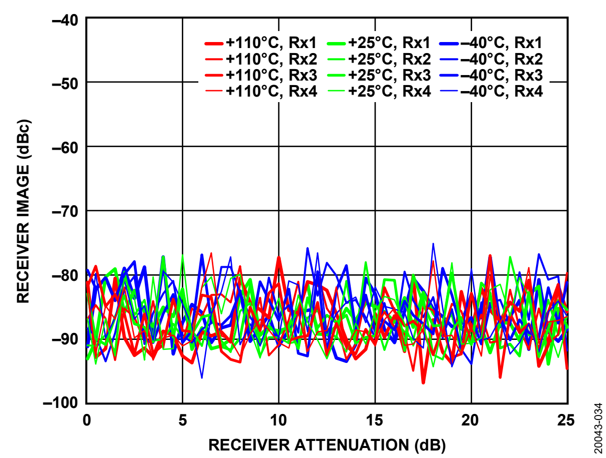


Figure 32. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

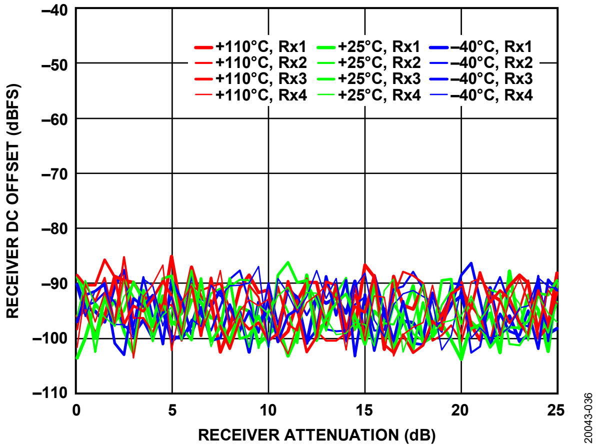


Figure 33. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

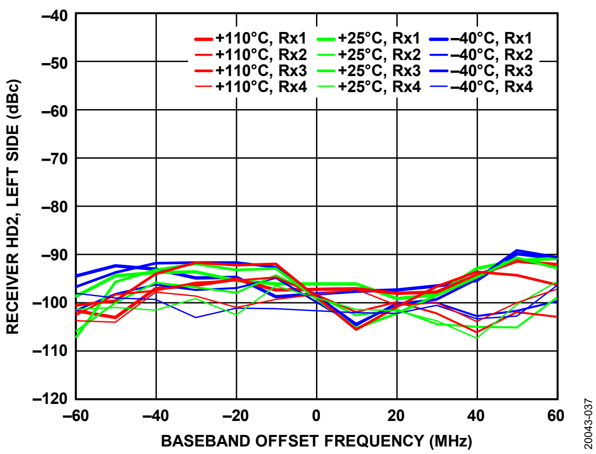


Figure 34. Receiver HD2, Left Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

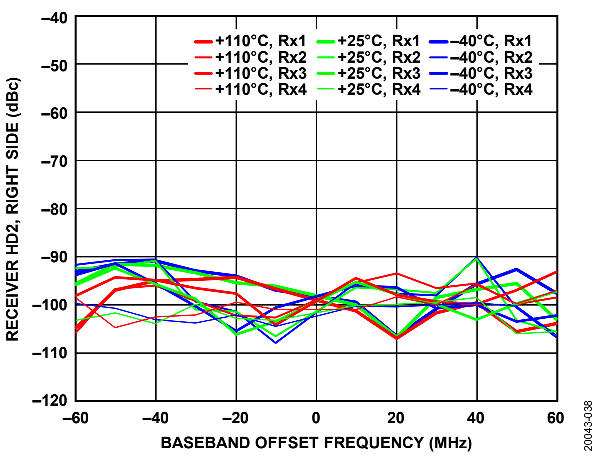


Figure 35. Receiver HD2, Right Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

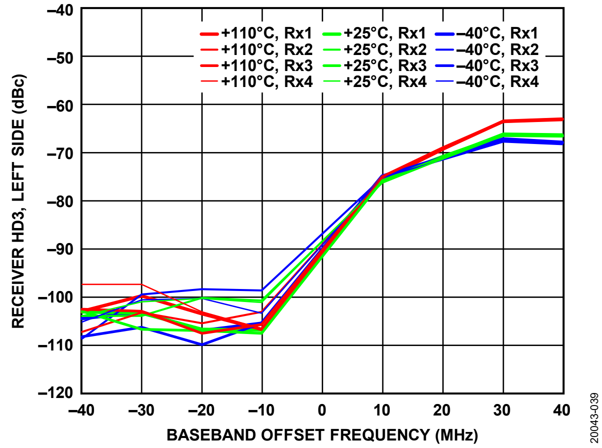


Figure 36. Receiver HD3, Left Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

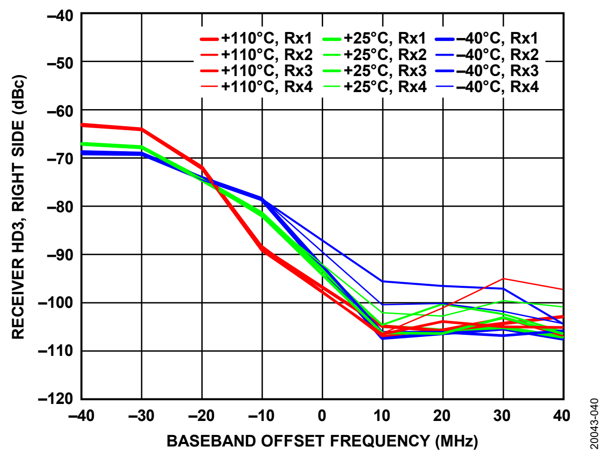


Figure 37. Receiver HD3, Right Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

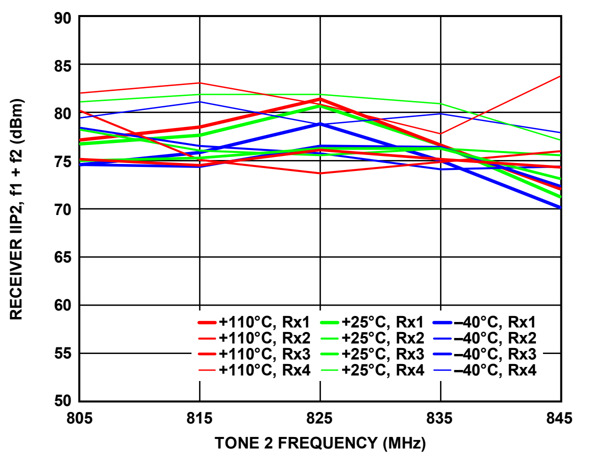


Figure 38. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

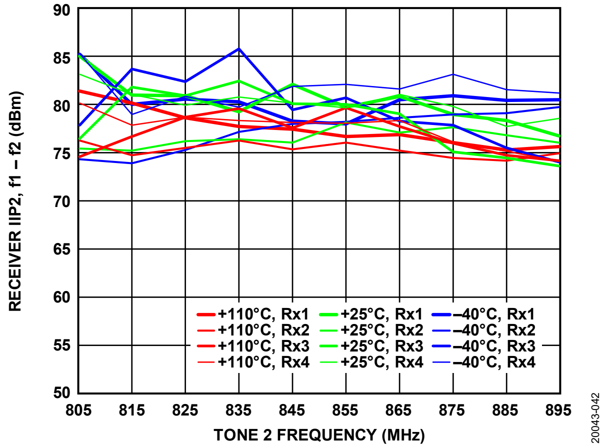


Figure 39. Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

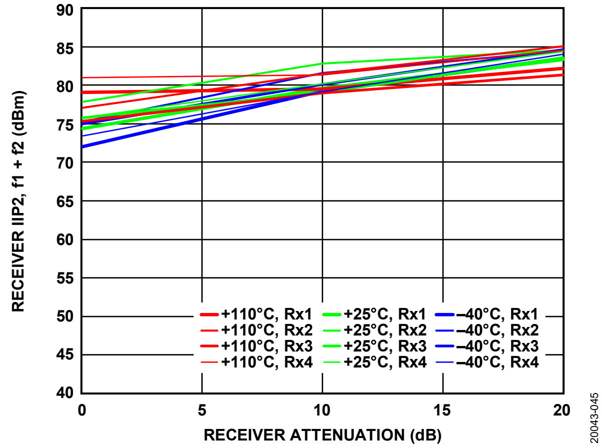


Figure 42. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

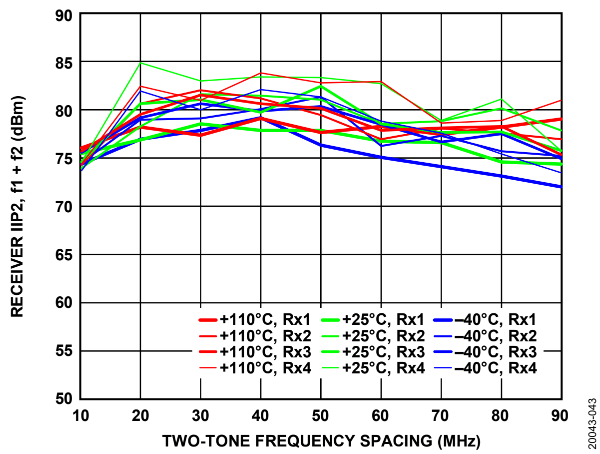


Figure 40. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

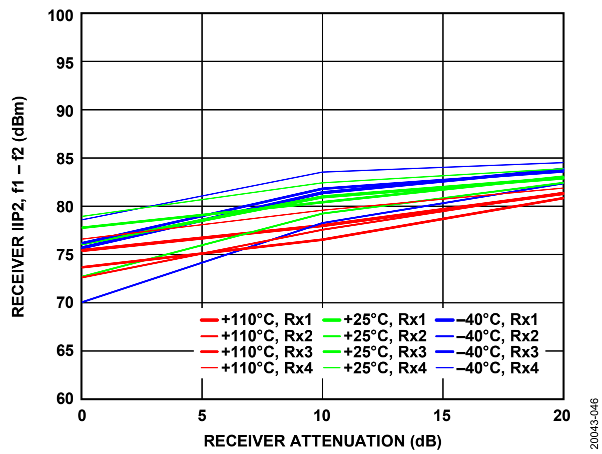


Figure 43. Receiver IIP2, f1 – f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

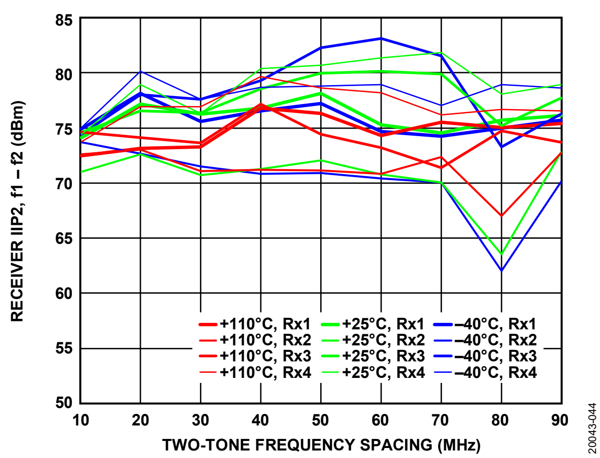


Figure 41. Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

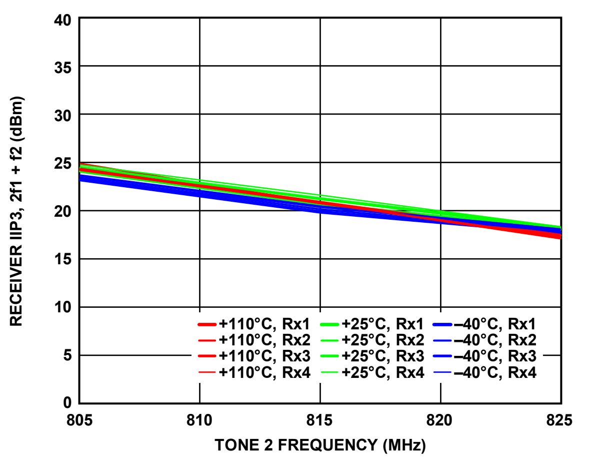


Figure 44. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

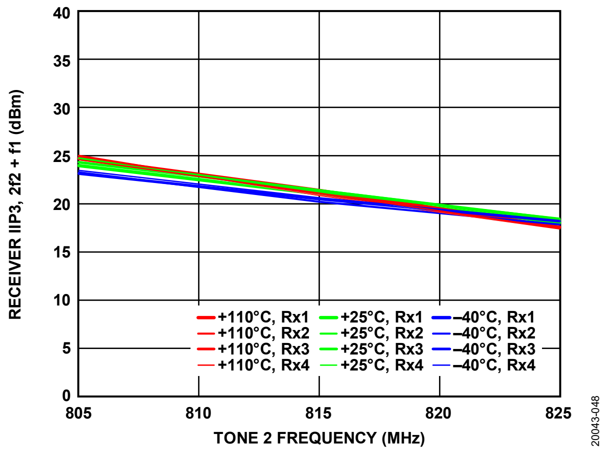


Figure 45. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

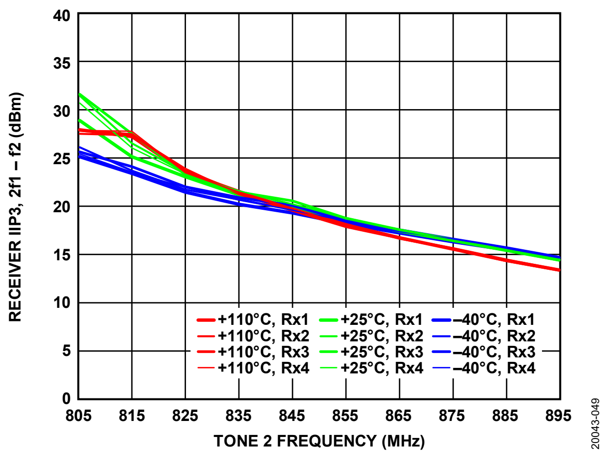


Figure 46. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

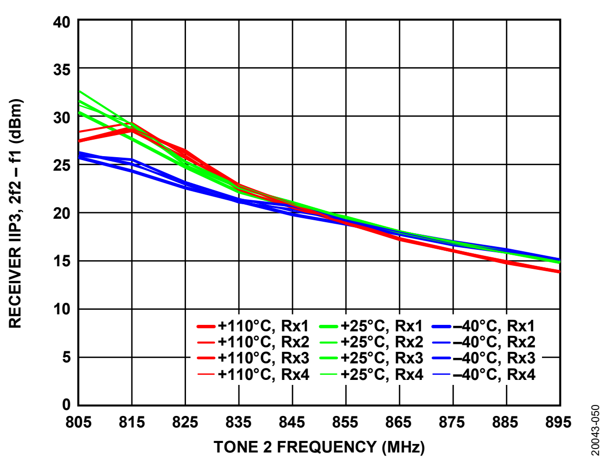


Figure 47. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

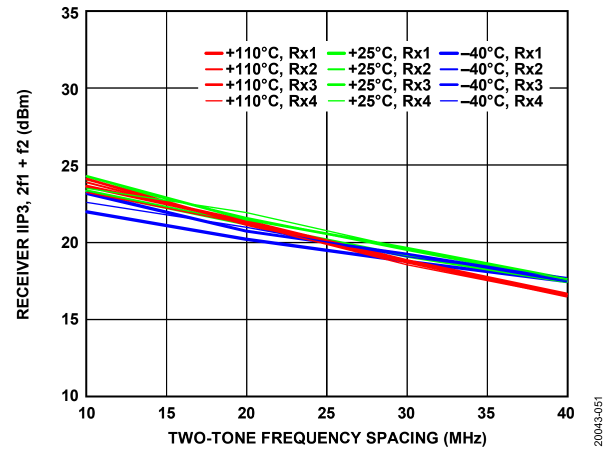


Figure 48. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

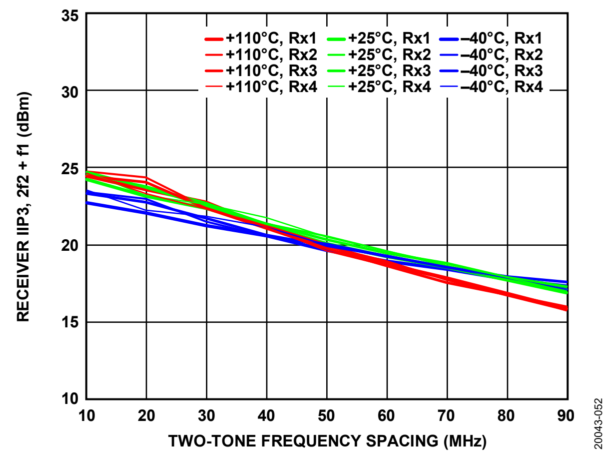


Figure 49. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

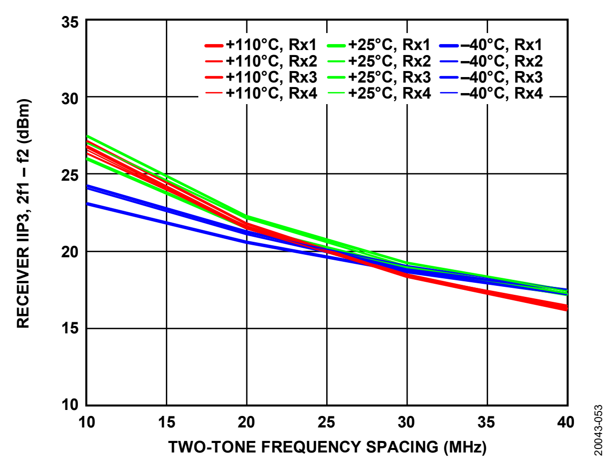


Figure 50. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

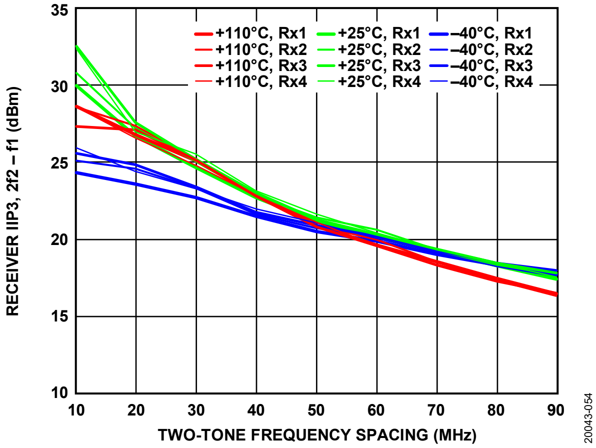


Figure 51. Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

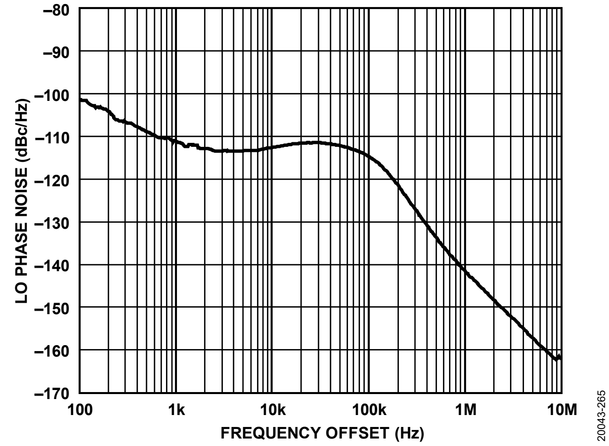


Figure 54. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 600 kHz, Phase Margin = 60°

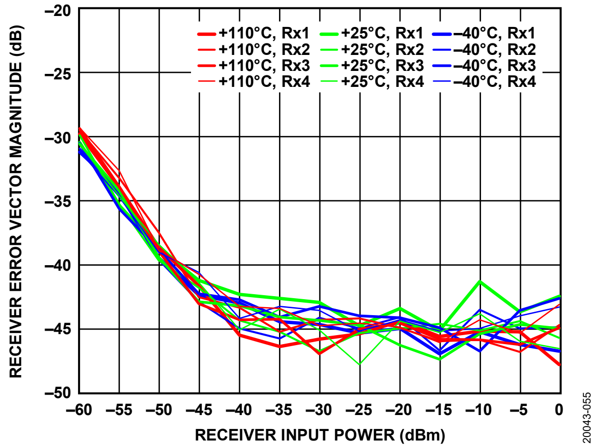


Figure 52. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

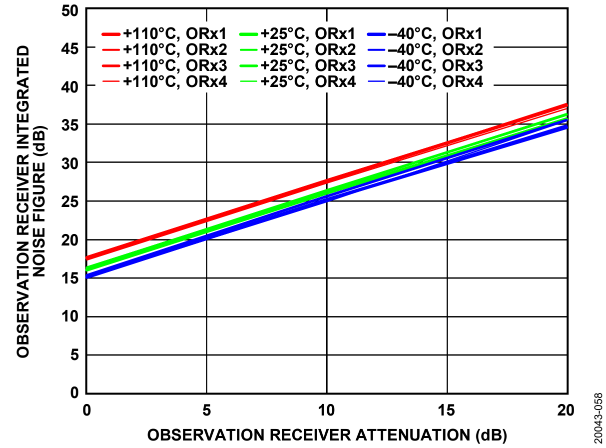


Figure 55. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

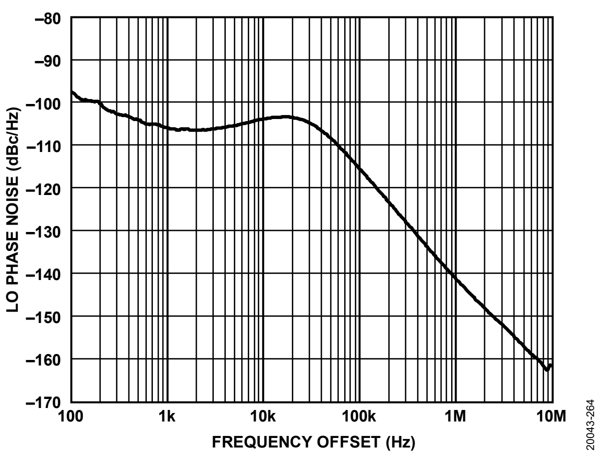


Figure 53. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 50 kHz, Phase Margin = 85°

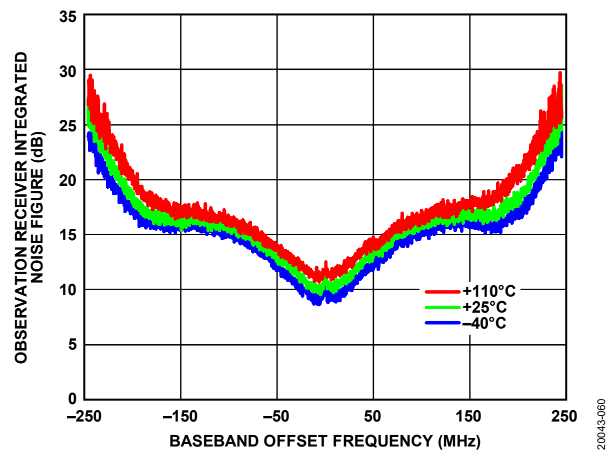


Figure 56. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

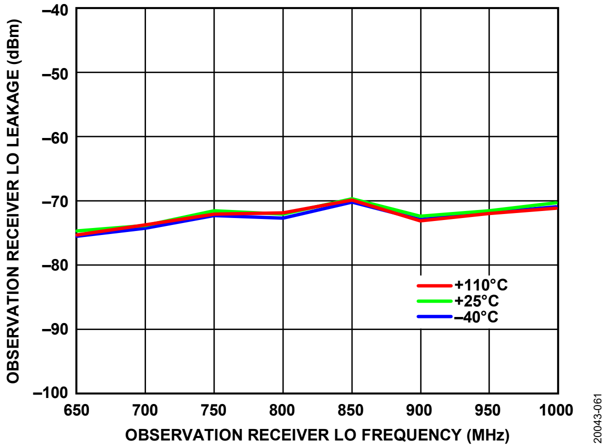


Figure 57. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

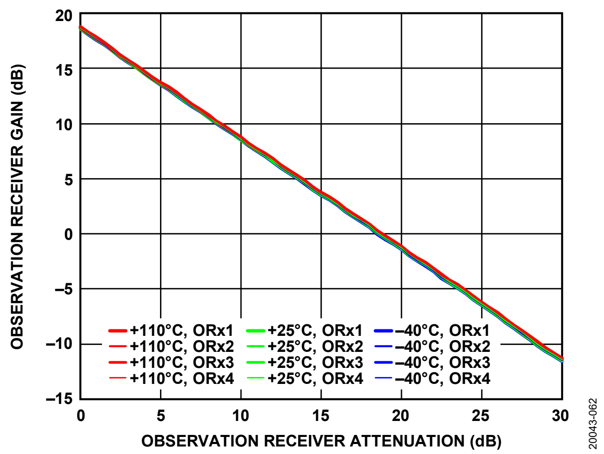


Figure 58. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

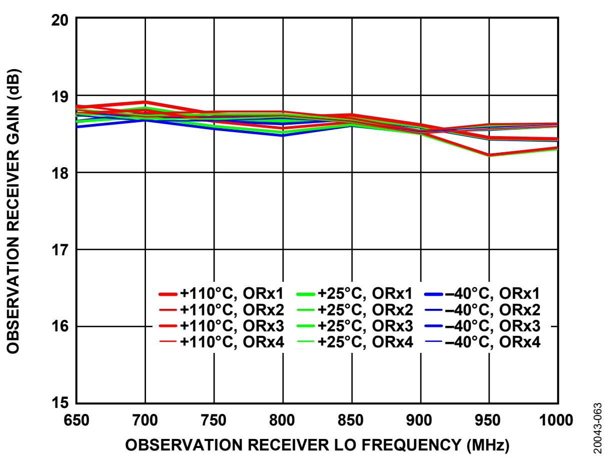


Figure 59. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

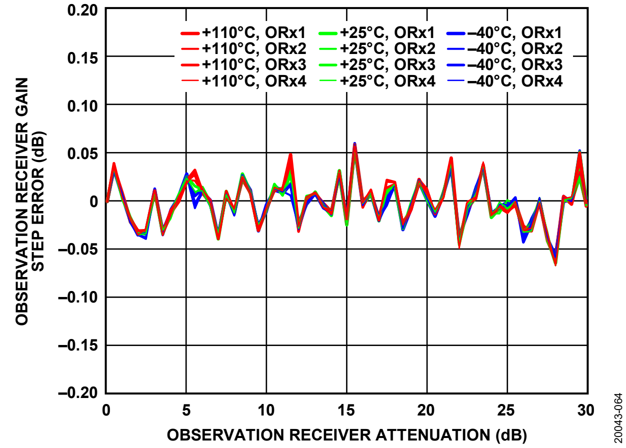


Figure 60. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

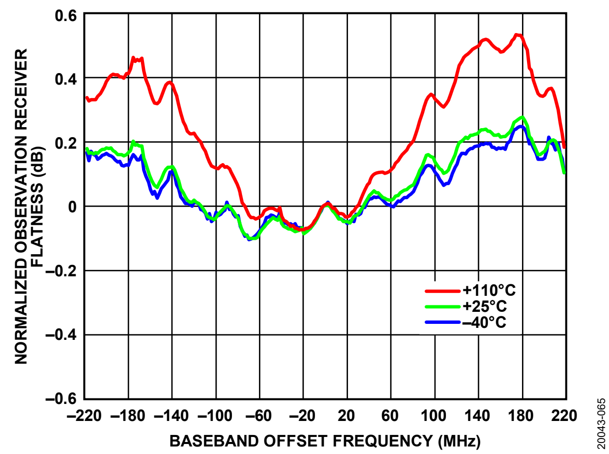


Figure 61. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, –25 dBm Input Signal, 0 dB Attenuation

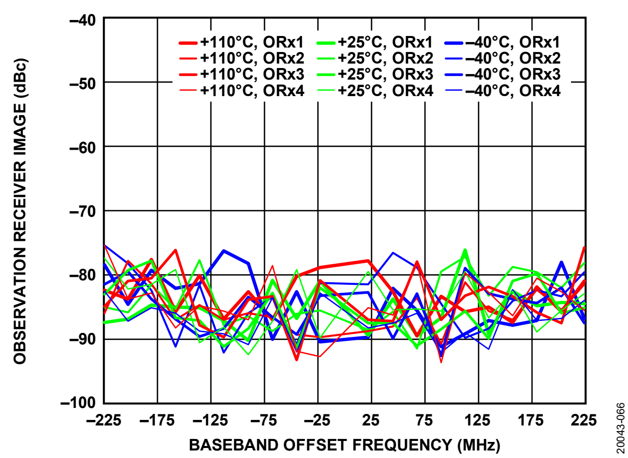


Figure 62. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

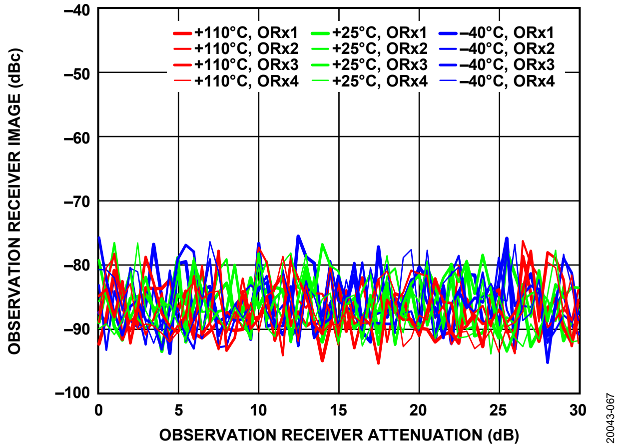


Figure 63. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

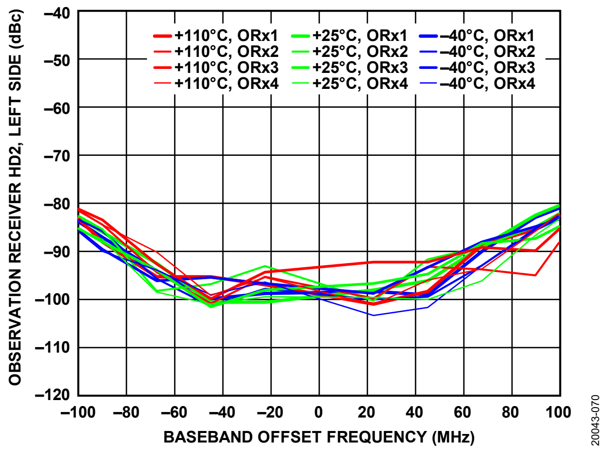


Figure 64. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

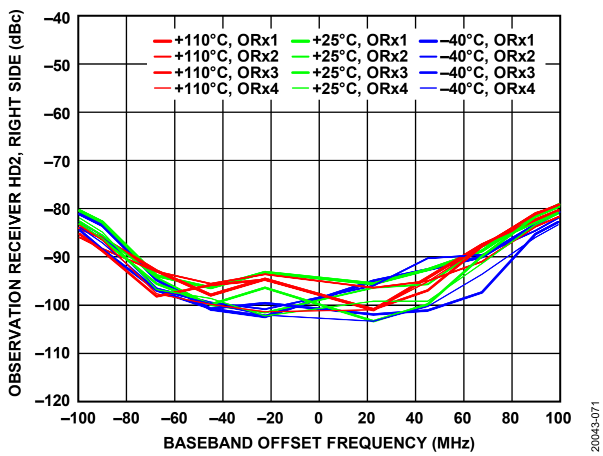


Figure 65. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

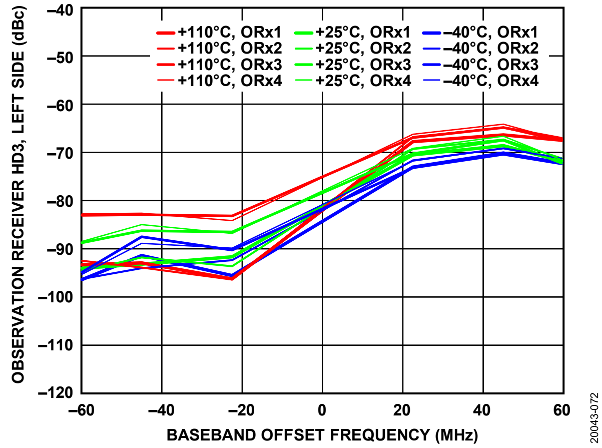


Figure 66. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

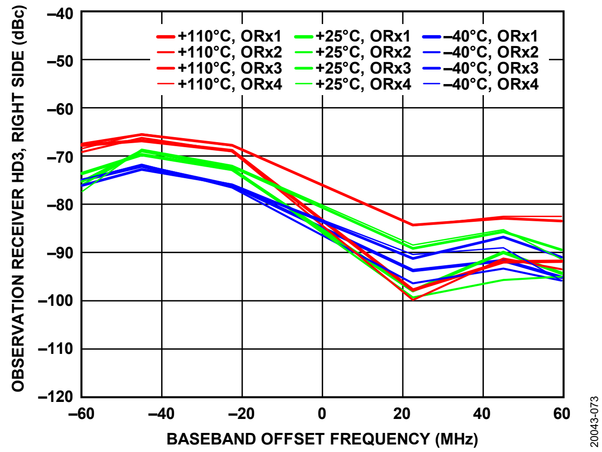


Figure 67. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

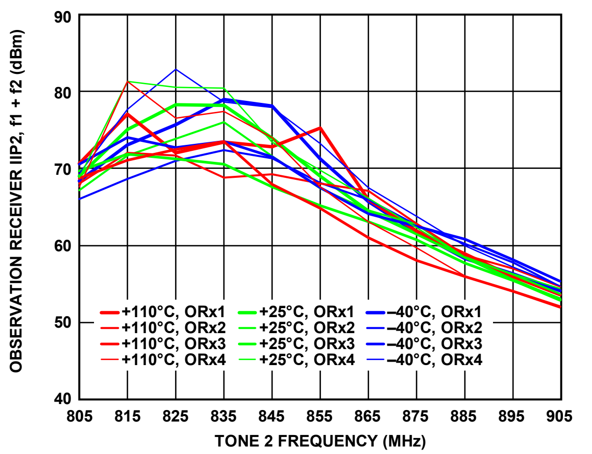


Figure 68. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

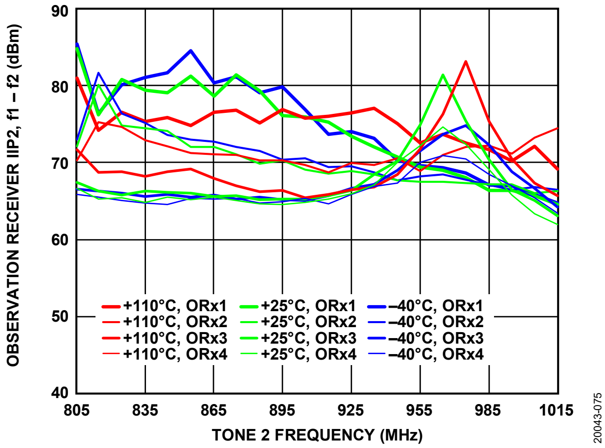


Figure 69. Observation Receiver IIP2, f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

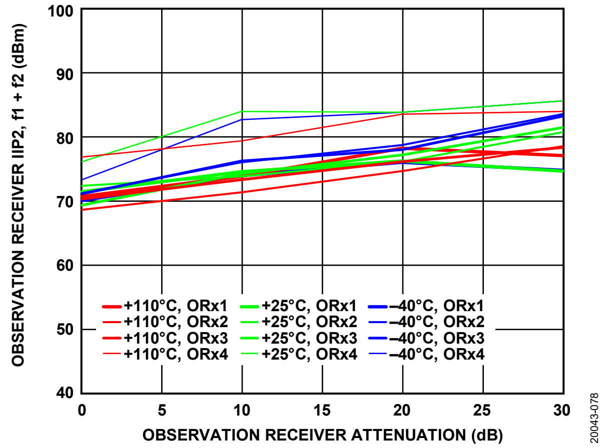


Figure 72. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

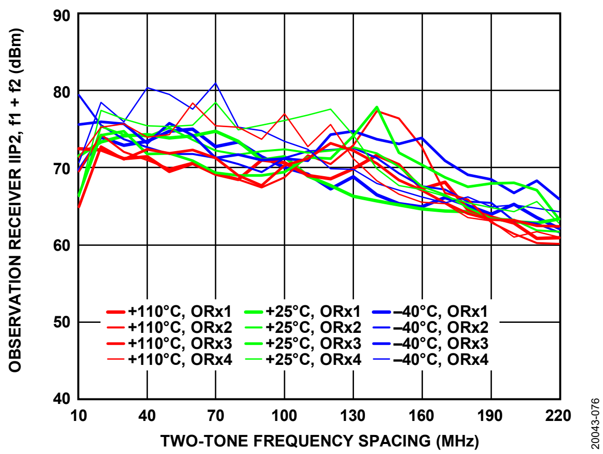


Figure 70. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

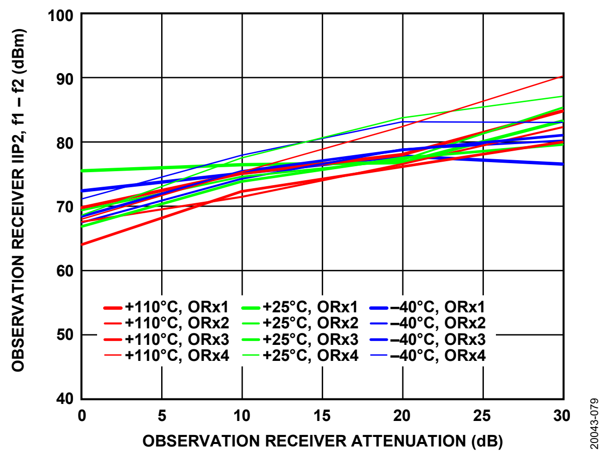


Figure 73. Observation Receiver IIP2, f1 − f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

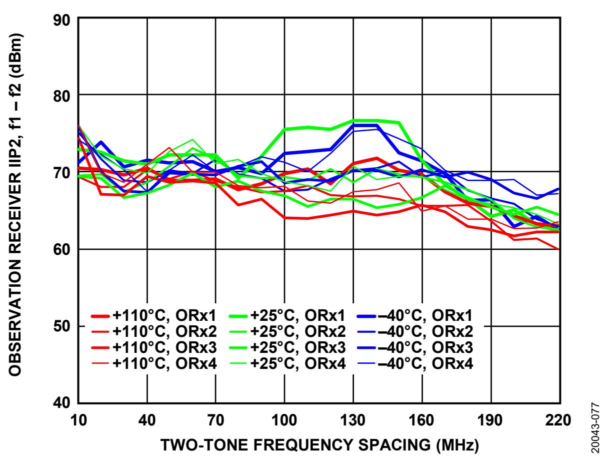


Figure 71. Observation Receiver IIP2, f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

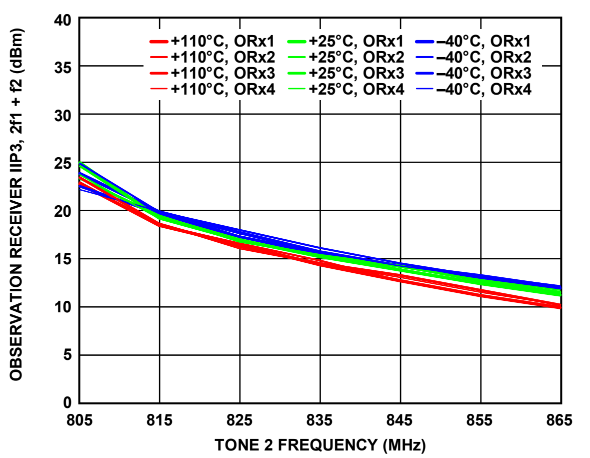


Figure 74. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

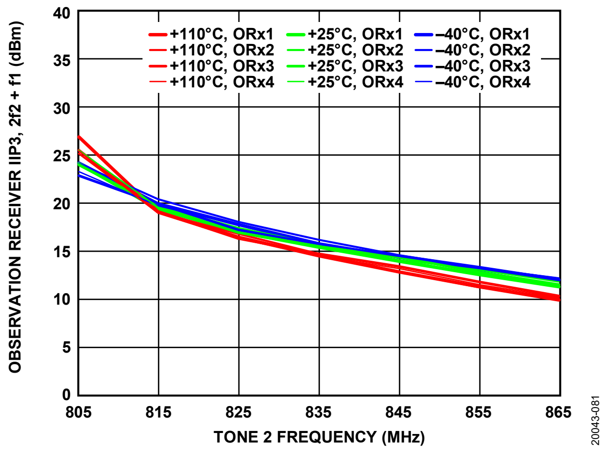


Figure 75. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

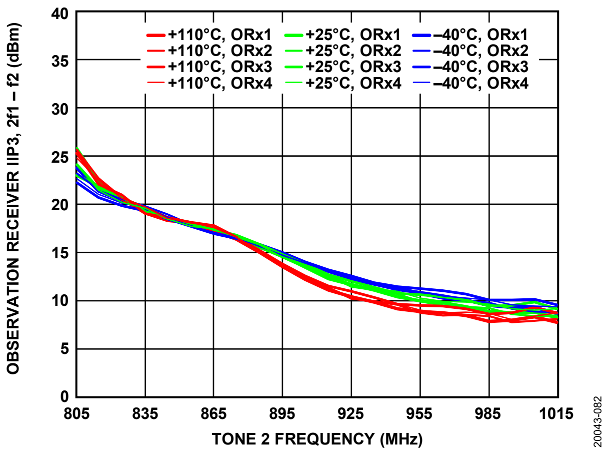


Figure 76. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

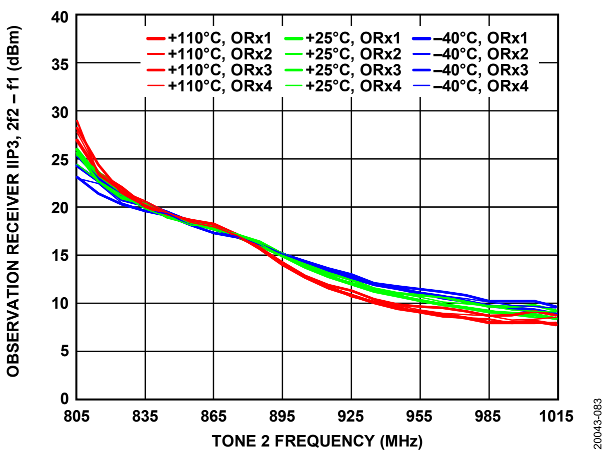


Figure 77. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

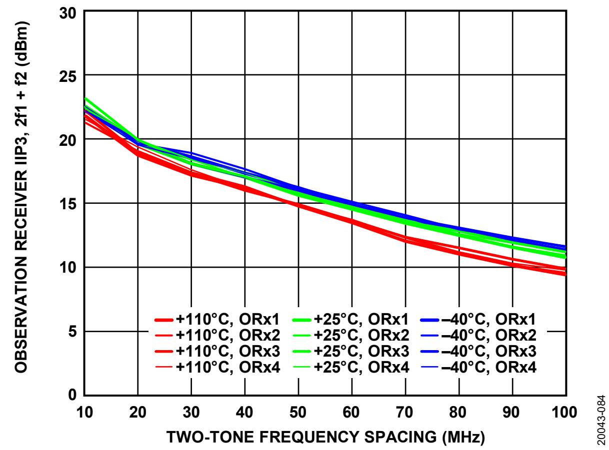


Figure 78. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

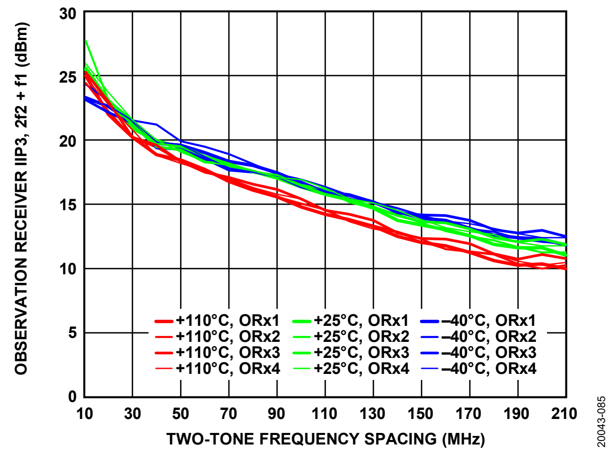


Figure 79. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

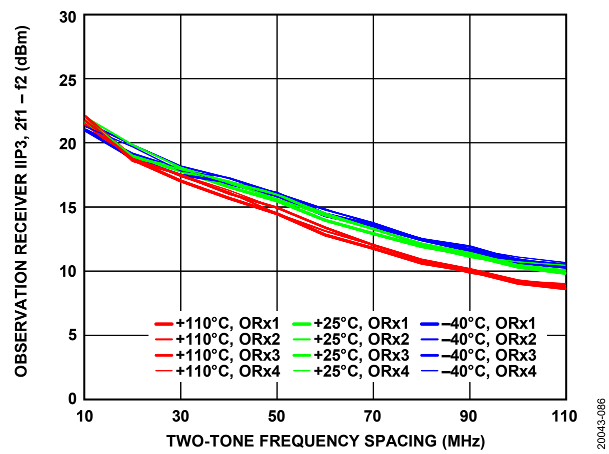


Figure 80. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

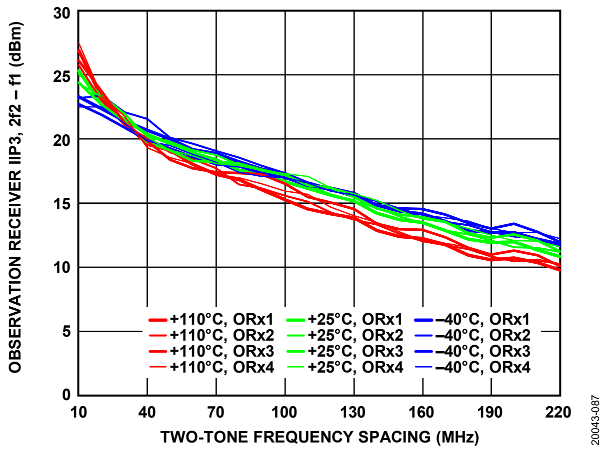


Figure 81. Observation Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

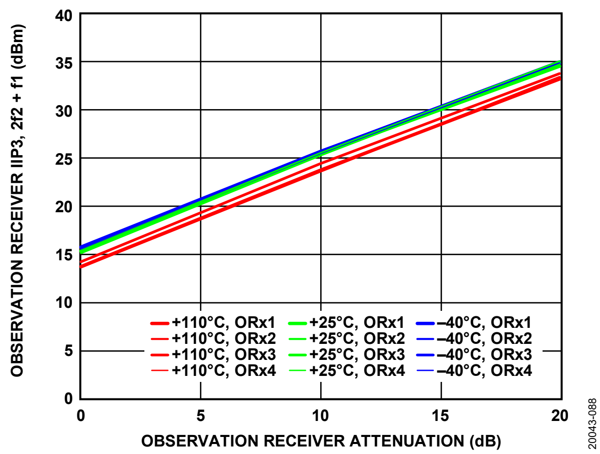


Figure 82. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

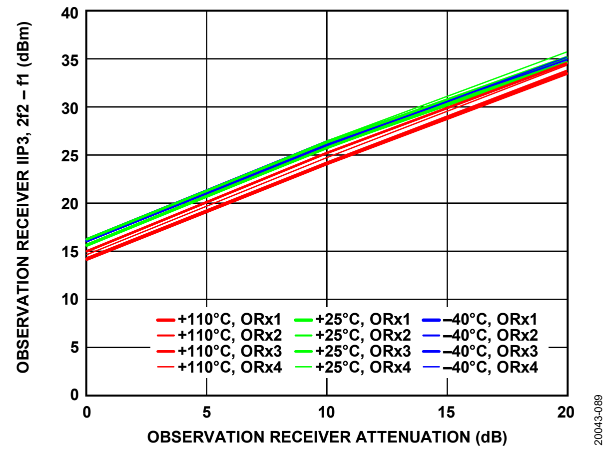


Figure 83. Observation Receiver IIP3, 2f2 – f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

1800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 1800 MHz, unless otherwise noted.

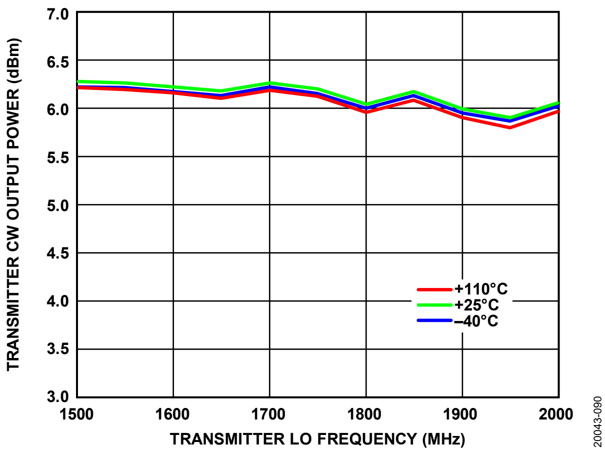


Figure 84. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

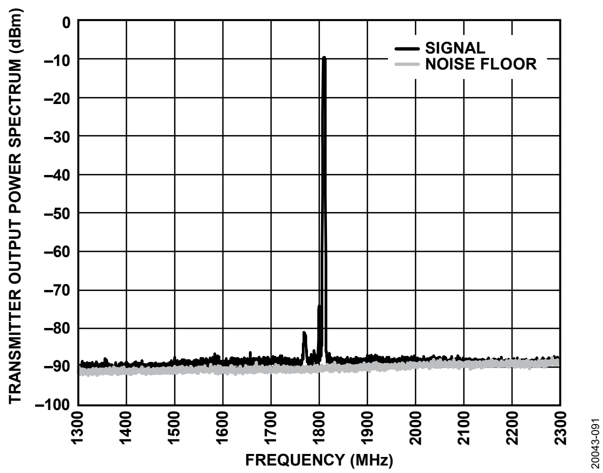


Figure 85. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

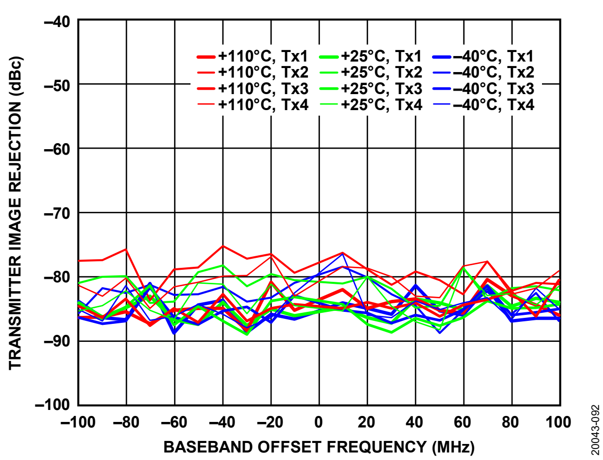


Figure 86. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

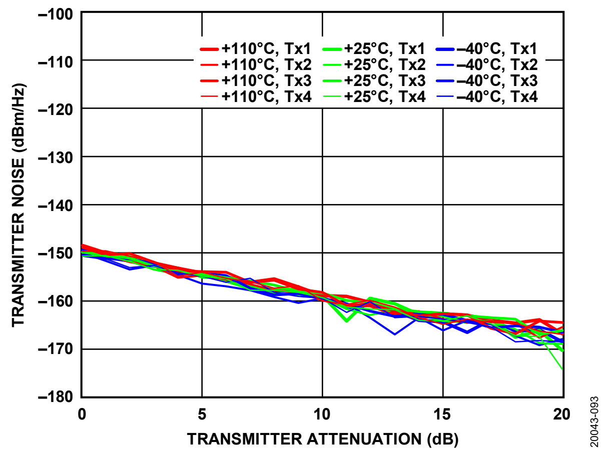


Figure 87. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset Frequency

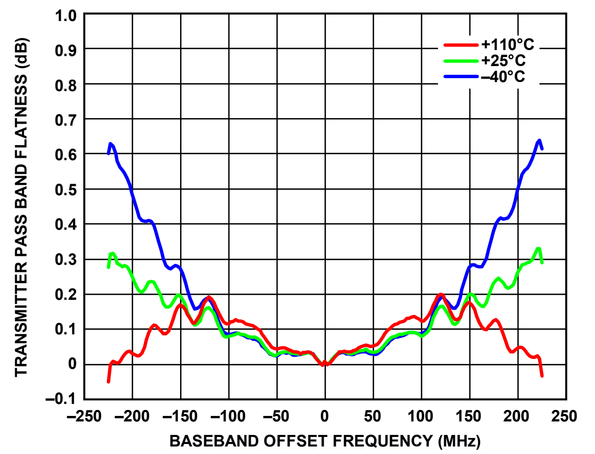


Figure 88. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

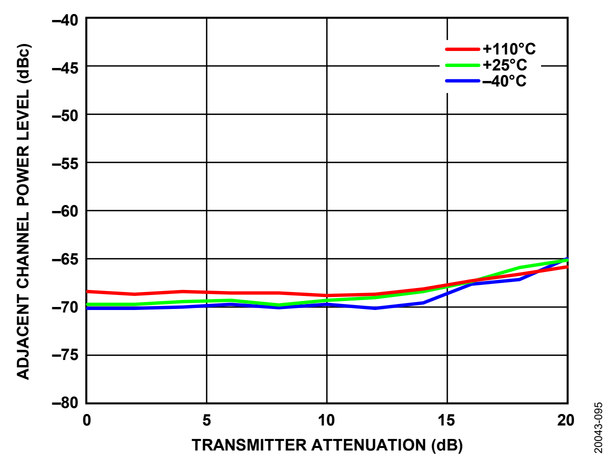


Figure 89. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

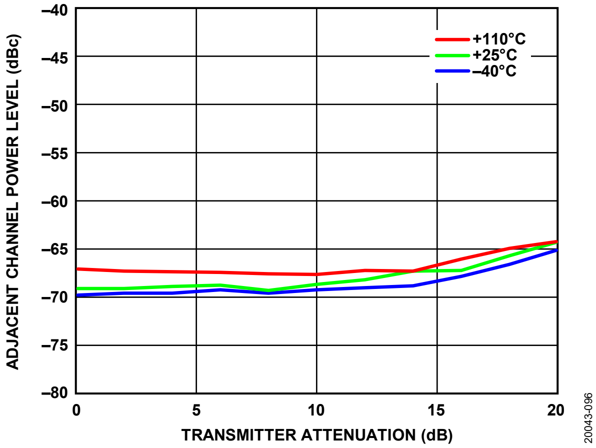


Figure 90. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

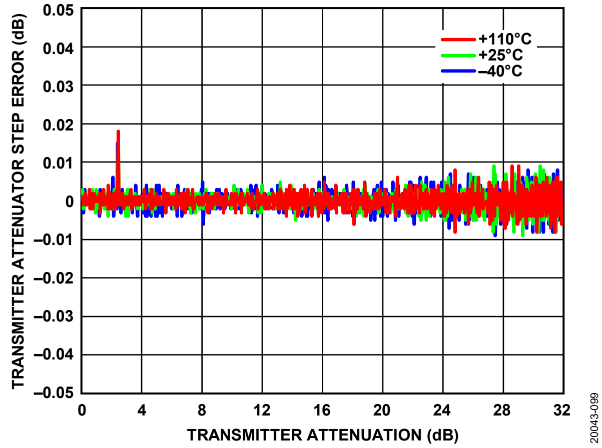


Figure 93. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

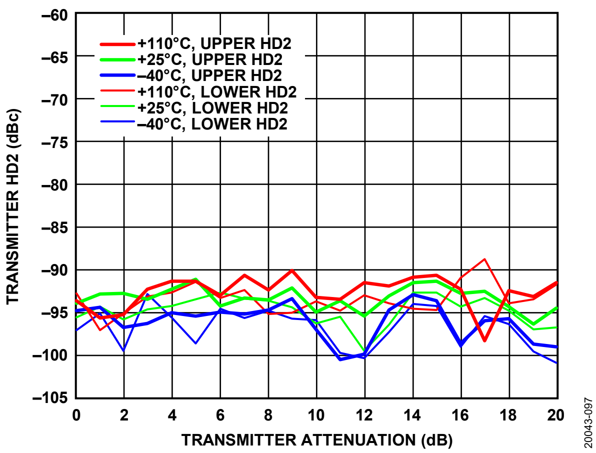


Figure 91. Transmitter HD2 vs. Transmitter Attenuation, 10 MHz Offset

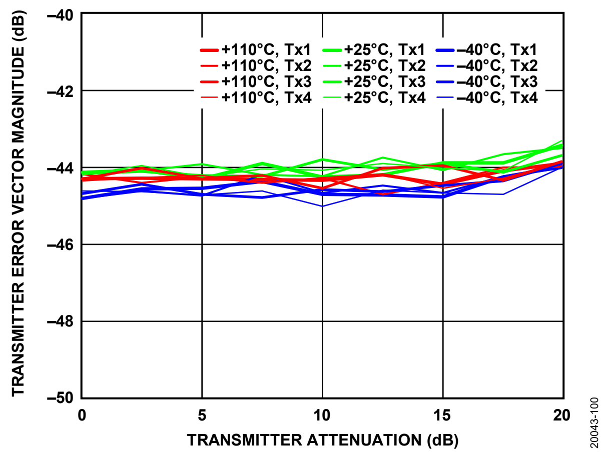


Figure 94. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

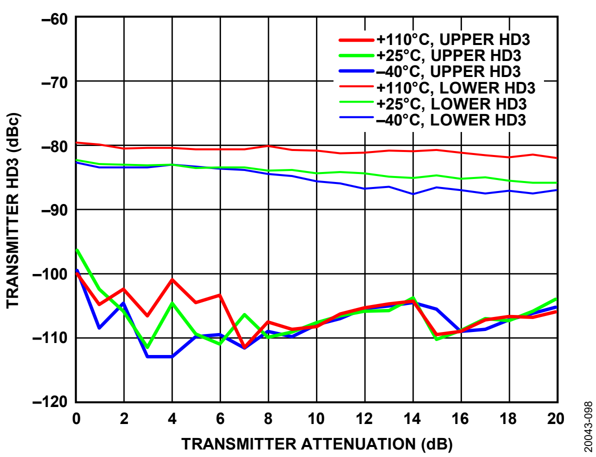


Figure 92. Transmitter HD3 vs. Transmitter Attenuation, 10 MHz Offset

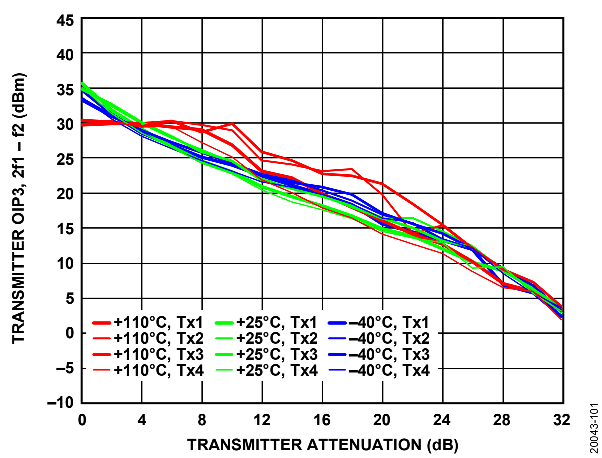


Figure 95. Transmitter OIP3, 2f1 − f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

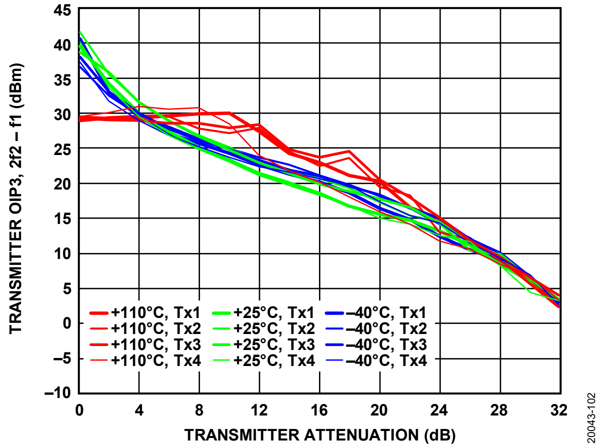


Figure 96. Transmitter OIP3, 2f2 – f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

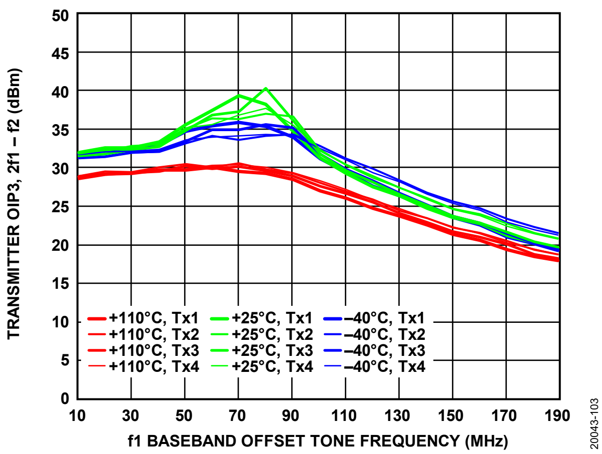


Figure 97. Transmitter OIP3, 2f1 – f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

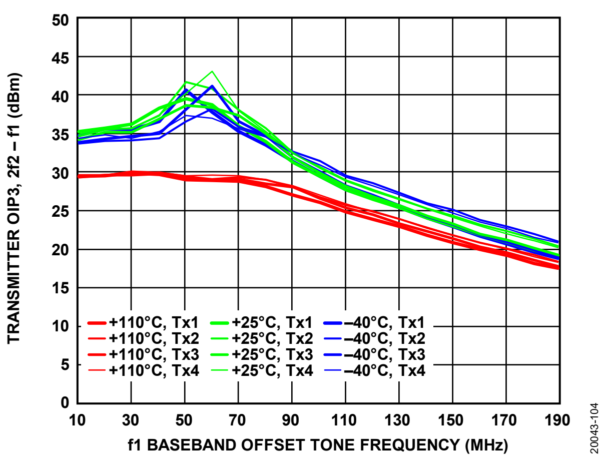


Figure 98. Transmitter OIP3, 2f2 – f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

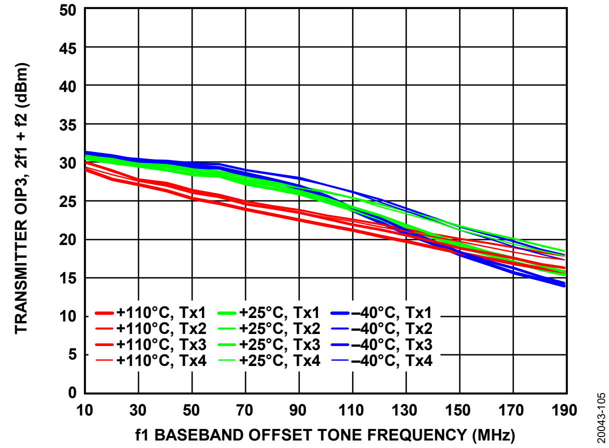


Figure 99. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

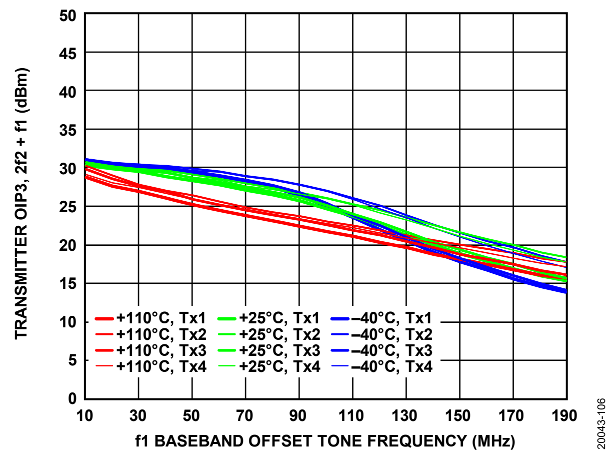


Figure 100. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

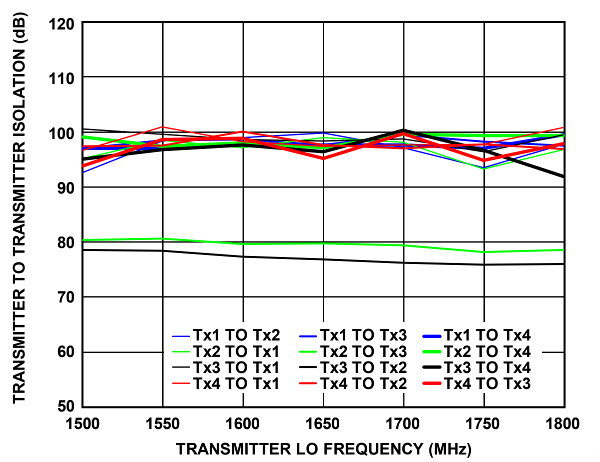


Figure 101. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

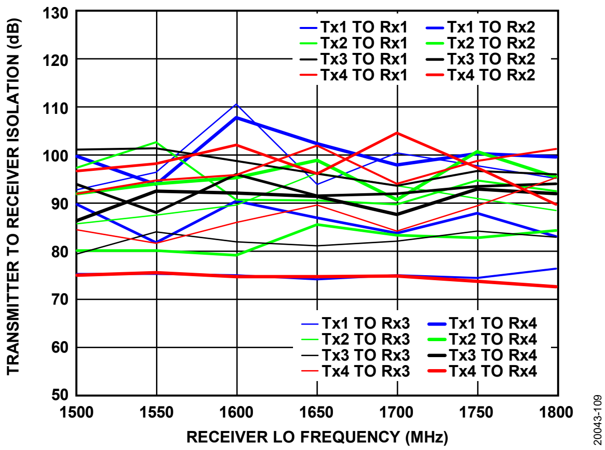


Figure 102. Transmitter to Receiver Isolation vs. Receiver LO Frequency

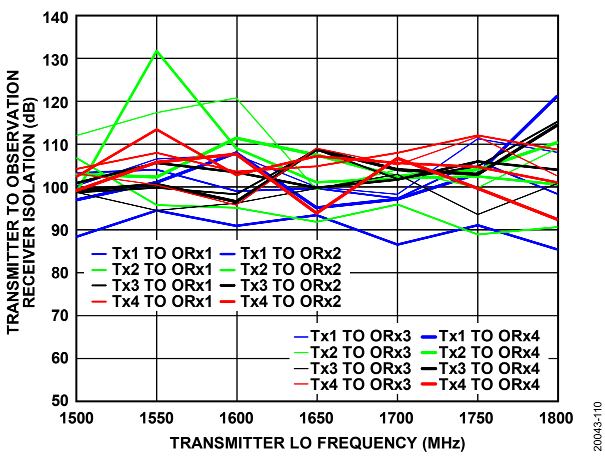


Figure 103. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

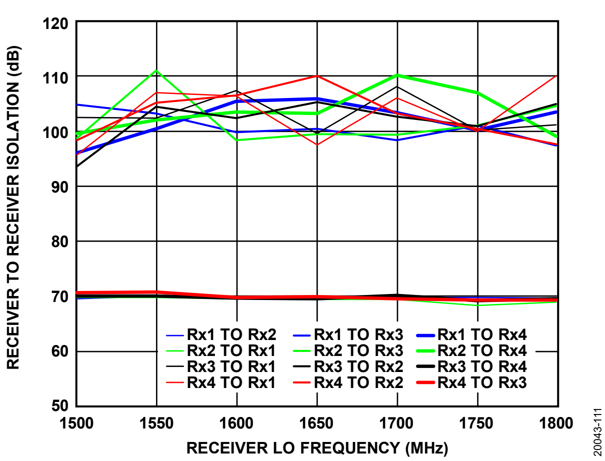


Figure 104. Receiver to Receiver Isolation vs. Receiver LO Frequency

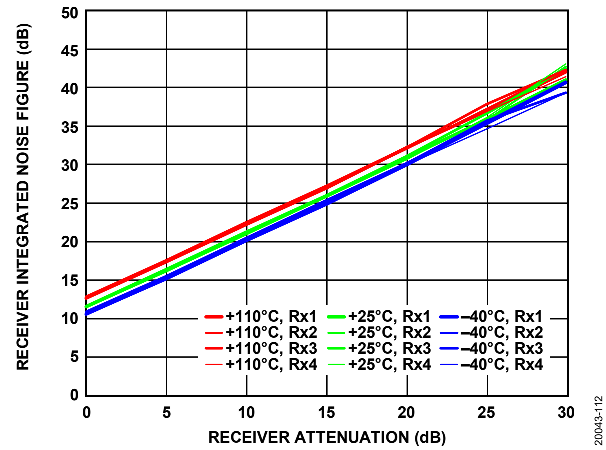


Figure 105. Receiver Integrated Noise Figure vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

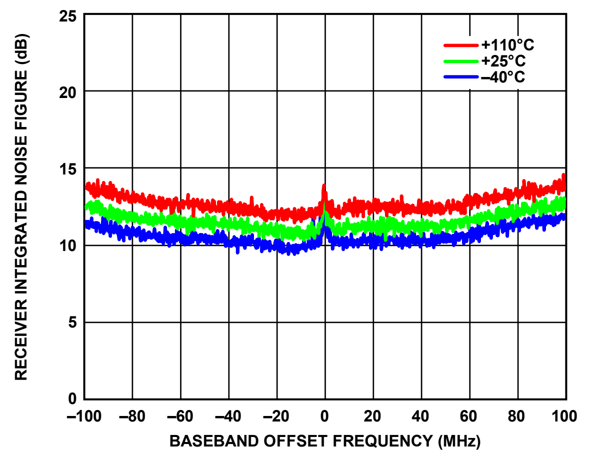


Figure 106. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

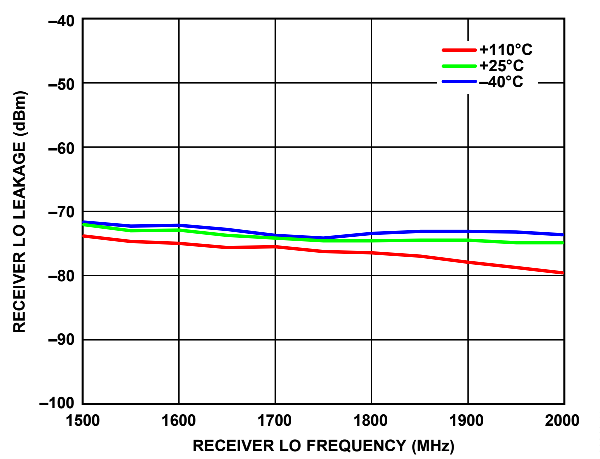


Figure 107. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

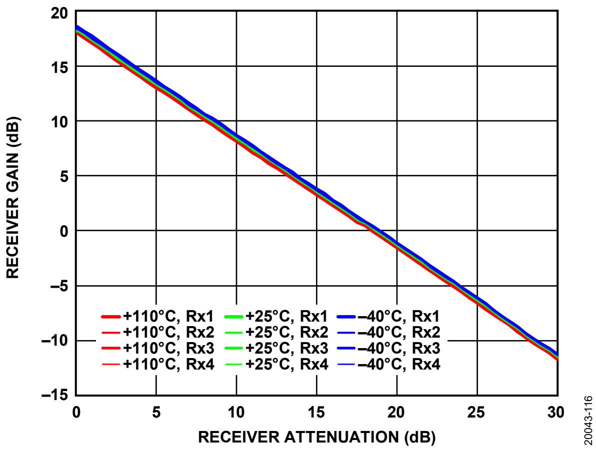


Figure 108. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

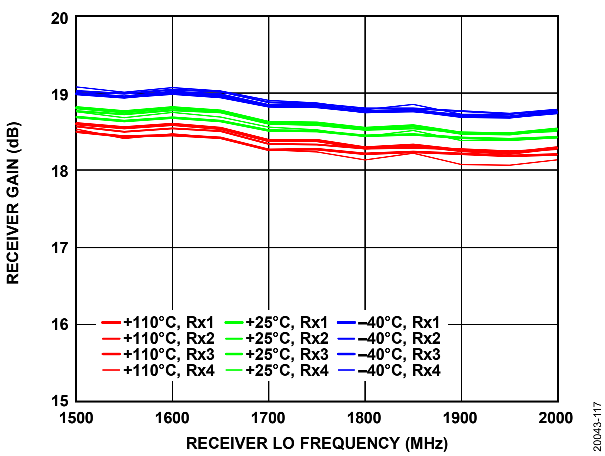


Figure 109. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

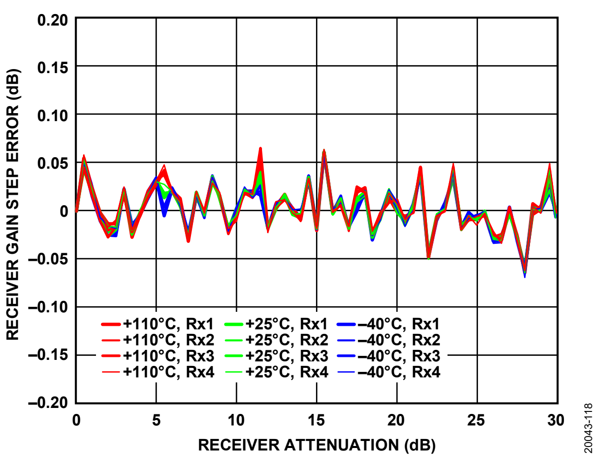


Figure 110. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

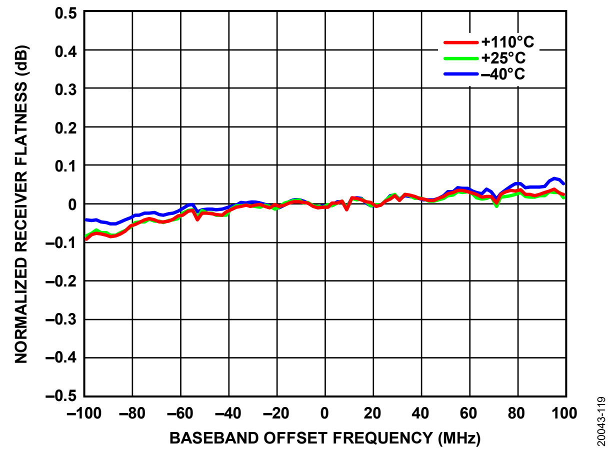


Figure 111. Normalized Receiver Flatness vs. Baseband Offset Frequency, −5 dBFS Input Signal

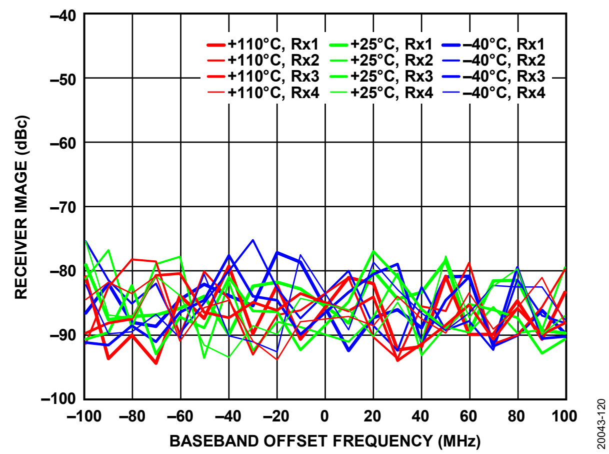


Figure 112. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

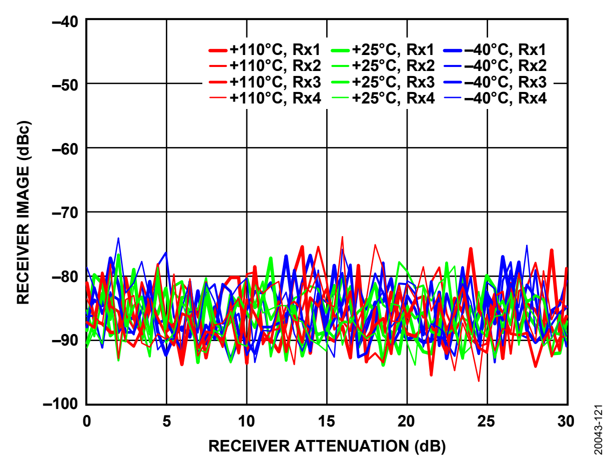


Figure 113. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

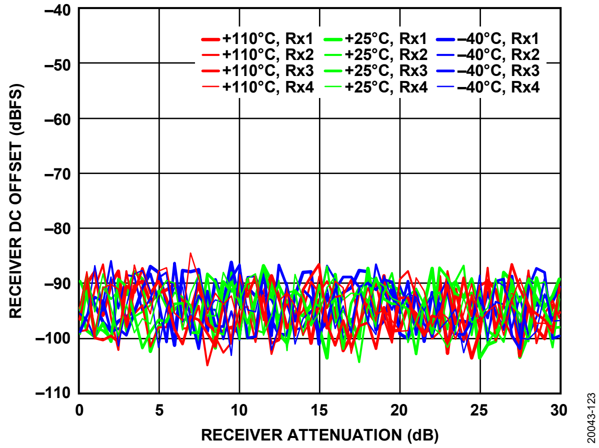


Figure 114. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

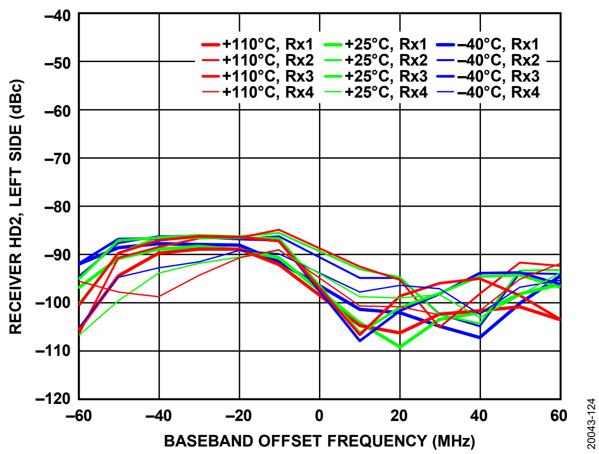


Figure 115. Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

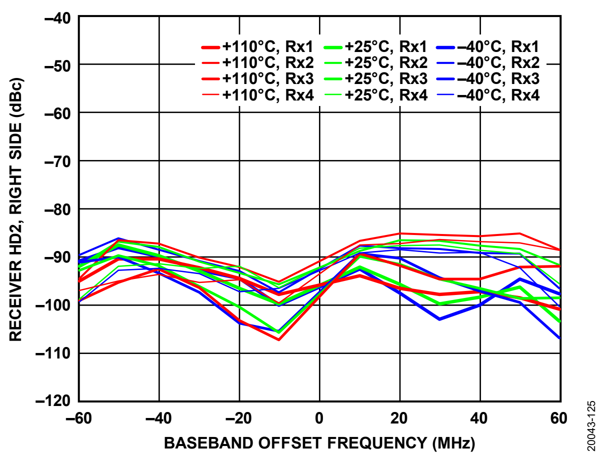


Figure 116. Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

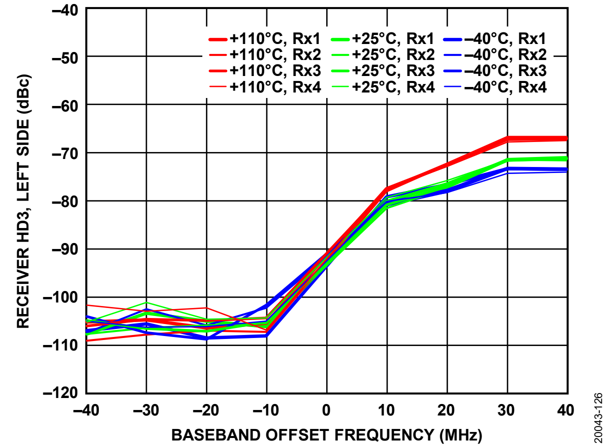


Figure 117. Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

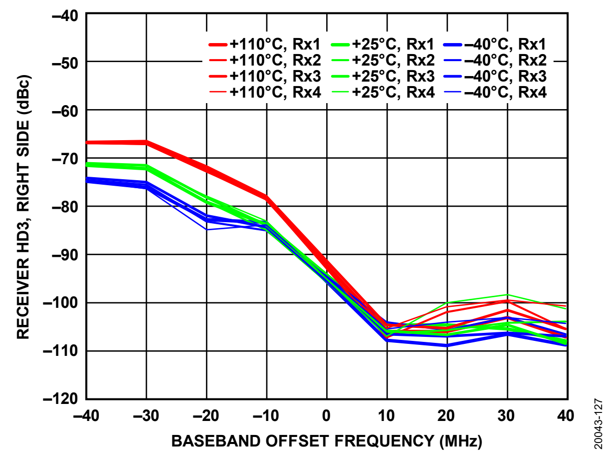


Figure 118. Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

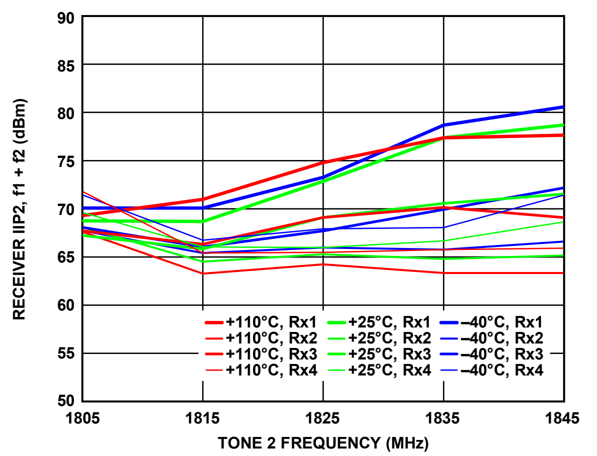


Figure 119. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

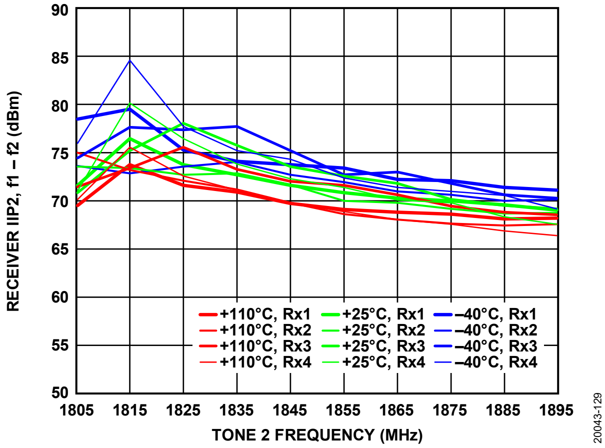


Figure 120. Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

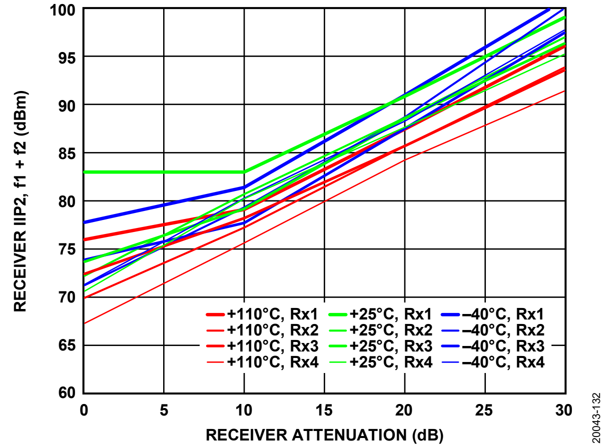


Figure 123. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

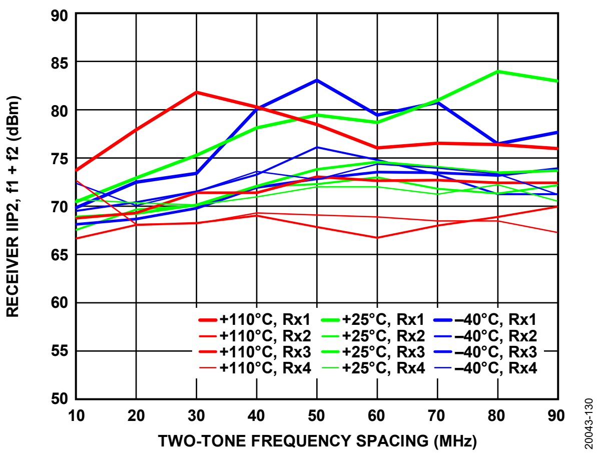


Figure 121. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

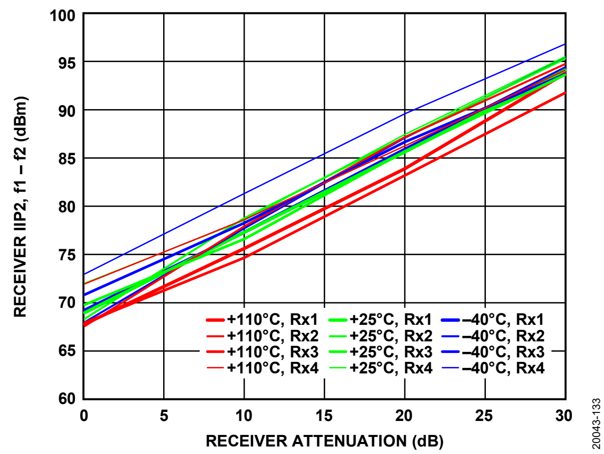


Figure 124. Receiver IIP2, f1 – f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

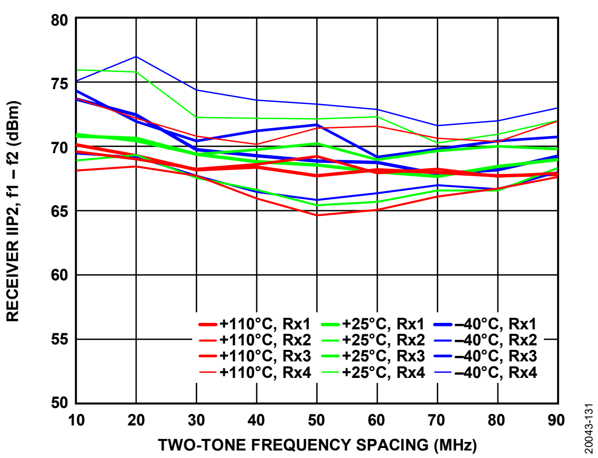


Figure 122. Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

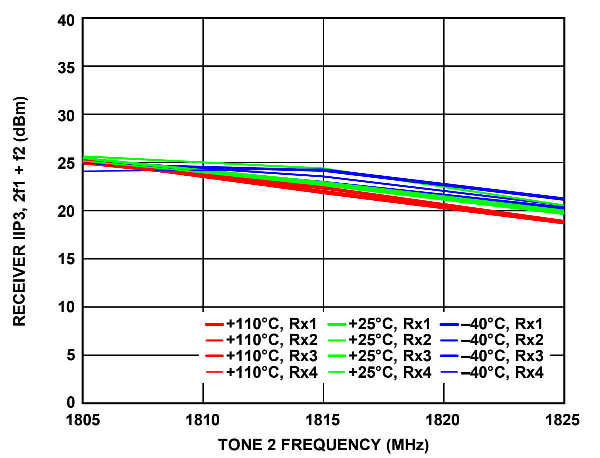


Figure 125. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

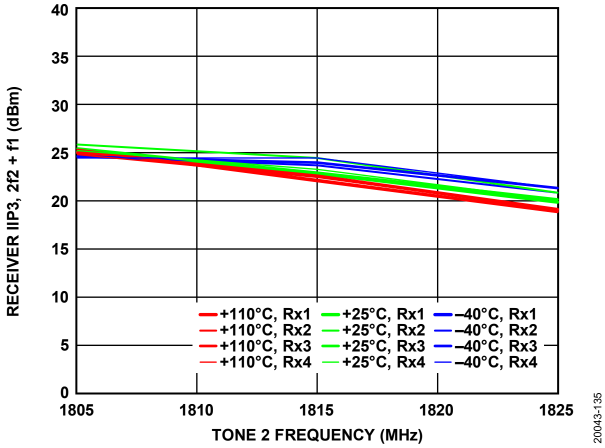


Figure 126. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

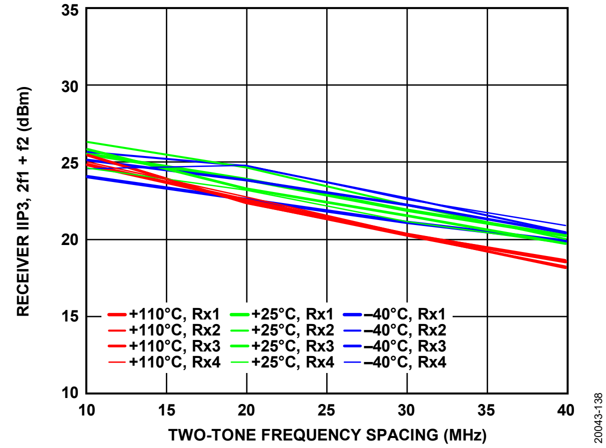


Figure 129. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

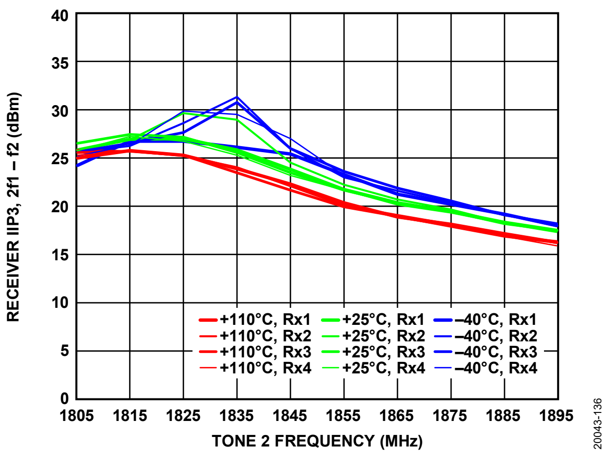


Figure 127. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

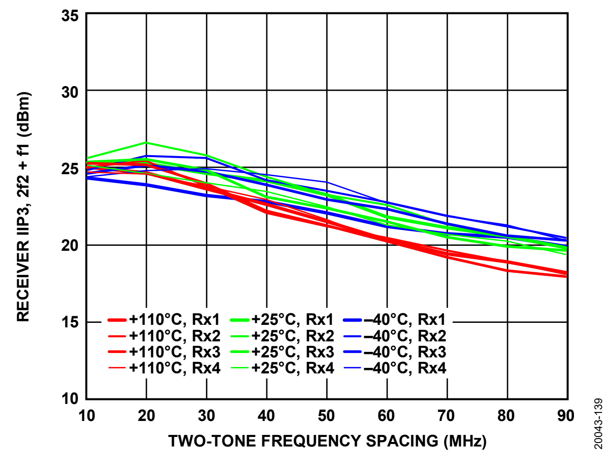


Figure 130. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

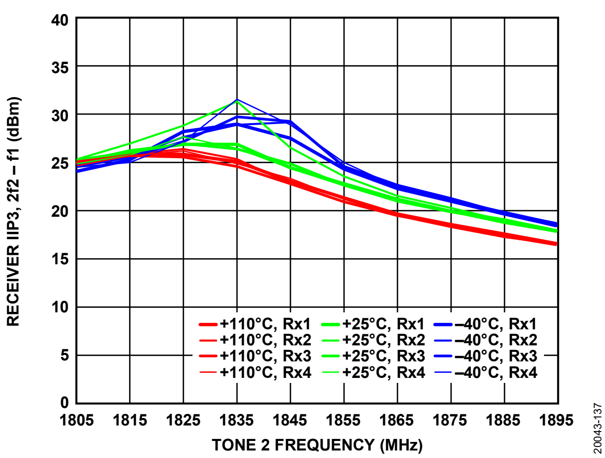


Figure 128. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

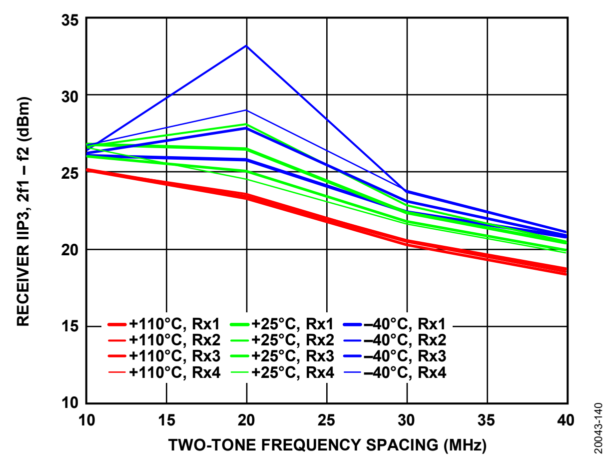


Figure 131. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

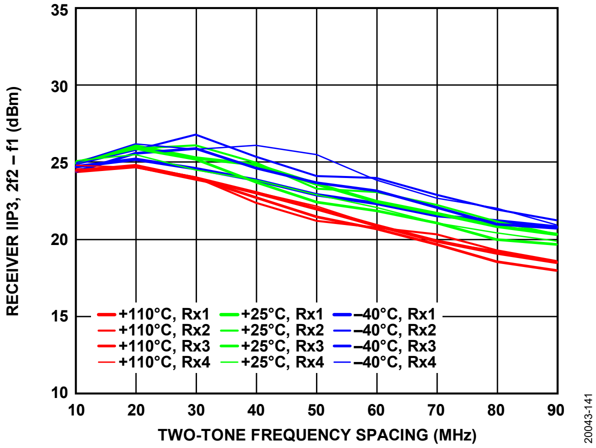


Figure 132. Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

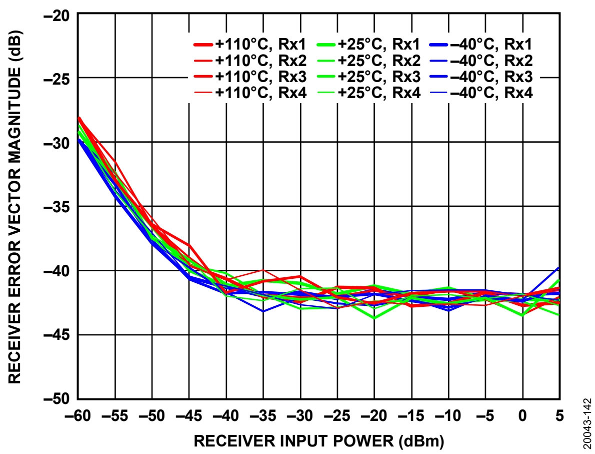


Figure 133. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 50 kHz, Loop Filter Phase Margin = 40°

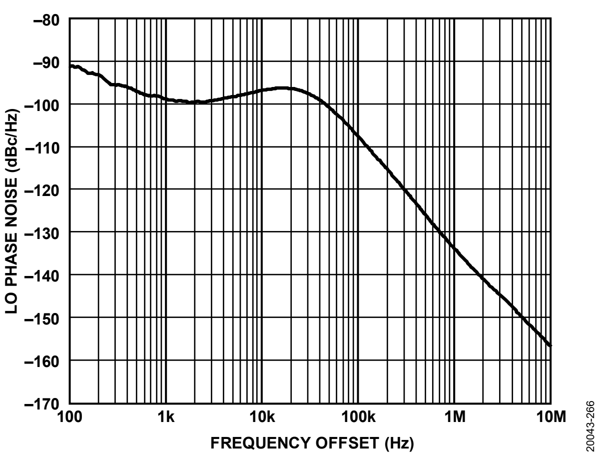


Figure 134. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 50 kHz, Phase Margin = 85°

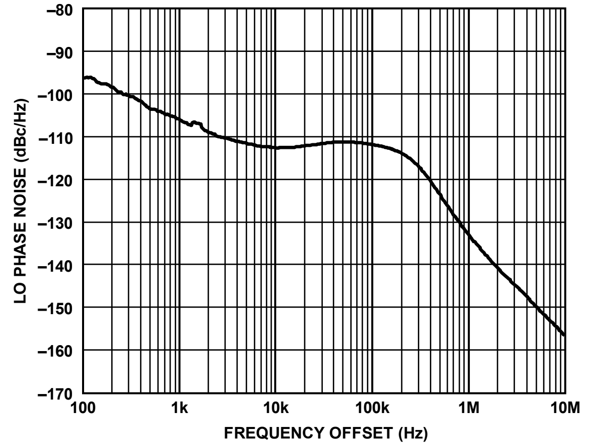


Figure 135. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 100 kHz, Phase Margin = 60°

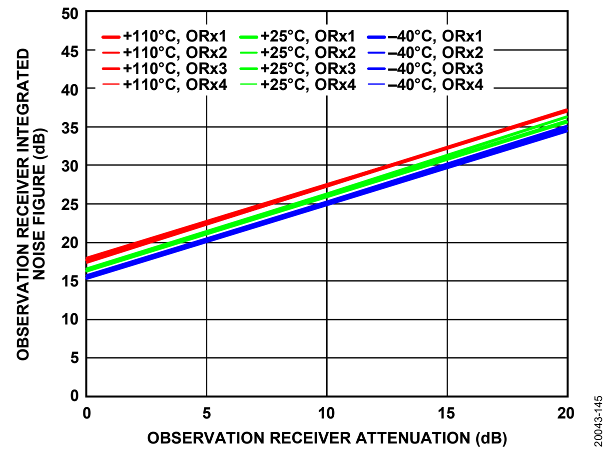


Figure 136. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

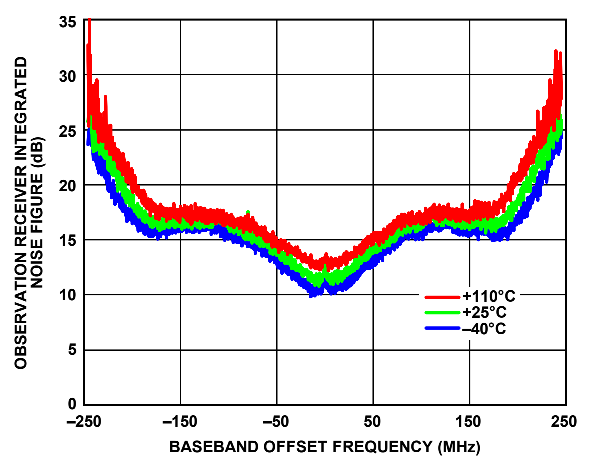


Figure 137. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

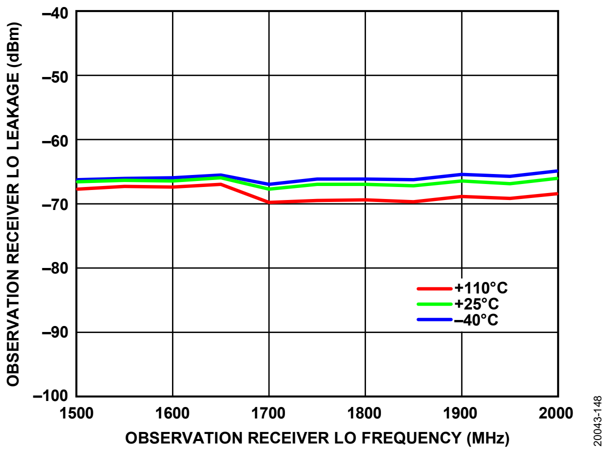


Figure 138. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

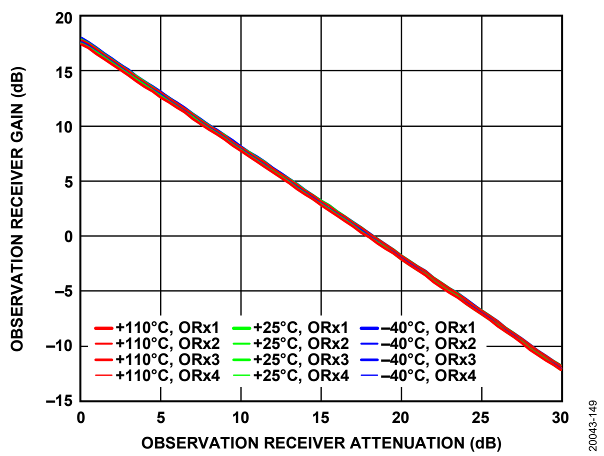


Figure 139. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

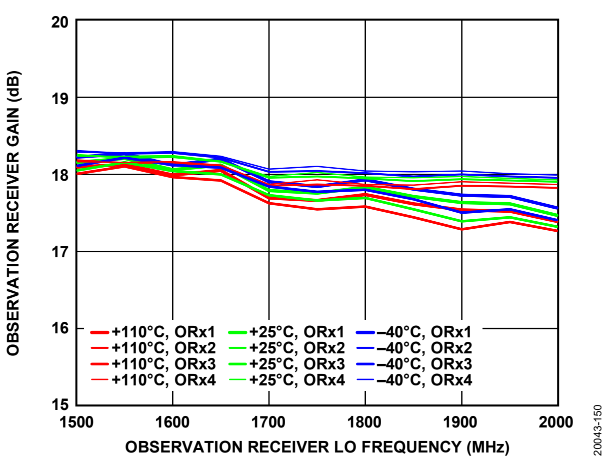


Figure 140. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

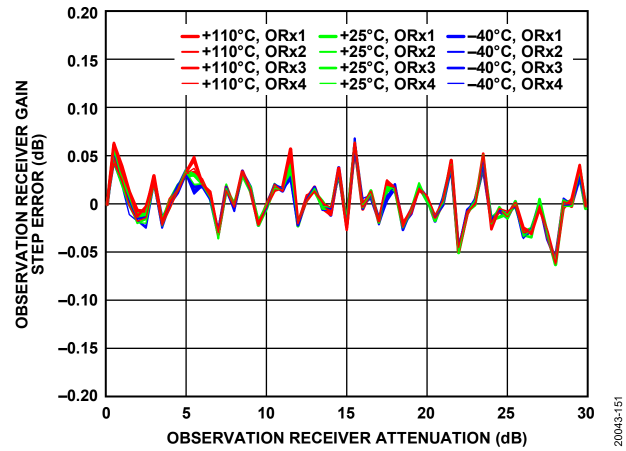


Figure 141. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

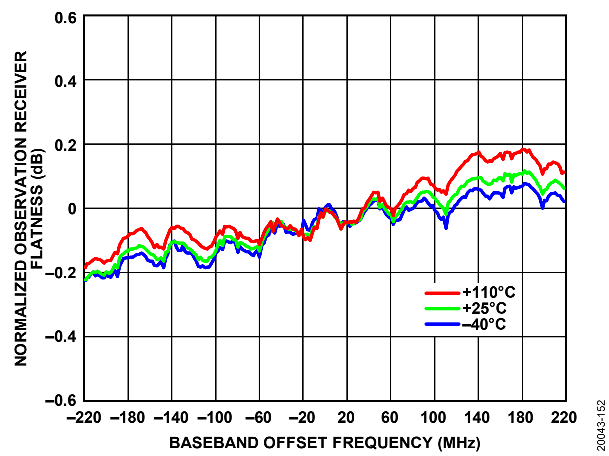


Figure 142. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, −25 dBm Input Signal, 0 dB Attenuation

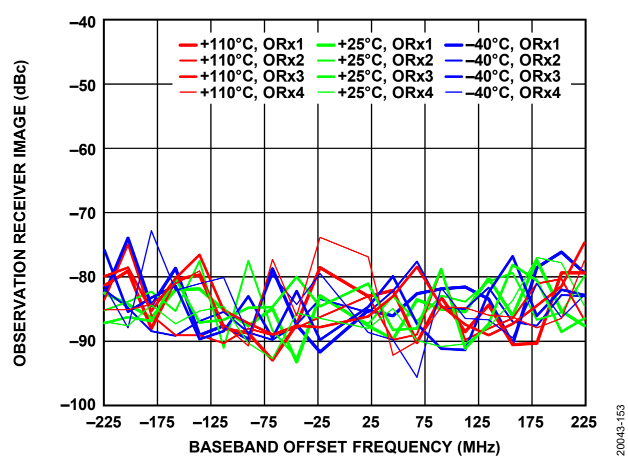


Figure 143. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

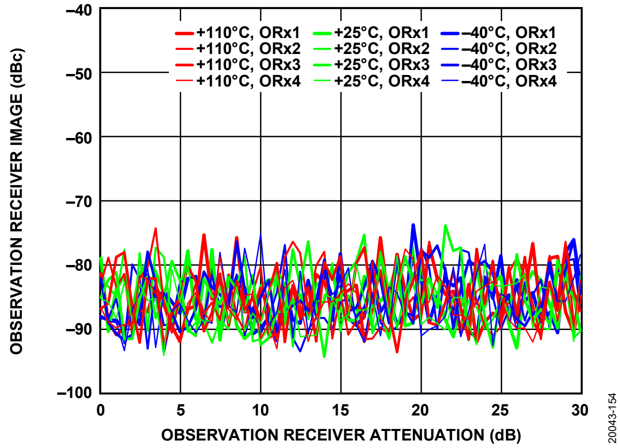


Figure 144. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

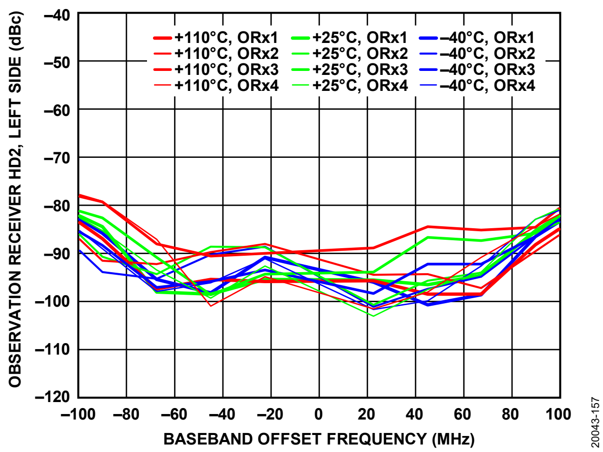


Figure 145. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

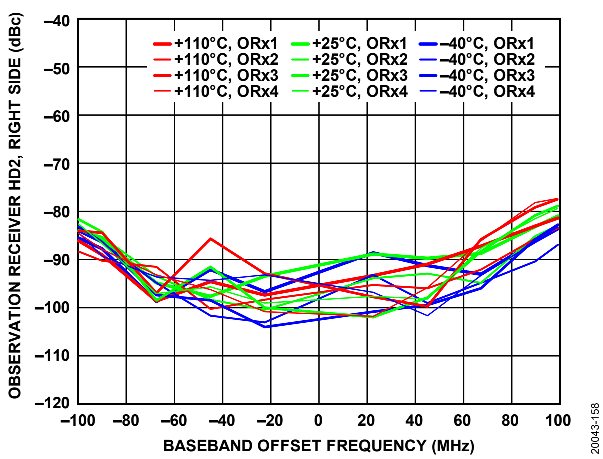


Figure 146. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

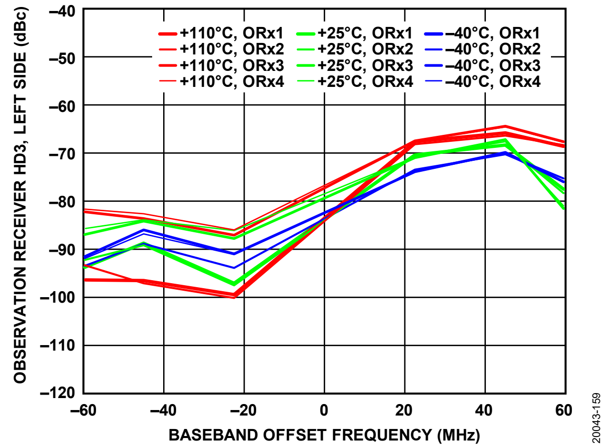


Figure 147. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

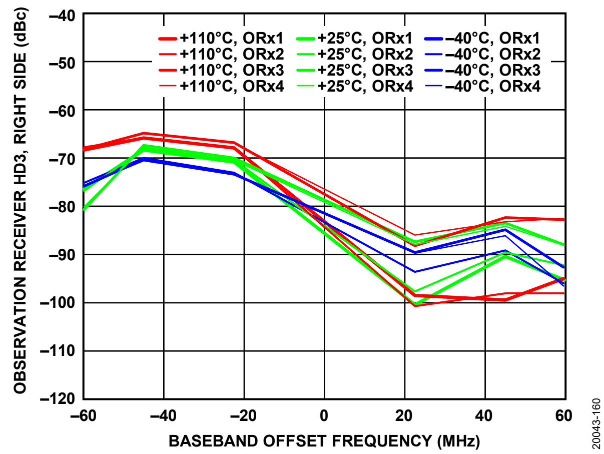


Figure 148. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

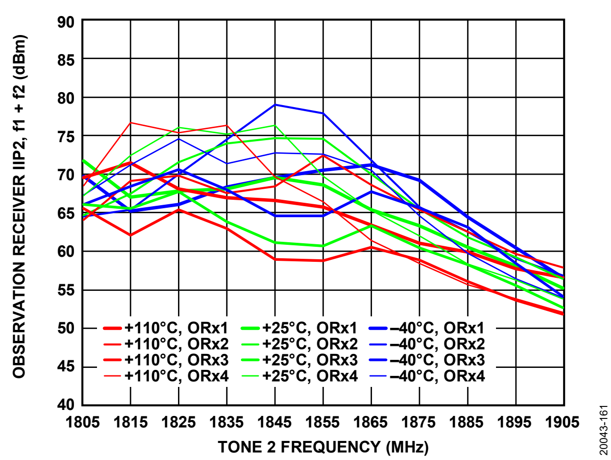


Figure 149. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

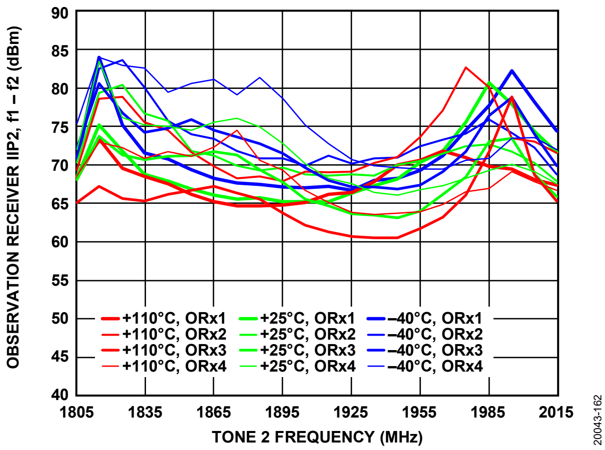


Figure 150. Observation Receiver IIP2, f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

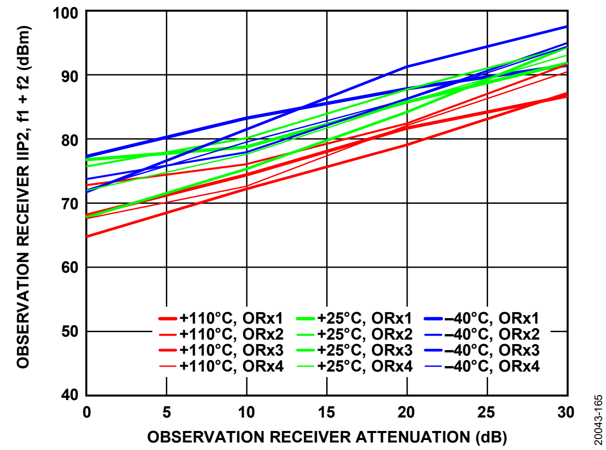


Figure 153. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

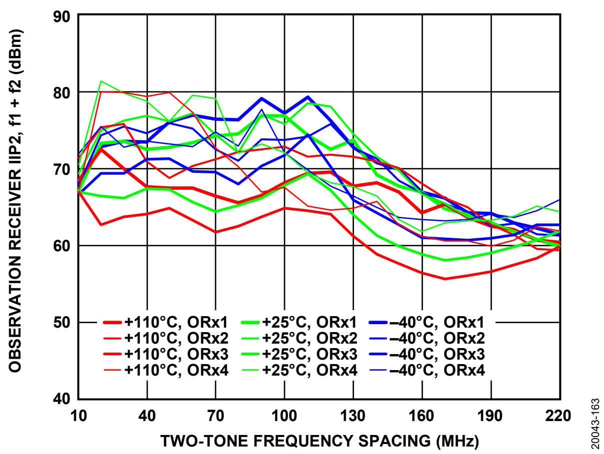


Figure 151. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

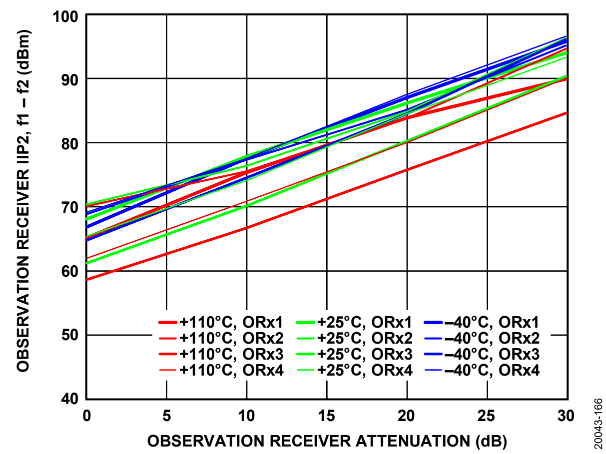


Figure 154. Observation Receiver IIP2, f1 − f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

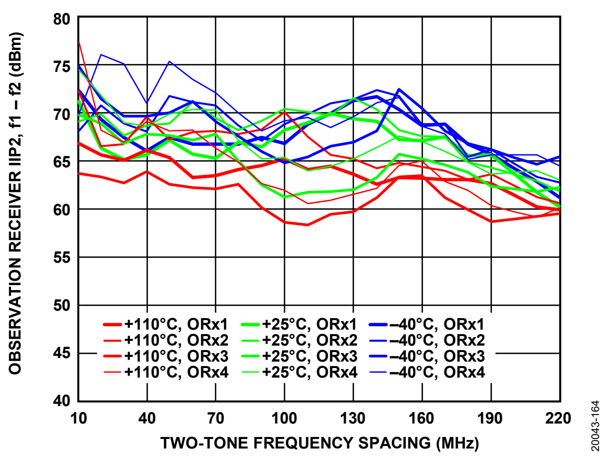


Figure 152. Observation Receiver IIP2, f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

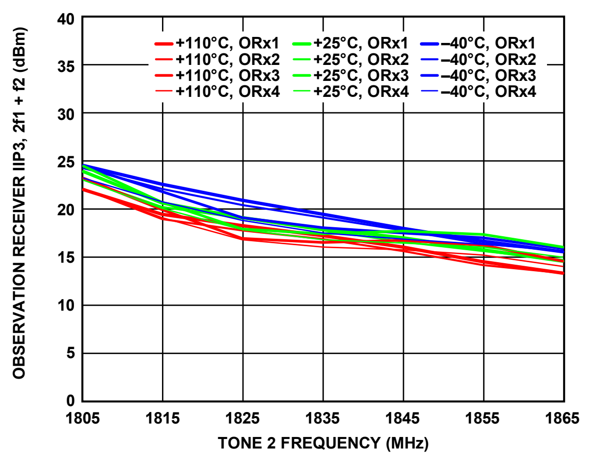


Figure 155. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

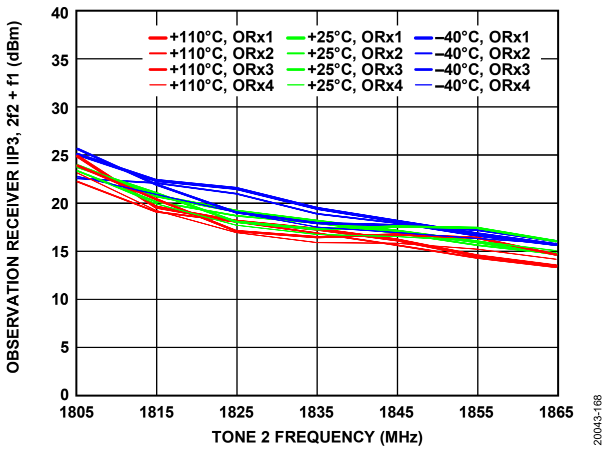


Figure 156. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

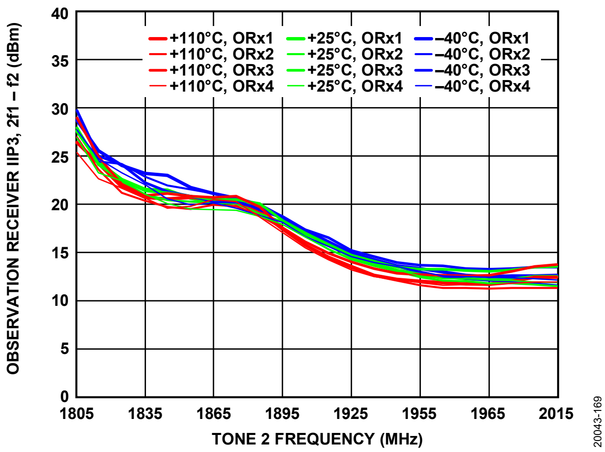


Figure 157. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

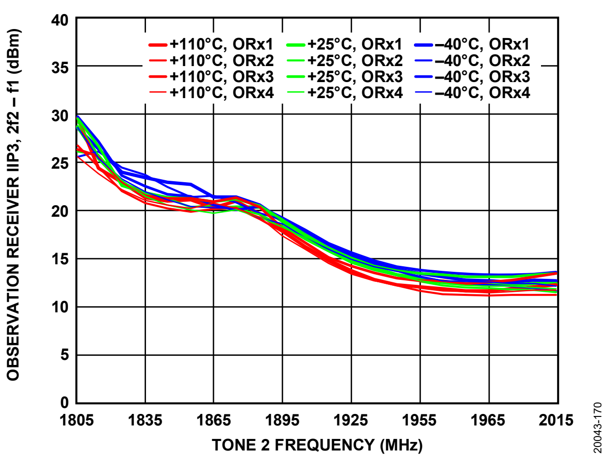


Figure 158. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

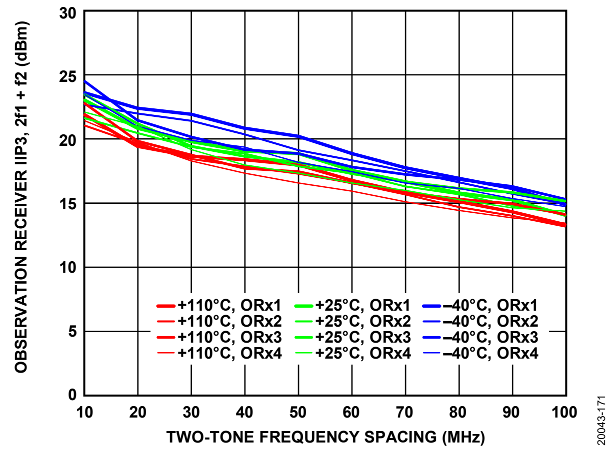


Figure 159. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

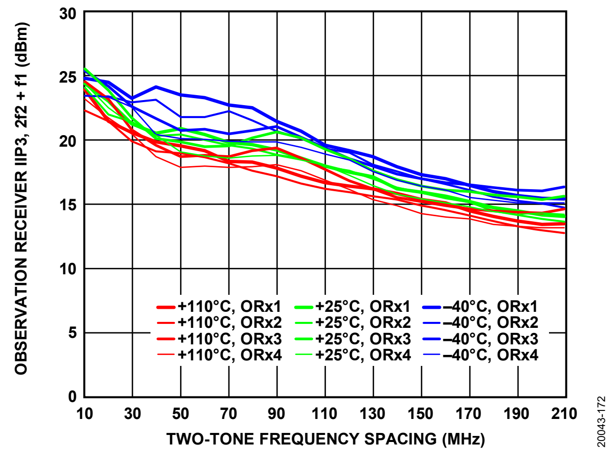


Figure 160. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

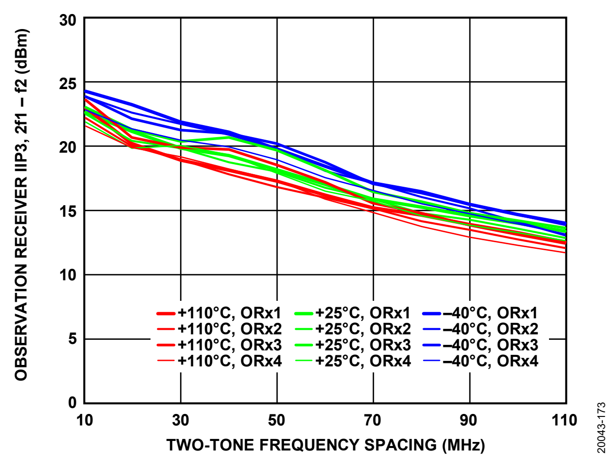


Figure 161. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

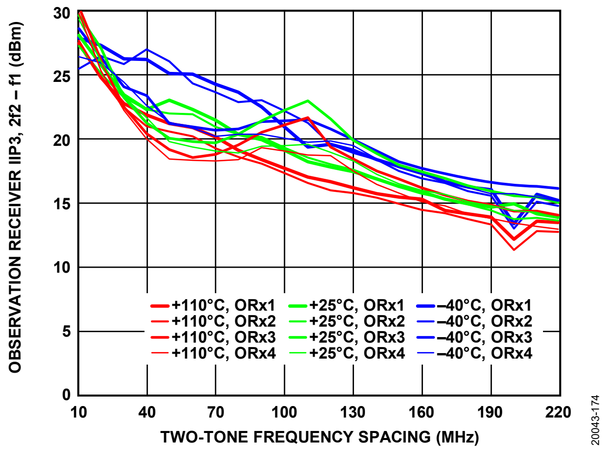


Figure 162. Observation Receiver IIP3, 2f2 − f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

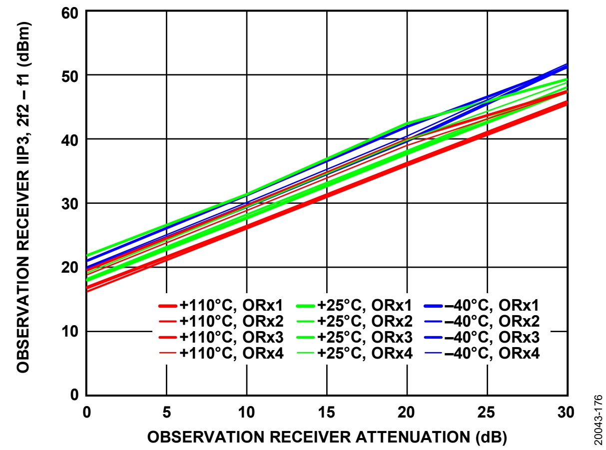


Figure 164. Observation Receiver IIP3, 2f2 − f1 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 122 MHz, f2 = 2 MHz

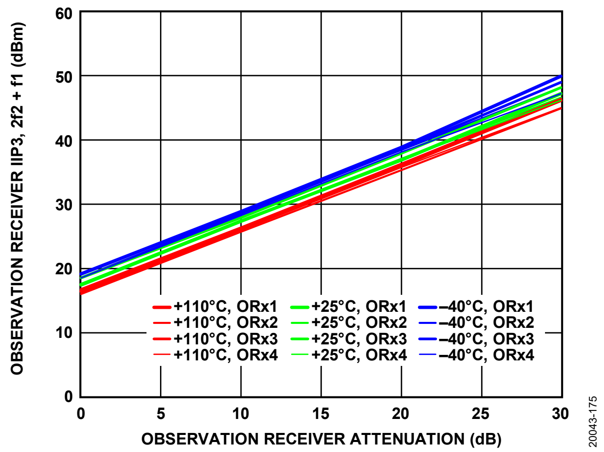


Figure 163. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 122 MHz, f2 = 2 MHz

2600 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 2600 MHz, unless otherwise noted.

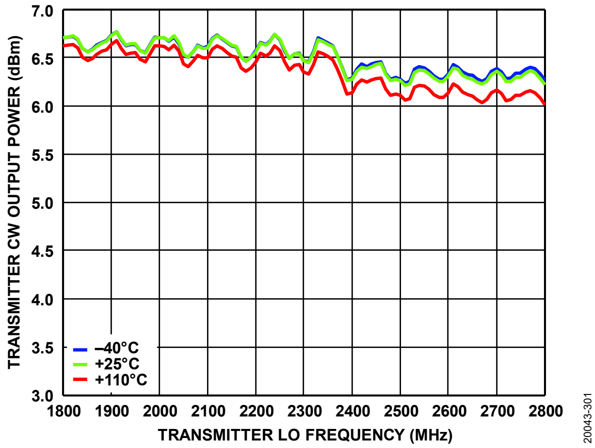


Figure 165. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

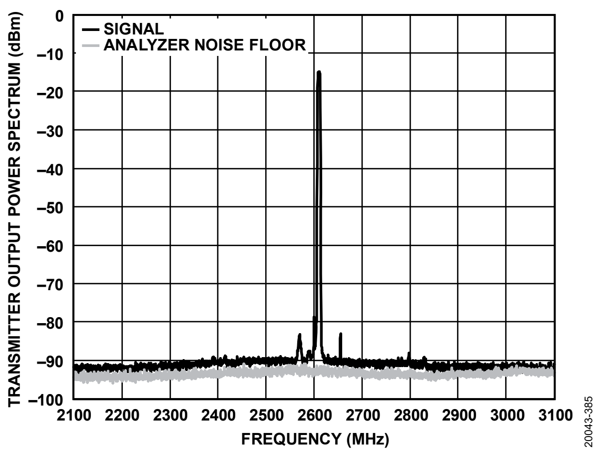


Figure 166. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

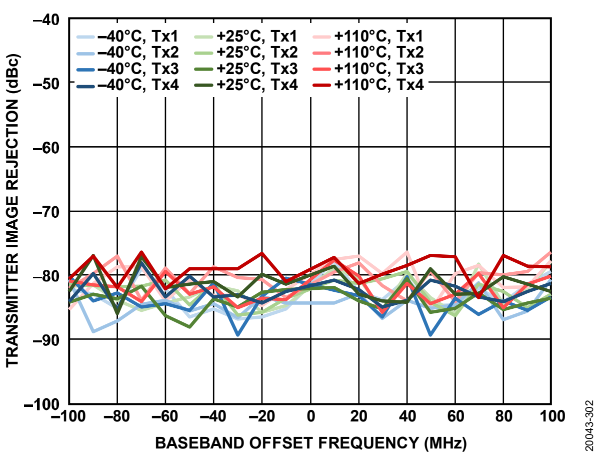


Figure 167. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

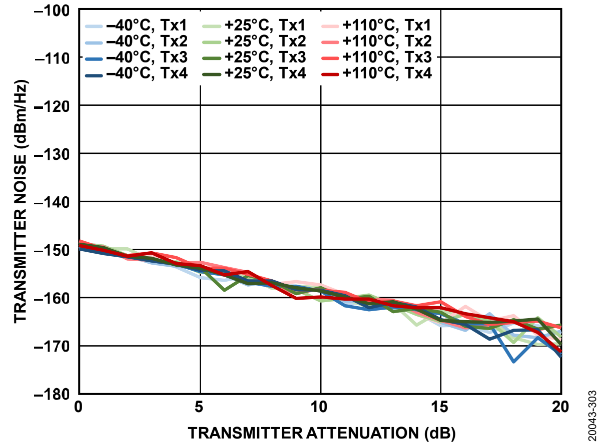


Figure 168. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset

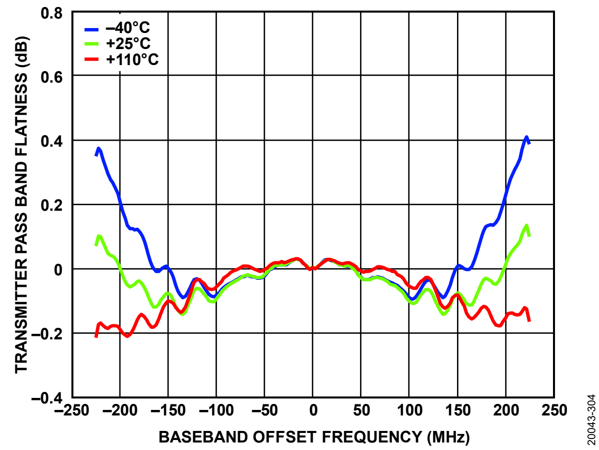


Figure 169. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

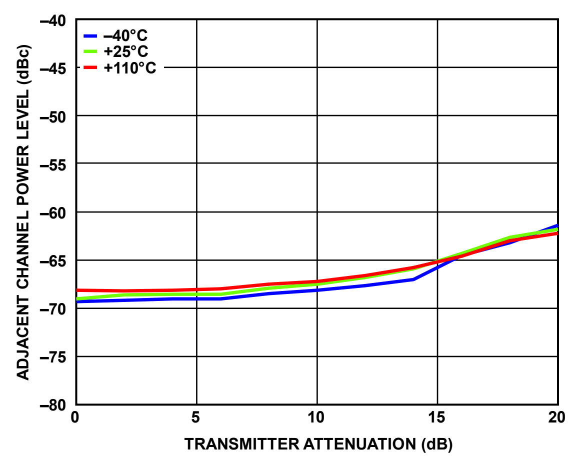


Figure 170. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

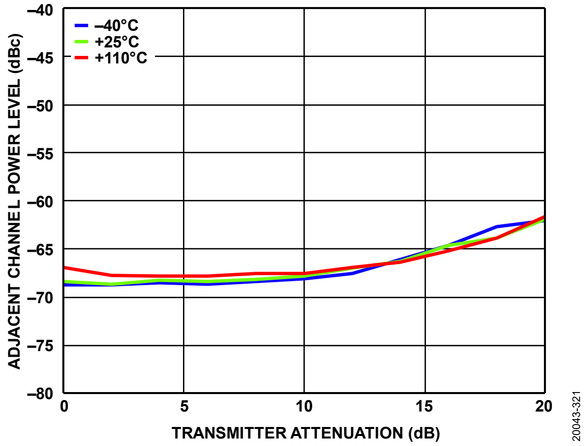


Figure 171. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

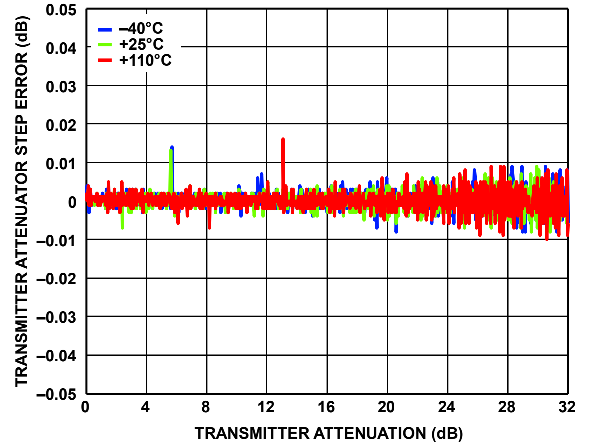


Figure 174. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

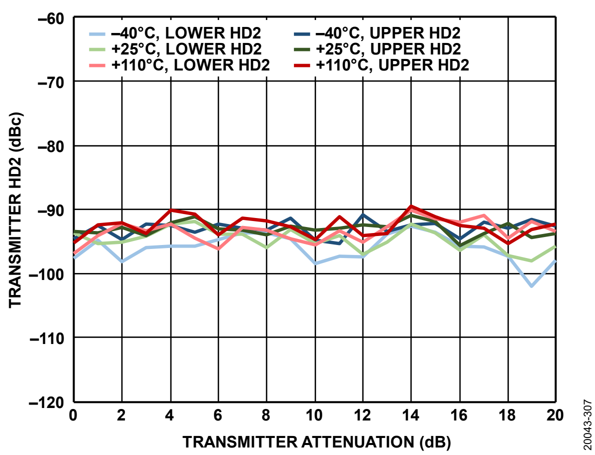


Figure 172. Transmitter HD2 vs. Transmitter Attenuation, 10 MHz Offset

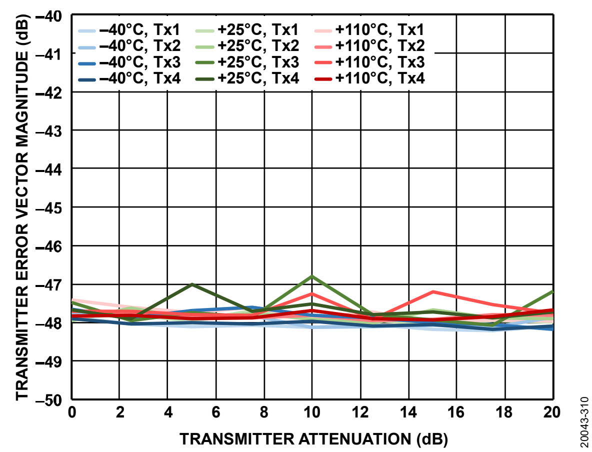


Figure 175. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

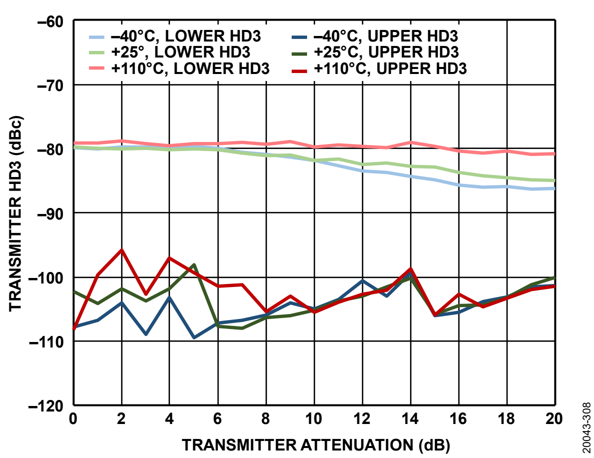


Figure 173. Transmitter HD3 vs. Transmitter Attenuation, 10 MHz Offset

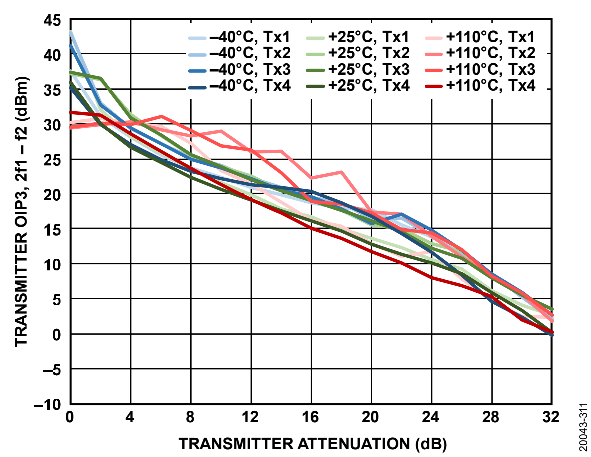


Figure 176. Transmitter OIP3, 2f1 – f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

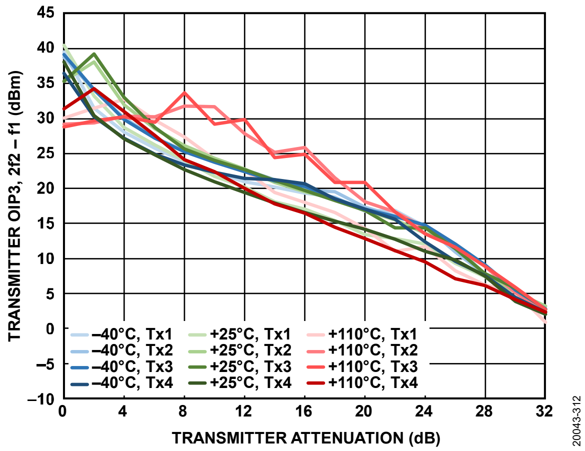


Figure 177. Transmitter OIP3, 2f2 – f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

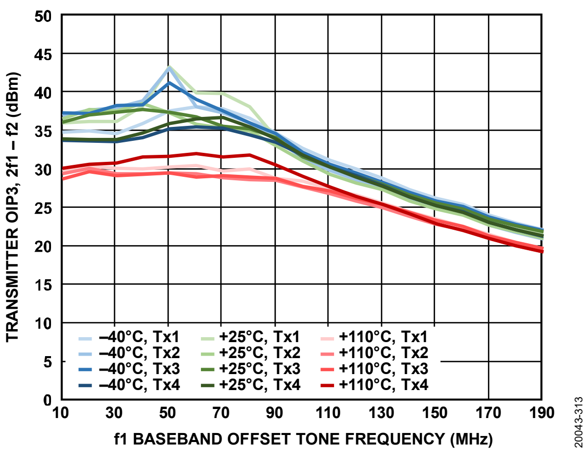


Figure 178. Transmitter OIP3, 2f1 – f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

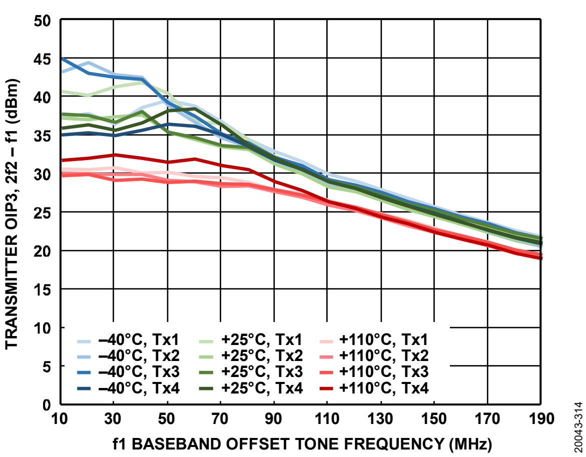


Figure 179. Transmitter OIP3, 2f2 – f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

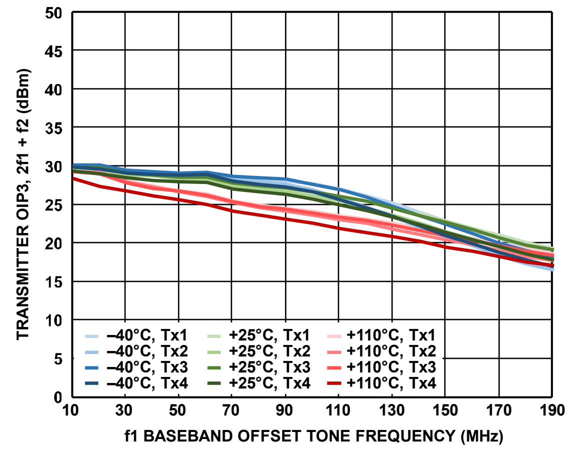


Figure 180. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

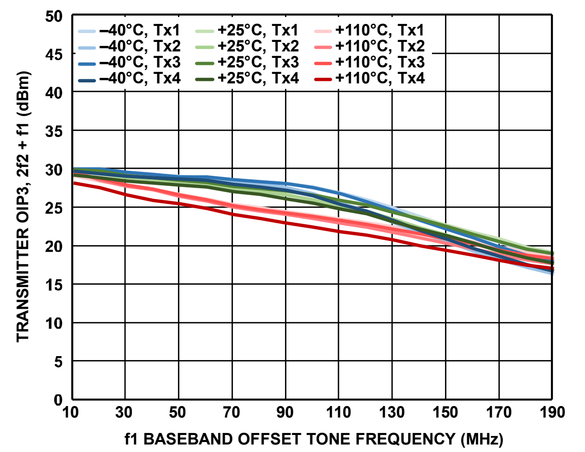


Figure 181. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

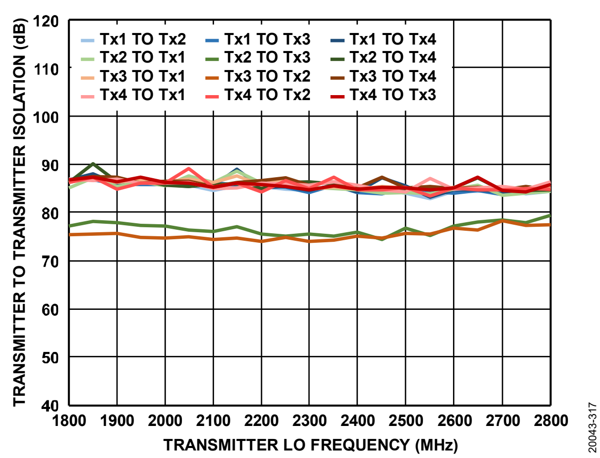


Figure 182. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

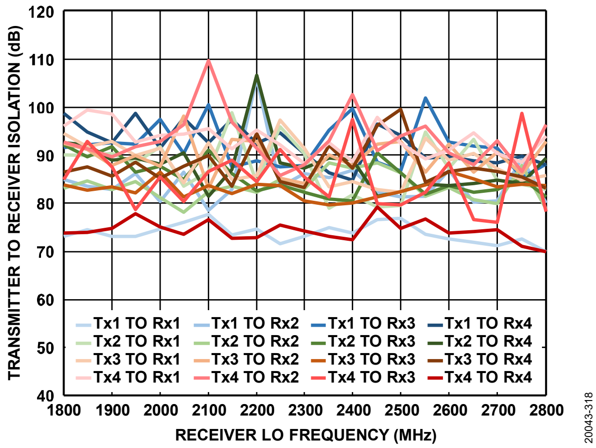


Figure 183. Transmitter to Receiver Isolation vs. Receiver LO Frequency

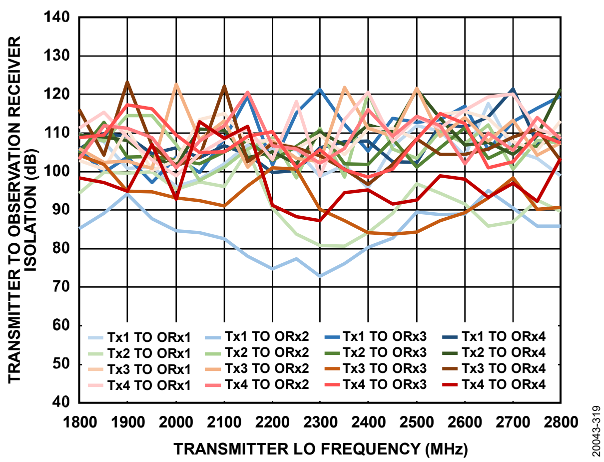


Figure 184. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

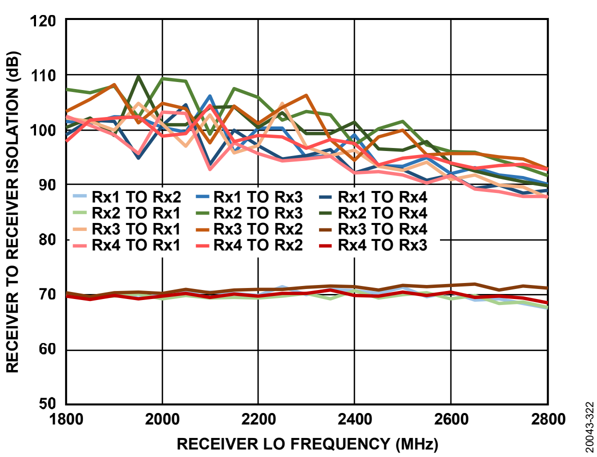


Figure 185. Receiver to Receiver Isolation vs. Receiver LO Frequency

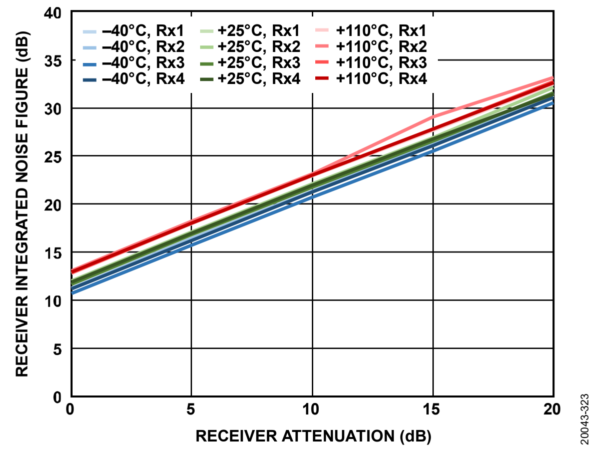


Figure 186. Receiver Integrated Noise Figure vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

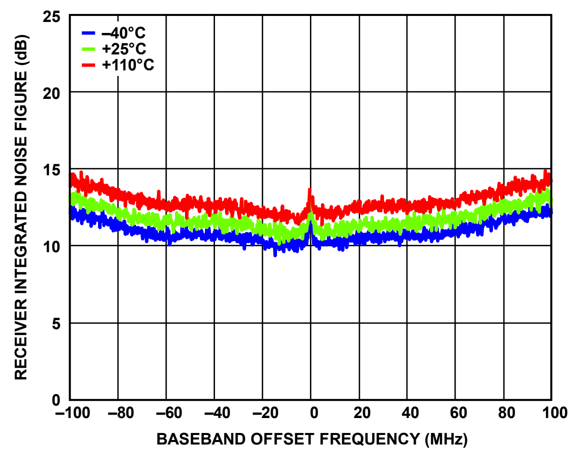


Figure 187. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

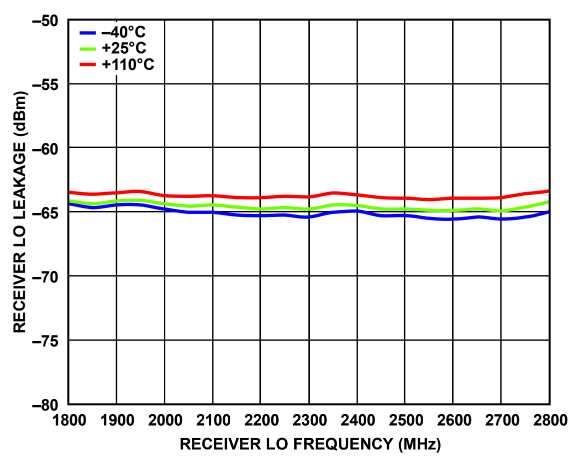


Figure 188. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

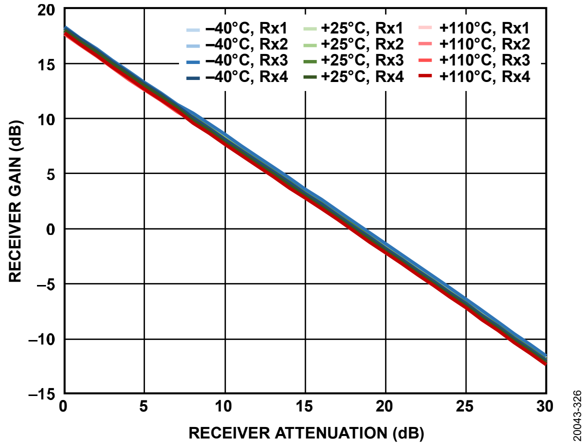


Figure 189. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

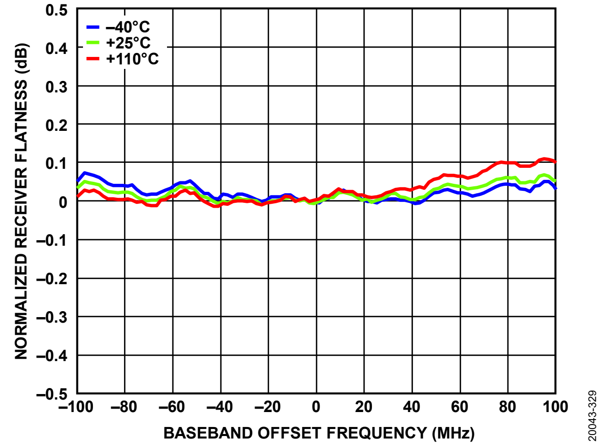


Figure 192. Normalized Receiver Flatness vs. Baseband Offset Frequency, –5 dBFS Input Signal

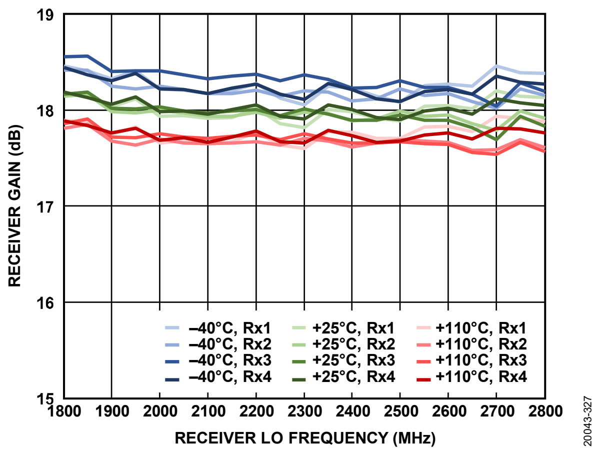


Figure 190. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

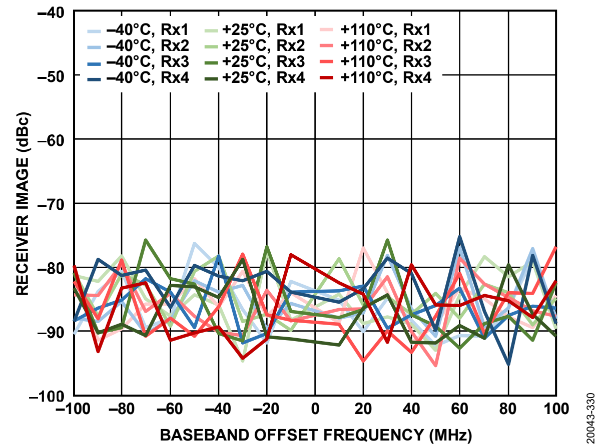


Figure 193. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

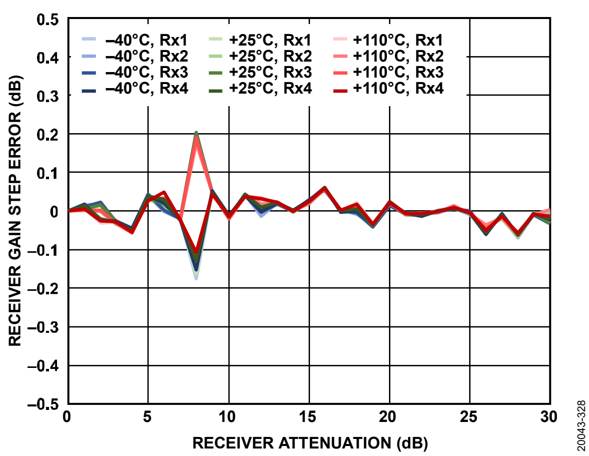


Figure 191. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

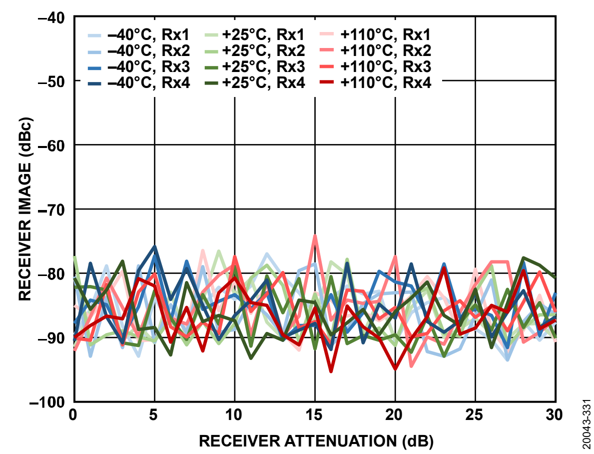


Figure 194. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

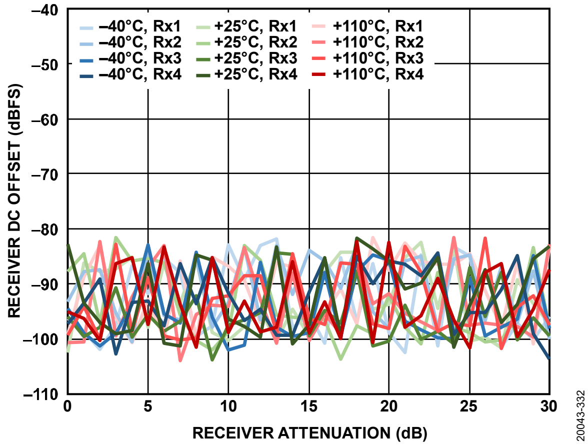


Figure 195. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

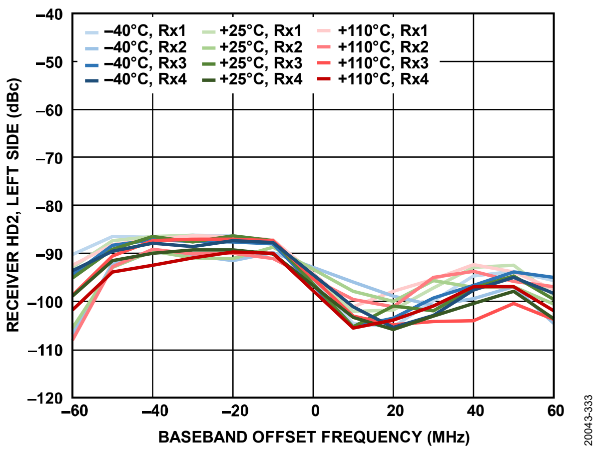


Figure 196. Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

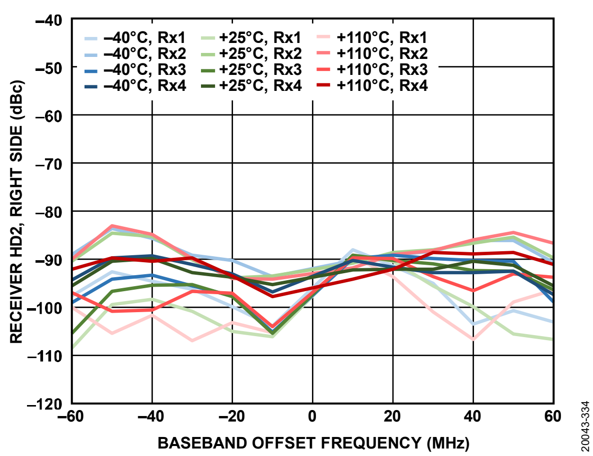


Figure 197. Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

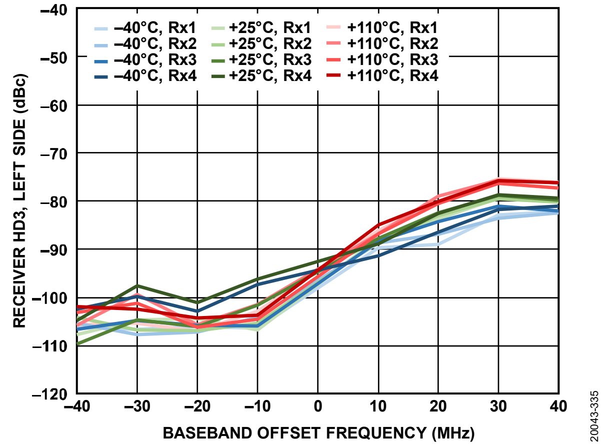


Figure 198. Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

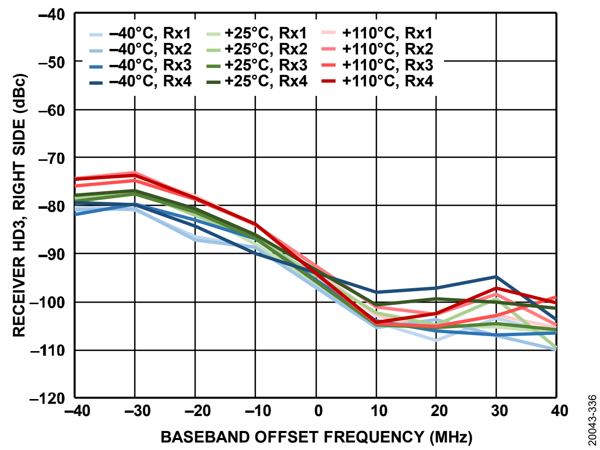


Figure 199. Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

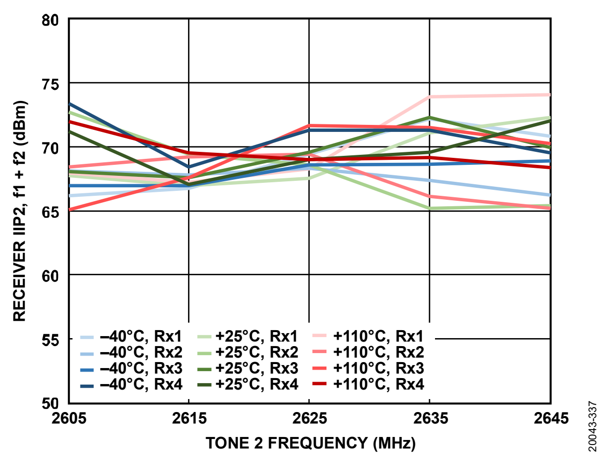


Figure 200. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

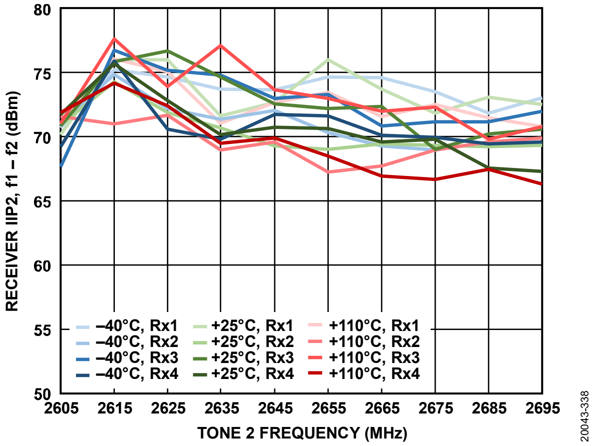


Figure 201. Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

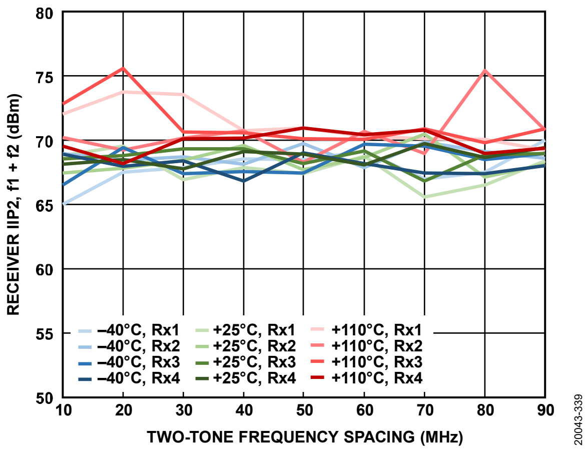


Figure 202. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

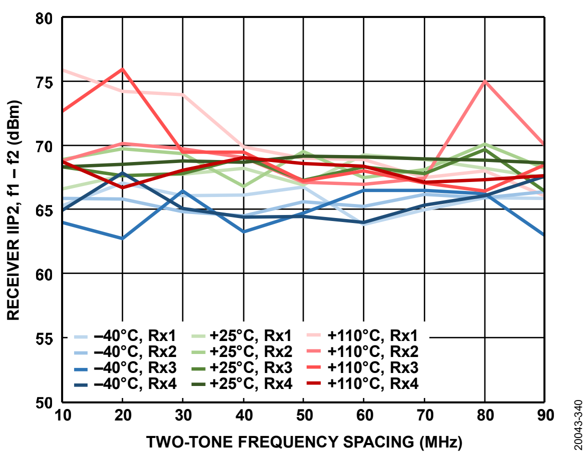


Figure 203. Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

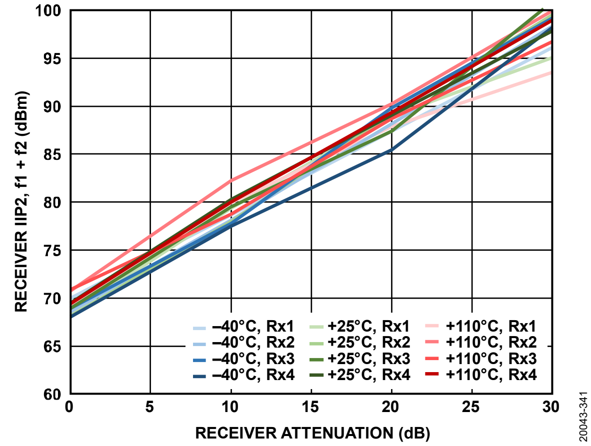


Figure 204. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

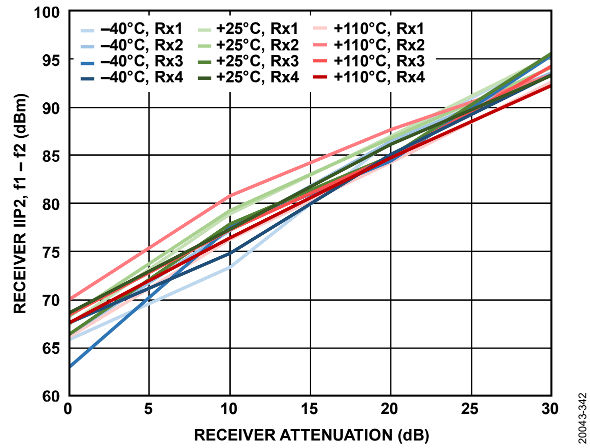


Figure 205. Receiver IIP2, f1 – f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

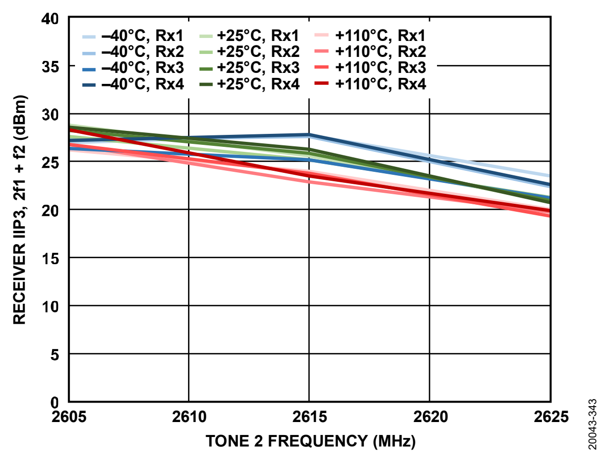


Figure 206. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

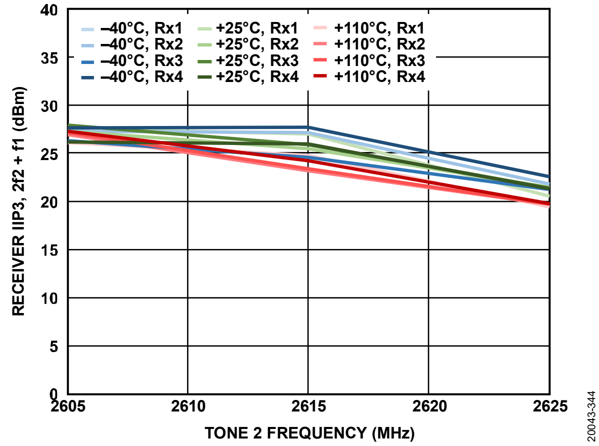


Figure 207. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

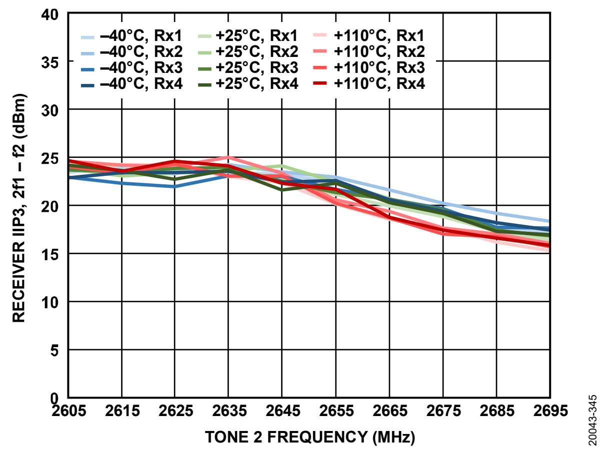


Figure 208. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

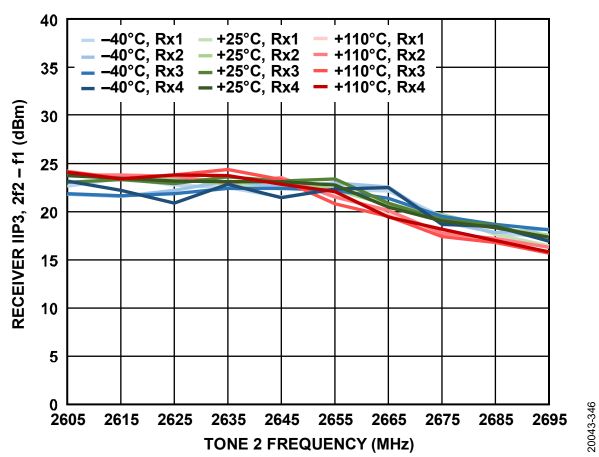


Figure 209. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

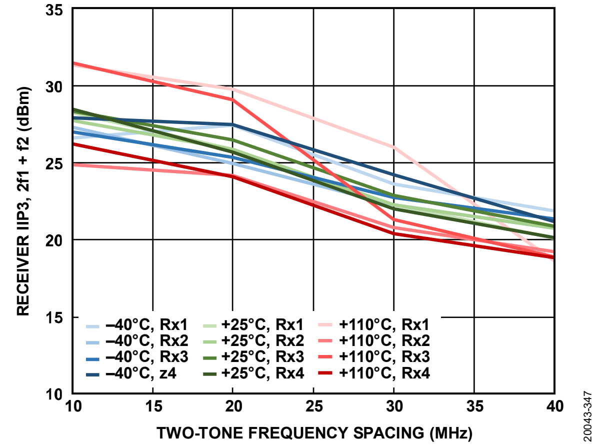


Figure 210. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

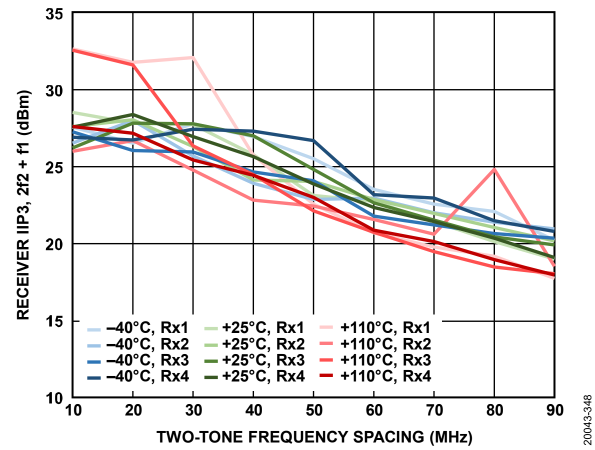


Figure 211. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

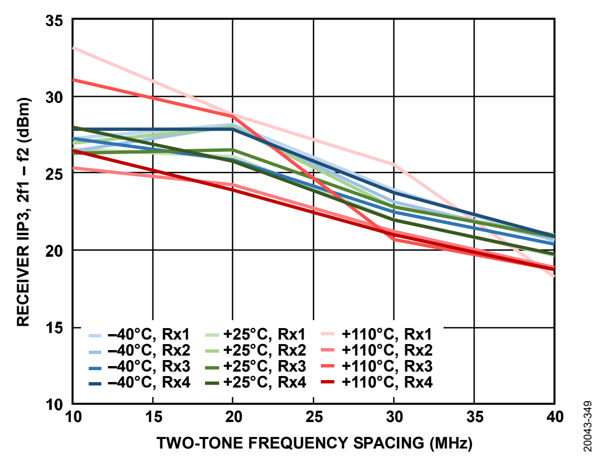


Figure 212. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

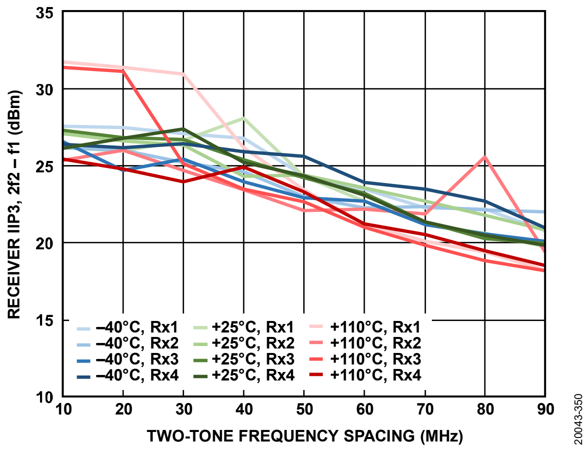


Figure 213. Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

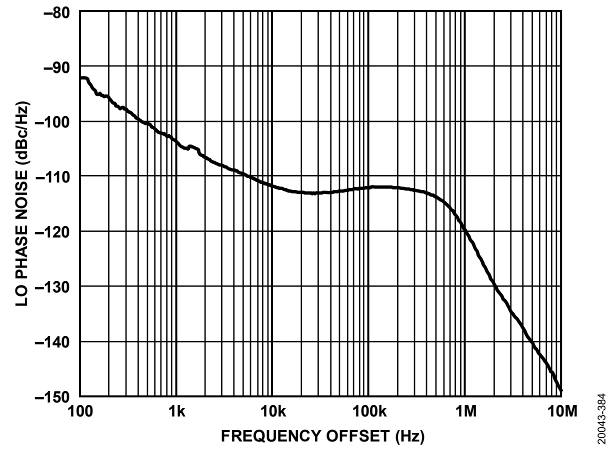


Figure 216. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 60°

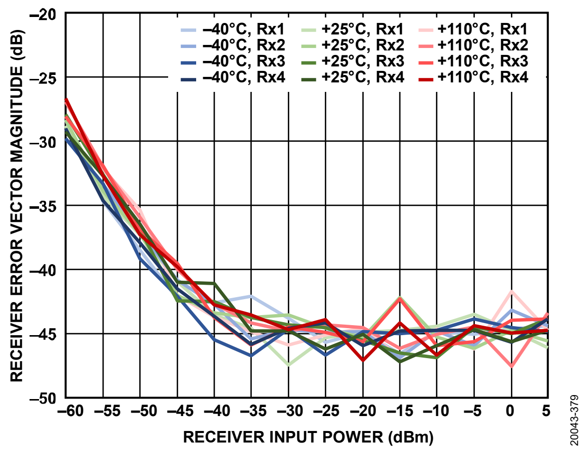


Figure 214. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

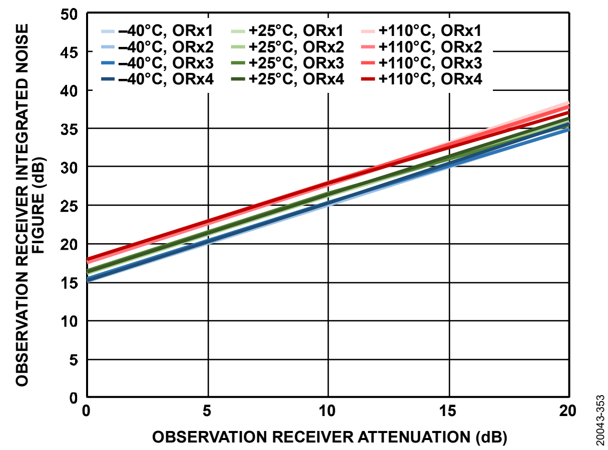


Figure 217. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

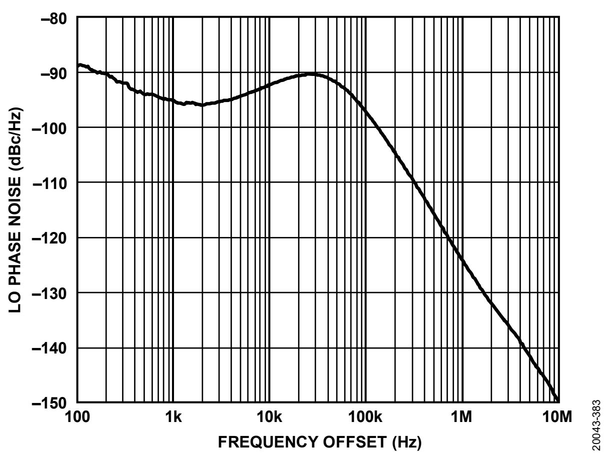


Figure 215. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

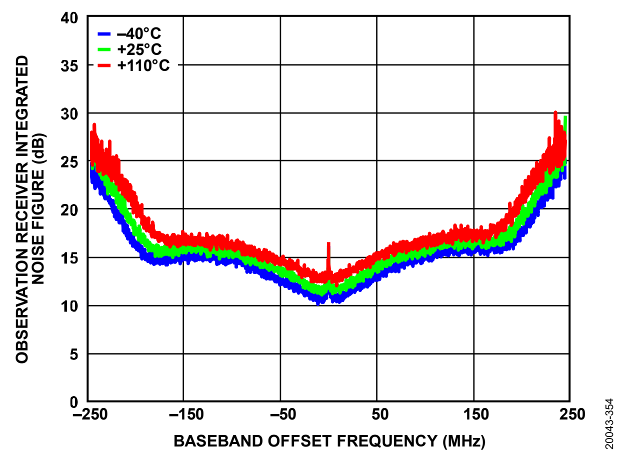


Figure 218. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

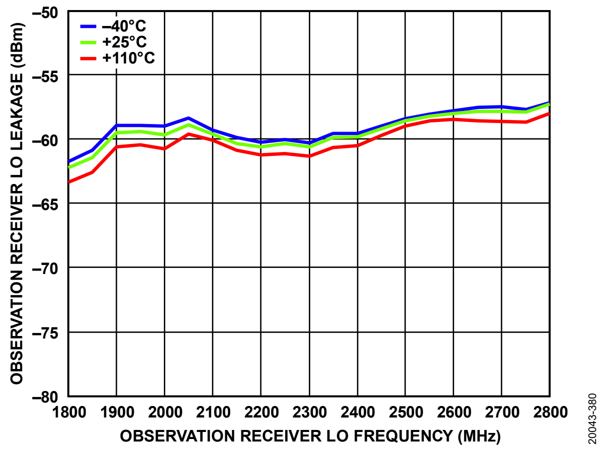


Figure 219. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

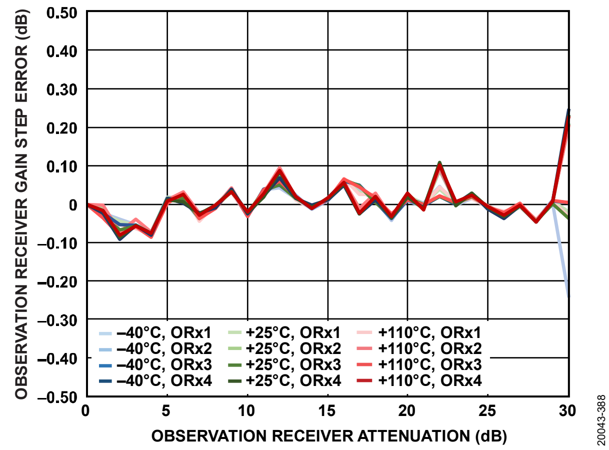


Figure 222. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

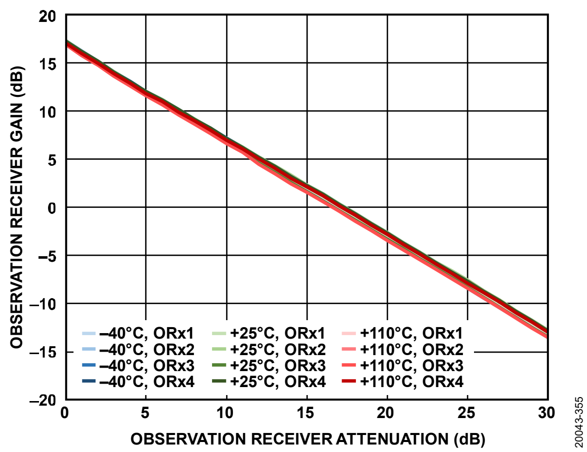


Figure 220. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

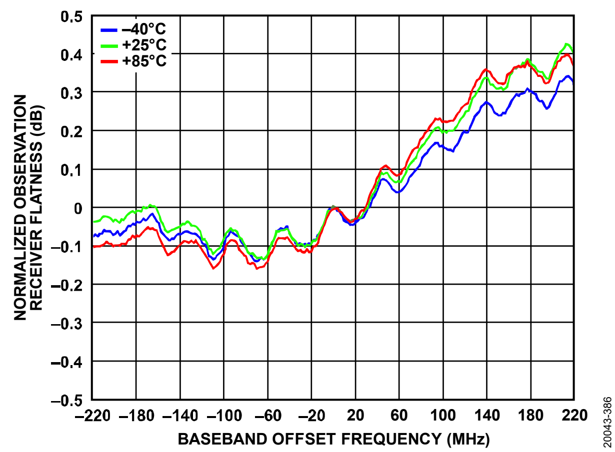


Figure 223. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, −25 dBm Input Signal, 0 dB Attenuation

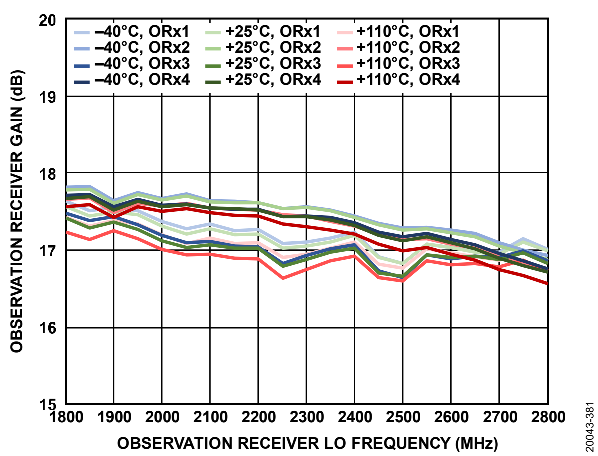


Figure 221. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

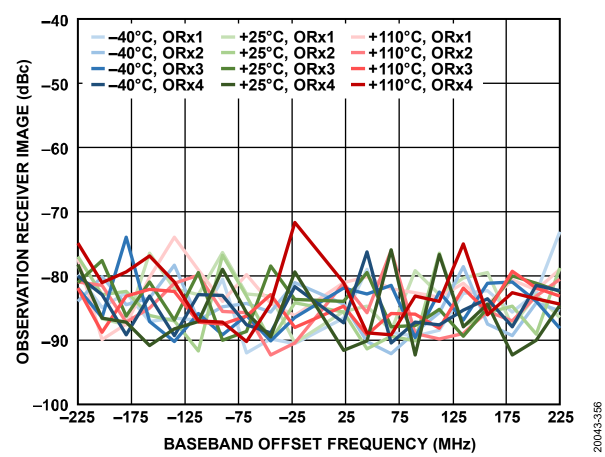


Figure 224. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

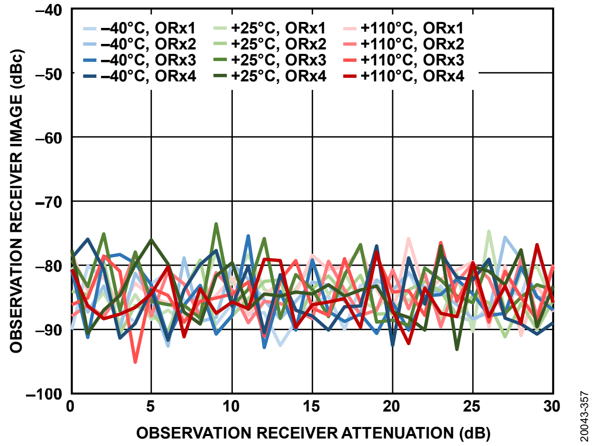


Figure 225. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

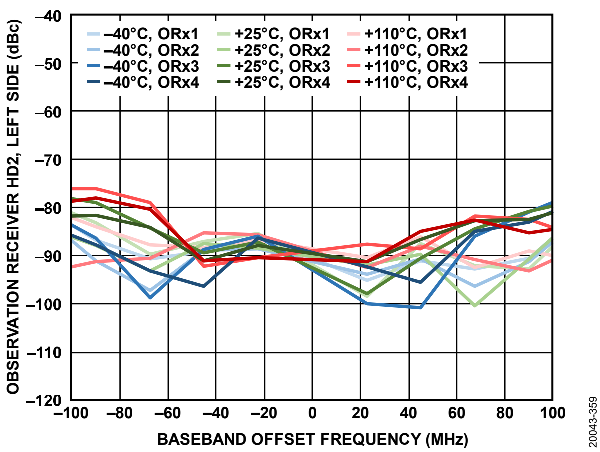


Figure 226. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

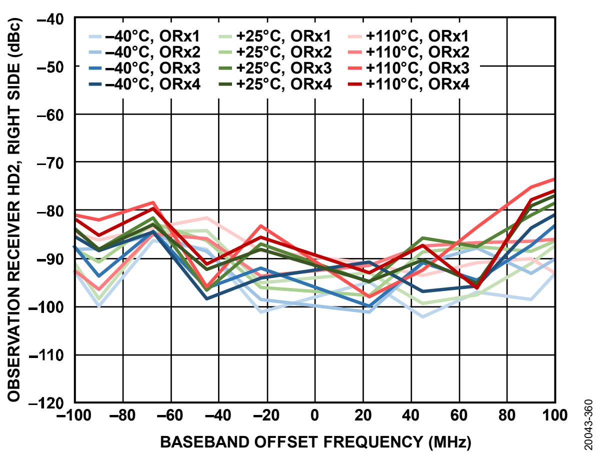


Figure 227. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

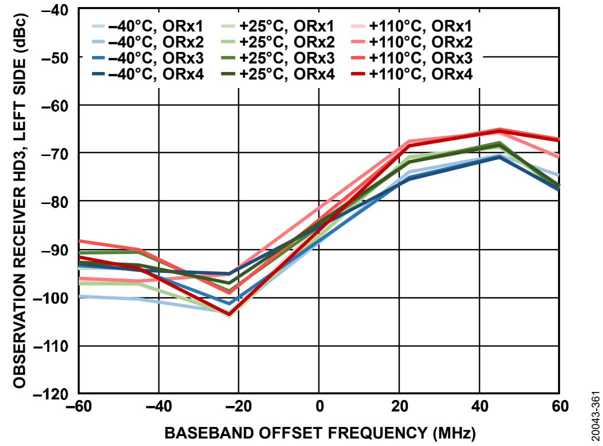


Figure 228. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

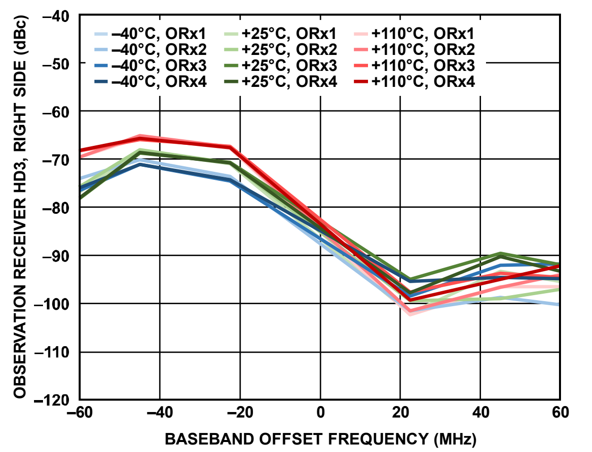


Figure 229. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

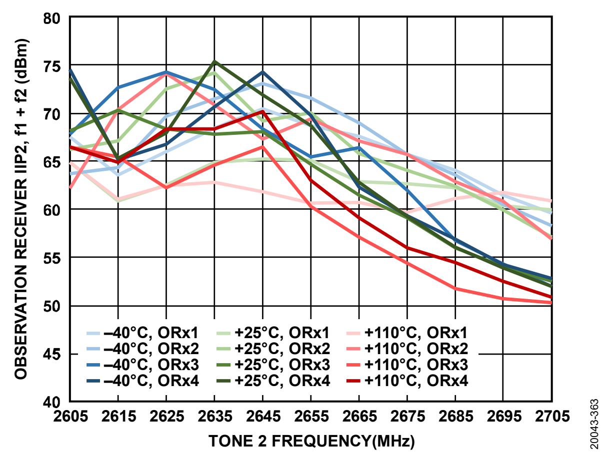


Figure 230. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

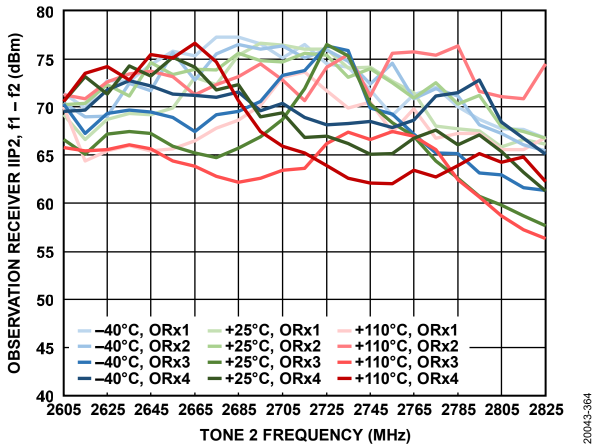


Figure 231. Observation Receiver IIP2, f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

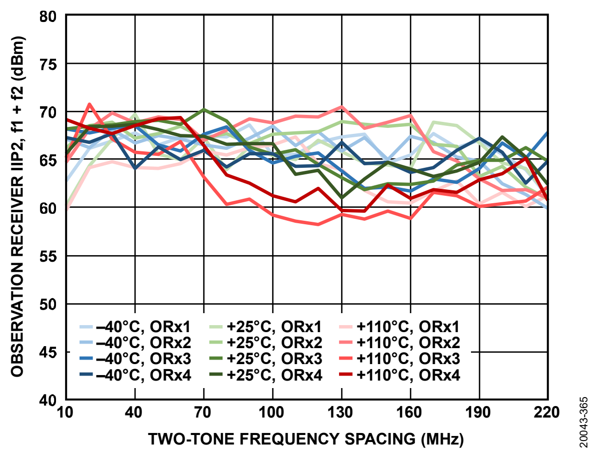


Figure 232. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

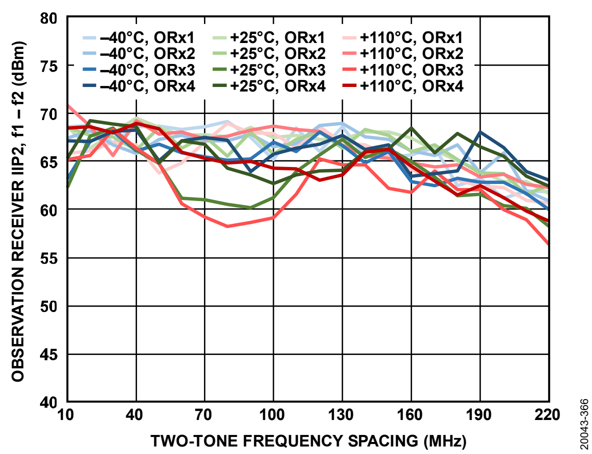


Figure 233. Observation Receiver IIP2, f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

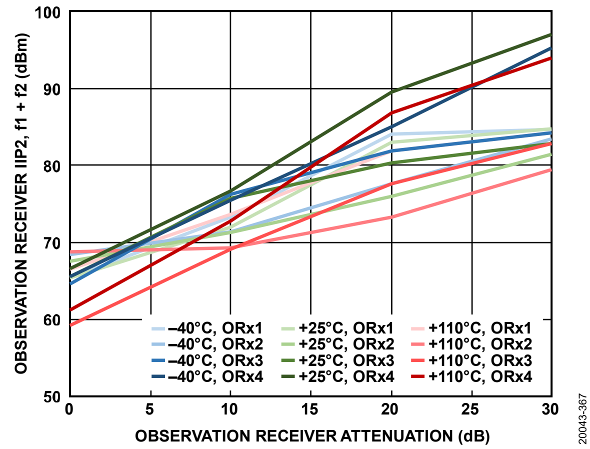


Figure 234. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

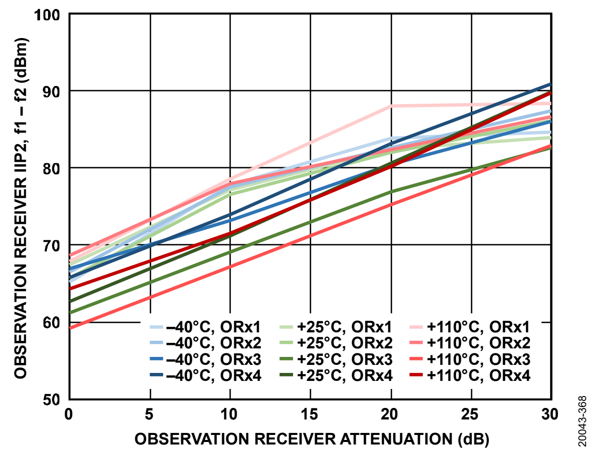


Figure 235. Observation Receiver IIP2, f1 − f2 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 102 MHz, f2 = 2 MHz

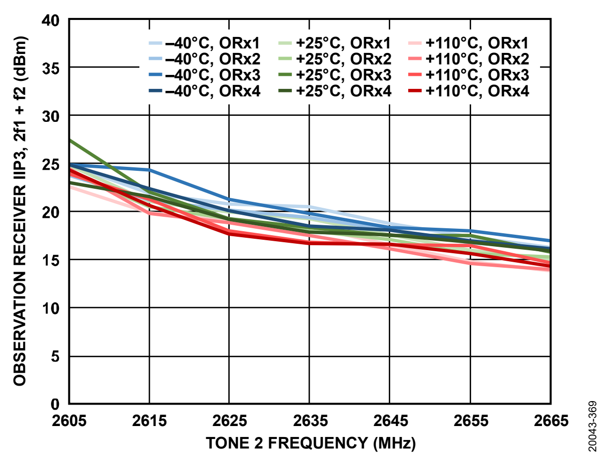


Figure 236. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

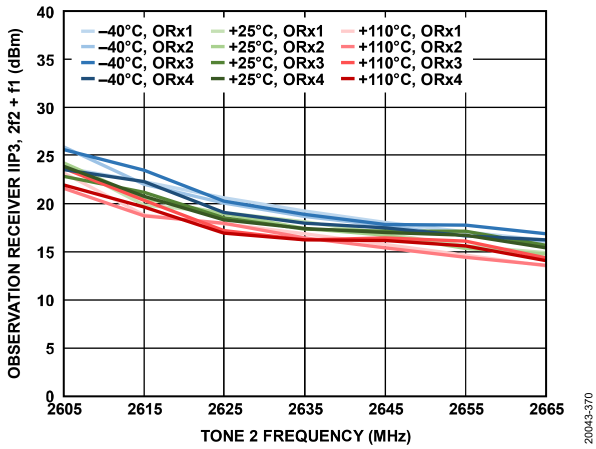


Figure 237. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

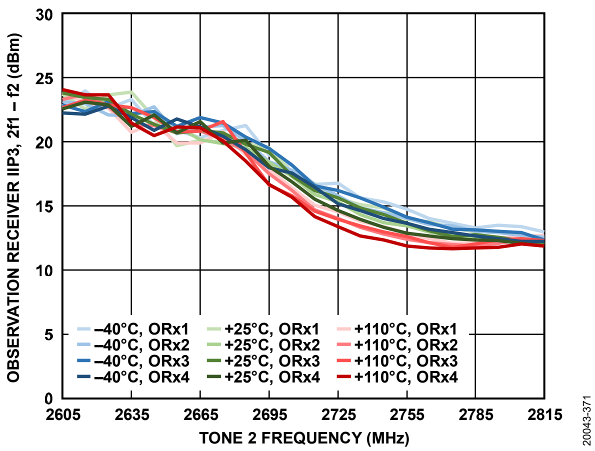


Figure 238. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

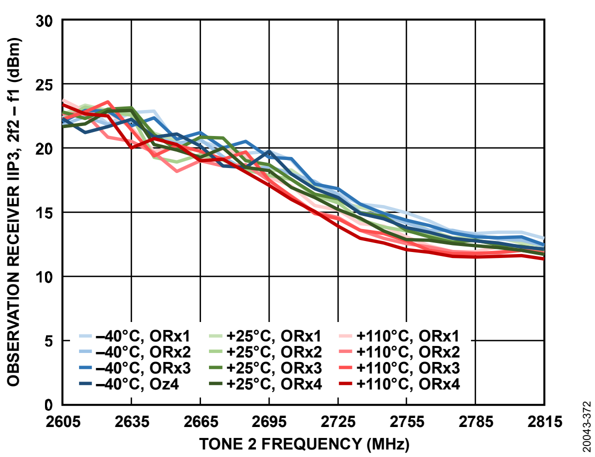


Figure 239. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

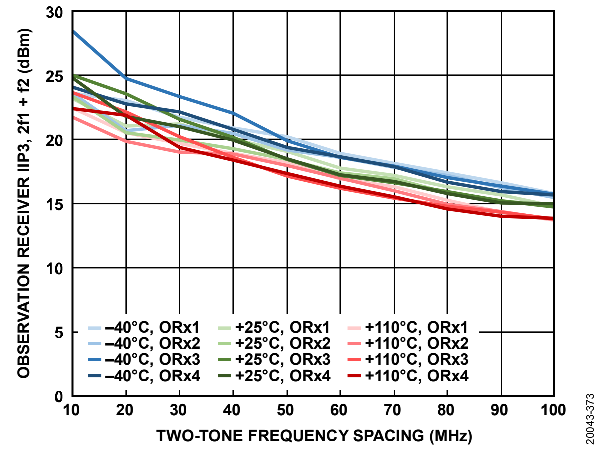


Figure 240. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

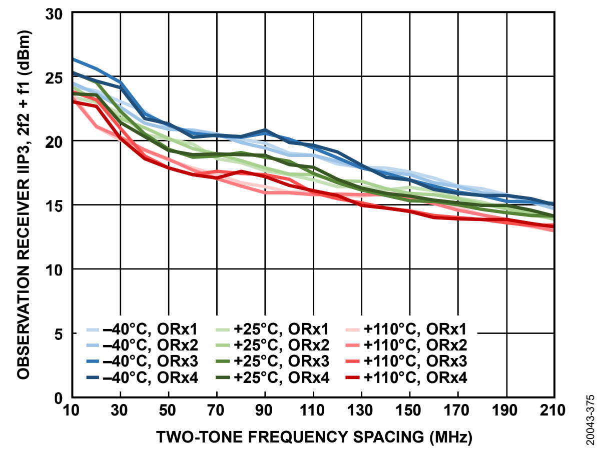


Figure 241. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

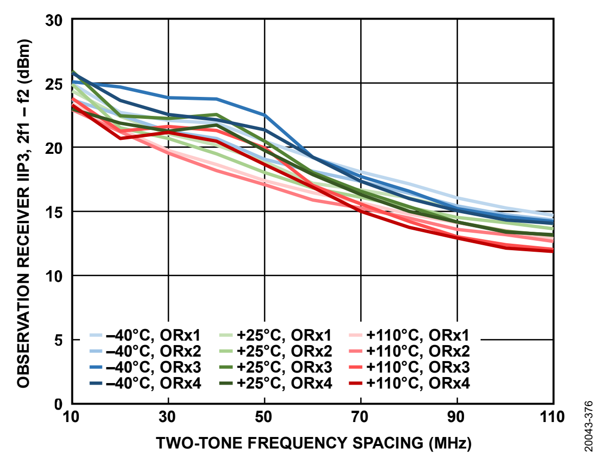


Figure 242. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

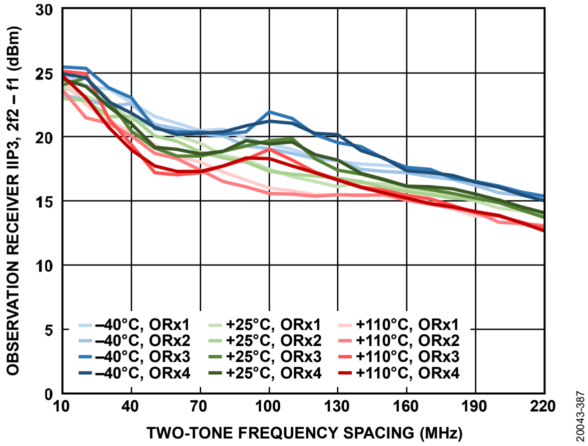


Figure 243. Observation Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

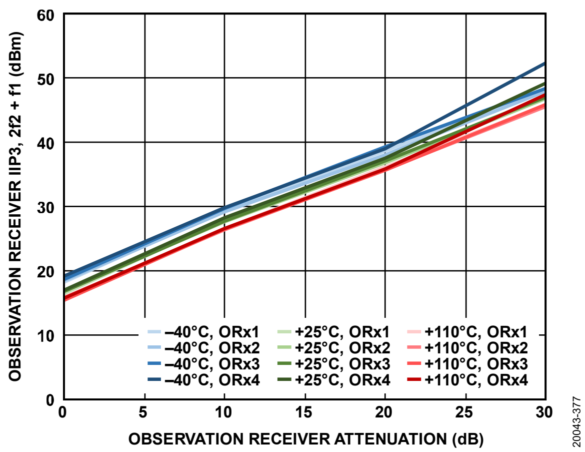


Figure 244. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

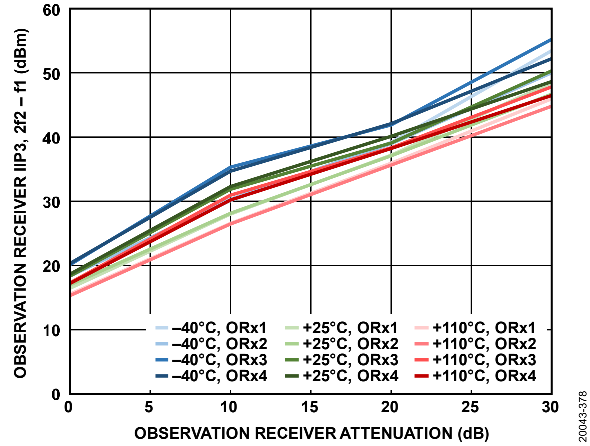


Figure 245. Observation Receiver IIP3, 2f2 – f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

3800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 3800 MHz, unless otherwise noted.

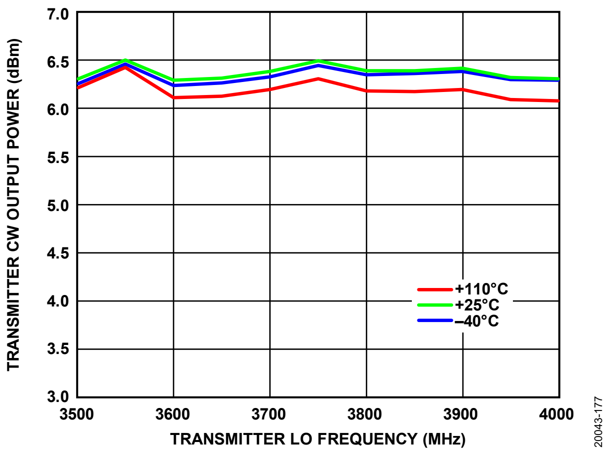


Figure 246. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

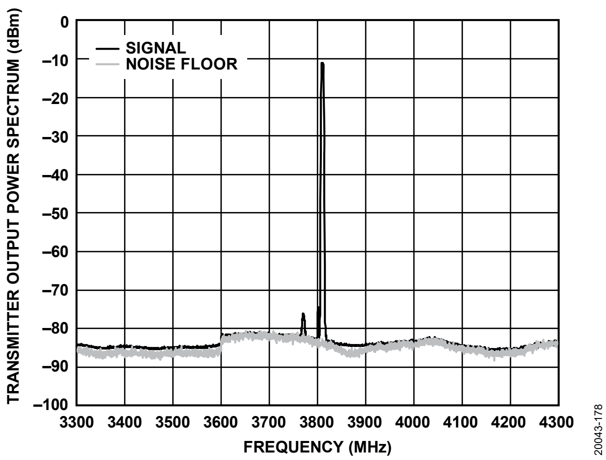


Figure 247. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C (Step at 3600 MHz Due to Spectrum Analyzer)

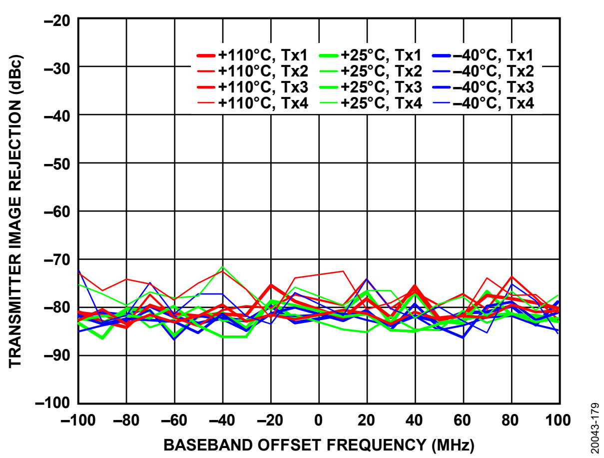


Figure 248. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

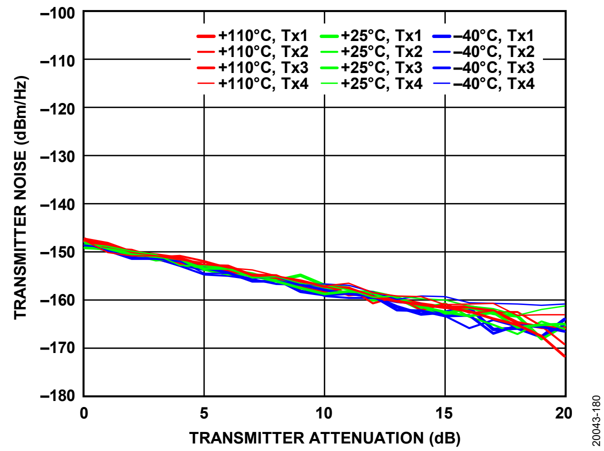


Figure 249. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset Frequency

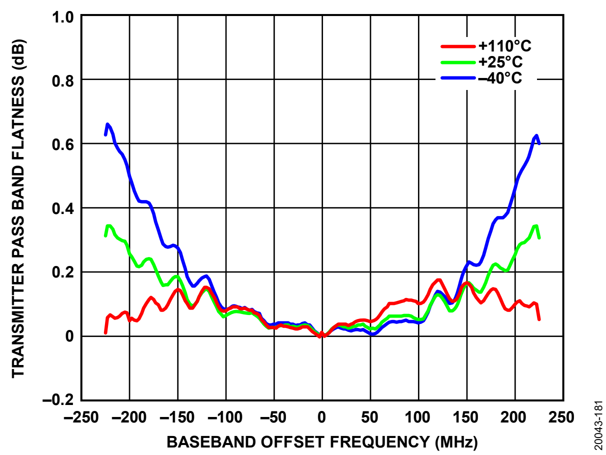


Figure 250. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

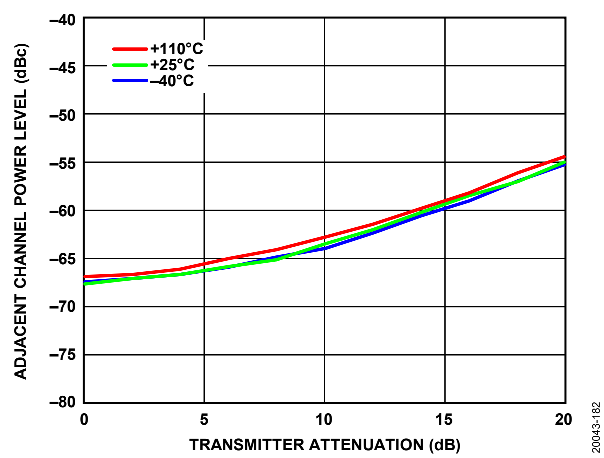


Figure 251. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 600 kHz, Loop Filter Phase Margin = 75°

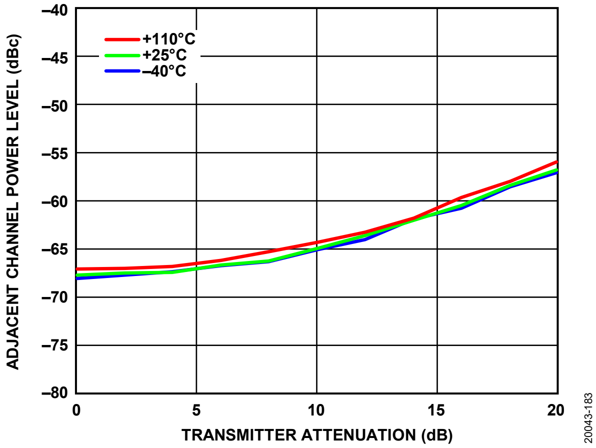


Figure 252. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 600 kHz, Loop Filter Phase Margin = 75°

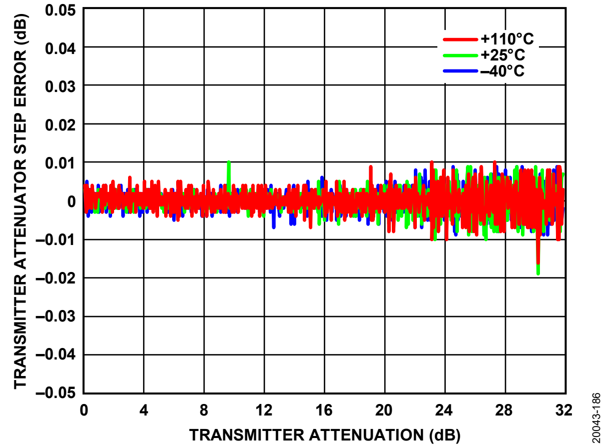


Figure 255. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

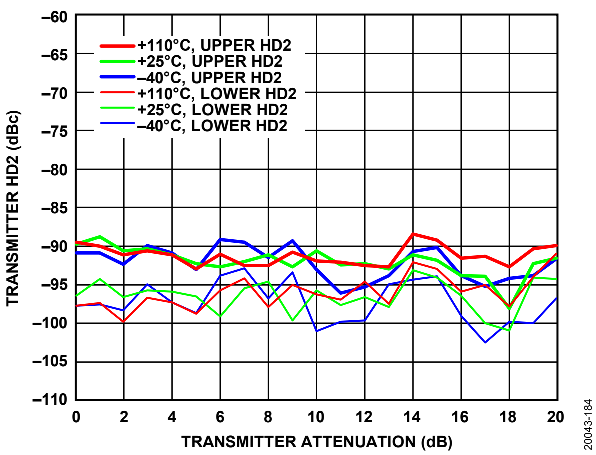


Figure 253. Transmitter HD2 vs. Transmitter Attenuation, 10 MHz Offset

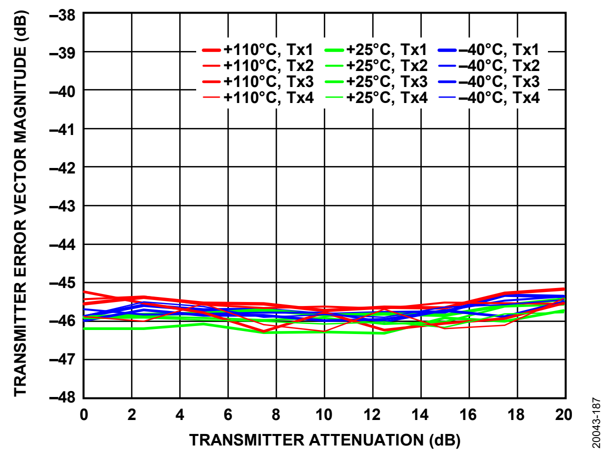


Figure 256. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 600 kHz, Loop Filter Phase Margin = 75°

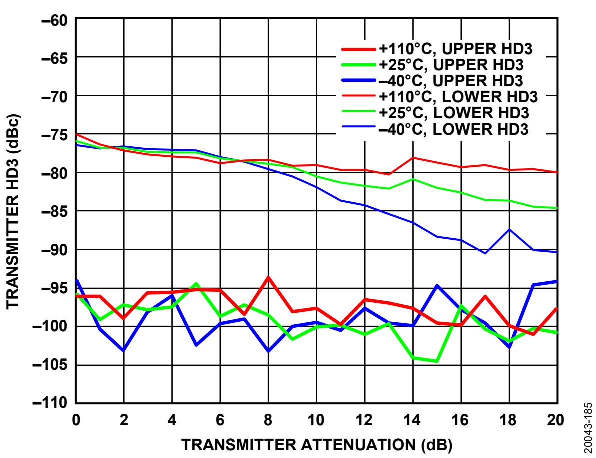


Figure 254. Transmitter HD3 vs. Transmitter Attenuation, 10 MHz Offset

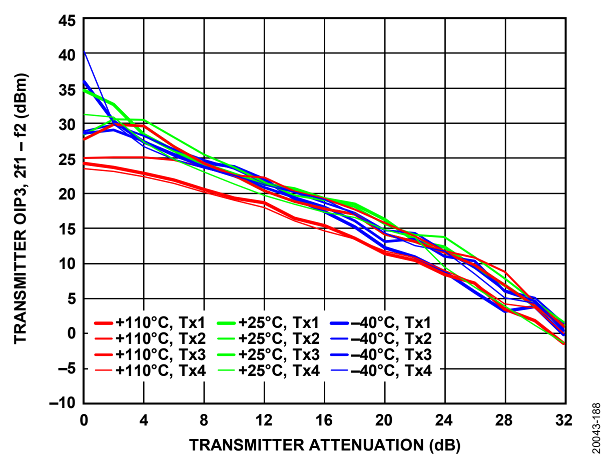


Figure 257. Transmitter OIP3, 2f1 – f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

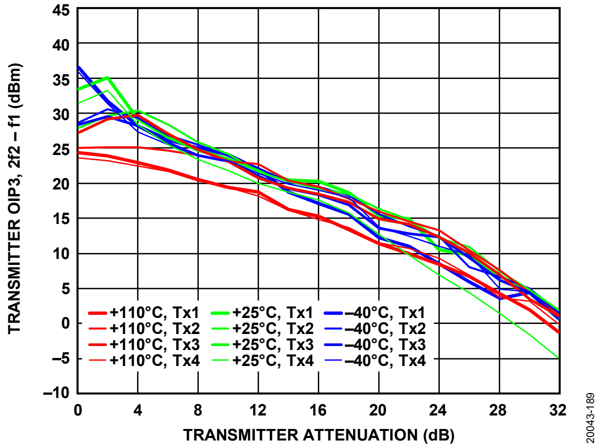


Figure 258. Transmitter OIP3, 2f2 – f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

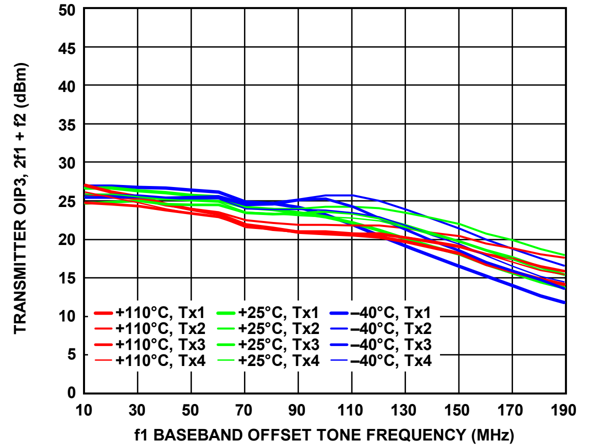


Figure 261. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

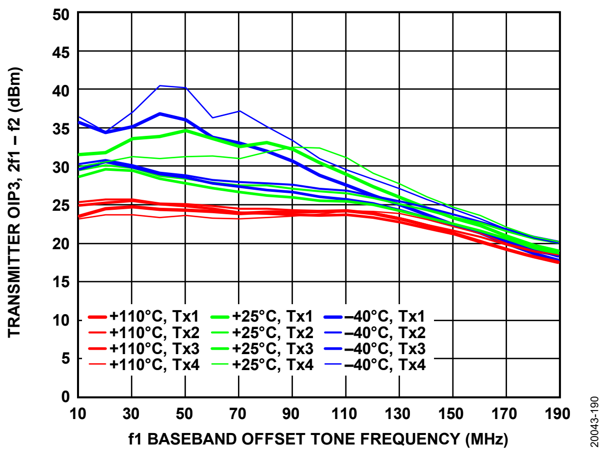


Figure 259. Transmitter OIP3, 2f1 – f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

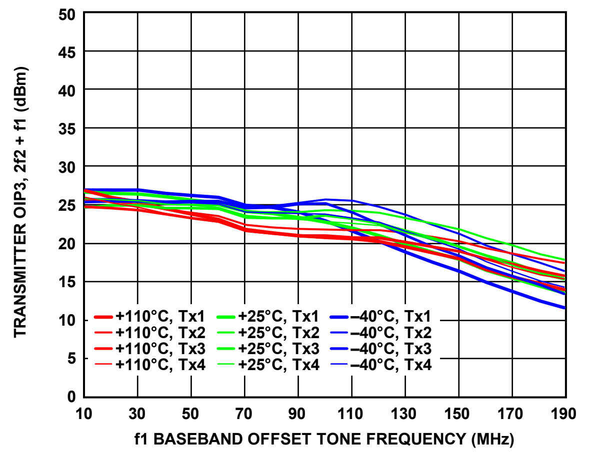


Figure 262. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

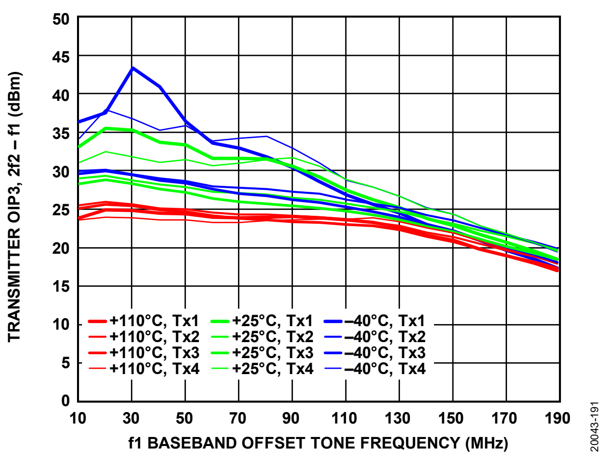


Figure 260. Transmitter OIP3, 2f2 – f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

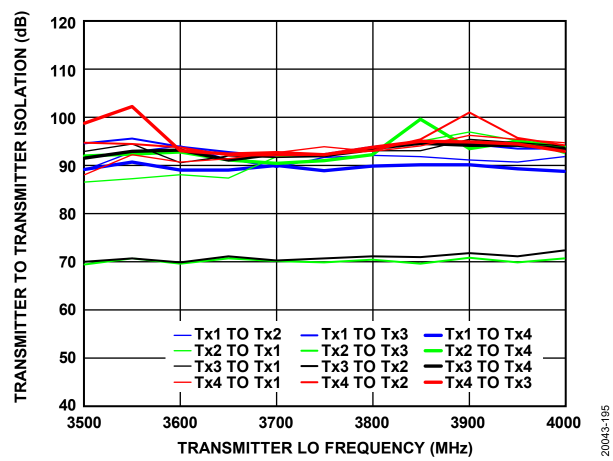


Figure 263. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

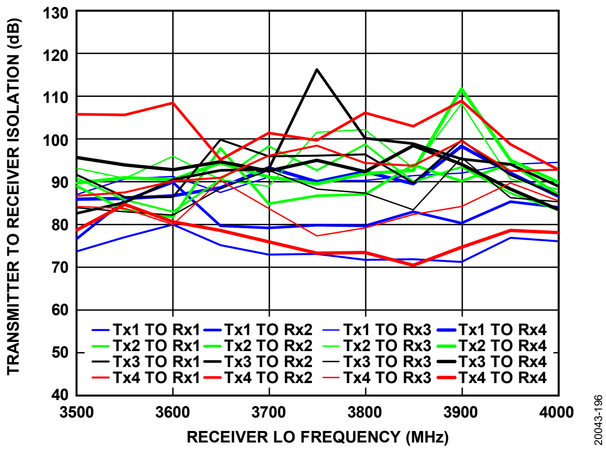


Figure 264. Transmitter to Receiver Isolation vs. Receiver LO Frequency

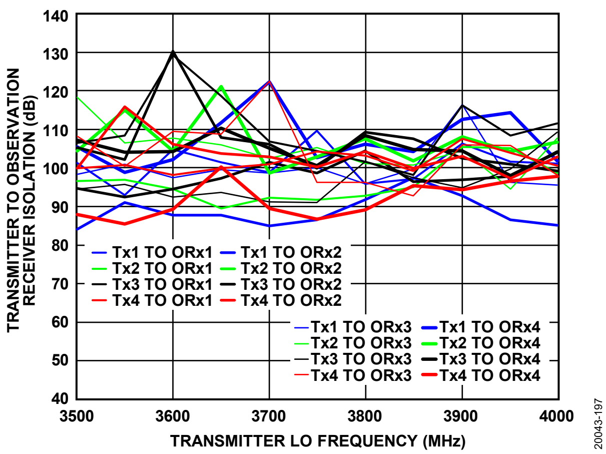


Figure 265. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

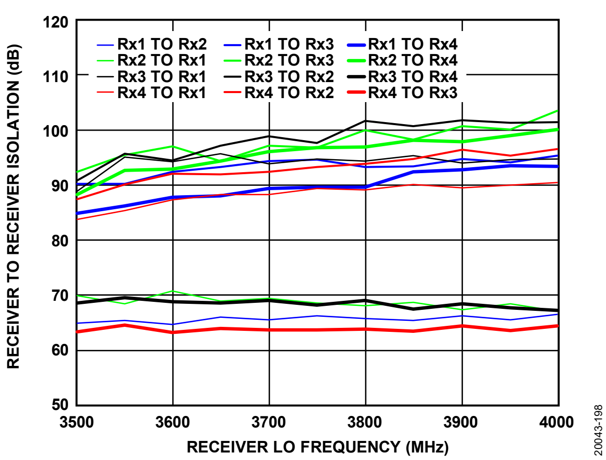


Figure 266. Receiver to Receiver Isolation vs. Receiver LO Frequency

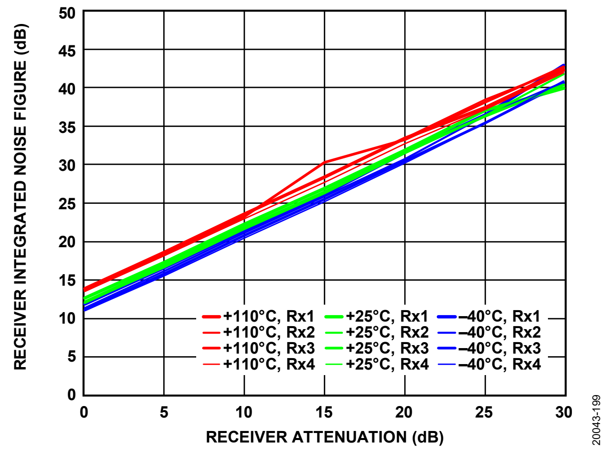


Figure 267. Receiver Integrated Noise Figure vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

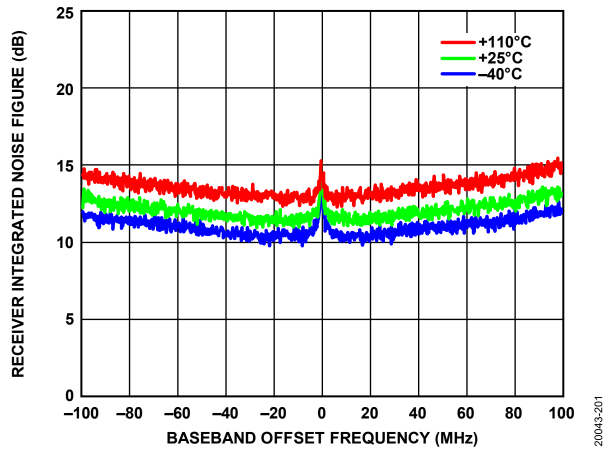


Figure 268. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

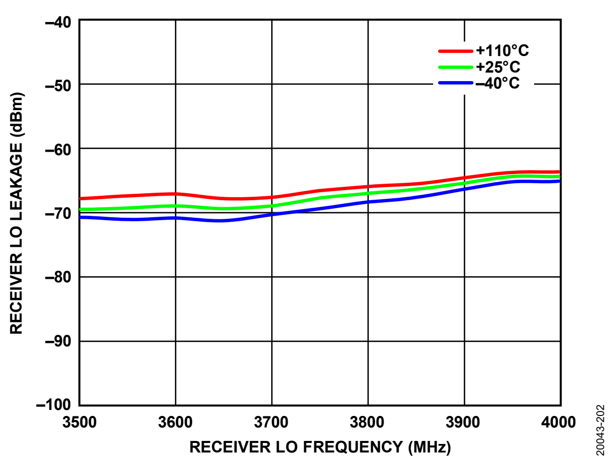


Figure 269. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

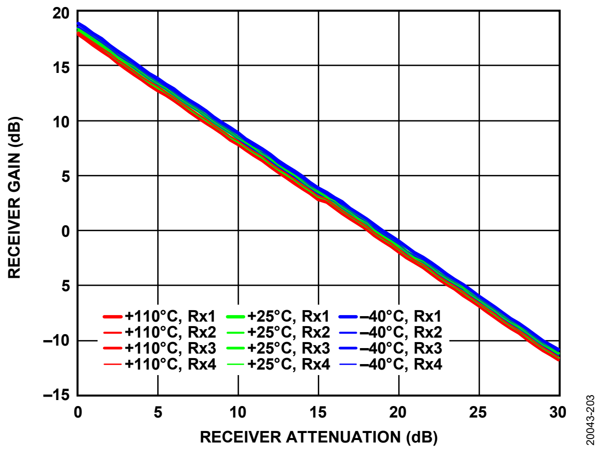


Figure 270. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

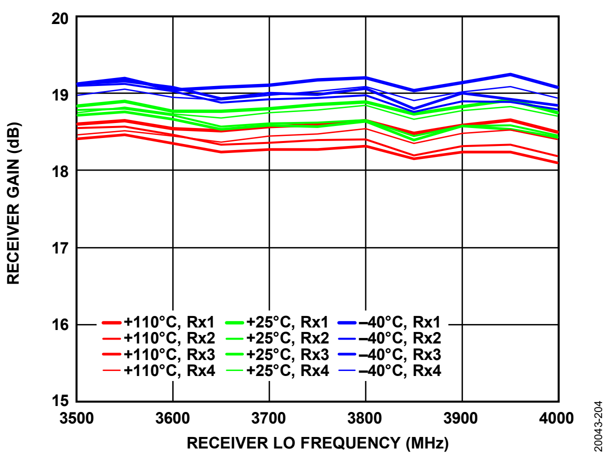


Figure 271. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

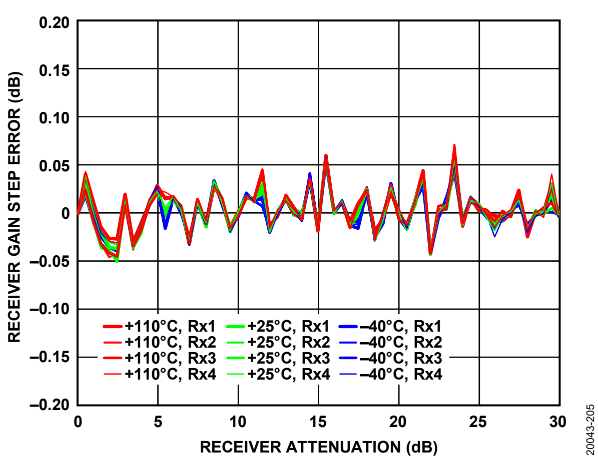


Figure 272. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

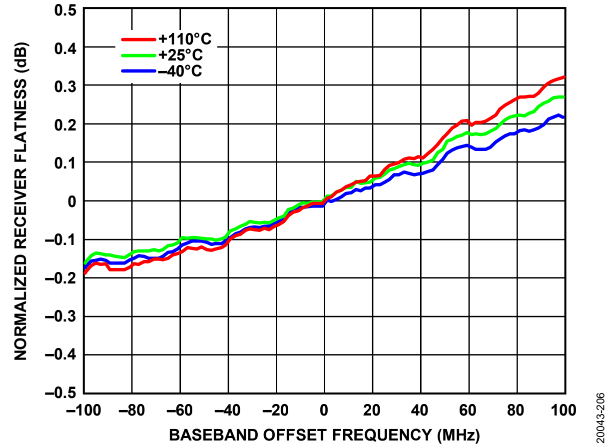


Figure 273. Normalized Receiver Flatness vs. Baseband Offset Frequency, –5 dBFS Input Signal

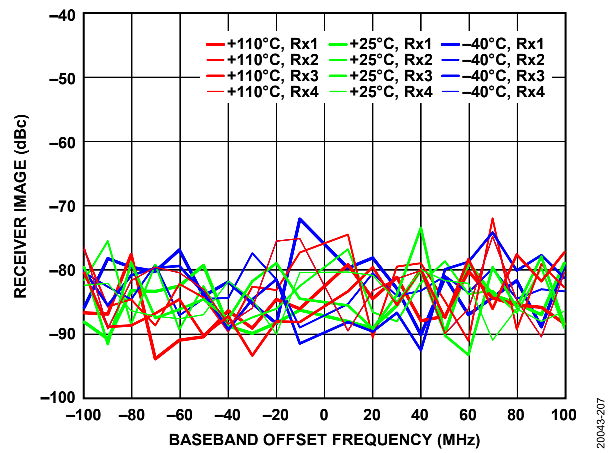


Figure 274. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

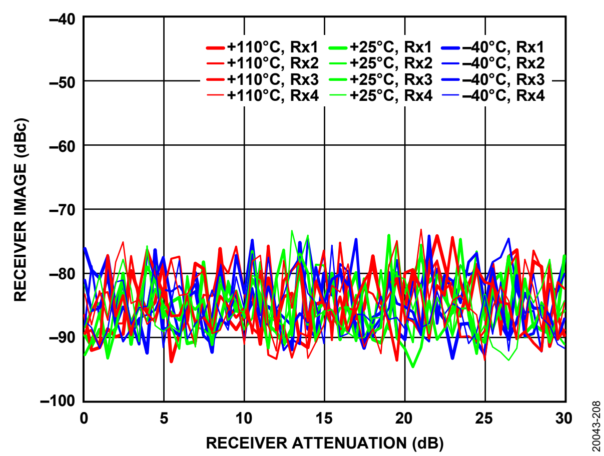


Figure 275. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

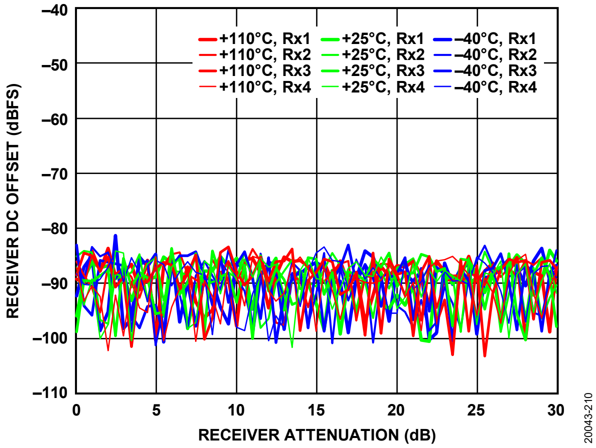


Figure 276. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

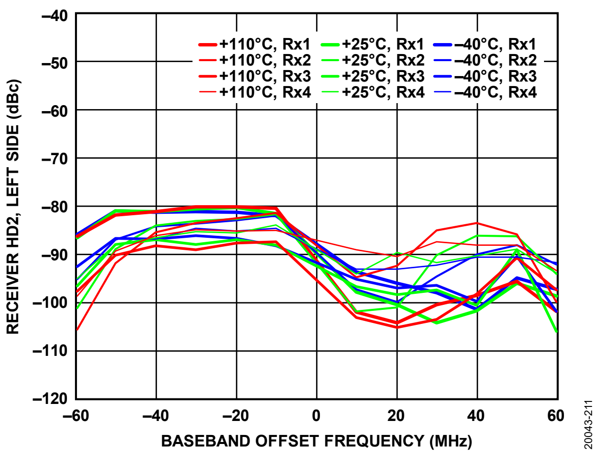


Figure 277. Receiver HD2, Left Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

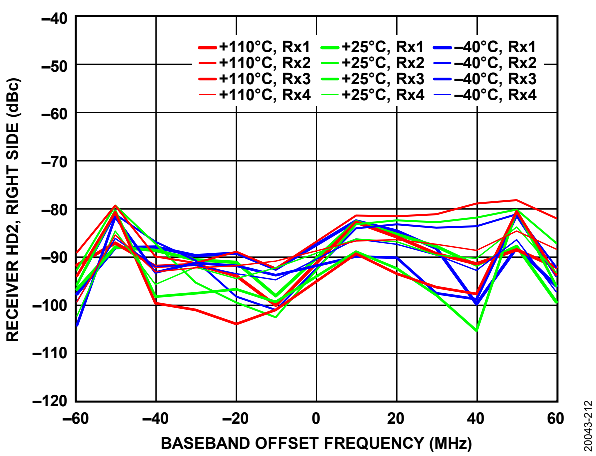


Figure 278. Receiver HD2, Right Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

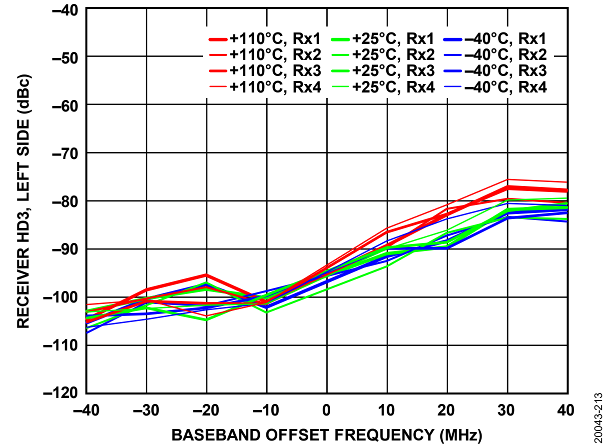


Figure 279. Receiver HD3, Left Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

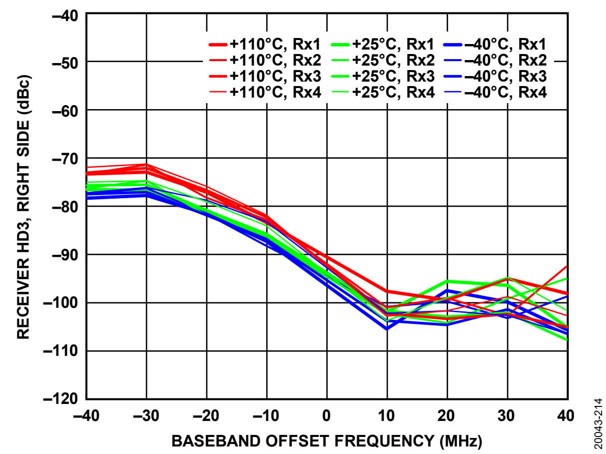


Figure 280. Receiver HD3, Right Side vs. Baseband Offset Frequency, –5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

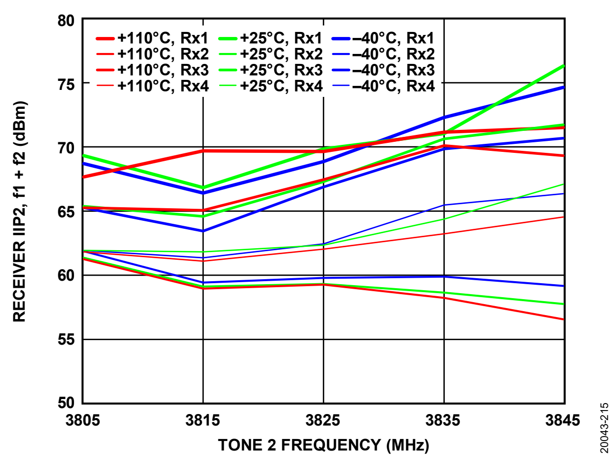


Figure 281. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

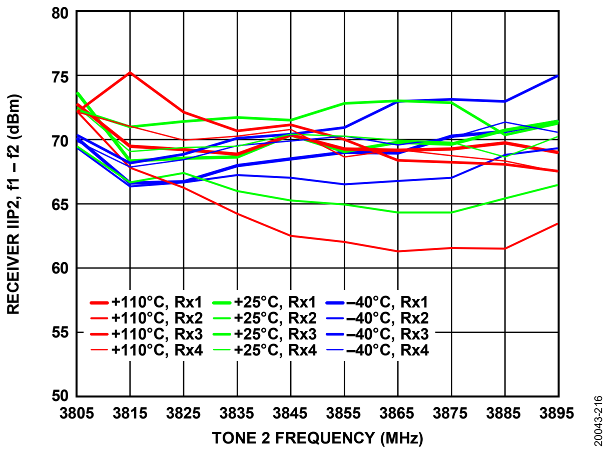


Figure 282. Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

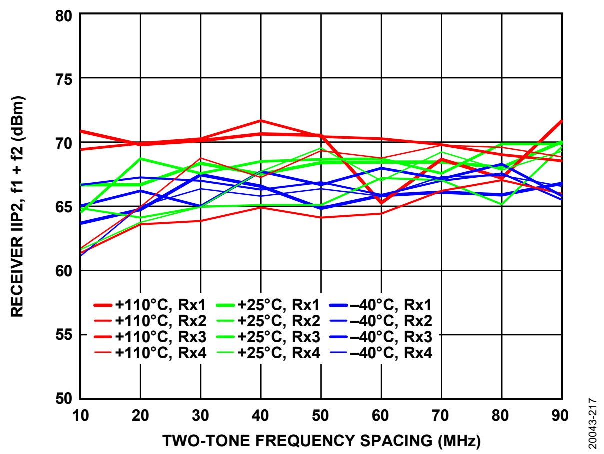


Figure 283. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

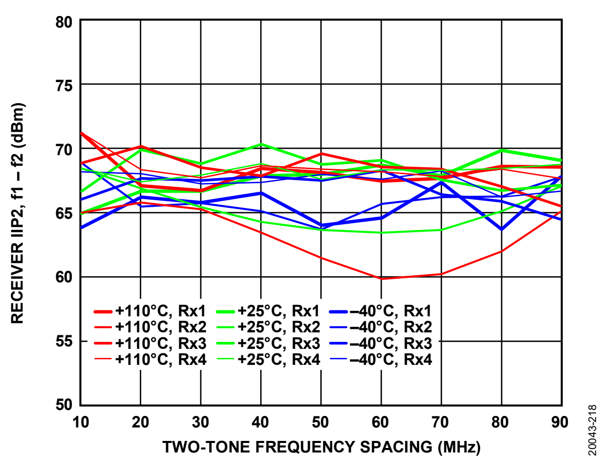


Figure 284. Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

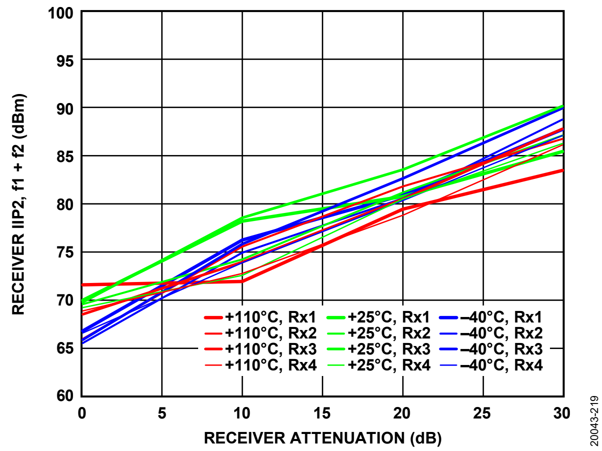


Figure 285. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

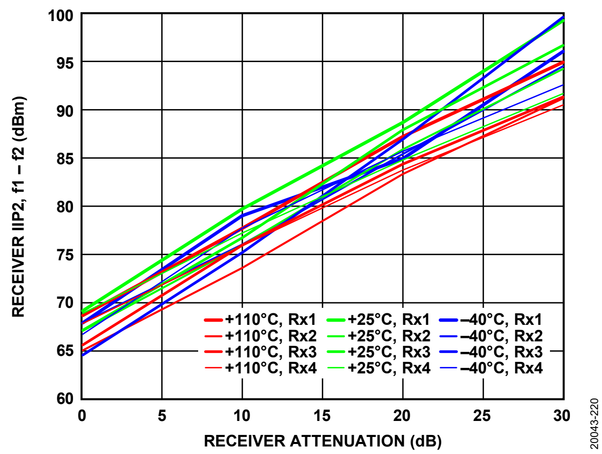


Figure 286. Receiver IIP2, f1 – f2 vs. Receiver Attenuation, Both Tones at –11 dBFS, f1 = 92 MHz, f2 = 2 MHz

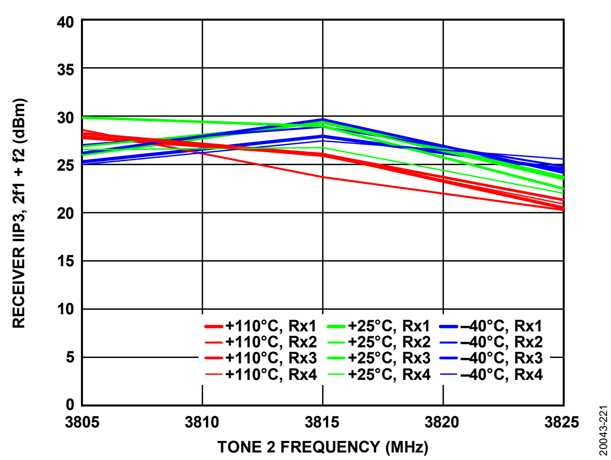


Figure 287. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

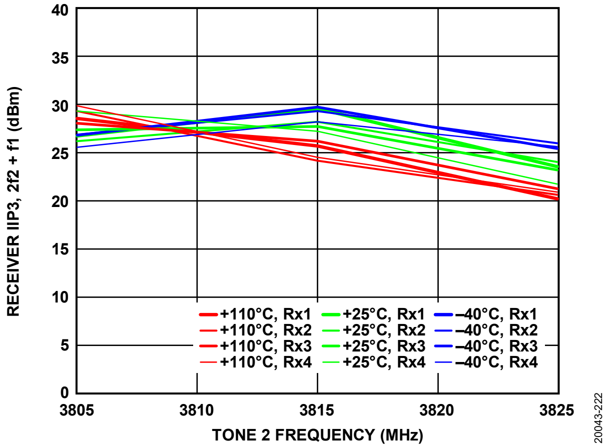


Figure 288. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

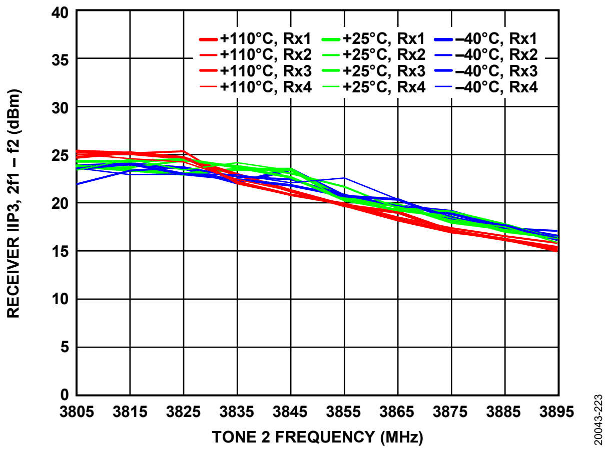


Figure 289. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

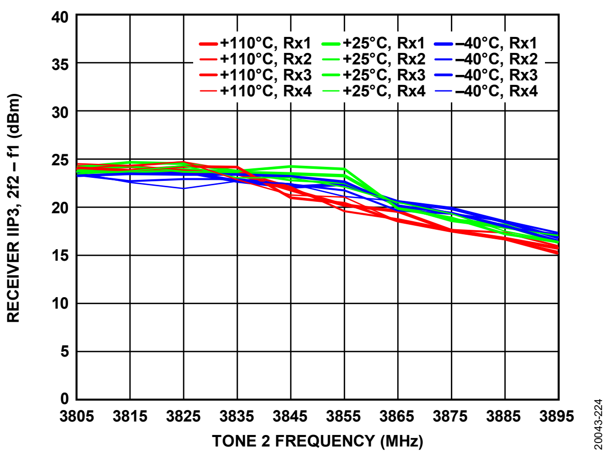


Figure 290. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

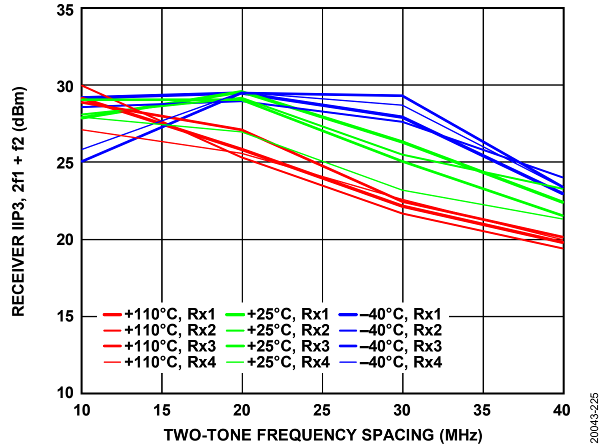


Figure 291. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

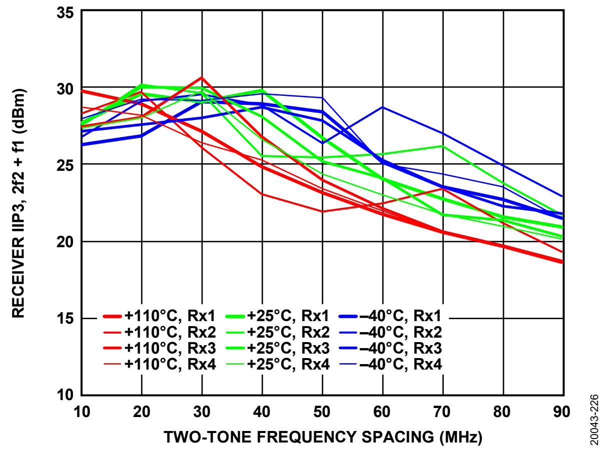


Figure 292. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

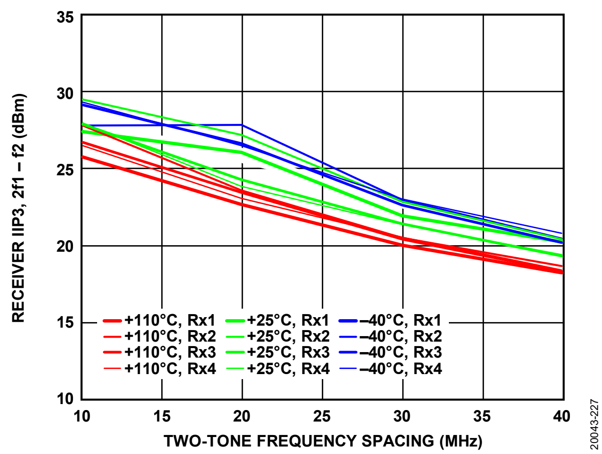


Figure 293. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

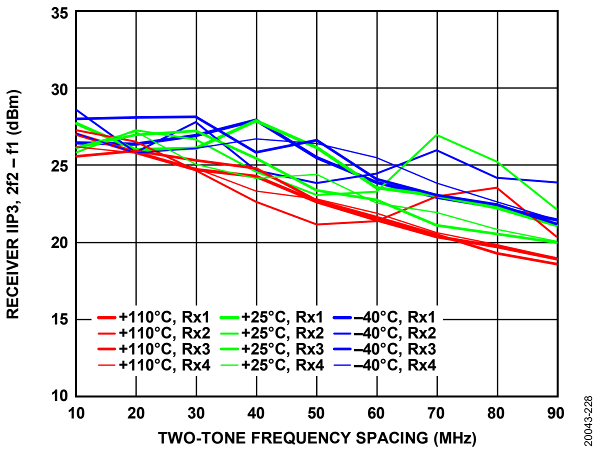


Figure 294. Receiver IIP3, 2f2 − f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

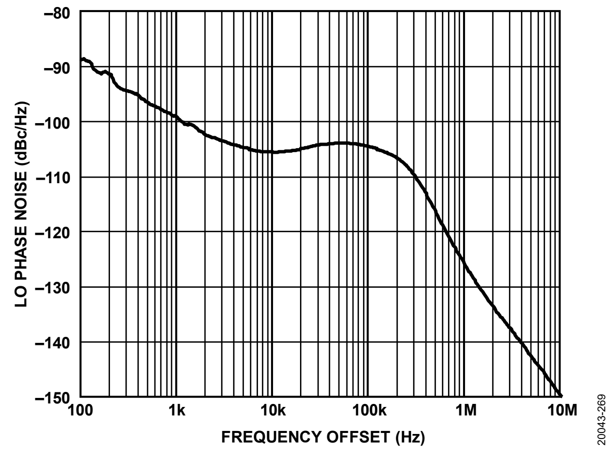


Figure 297. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 600 kHz, Phase Margin = 60°

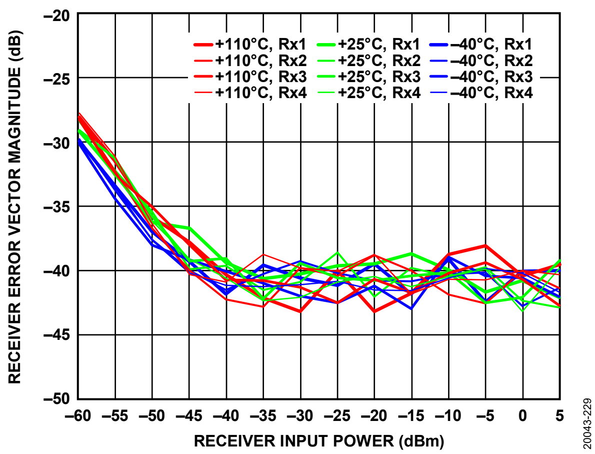


Figure 295. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 600 kHz, Loop Filter Phase Margin = 75°

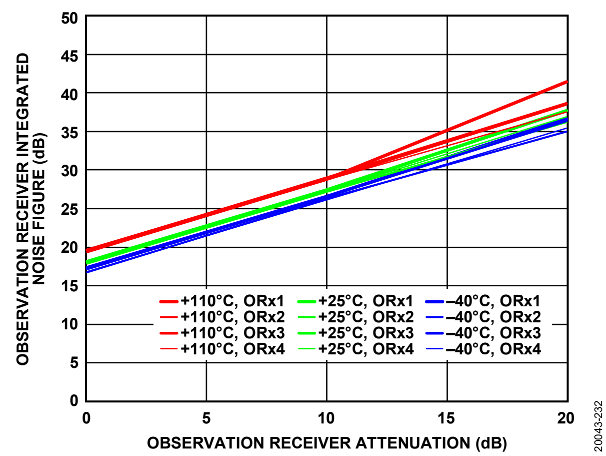


Figure 298. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

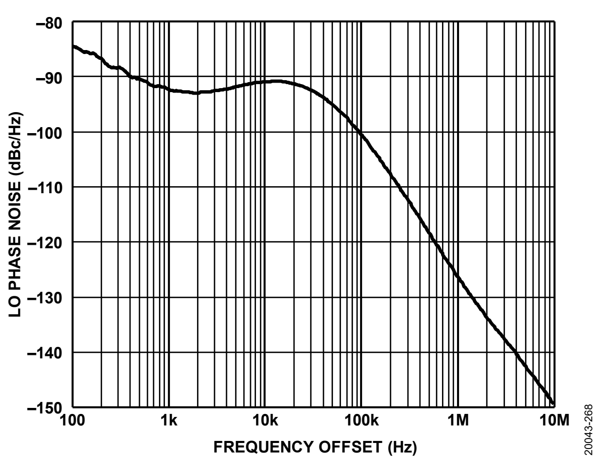


Figure 296. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

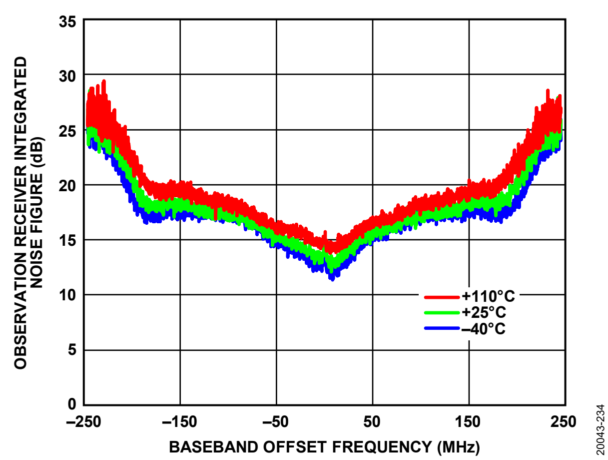


Figure 299. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

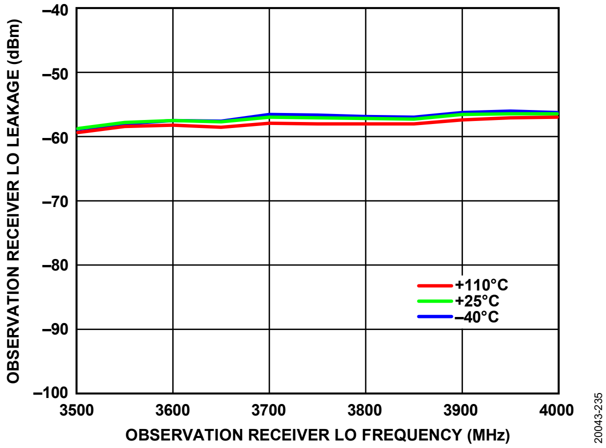


Figure 300. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

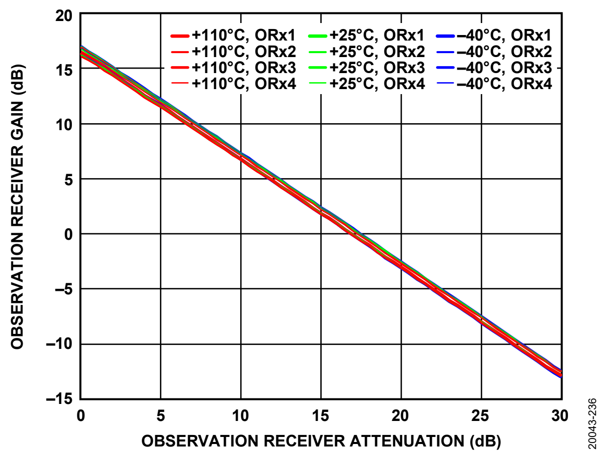


Figure 301. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

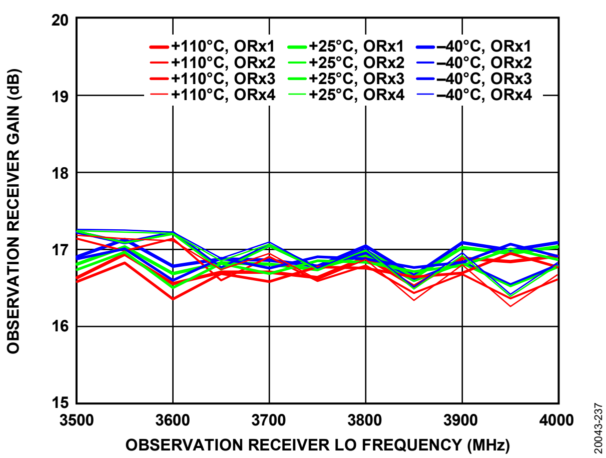


Figure 302. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

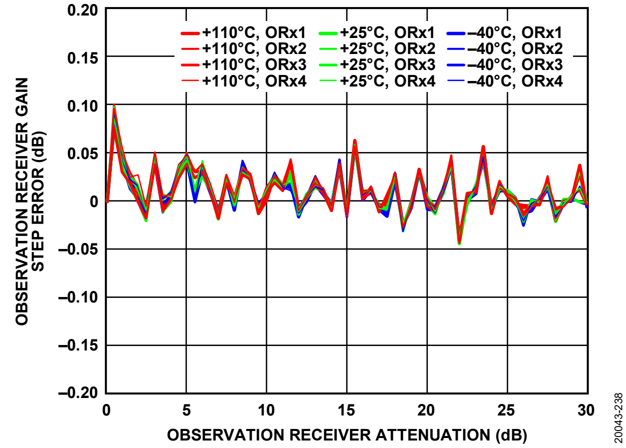


Figure 303. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

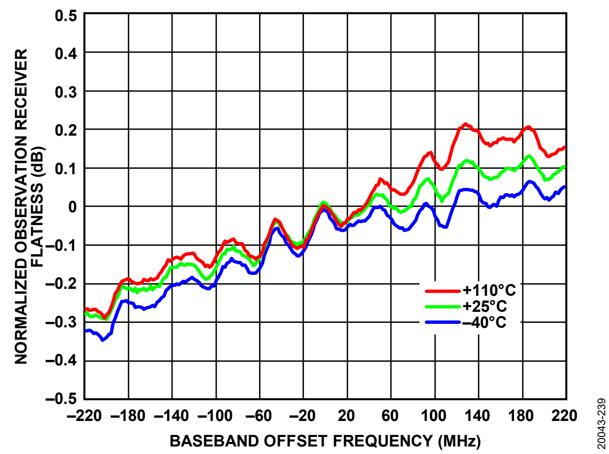


Figure 304. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, –25 dBm Input Signal, 0 dB Attenuation

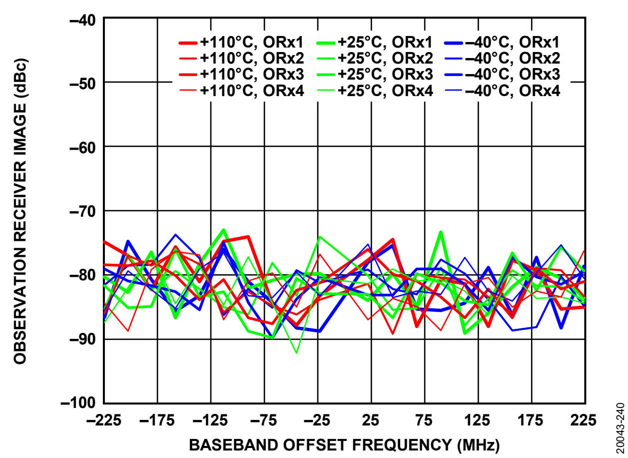


Figure 305. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

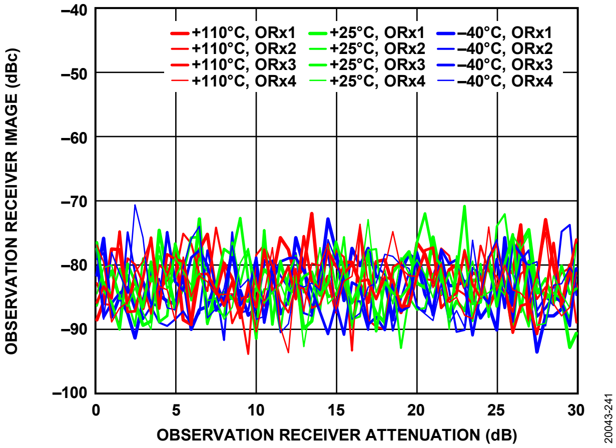


Figure 306. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

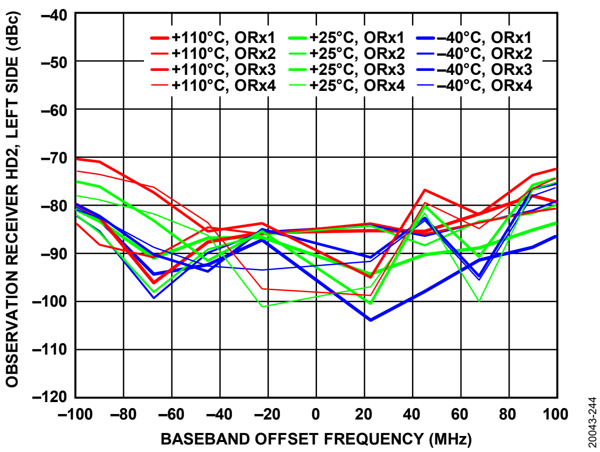


Figure 307. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

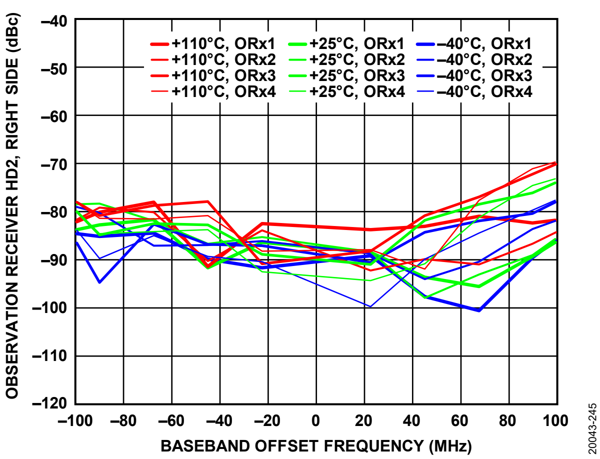


Figure 308. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

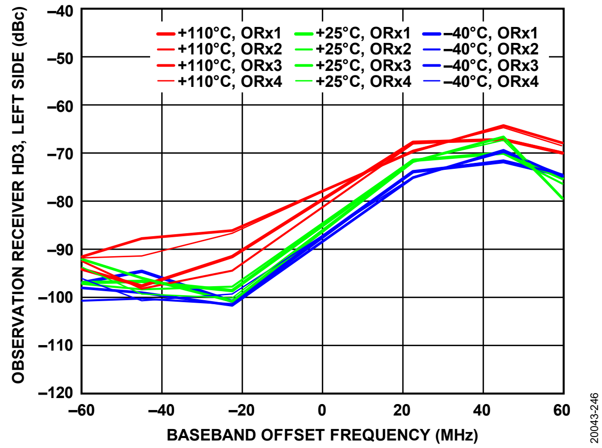


Figure 309. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

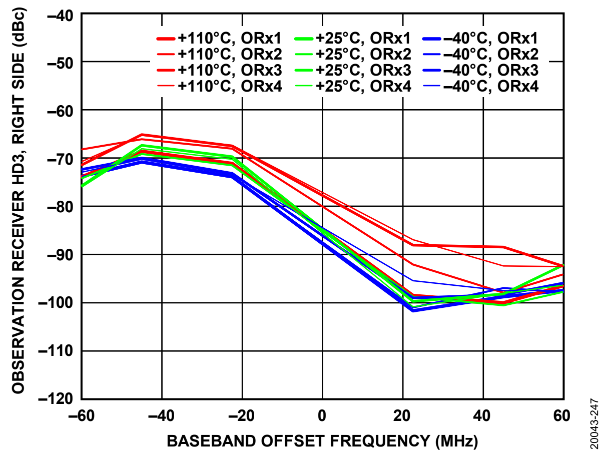


Figure 310. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

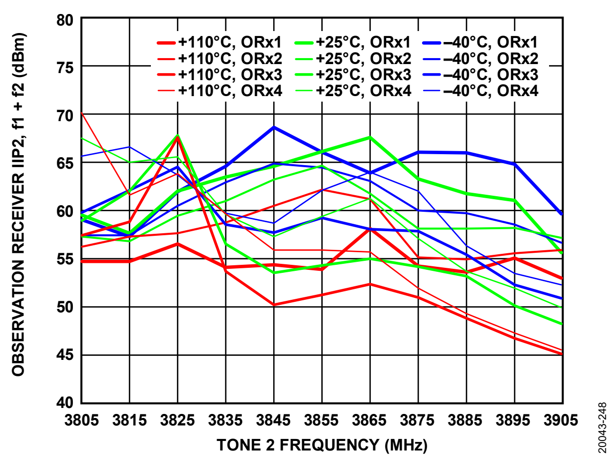


Figure 311. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

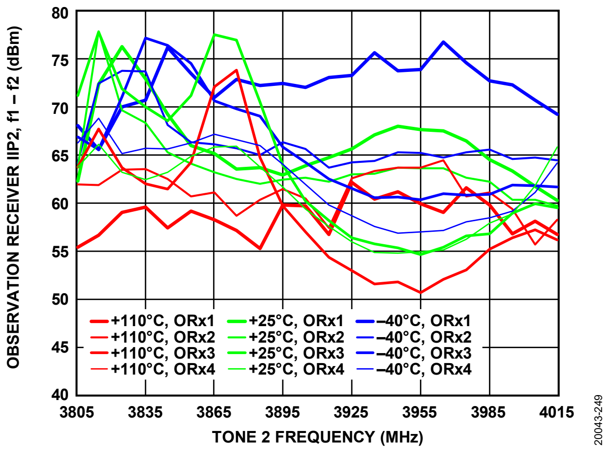


Figure 312. Observation Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

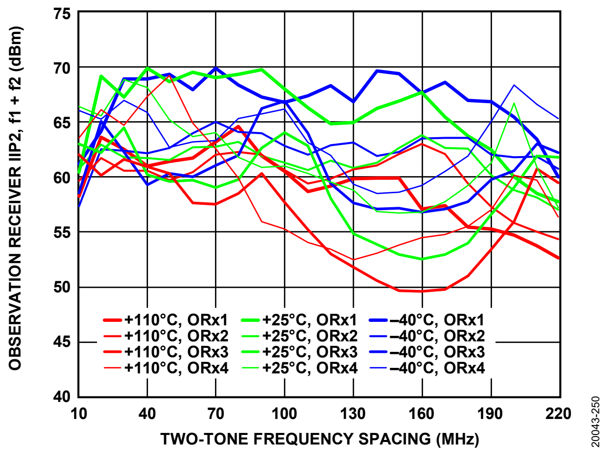


Figure 313. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

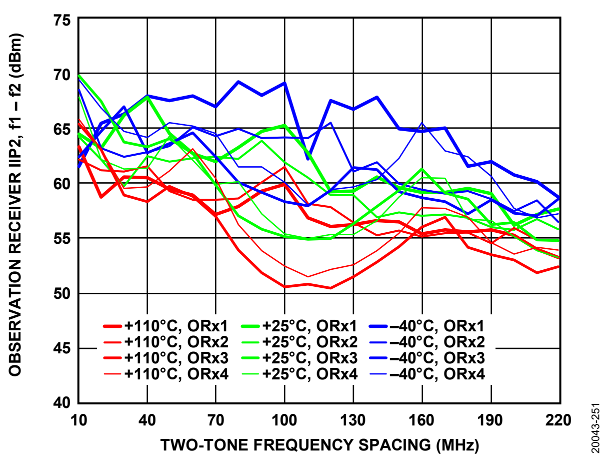


Figure 314. Observation Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

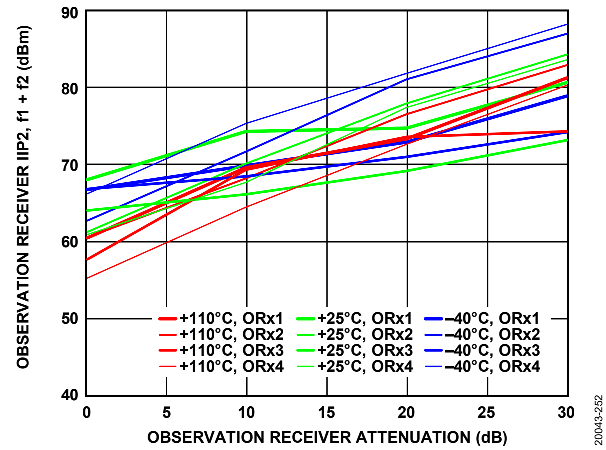


Figure 315. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

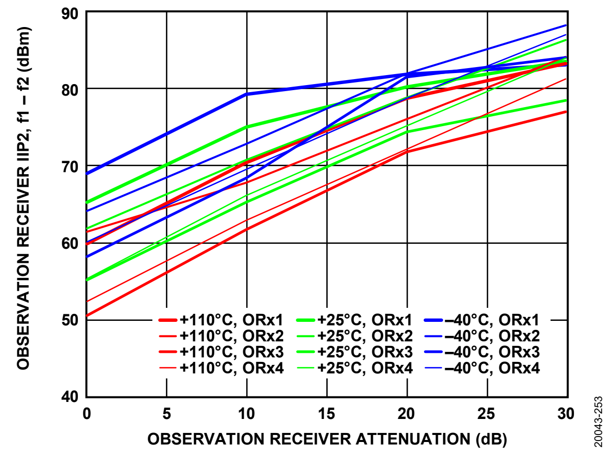


Figure 316. Observation Receiver IIP2, f1 – f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

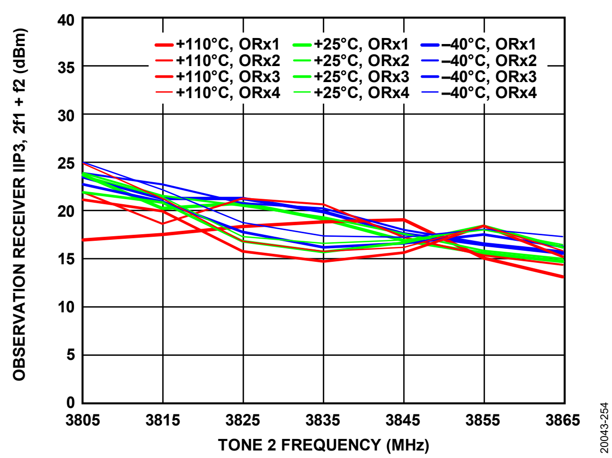


Figure 317. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

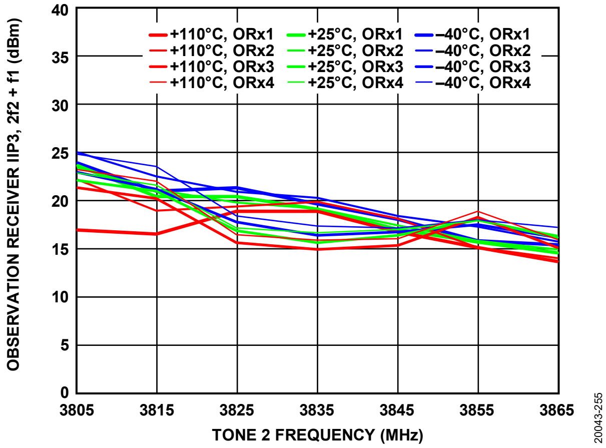


Figure 318. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

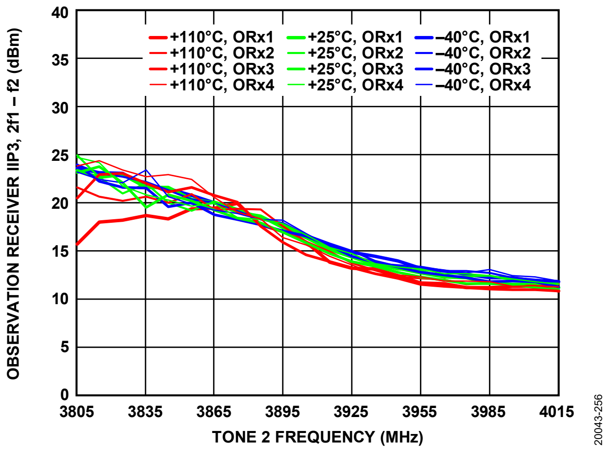


Figure 319. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

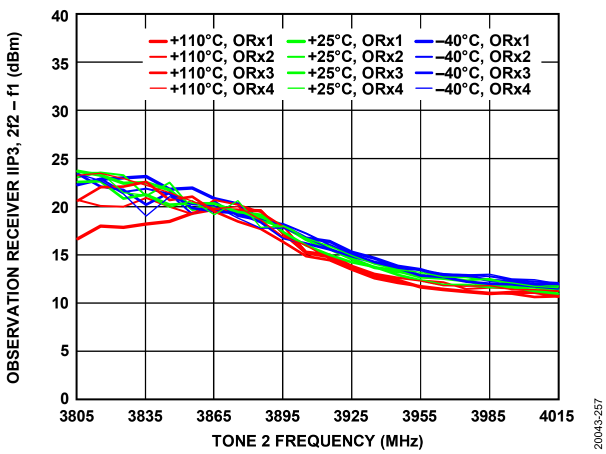


Figure 320. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

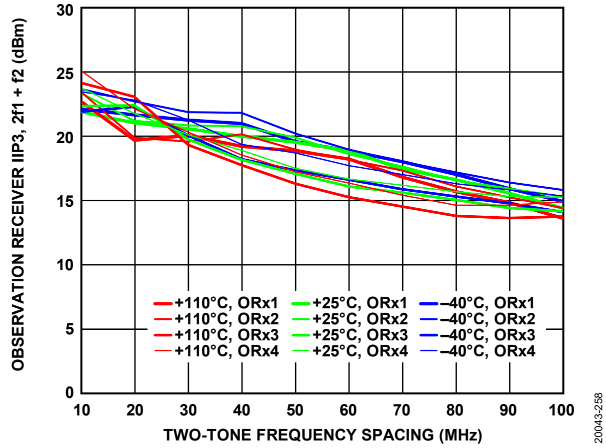


Figure 321. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

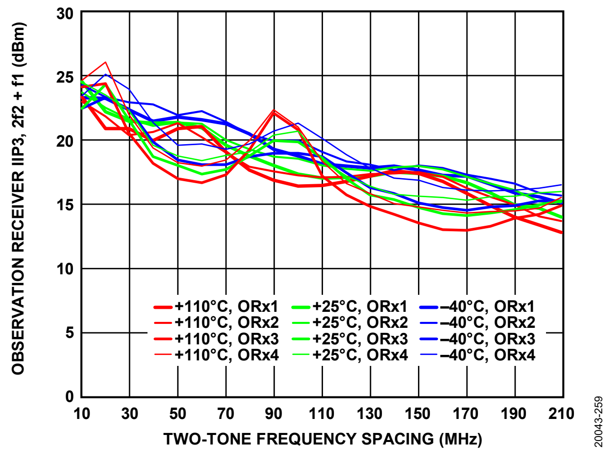


Figure 322. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

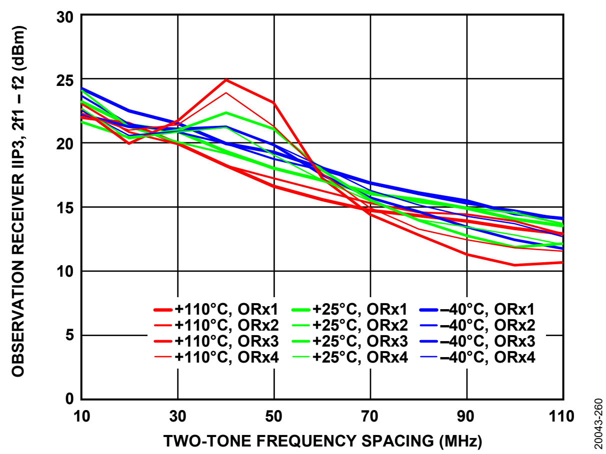


Figure 323. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

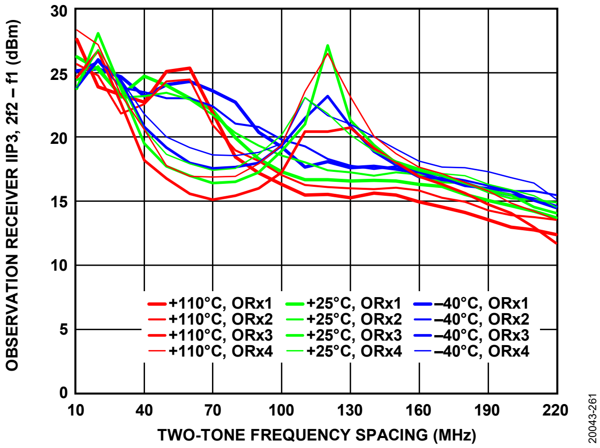


Figure 324. Observation Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

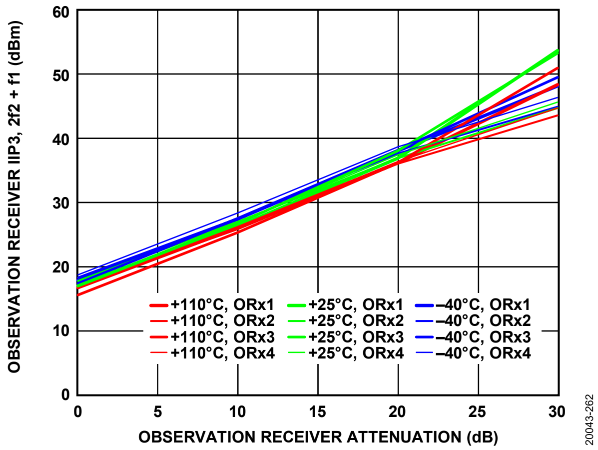


Figure 325. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

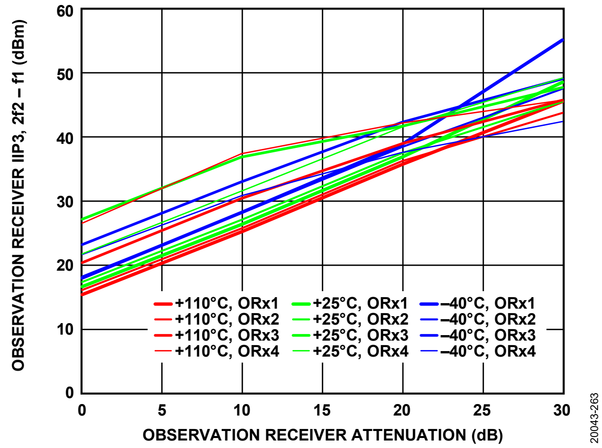


Figure 326. Observation Receiver IIP3, 2f2 – f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

4800 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 4800 MHz, unless otherwise noted.

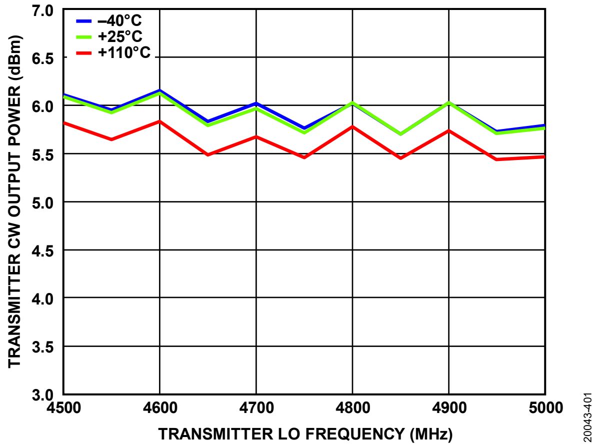


Figure 327. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

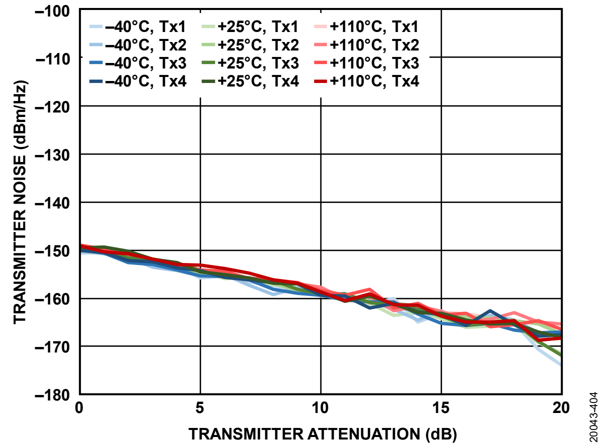


Figure 330. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset

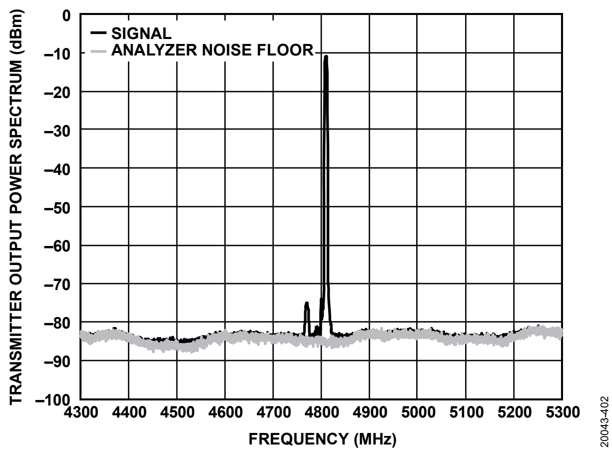


Figure 328. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

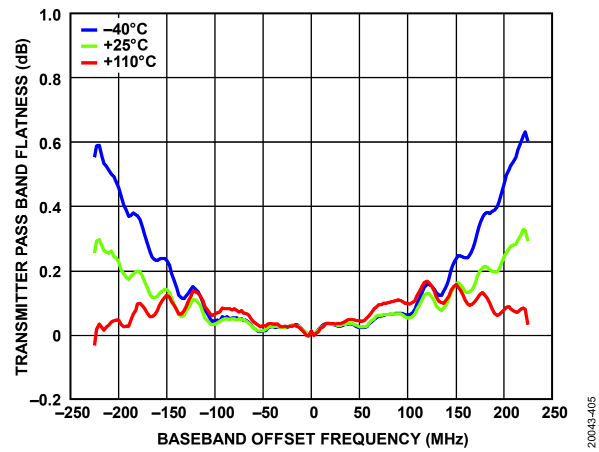


Figure 331. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

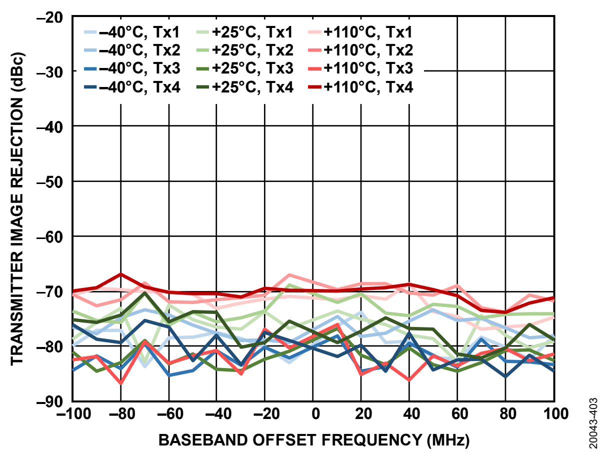


Figure 329. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

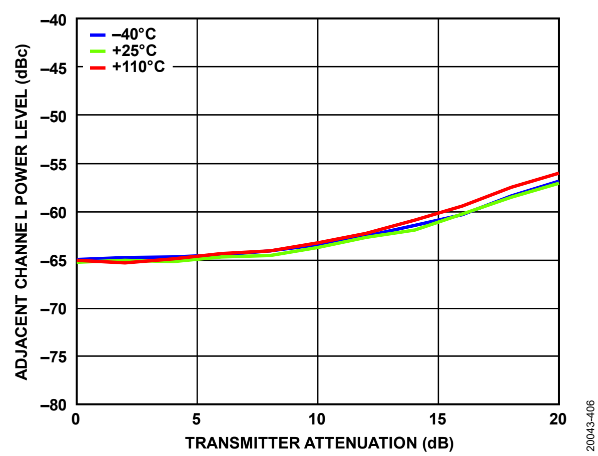


Figure 332. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 800 kHz, Loop Filter Phase Margin = 75°

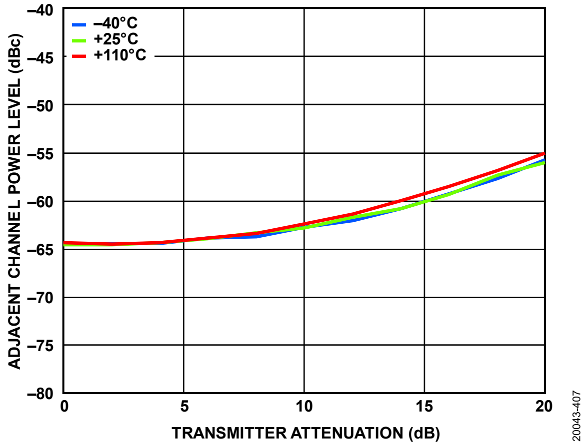


Figure 333. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 800 kHz, Loop Filter Phase Margin = 75°

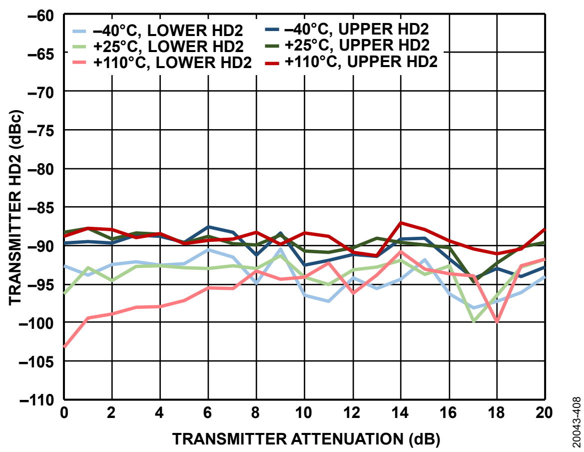


Figure 334. Transmitter HD2 vs. Transmitter Attenuation, 10 MHz Offset

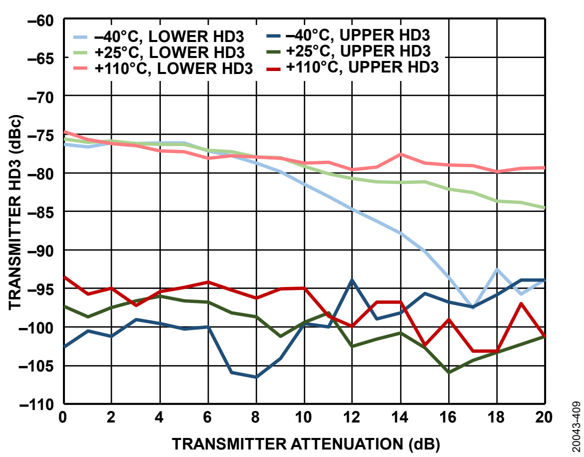


Figure 335. Transmitter HD3 vs. Transmitter Attenuation, 10 MHz Offset

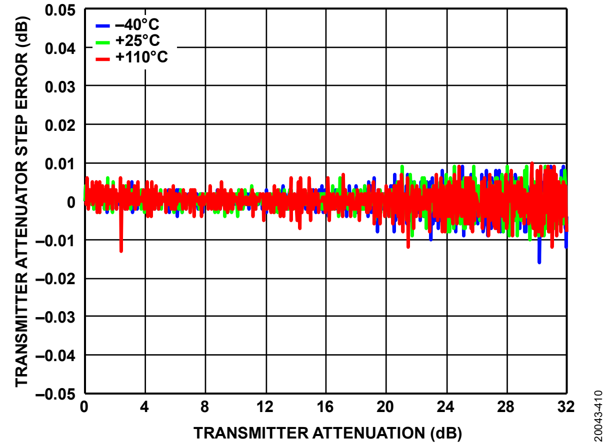


Figure 336. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

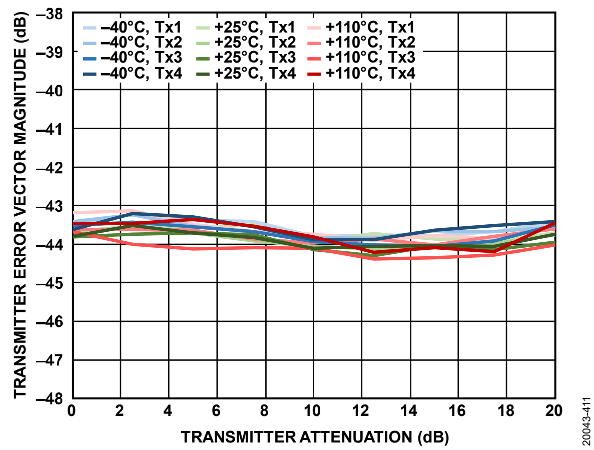


Figure 337. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52 MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 800 kHz, Loop Filter Phase Margin = 75°

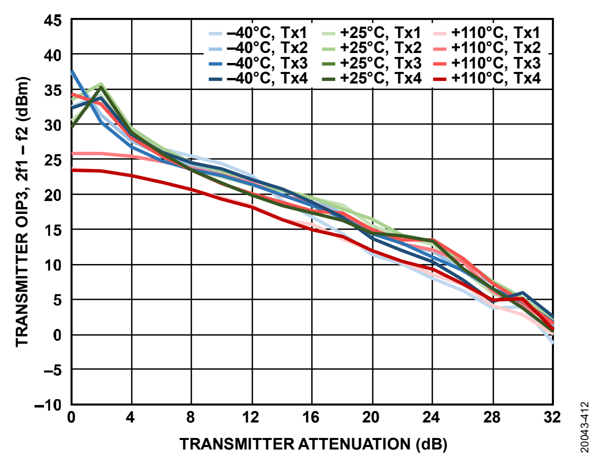


Figure 338. Transmitter OIP3, 2f1 − f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

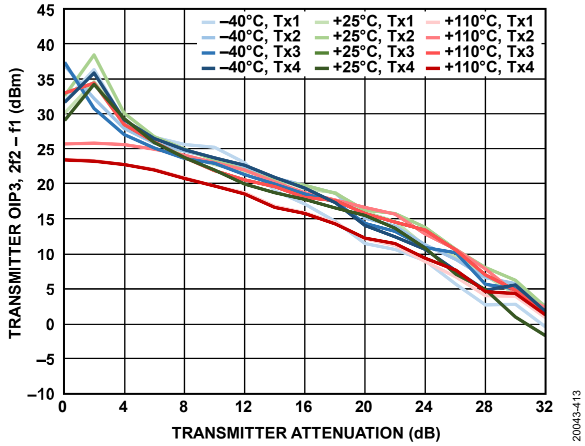


Figure 339. Transmitter OIP3, 2f2 – f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

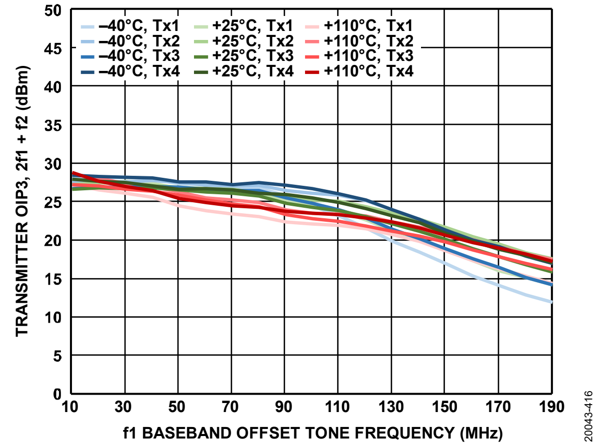


Figure 342. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

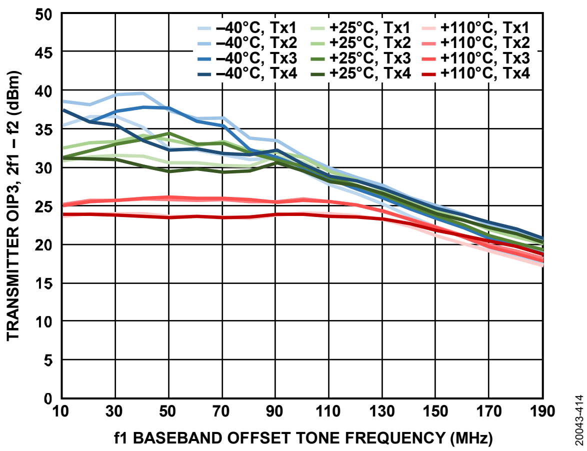


Figure 340. Transmitter OIP3, 2f1 – f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

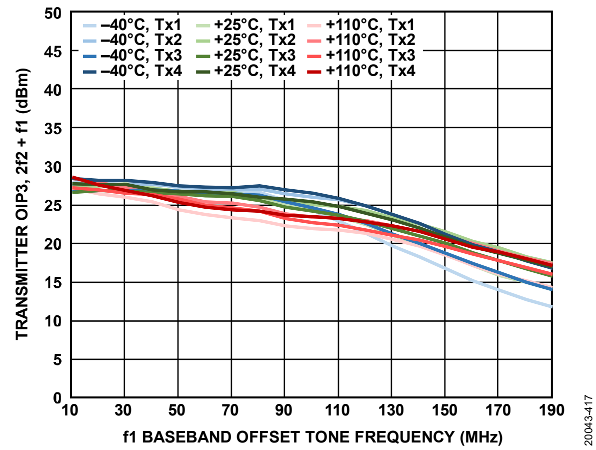


Figure 343. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

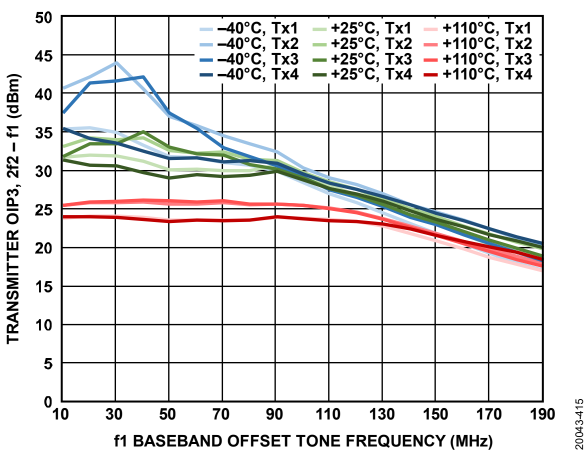


Figure 341. Transmitter OIP3, 2f2 – f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

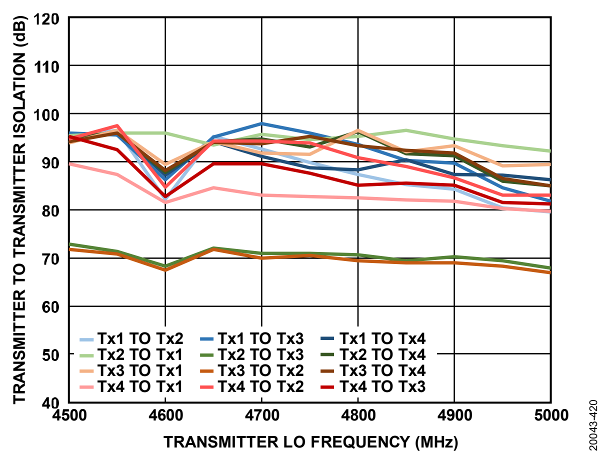


Figure 344. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

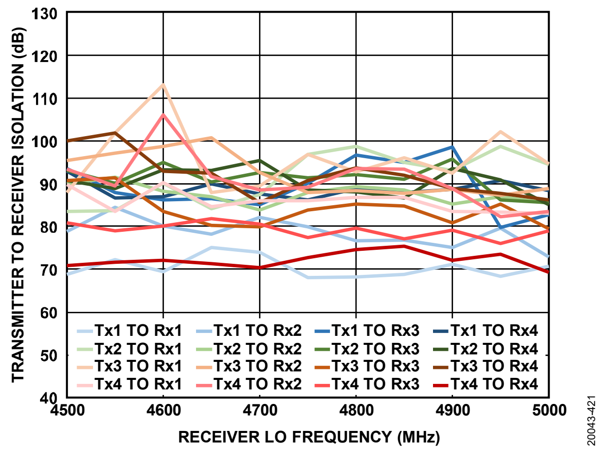


Figure 345. Transmitter to Receiver Isolation vs. Receiver LO Frequency

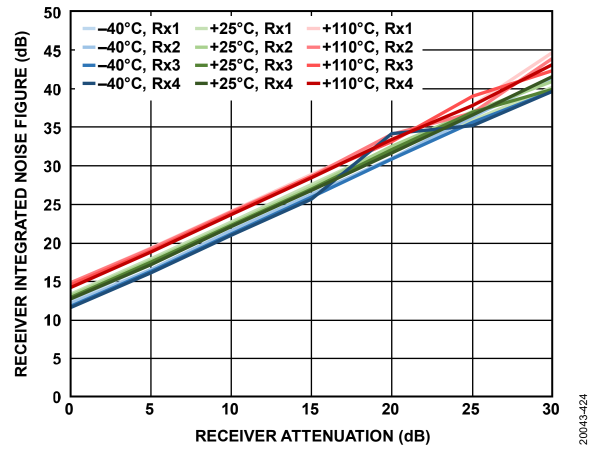


Figure 348. Receiver Integrated Noise Figure vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

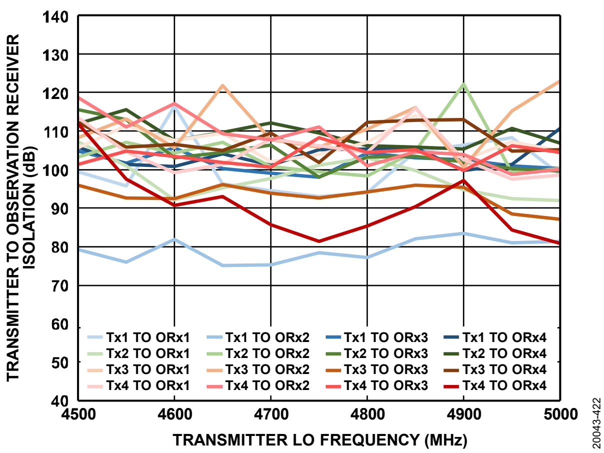


Figure 346. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

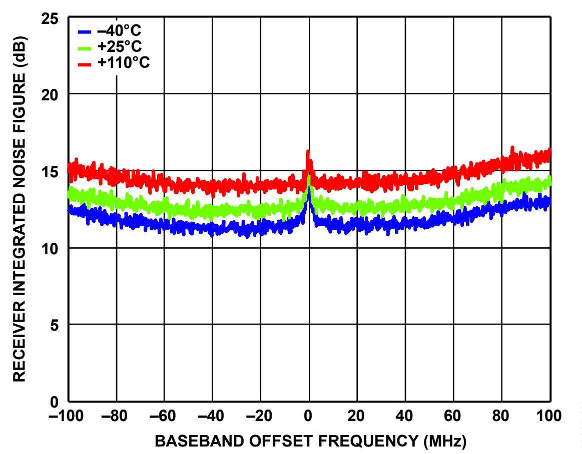


Figure 349. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

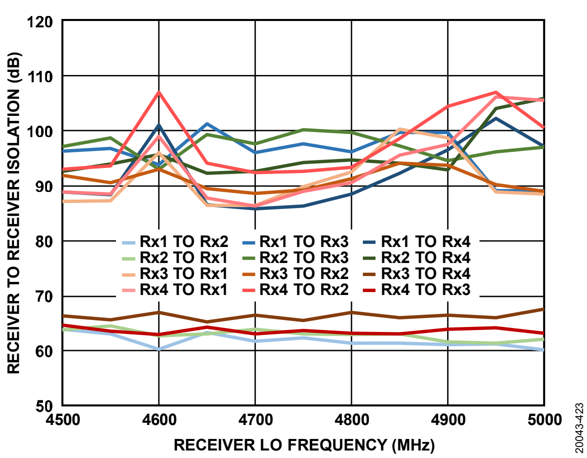


Figure 347. Receiver to Receiver Isolation vs. Receiver LO Frequency

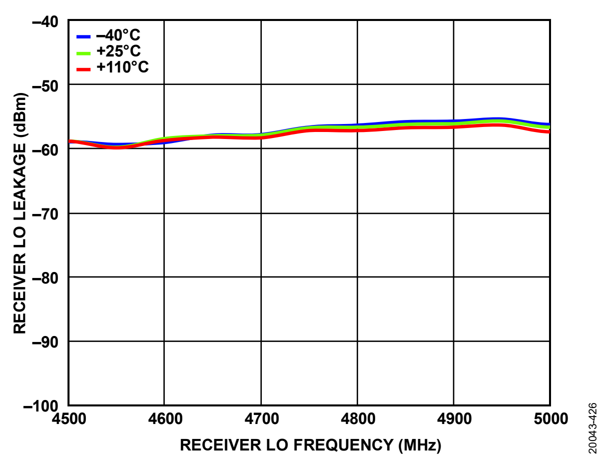


Figure 350. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

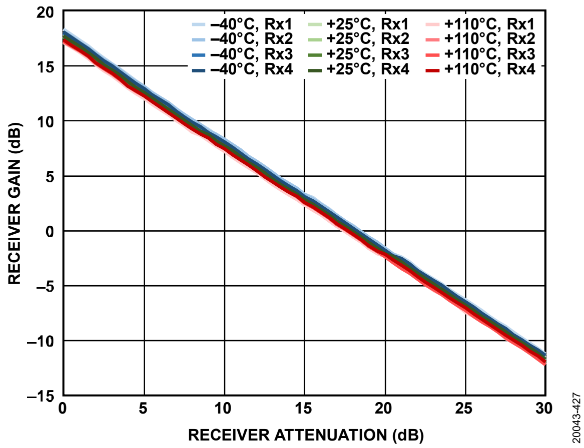


Figure 351. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

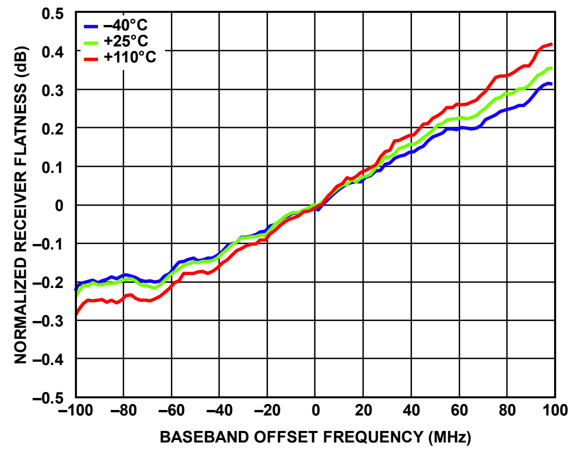


Figure 354. Normalized Receiver Flatness vs. Baseband Offset Frequency, −5 dBFS Input Signal

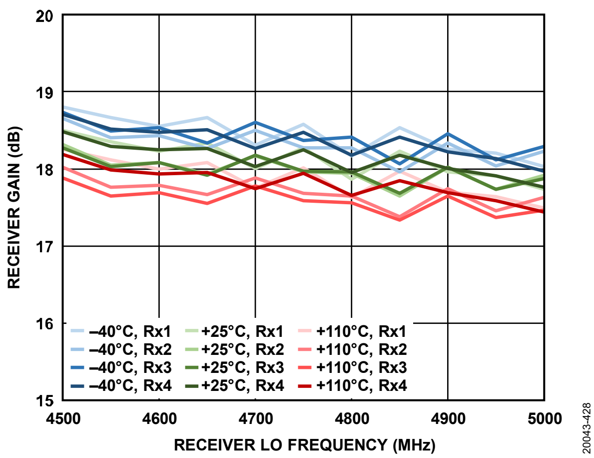


Figure 352. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

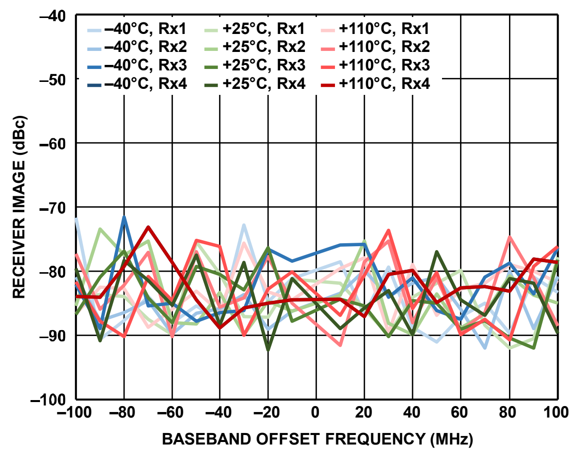


Figure 355. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

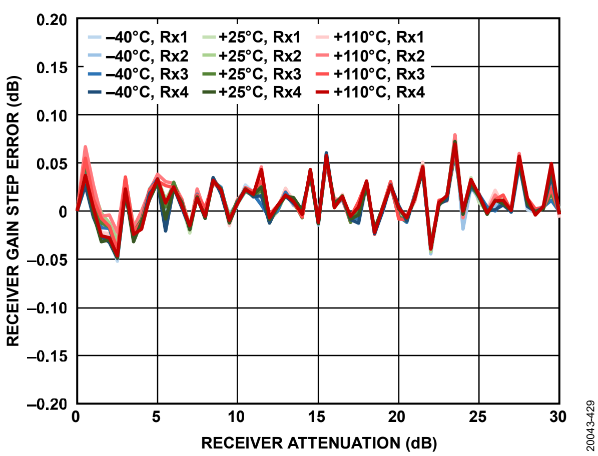


Figure 353. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

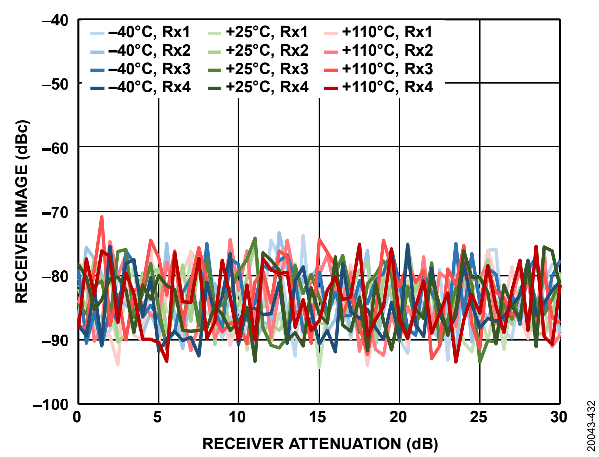


Figure 356. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, −5 dBFS Input Signal

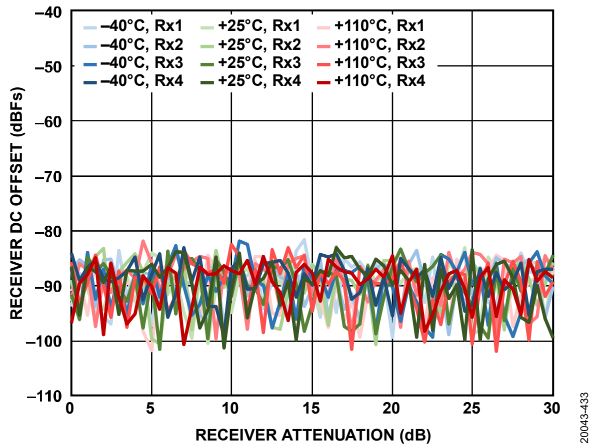


Figure 357. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

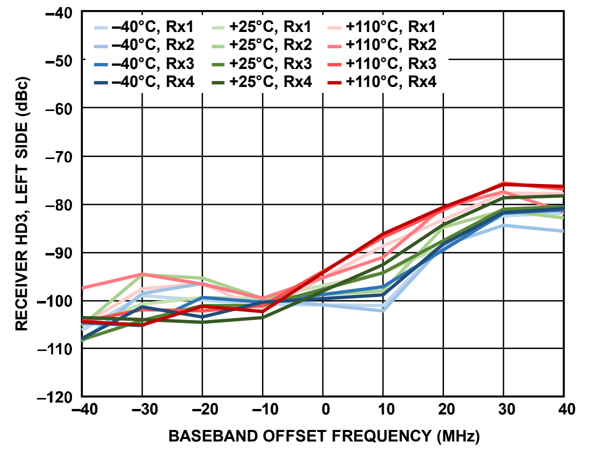


Figure 360. Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

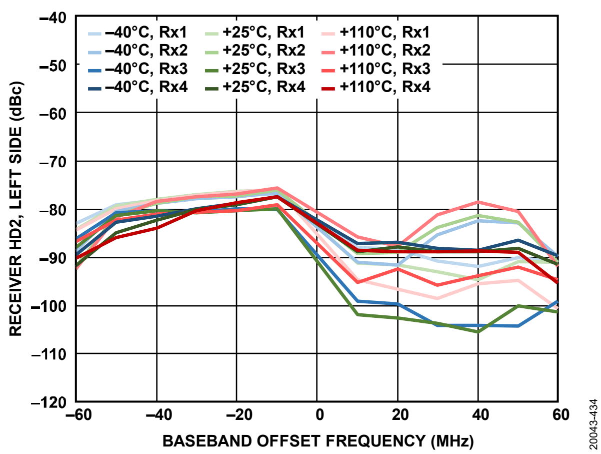


Figure 358. Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

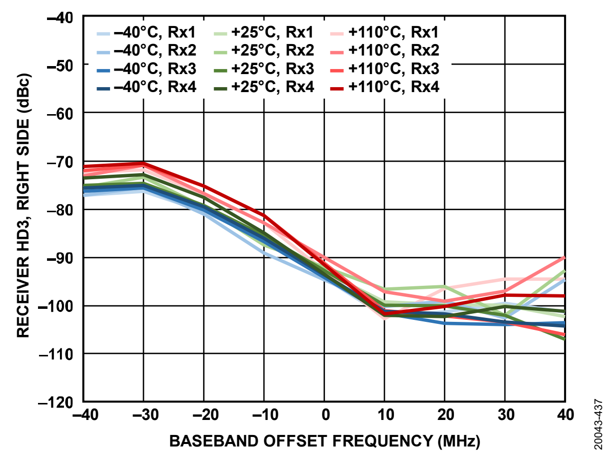


Figure 361. Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

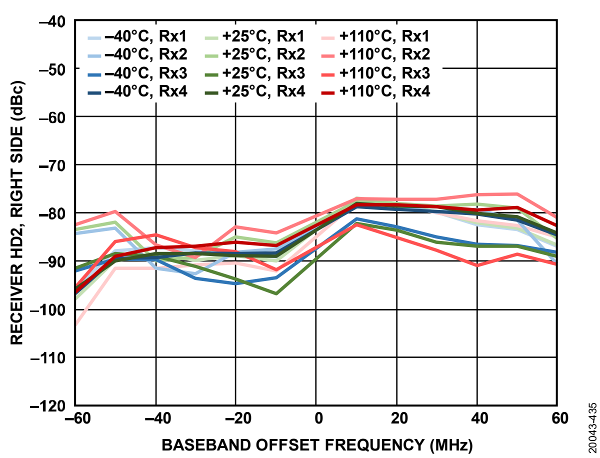


Figure 359. Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

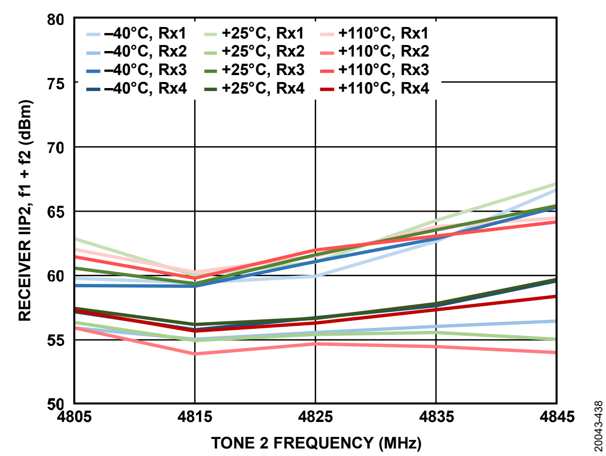


Figure 362. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

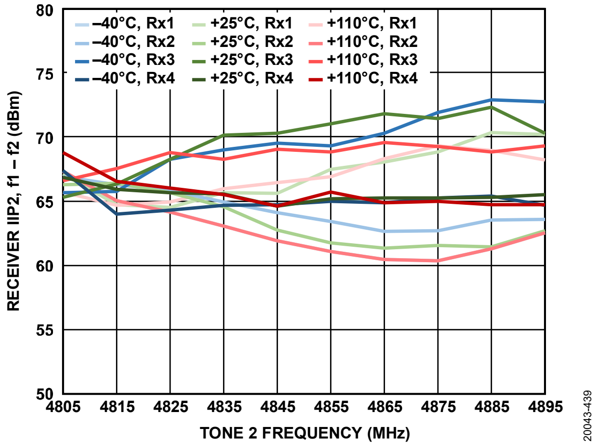


Figure 363. Receiver IIP2, f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

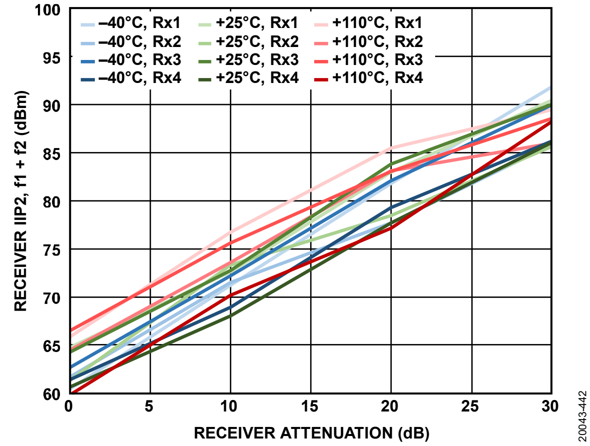


Figure 366. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at −11 dBFS, f1 = 92 MHz, f2 = 2 MHz

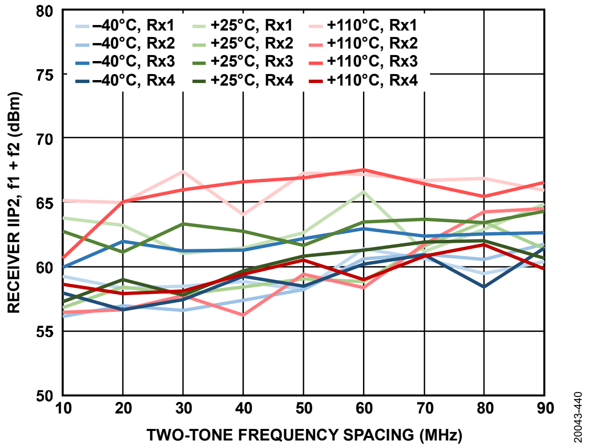


Figure 364. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

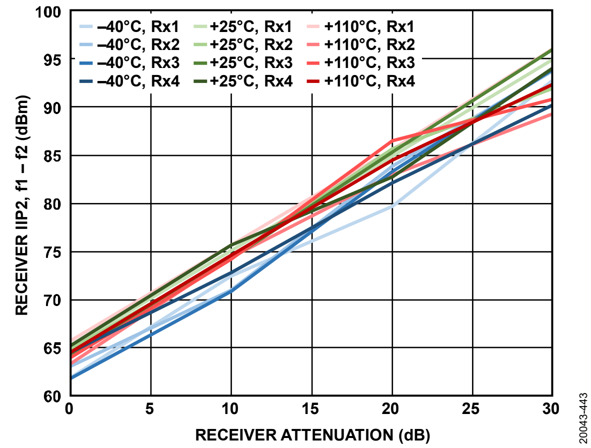


Figure 367. Receiver IIP2, f1 − f2 vs. Receiver Attenuation, Both Tones at −11 dBFS, f1 = 92 MHz, f2 = 2 MHz

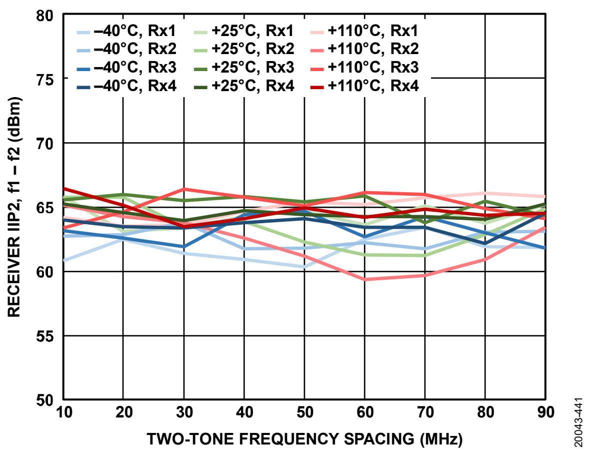


Figure 365. Receiver IIP2, f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

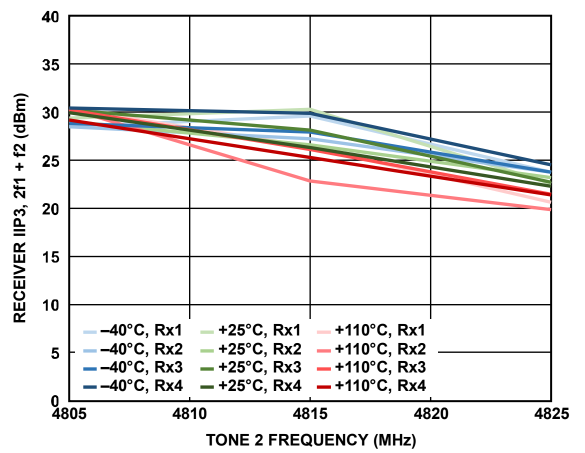


Figure 368. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

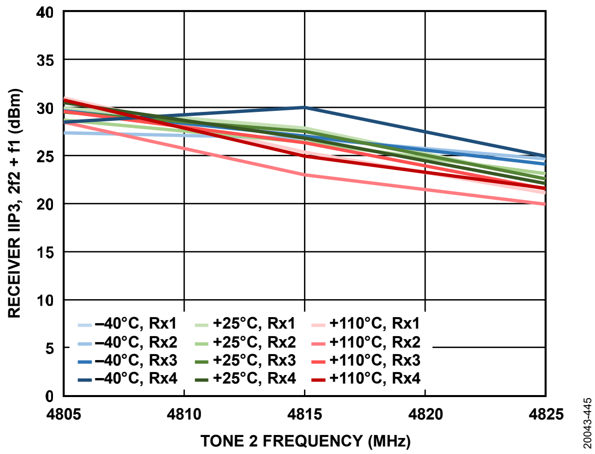


Figure 369. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

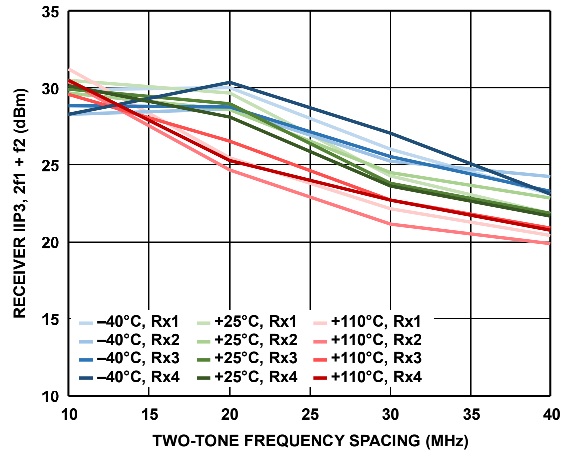


Figure 372. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

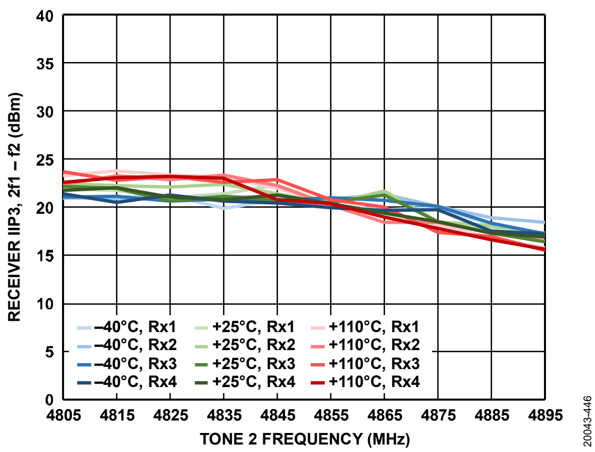


Figure 370. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

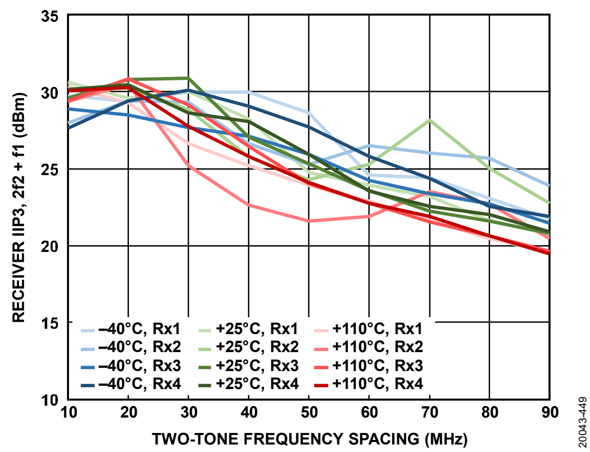


Figure 373. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

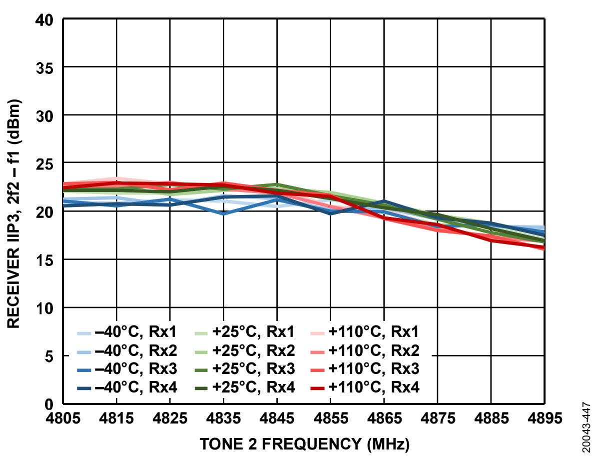


Figure 371. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

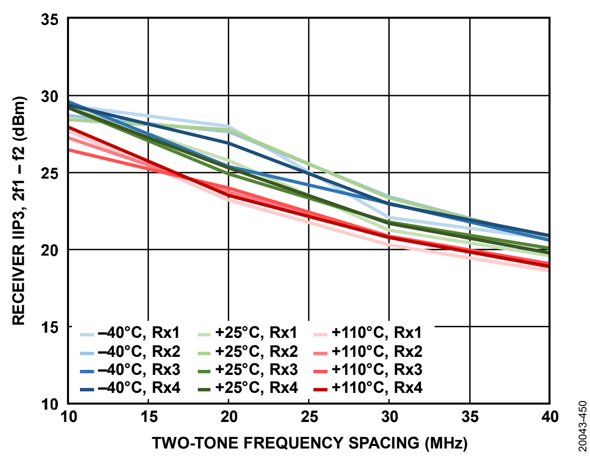


Figure 374. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

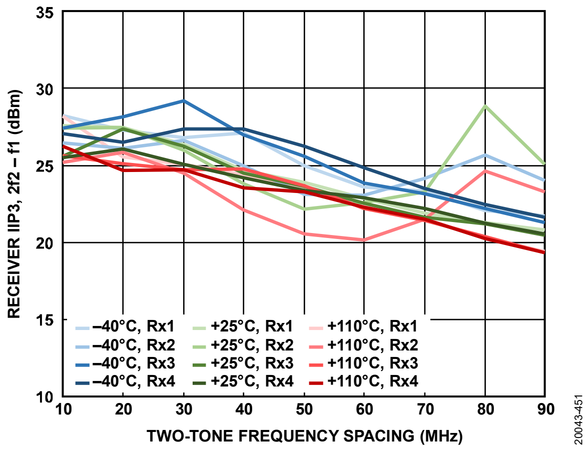


Figure 375. Receiver IIP3, 2f2 − f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

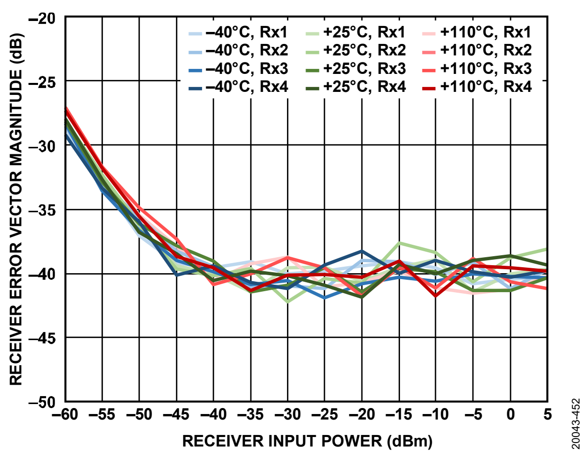


Figure 376. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 800 kHz, Loop Filter Phase Margin = 75°

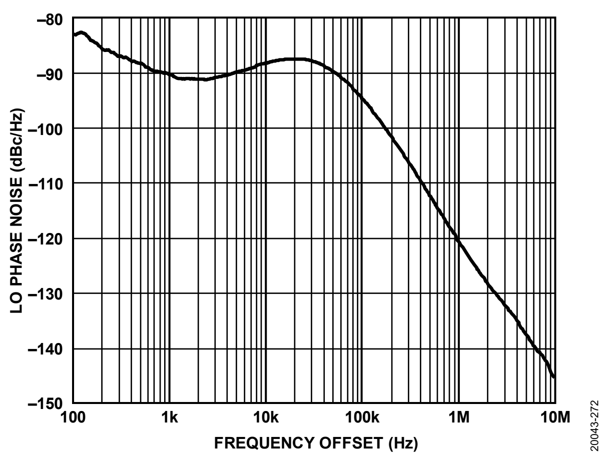


Figure 377. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

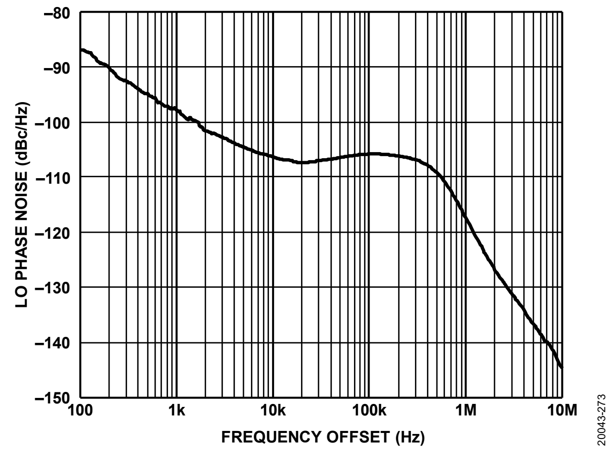


Figure 378. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 400 kHz, Phase Margin = 60°

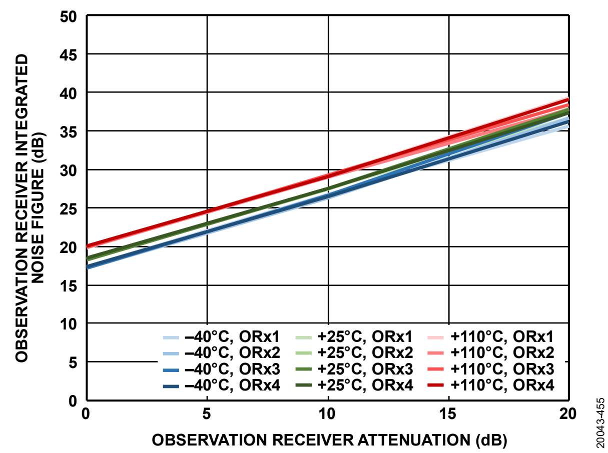


Figure 379. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

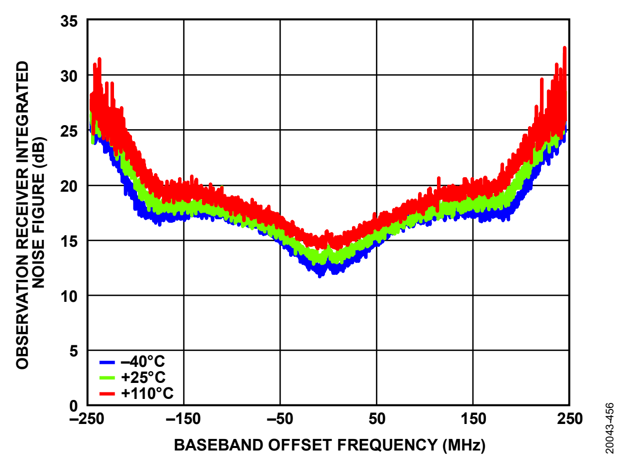


Figure 380. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

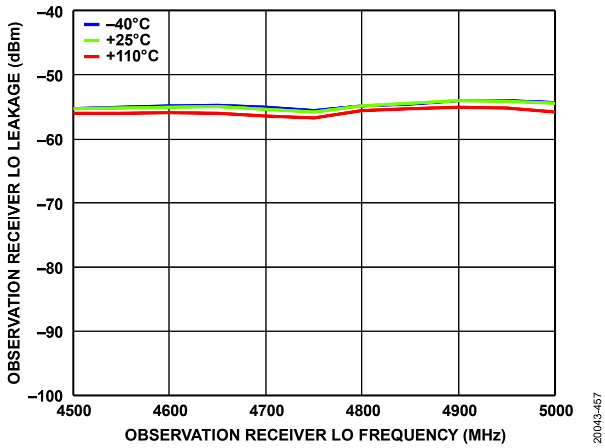


Figure 381. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

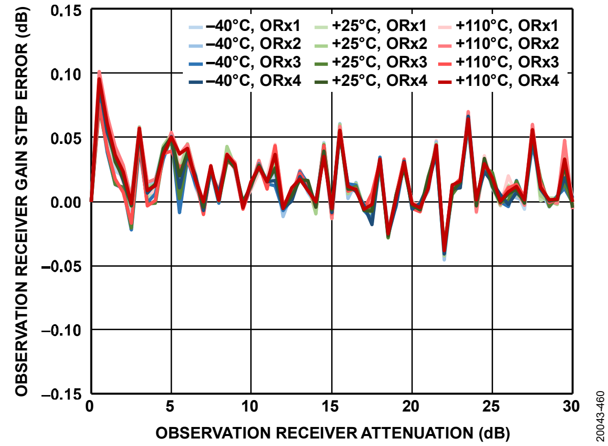


Figure 384. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

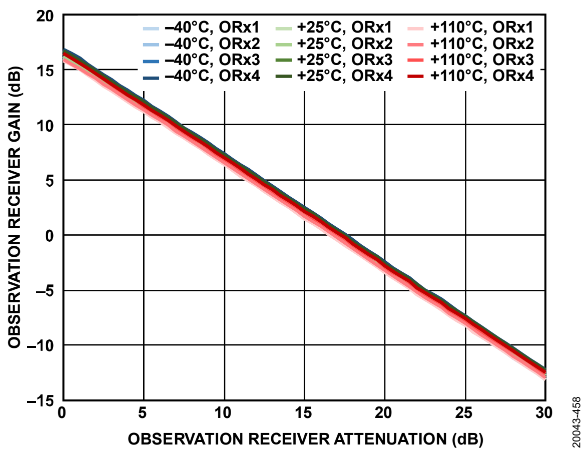


Figure 382. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

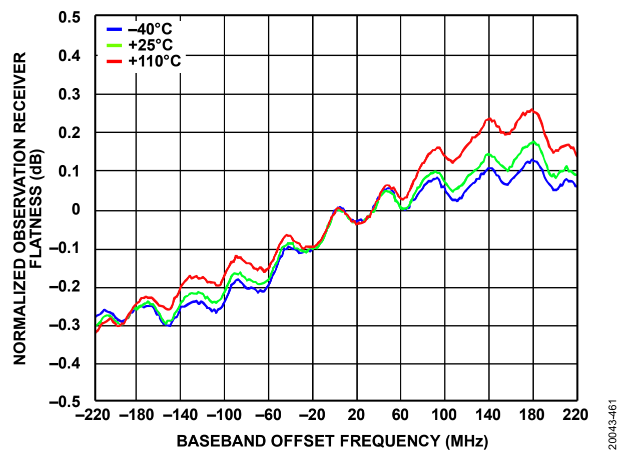


Figure 385. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, −25 dBm Input Signal, 0 dB Attenuation

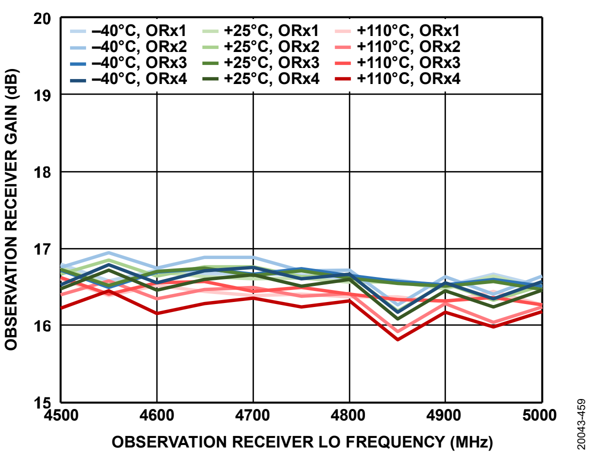


Figure 383. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

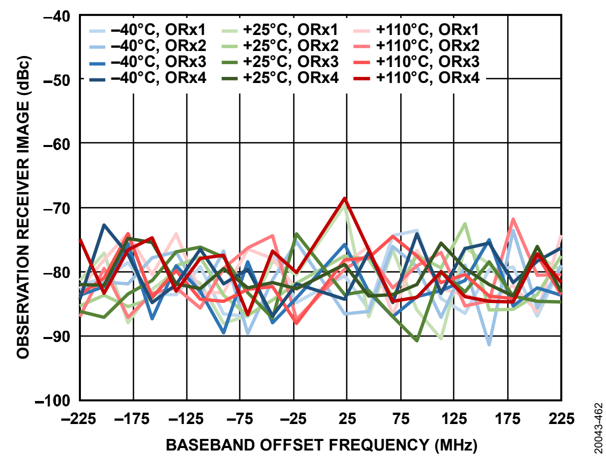


Figure 386. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

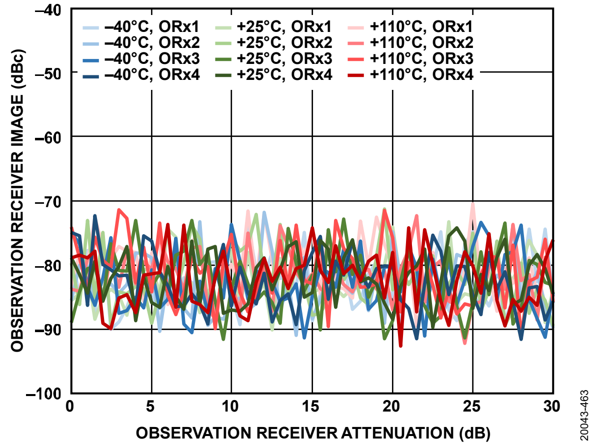


Figure 387. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

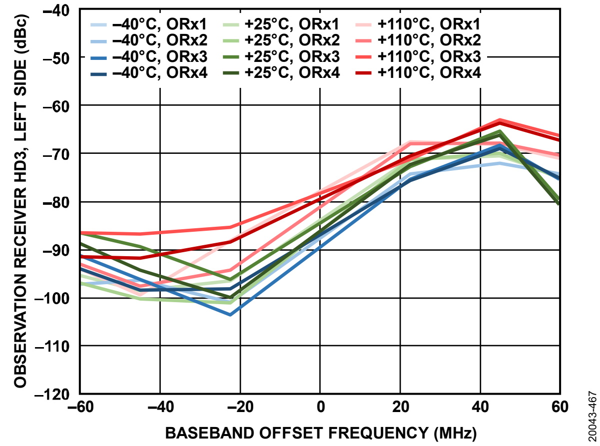


Figure 390. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

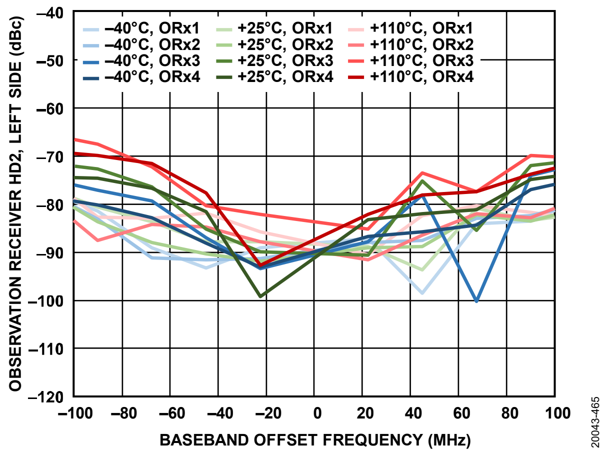


Figure 388. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

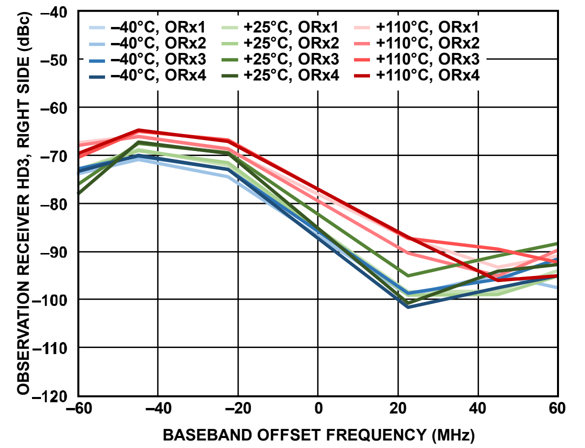


Figure 391. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

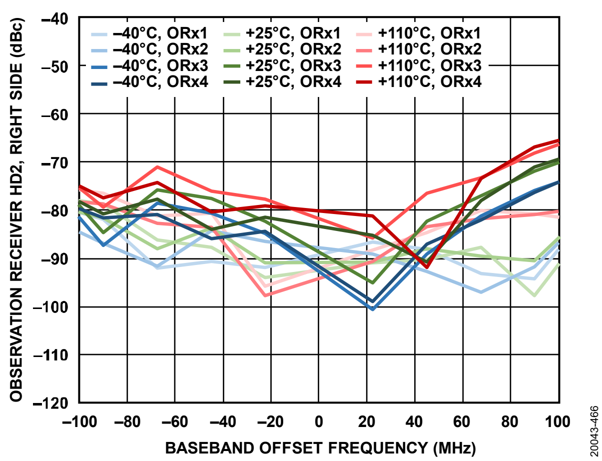


Figure 389. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

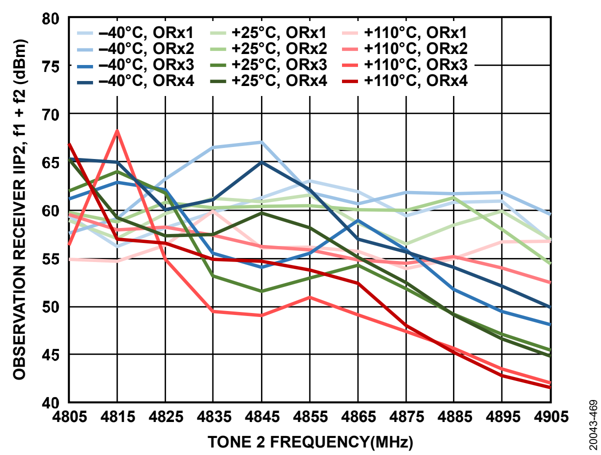


Figure 392. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

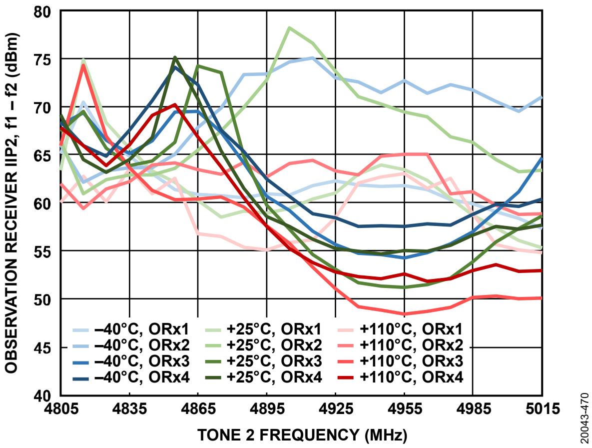


Figure 393. Observation Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

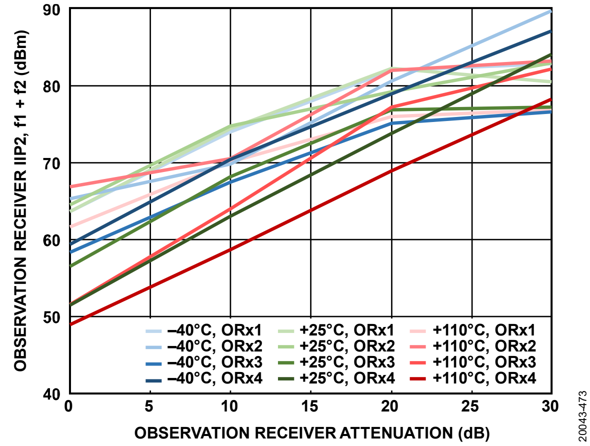


Figure 396. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

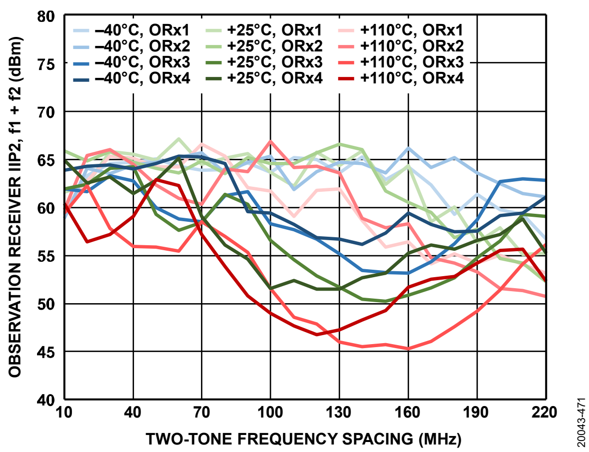


Figure 394. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

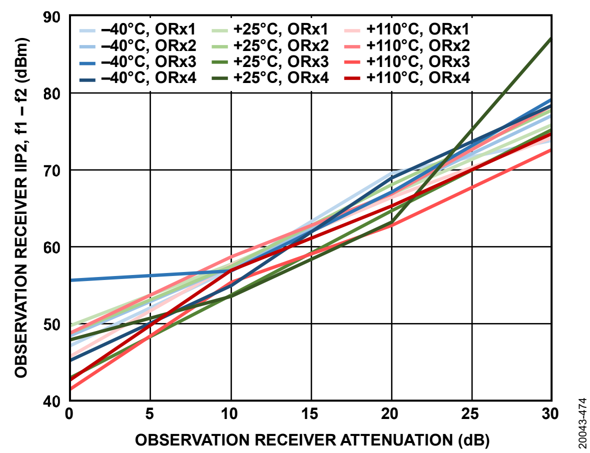


Figure 397. Observation Receiver IIP2, f1 – f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

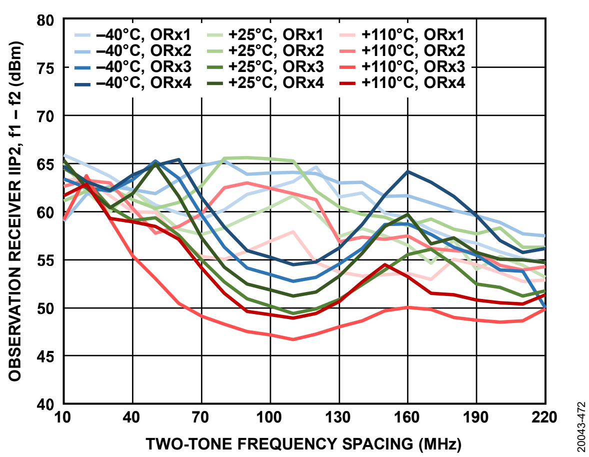


Figure 395. Observation Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

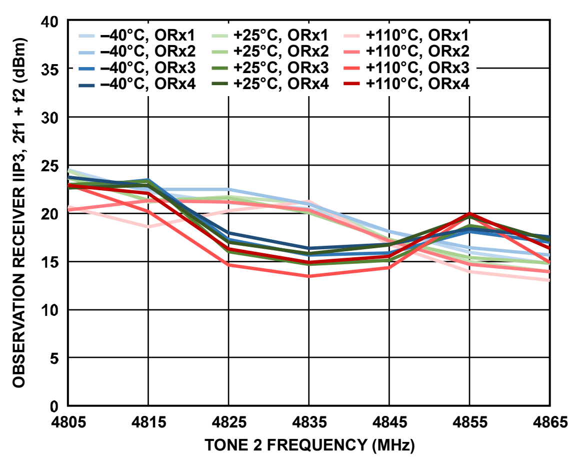


Figure 398. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

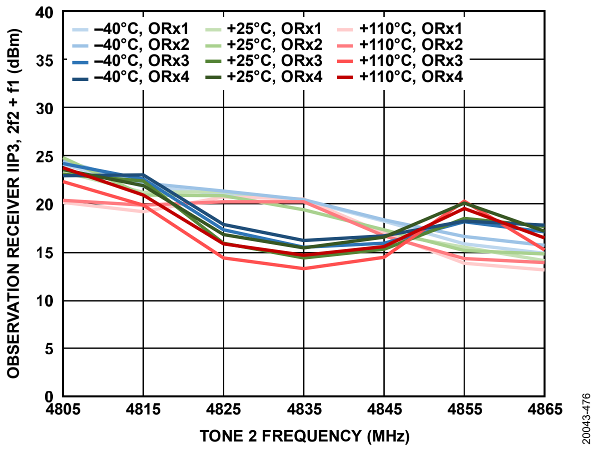


Figure 399. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

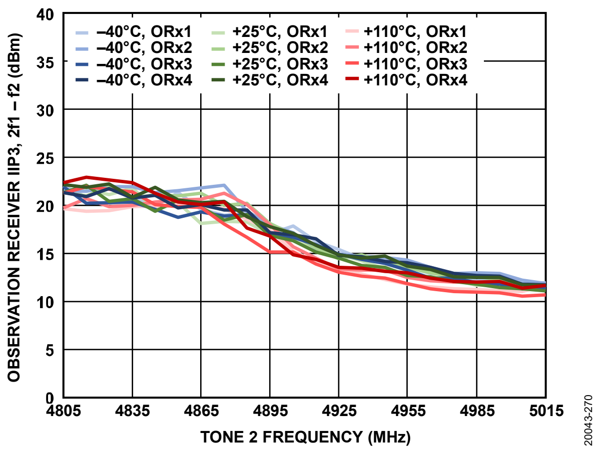


Figure 400. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

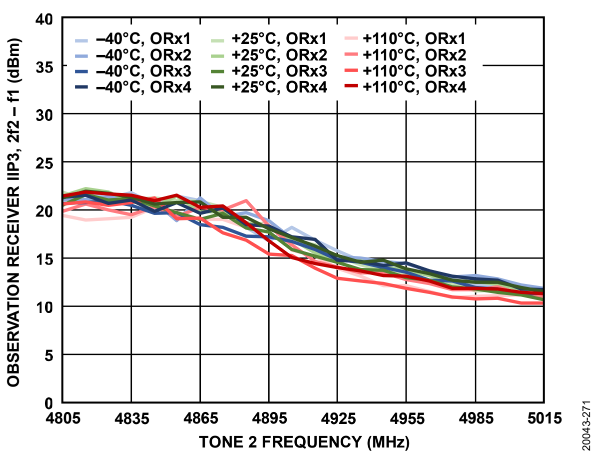


Figure 401. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

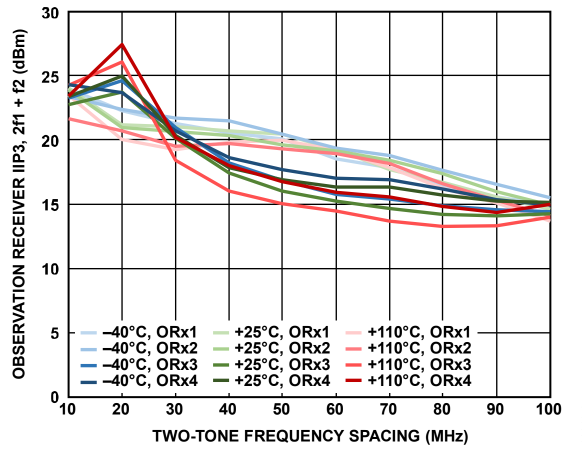


Figure 402. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

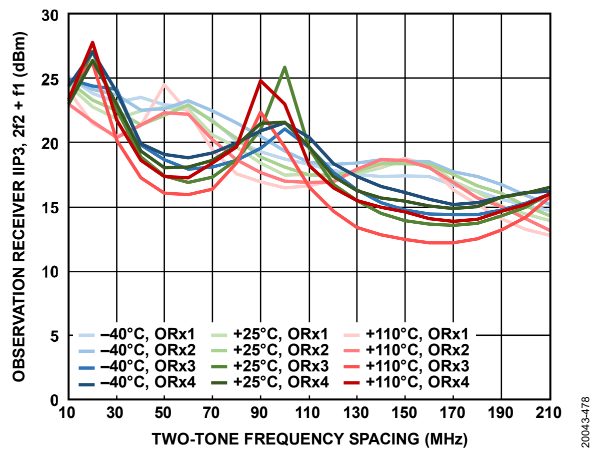


Figure 403. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

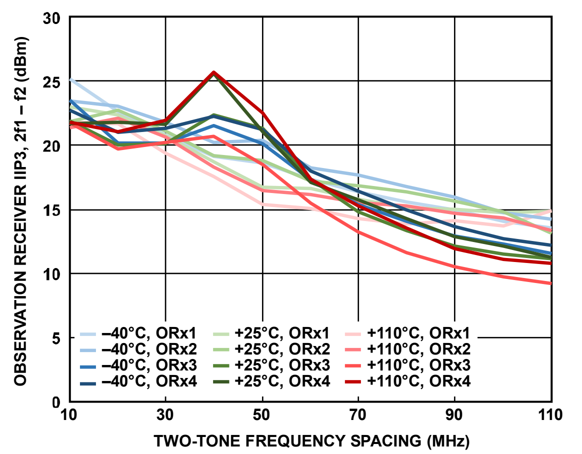


Figure 404. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

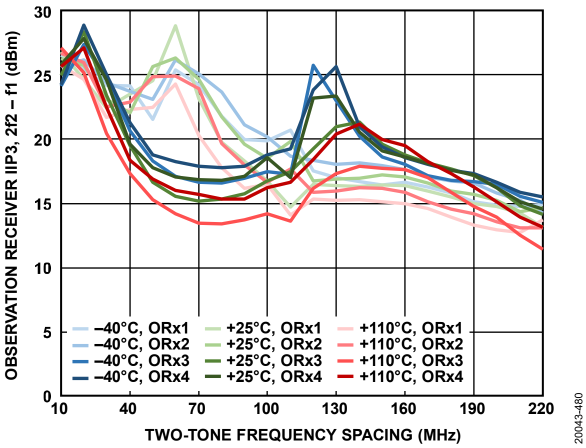


Figure 405. Observation Receiver IIP3, 2f2 − f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

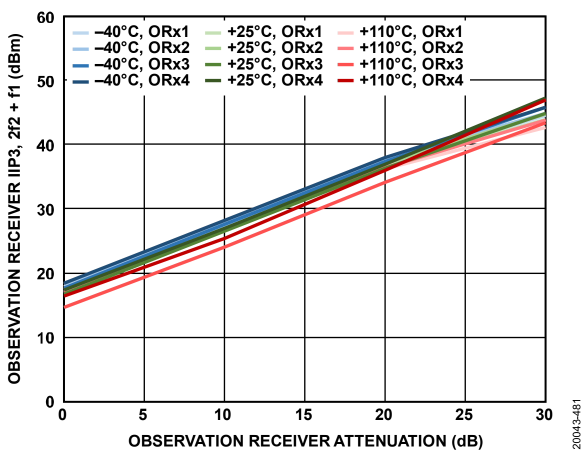


Figure 406. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 122 MHz, f2 = 2 MHz

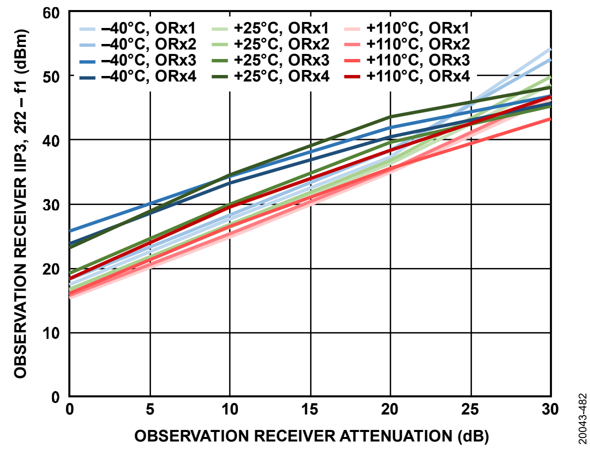


Figure 407. Observation Receiver IIP3, 2f2 − f1 vs. Observation Receiver Attenuation, Both Tones at −11 dBFS, f1 = 122 MHz, f2 = 2 MHz

5700 MHz BAND

The temperature settings refer to the die temperature. All LO frequencies set to 5700 MHz, unless otherwise noted.

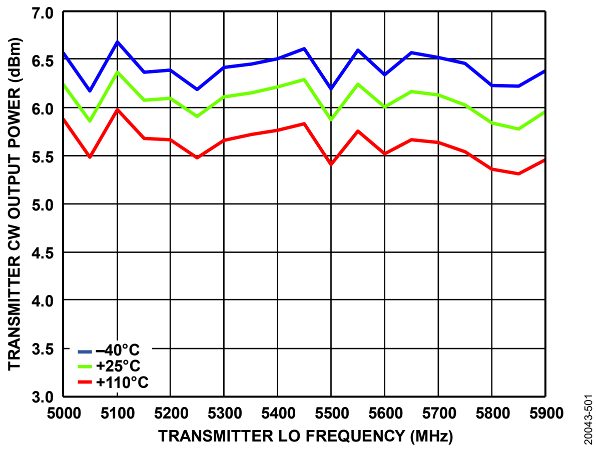


Figure 408. Transmitter CW Output Power vs. Transmitter LO Frequency, 10 MHz Offset, 0 dB Attenuation

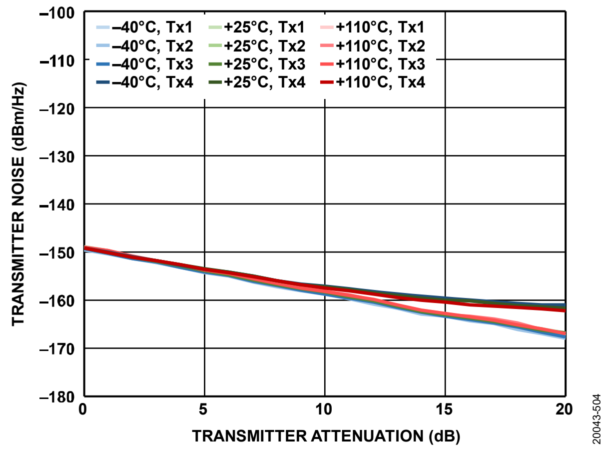


Figure 411. Transmitter Noise vs. Transmitter Attenuation, 50 MHz Offset Frequency

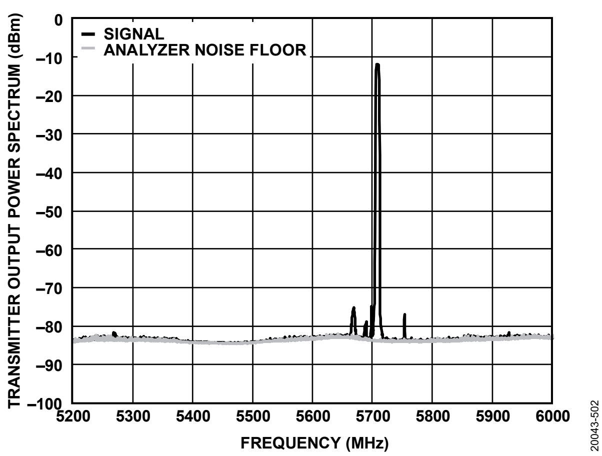


Figure 409. Transmitter Output Power Spectrum, Tx1, 5 MHz LTE, 10 MHz Offset, −10 dBFS RMS, 1 MHz Resolution Bandwidth, T = 25°C

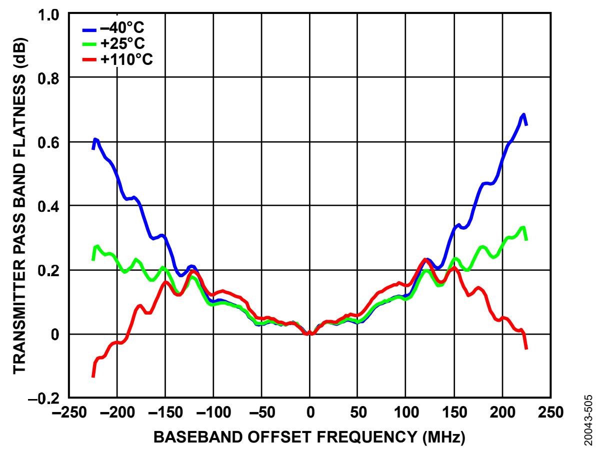


Figure 412. Transmitter Pass Band Flatness vs. Baseband Offset Frequency

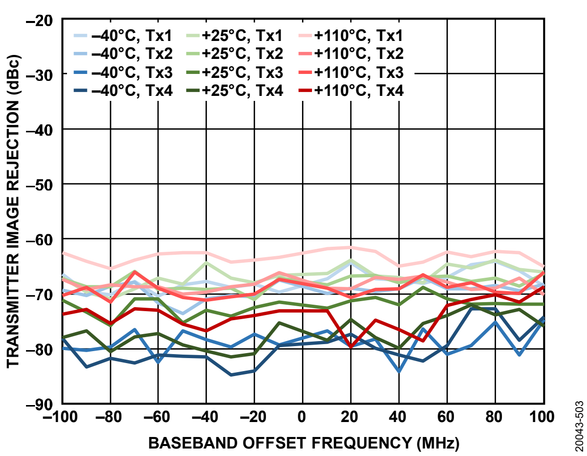


Figure 410. Transmitter Image Rejection vs. Baseband Offset Frequency, 0 dB Attenuation, QEC Tracking Enabled

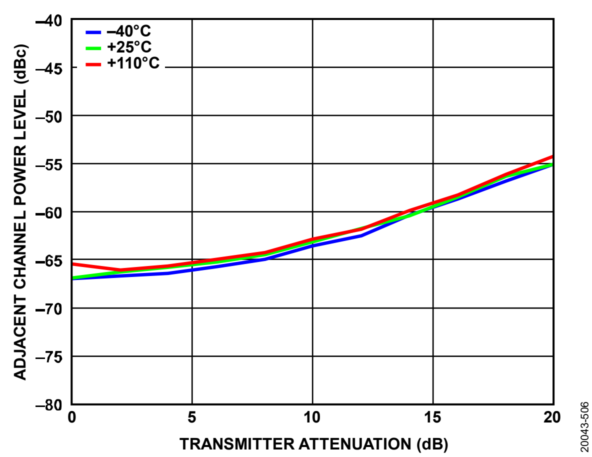


Figure 413. Adjacent Channel Power Level vs. Transmitter Attenuation, −10 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

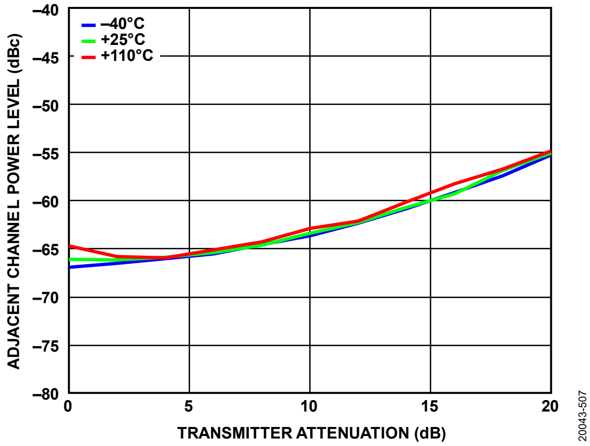


Figure 414. Adjacent Channel Power Level vs. Transmitter Attenuation, 90 MHz Baseband Offset, 20 MHz LTE, PAR = 12 dB, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

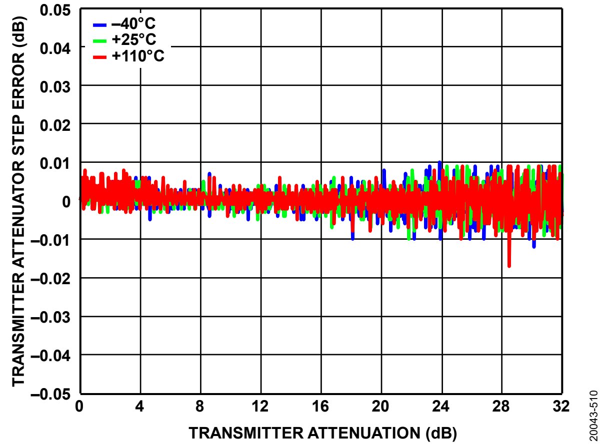


Figure 417. Transmitter Attenuator Step Error vs. Transmitter Attenuation, 10 MHz Offset

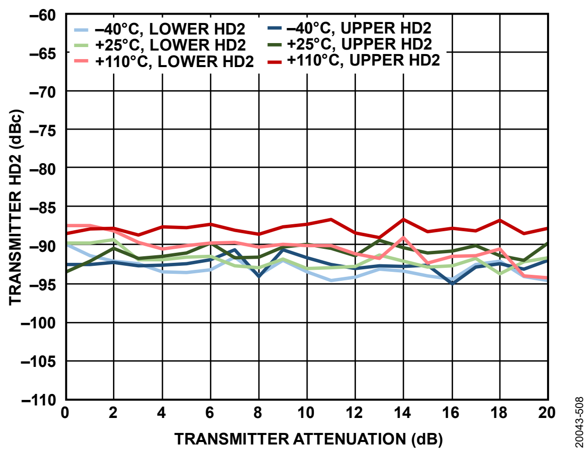


Figure 415. Transmitter HD2 vs. Transmitter Attenuation, 10 MHz Offset

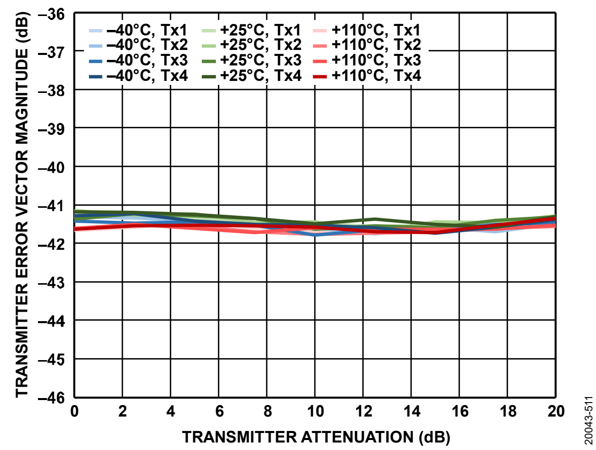


Figure 418. Transmitter Error Vector Magnitude vs. Transmitter Attenuation, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 491.52MSPS, QEC Tracking Enabled, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

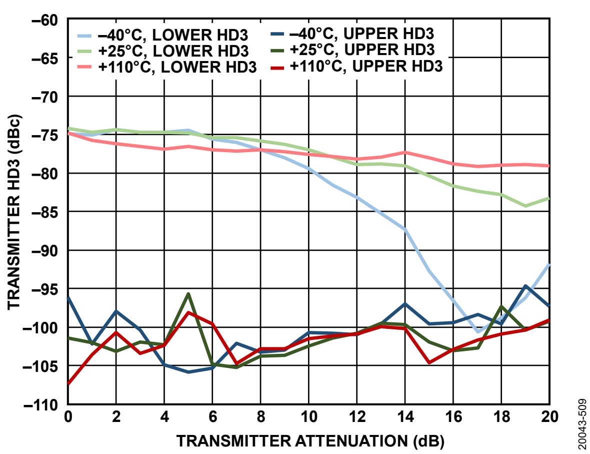


Figure 416. Transmitter HD3 vs. Transmitter Attenuation, 10 MHz Offset

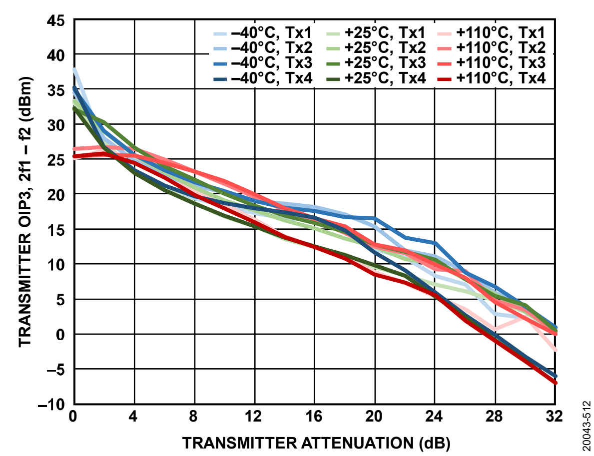


Figure 419. Transmitter OIP3, 2f1 – f2 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

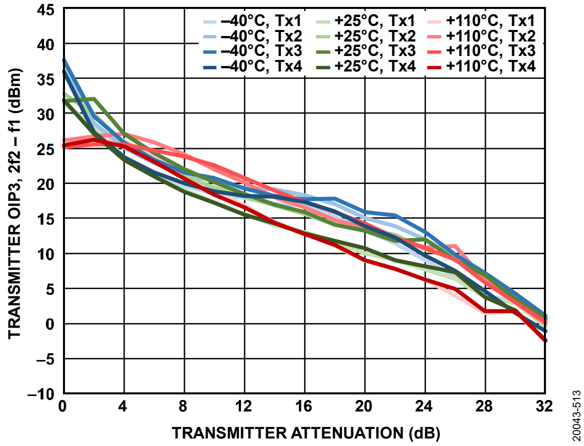


Figure 420. Transmitter OIP3, 2f2 – f1 vs. Transmitter Attenuation, 15 dB Digital Backoff per Tone, f1 = 50.5 MHz, f2 = 55.5 MHz

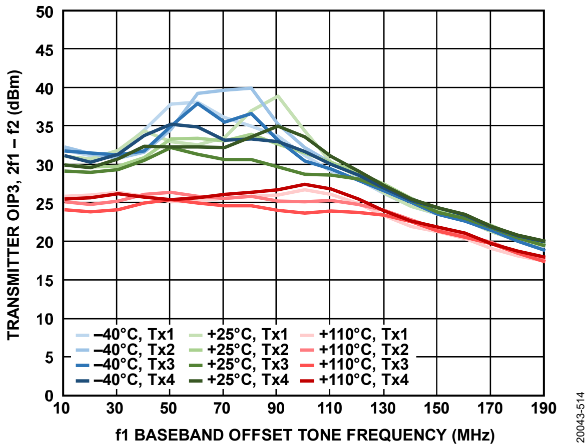


Figure 421. Transmitter OIP3, 2f1 – f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

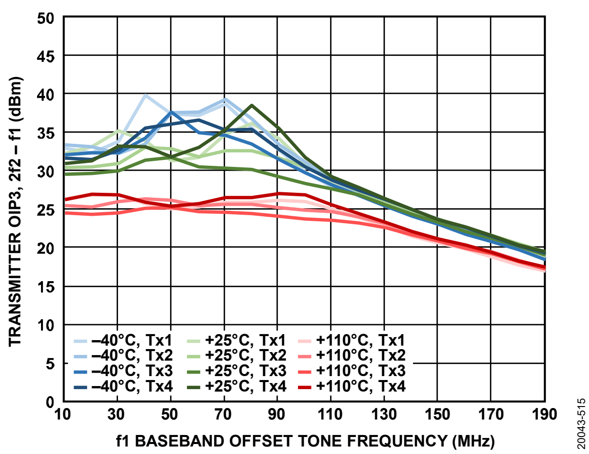


Figure 422. Transmitter OIP3, 2f2 – f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

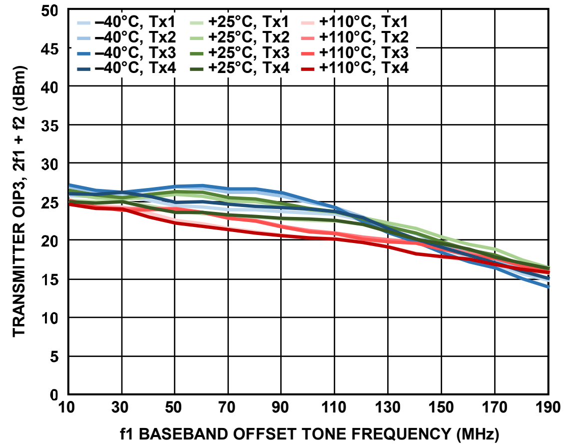


Figure 423. Transmitter OIP3, 2f1 + f2 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

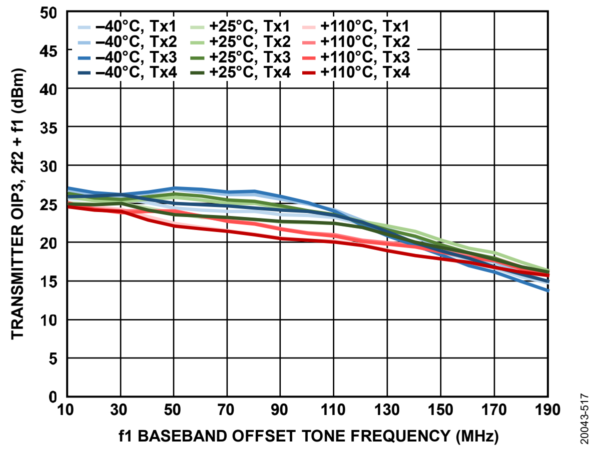


Figure 424. Transmitter OIP3, 2f2 + f1 vs. f1 Baseband Offset Tone Frequency, f2 = f1 + 5 MHz, 15 dB Digital Backoff per Tone

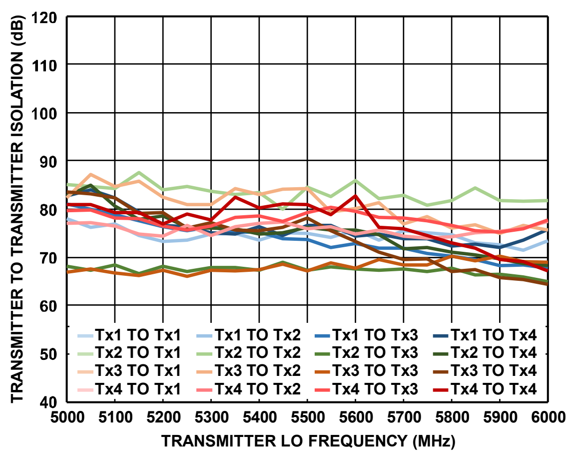


Figure 425. Transmitter to Transmitter Isolation vs. Transmitter LO Frequency

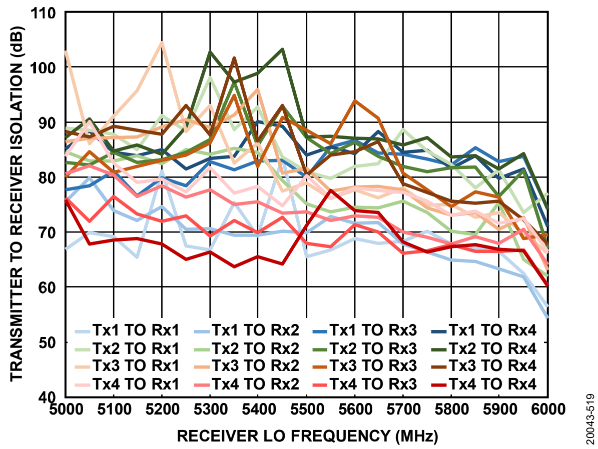


Figure 426. Transmitter to Receiver Isolation vs. Receiver LO Frequency

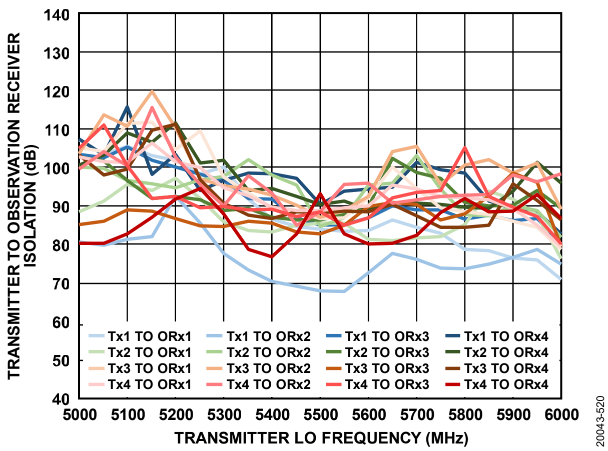


Figure 427. Transmitter to Observation Receiver Isolation vs. Transmitter LO Frequency

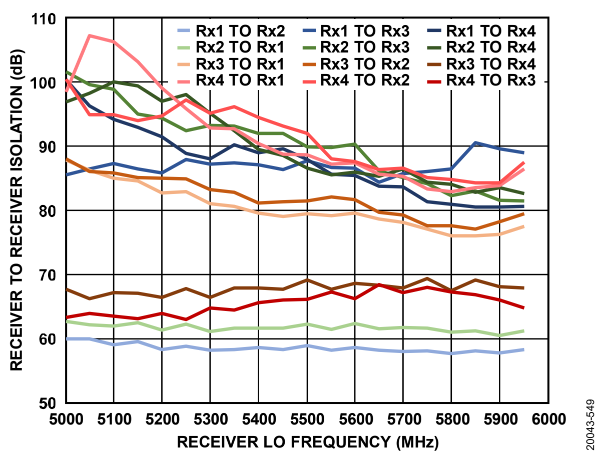


Figure 428. Receiver to Receiver Isolation vs. Receiver LO Frequency

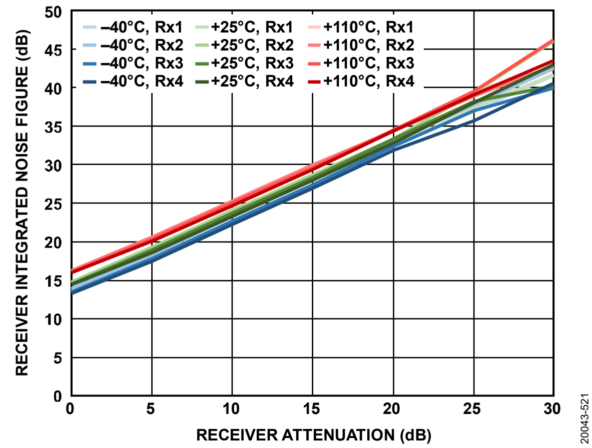


Figure 429. Receiver Integrated Noise Figure vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

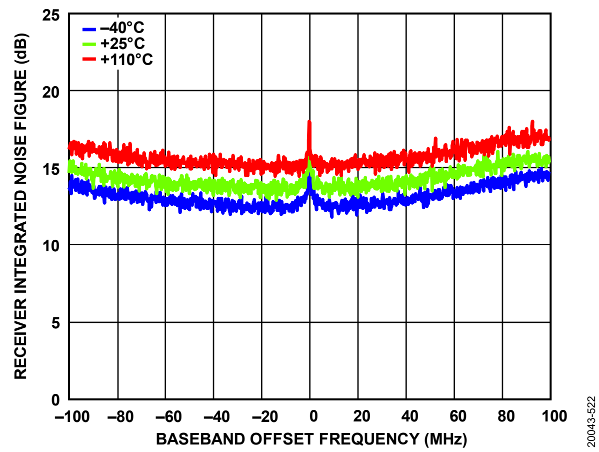


Figure 430. Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS, Integrated in 200 kHz Steps

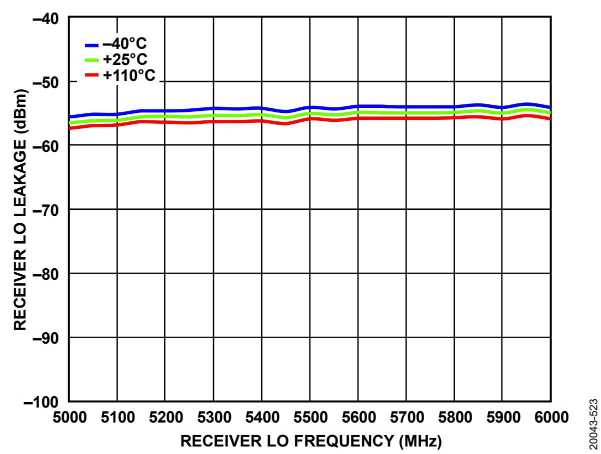


Figure 431. Receiver LO Leakage vs. Receiver LO Frequency, Attenuation = 0 dB, Sample Rate = 245.76 MSPS

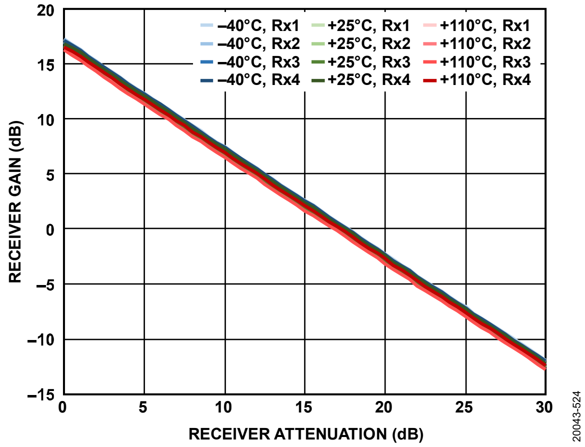


Figure 432. Receiver Gain vs. Receiver Attenuation, 20 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

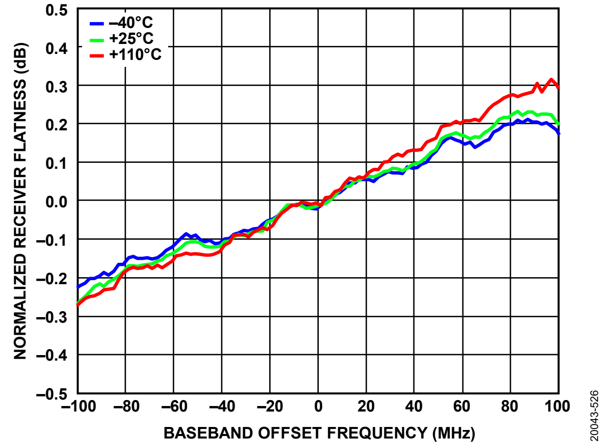


Figure 435. Normalized Receiver Flatness vs. Baseband Offset Frequency, –5 dBFS Input Signal

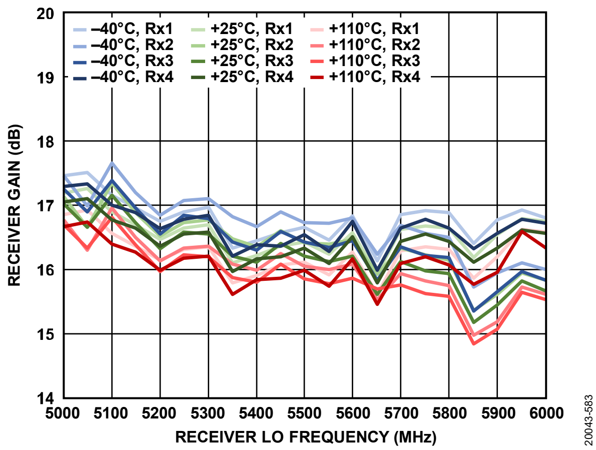


Figure 433. Receiver Gain vs. Receiver LO Frequency, 10 MHz Offset, 200 MHz Bandwidth, Sample Rate = 245.76 MSPS

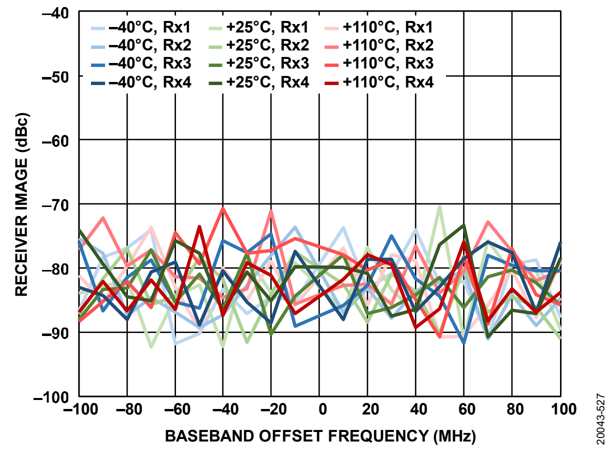


Figure 436. Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

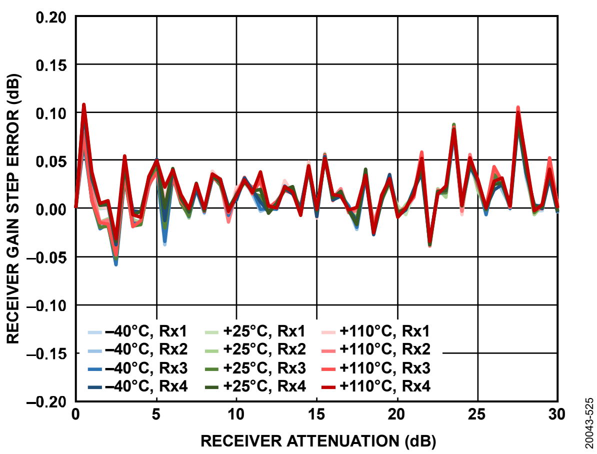


Figure 434. Receiver Gain Step Error vs. Receiver Attenuation, 20 MHz Offset, –5 dBFS Input Signal

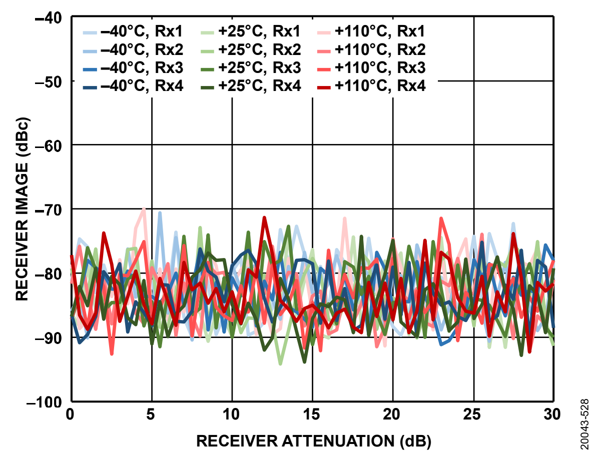


Figure 437. Receiver Image vs. Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 245.76 MSPS, –5 dBFS Input Signal

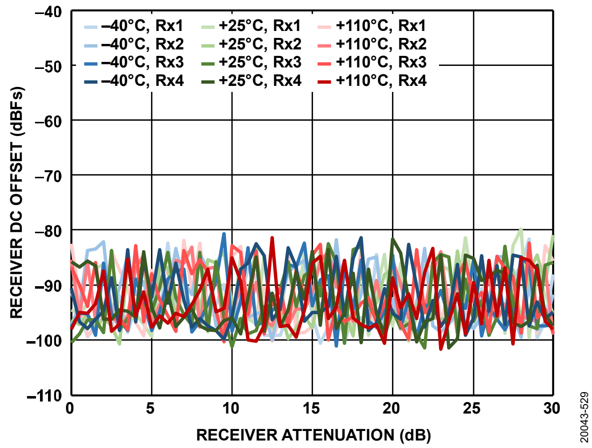


Figure 438. Receiver DC Offset vs. Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

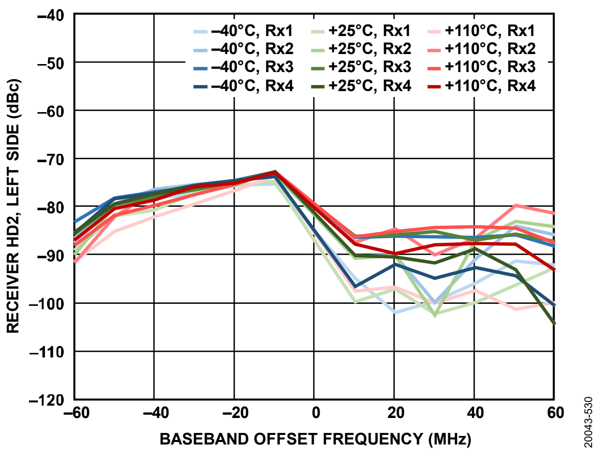


Figure 439. Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz (HD2 Canceller Not Enabled)

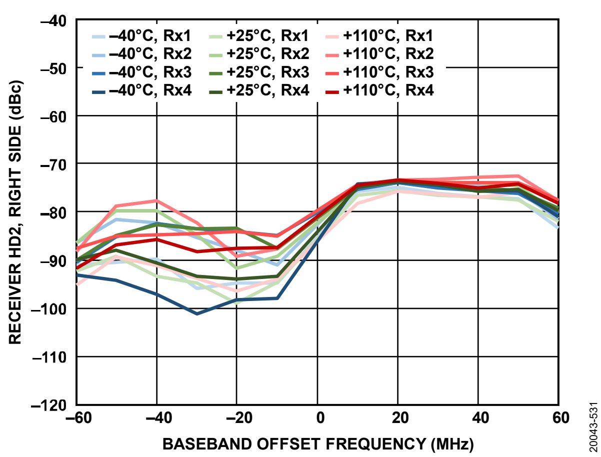


Figure 440. Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz (HD2 Canceller Not Enabled)

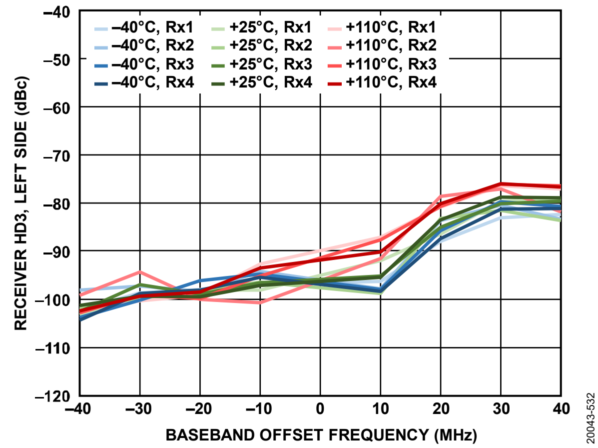


Figure 441. Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

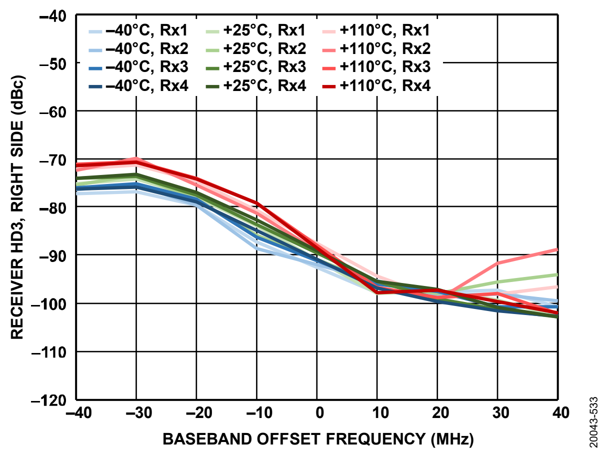


Figure 442. Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

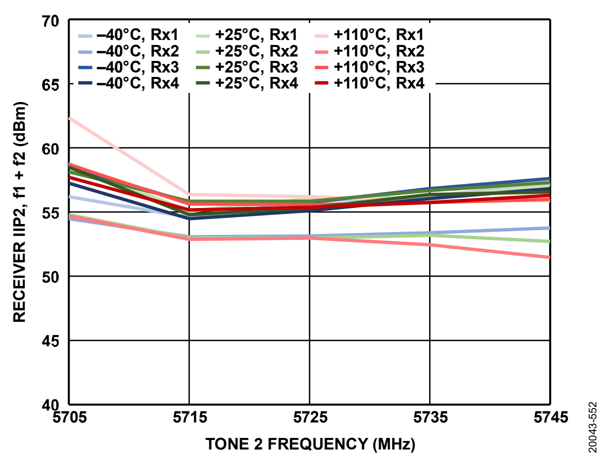


Figure 443. Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

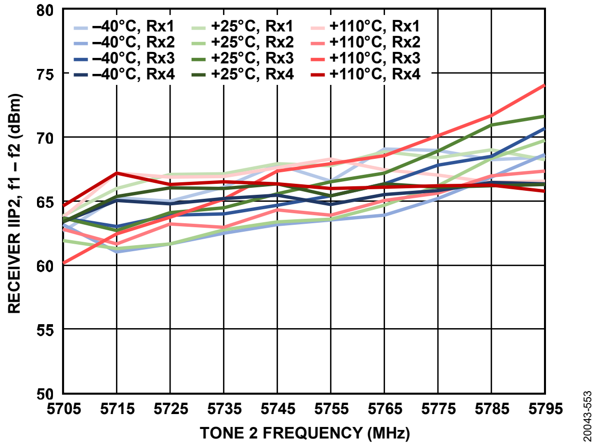


Figure 444. Receiver IIP2, f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

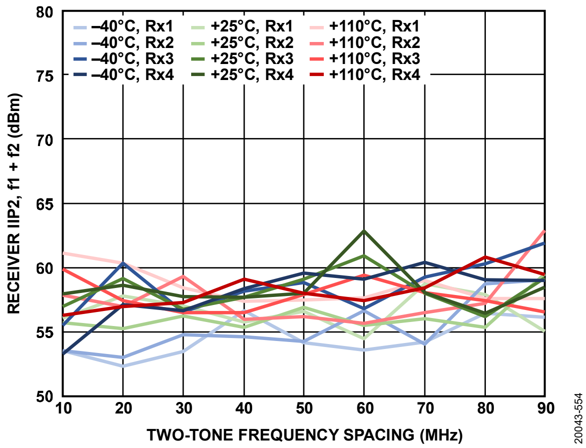


Figure 445. Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

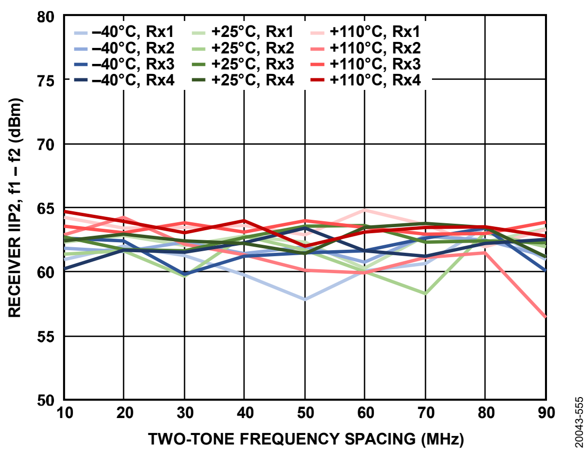


Figure 446. Receiver IIP2, f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

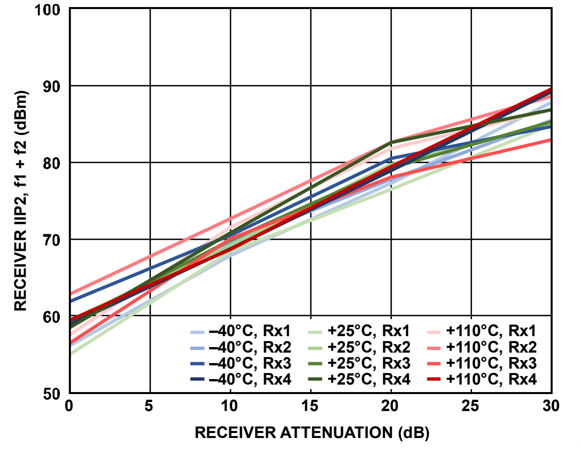


Figure 447. Receiver IIP2, f1 + f2 vs. Receiver Attenuation, Both Tones at −11 dBFS, f1 = 92 MHz, f2 = 2 MHz

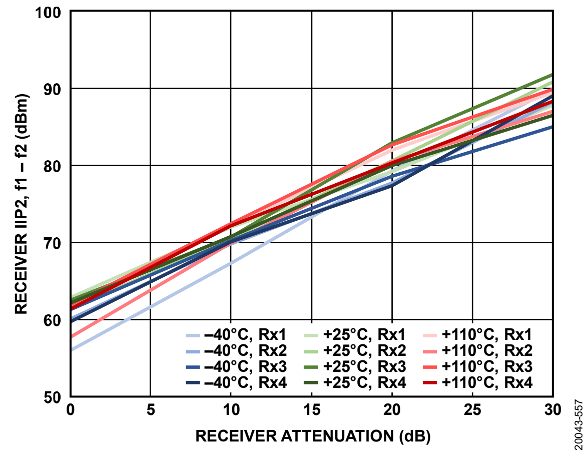


Figure 448. Receiver IIP2, f1 − f2 vs. Receiver Attenuation, Both Tones at −11 dBFS, f1 = 92 MHz, f2 = 2 MHz

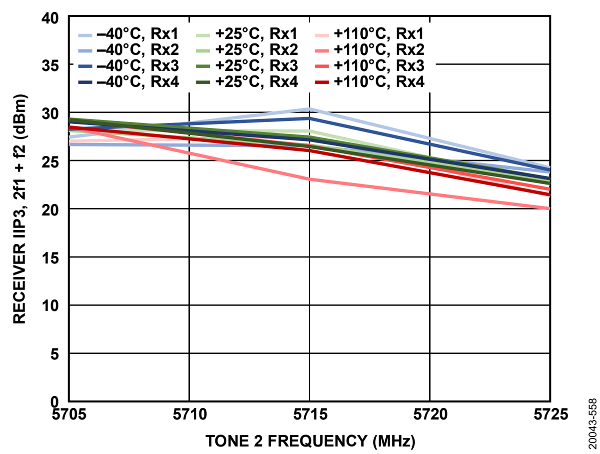


Figure 449. Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

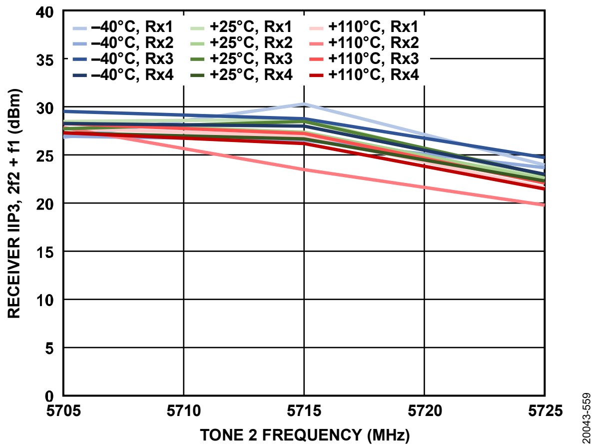


Figure 450. Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

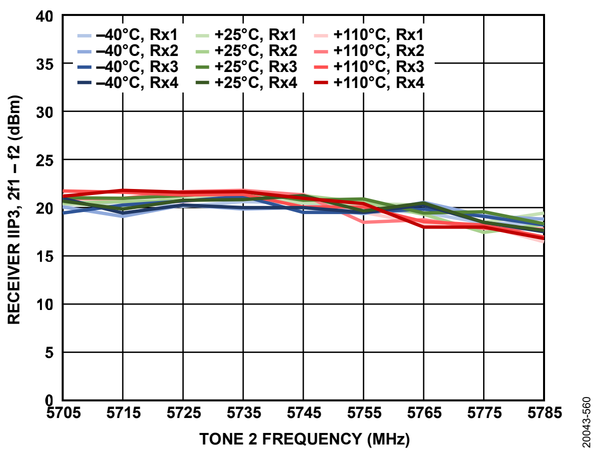


Figure 451. Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

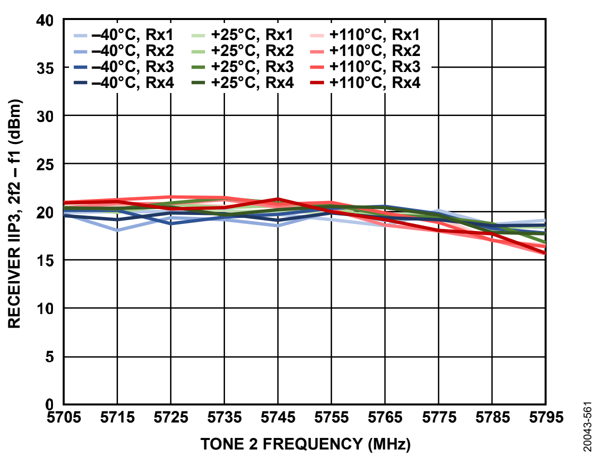


Figure 452. Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

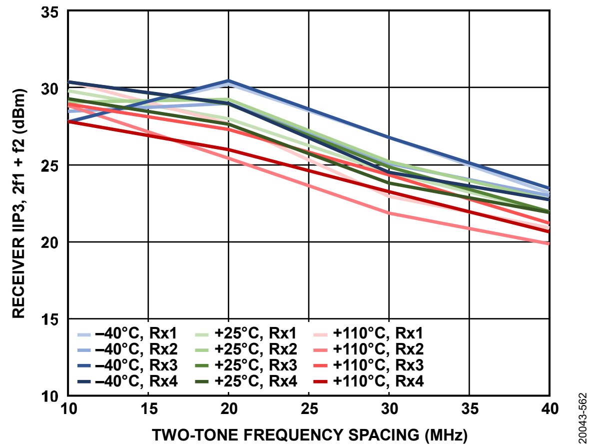


Figure 453. Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

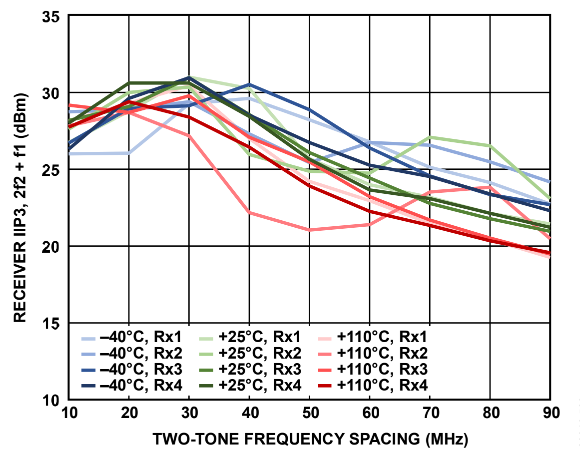


Figure 454. Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

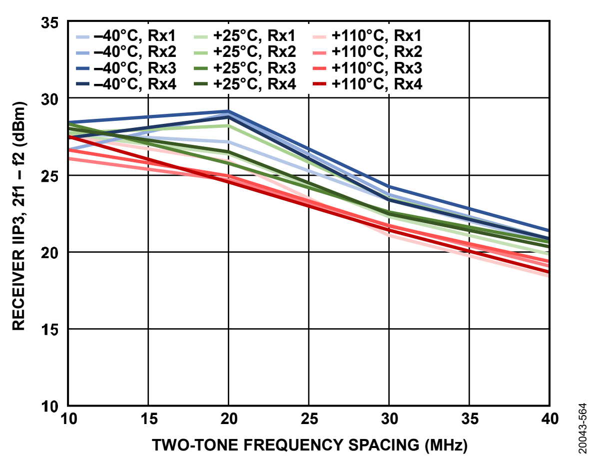


Figure 455. Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

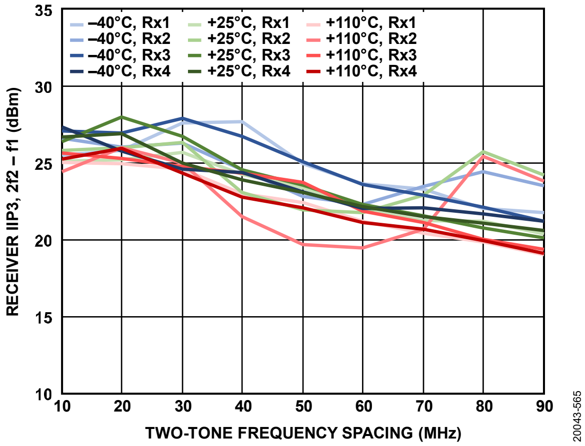


Figure 456. Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

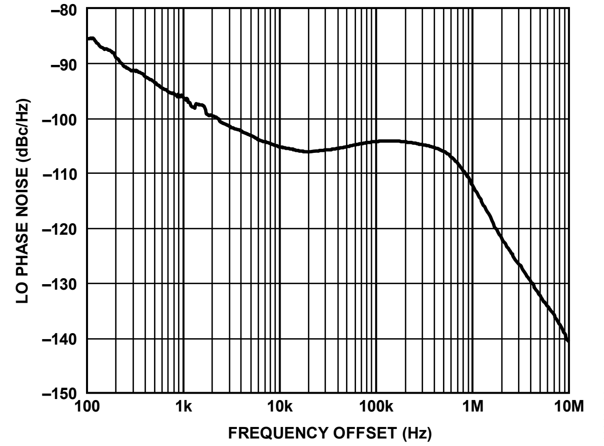


Figure 459. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 500 kHz, Phase Margin = 60°

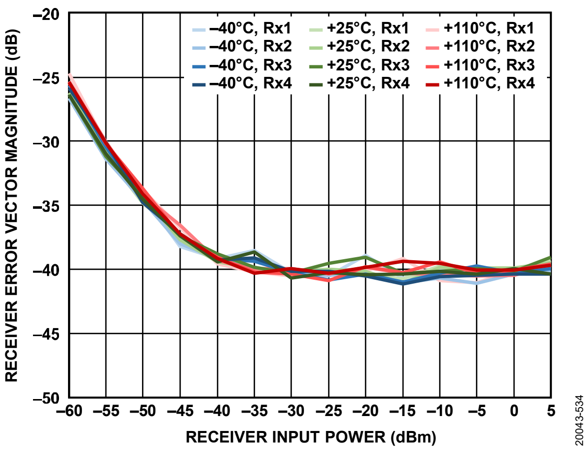


Figure 457. Receiver Error Vector Magnitude vs. Receiver Input Power, 20 MHz LTE Signal Centered at LO Frequency, Sample Rate = 245.76 MSPS, Loop Filter Bandwidth = 500 kHz, Loop Filter Phase Margin = 60°

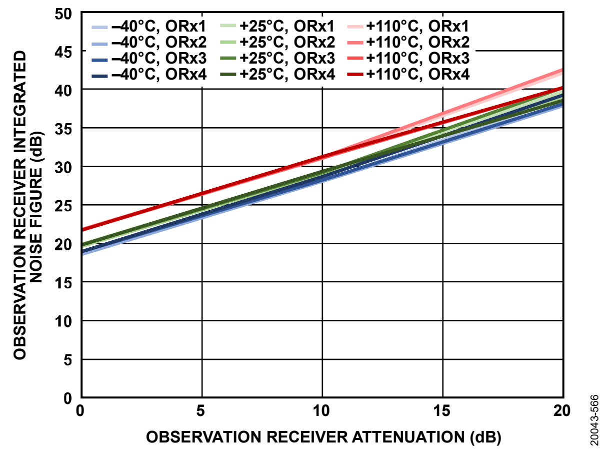


Figure 460. Observation Receiver Integrated Noise Figure vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integration Bandwidth = 500 kHz to 100 MHz

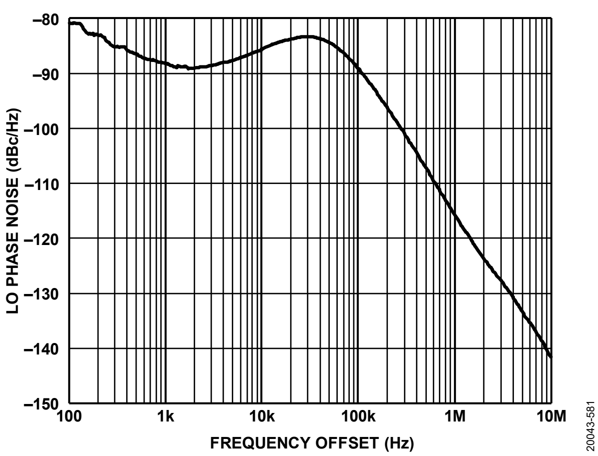


Figure 458. LO Phase Noise vs. Frequency Offset, Loop Bandwidth = 75 kHz, Phase Margin = 85°

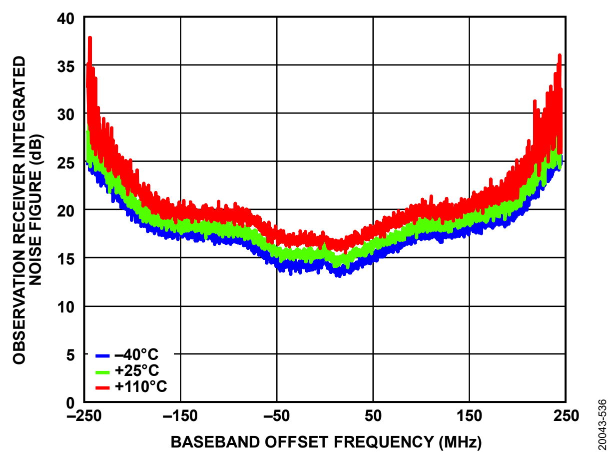


Figure 461. Observation Receiver Integrated Noise Figure vs. Baseband Offset Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS, Integrated in 200 kHz Steps

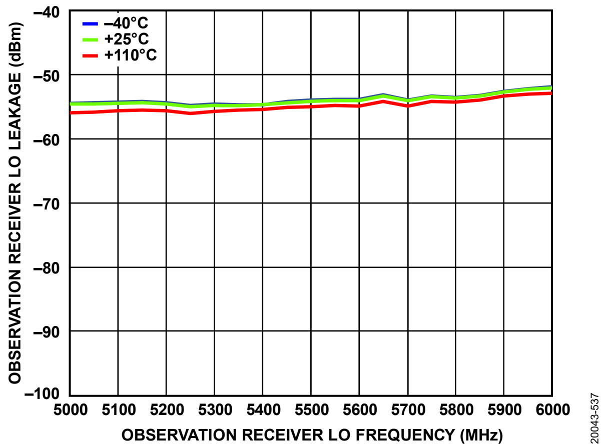


Figure 462. Observation Receiver LO Leakage vs. Observation Receiver LO Frequency, 0 dB Attenuation, Sample Rate = 491.52 MSPS

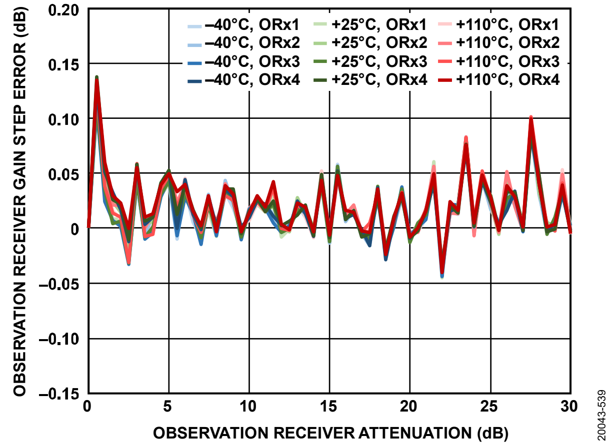


Figure 465. Observation Receiver Gain Step Error vs. Observation Receiver Attenuation, 20 MHz Offset, −5 dBFS Input Signal

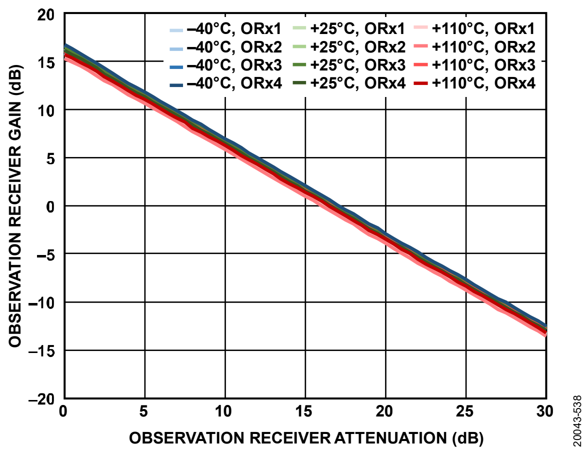


Figure 463. Observation Receiver Gain vs. Observation Receiver Attenuation, 20 MHz Offset, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

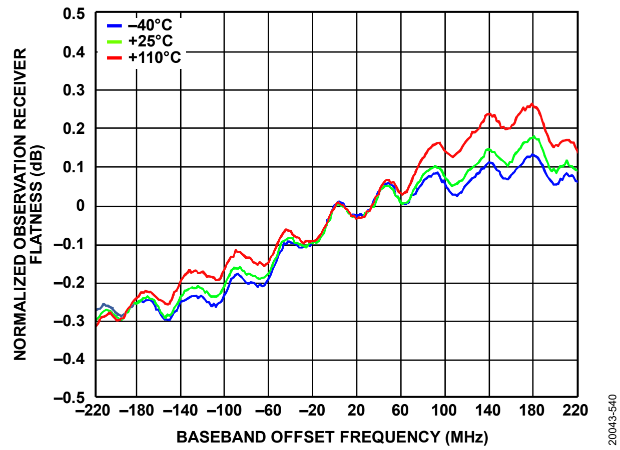


Figure 466. Normalized Observation Receiver Flatness vs. Baseband Offset Frequency, −25 dBm Input Signal, 0 dB Attenuation

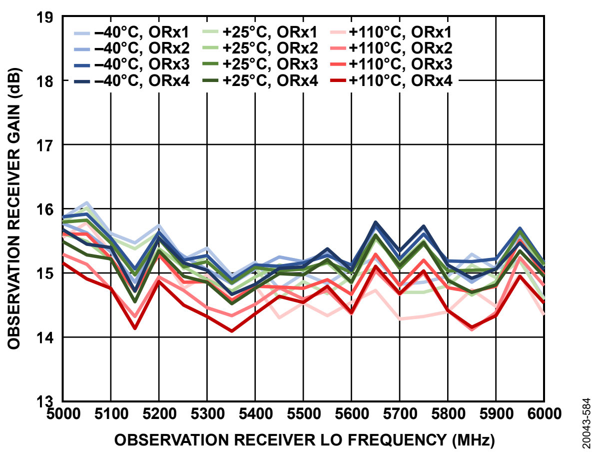


Figure 464. Observation Receiver Gain vs. Observation Receiver LO Frequency, 450 MHz Bandwidth, Sample Rate = 491.52 MSPS

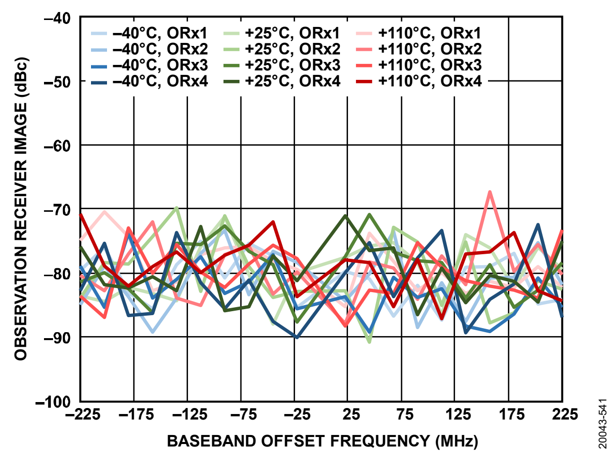


Figure 467. Observation Receiver Image vs. Baseband Offset Frequency, Tracking Calibration Active, Sample Rate = 491.52 MSPS

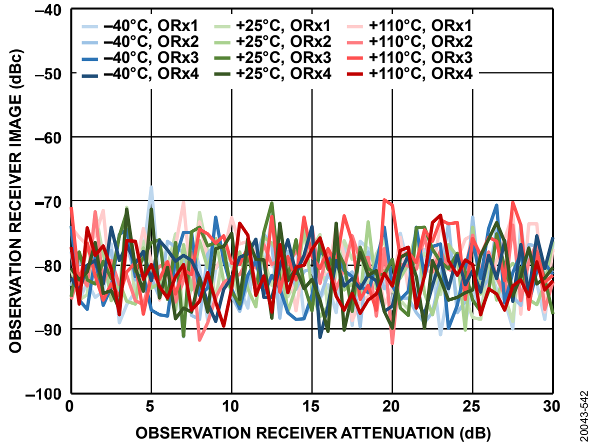


Figure 468. Observation Receiver Image vs. Observation Receiver Attenuation, 20 MHz Offset, Tracking Calibration Active, Sample Rate = 491.52 MSPS

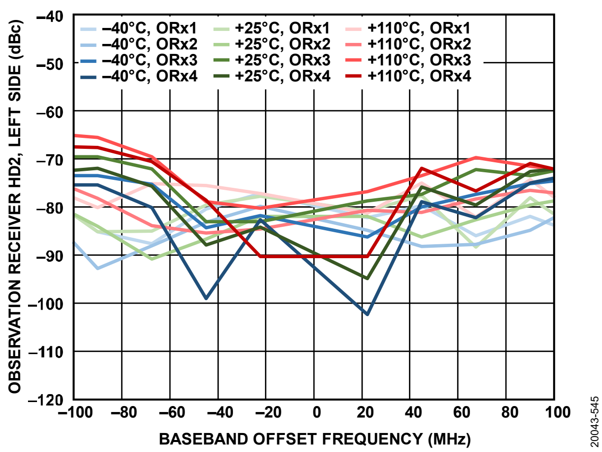


Figure 469. Observation Receiver HD2, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

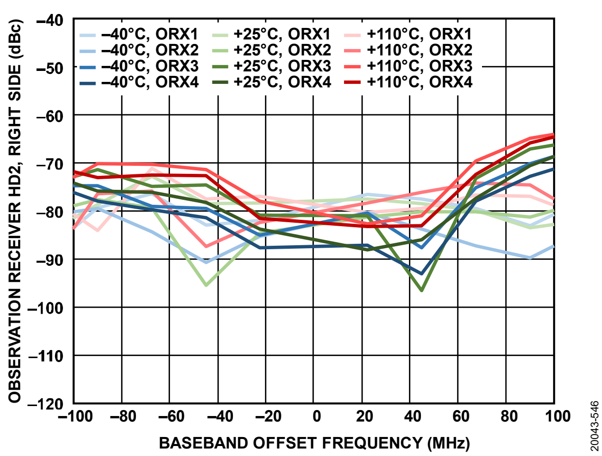


Figure 470. Observation Receiver HD2, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

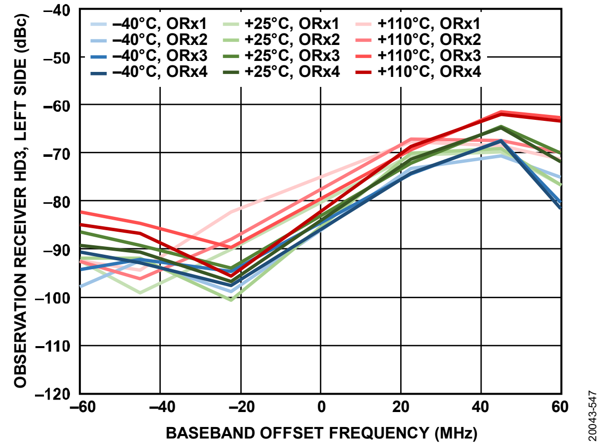


Figure 471. Observation Receiver HD3, Left Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Left of 0 Hz

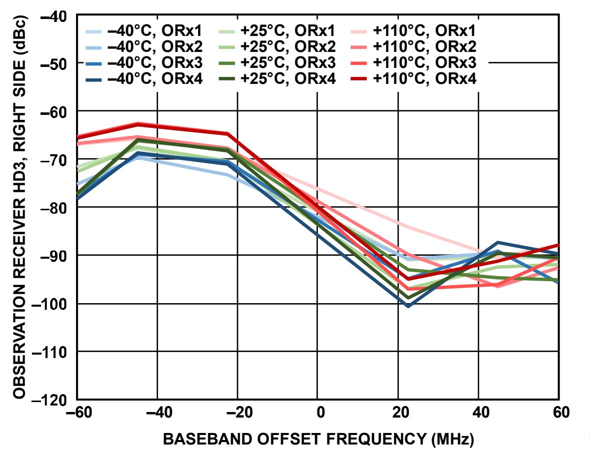


Figure 472. Observation Receiver HD3, Right Side vs. Baseband Offset Frequency, −5 dBFS Input Signal, Distortion Tone Measured Right of 0 Hz

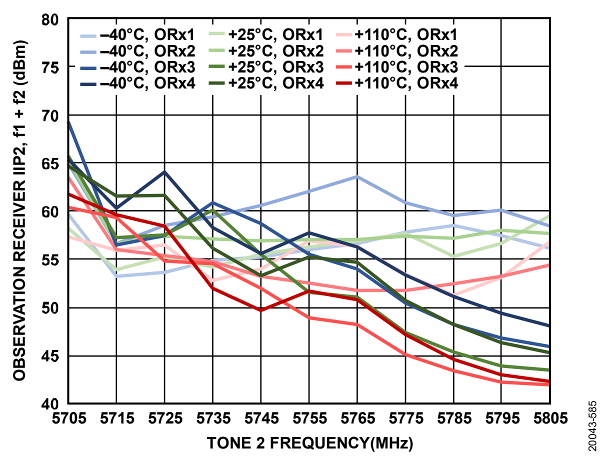


Figure 473. Observation Receiver IIP2, f1 + f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

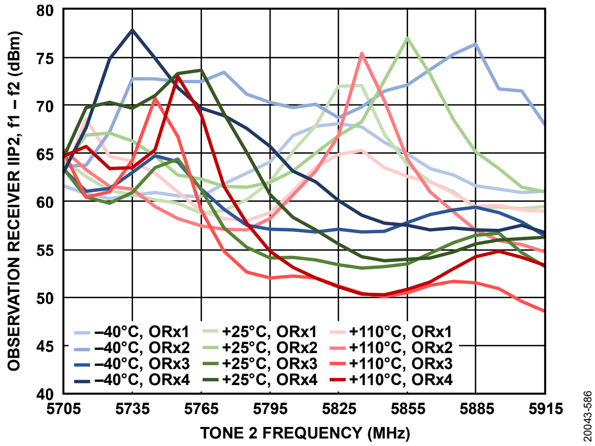


Figure 474. Observation Receiver IIP2, f1 – f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

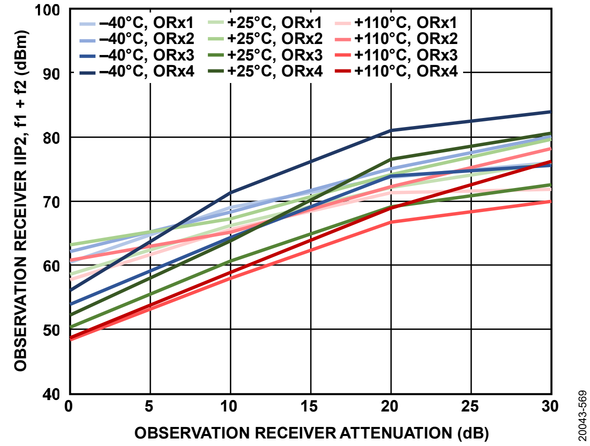


Figure 477. Observation Receiver IIP2, f1 + f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

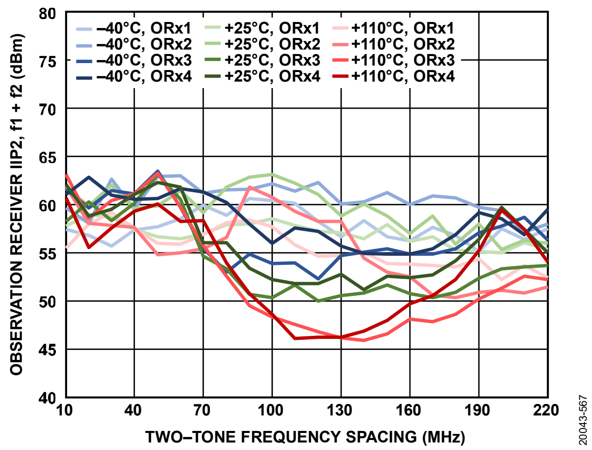


Figure 475. Observation Receiver IIP2, f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, f2 = 2 MHz

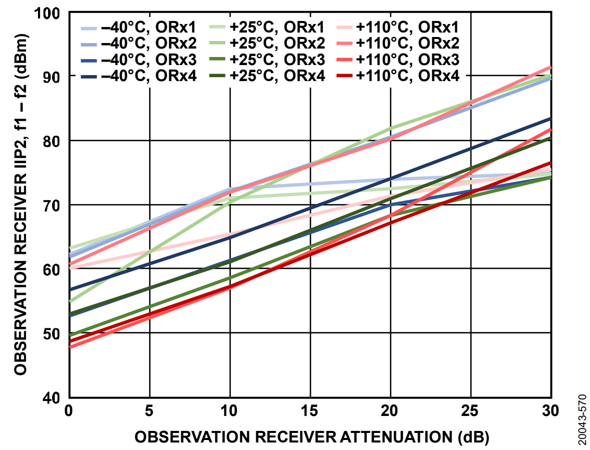


Figure 478. Observation Receiver IIP2, f1 – f2 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 102 MHz, f2 = 2 MHz

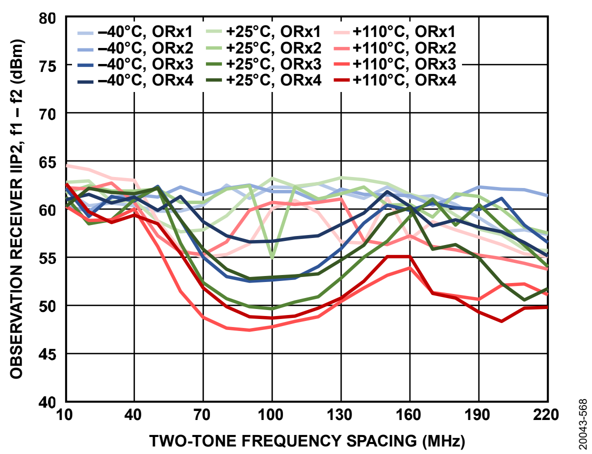


Figure 476. Observation Receiver IIP2, f1 – f2 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

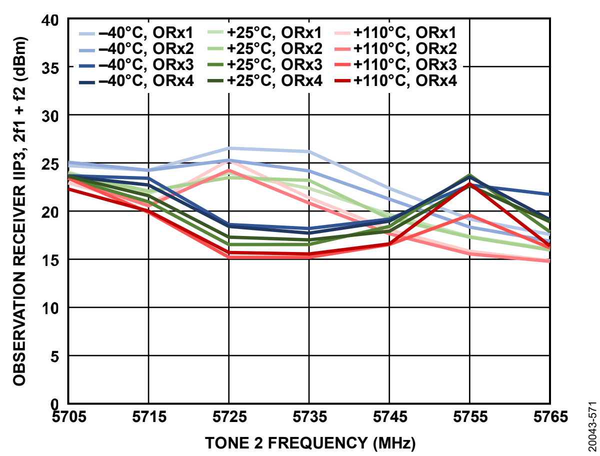


Figure 479. Observation Receiver IIP3, 2f1 + f2 vs. Tone 2 Frequency, Both Tones at –11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

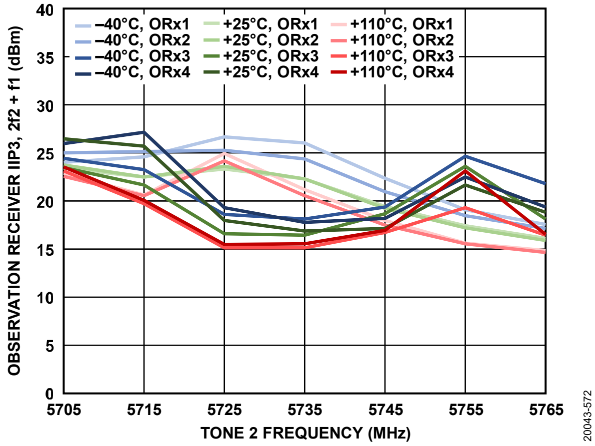


Figure 480. Observation Receiver IIP3, 2f2 + f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

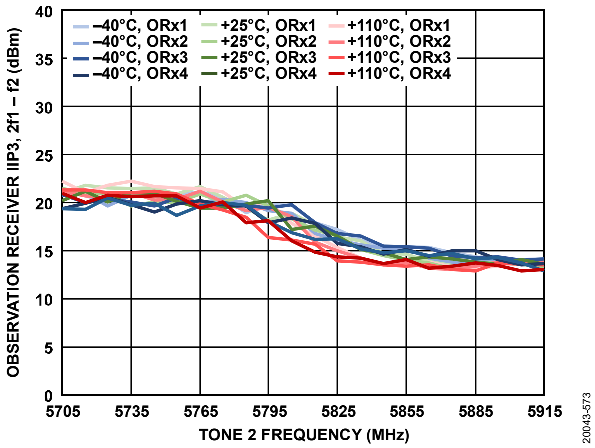


Figure 481. Observation Receiver IIP3, 2f1 − f2 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

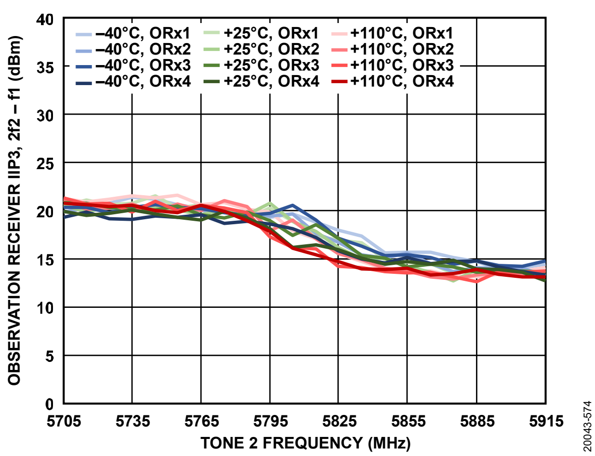


Figure 482. Observation Receiver IIP3, 2f2 − f1 vs. Tone 2 Frequency, Both Tones at −11 dBFS, 0 dB Attenuation, f1 = f2 + 2 MHz

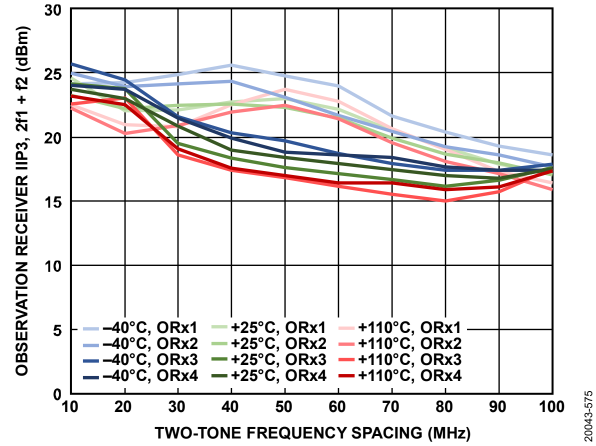


Figure 483. Observation Receiver IIP3, 2f1 + f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

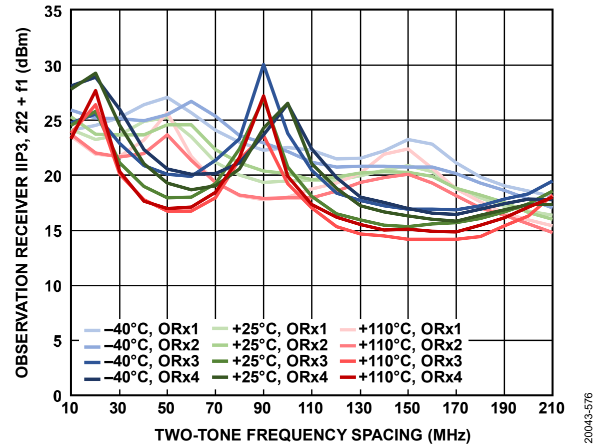


Figure 484. Observation Receiver IIP3, 2f2 + f1 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

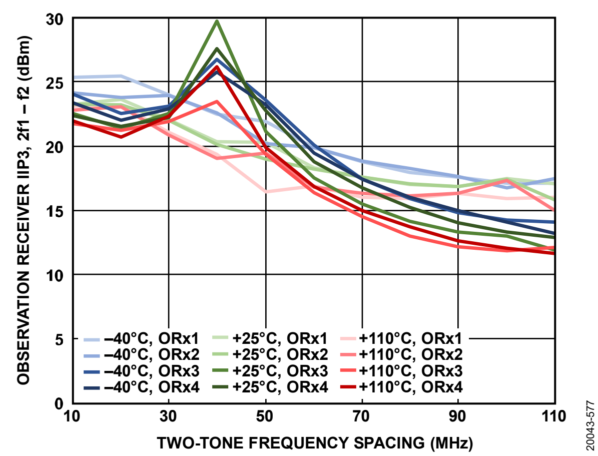


Figure 485. Observation Receiver IIP3, 2f1 − f2 vs. Two-Tone Frequency Spacing, Both Tones at −11 dBFS, 0 dB Attenuation, f2 = 2 MHz

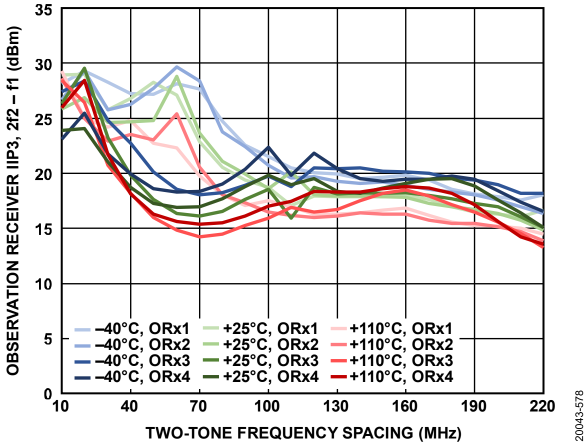


Figure 486. Observation Receiver IIP3, 2f2 – f1 vs. Two-Tone Frequency Spacing, Both Tones at –11 dBFS, 0 dB Attenuation, f2 = 2 MHz

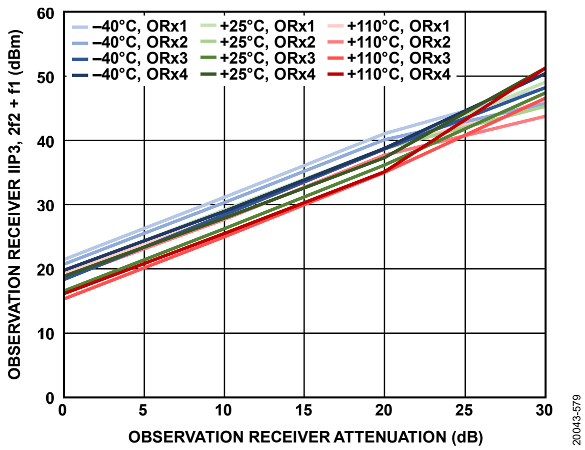


Figure 487. Observation Receiver IIP3, 2f2 + f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

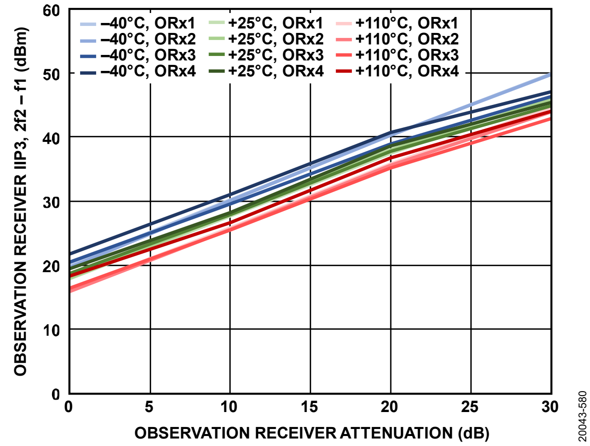


Figure 488. Observation Receiver IIP3, 2f2 – f1 vs. Observation Receiver Attenuation, Both Tones at –11 dBFS, f1 = 122 MHz, f2 = 2 MHz

THEORY OF OPERATION

GENERAL

The ADRV9010 is a highly integrated RF transceiver capable of being configured for a wide range of applications. The device integrates all the RF, mixed-signal, and digital blocks necessary to provide all transmitter, traffic receiver, and observation receiver functions in a single device. Programmability allows the device to be adapted for use in various TDD systems using 3G/4G/5G cellular standards.

Four observation receiver channels are included to monitor the transmitter outputs and to provide tracking correction of dc offset, quadrature error, and transmitter LO leakage to maintain a high performance level under varying temperatures and input signal conditions. Firmware supplied with the device implements all initialization and calibration with no user interaction. Additionally, the device includes test modes allowing system designers to debug designs during prototyping and to optimize radio configurations.

The ADRV9010 contains eight high speed serial interface (SERDES) links for the transmit chain and eight high speed links shared by the receiver and observation receiver chains (JESD204B Subclass 1 compliant and JESD204C supported).

TRANSMITTER

The ADRV9010 transmitter section consists of four identical and independently controlled channels that provide all the digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data from the SERDES lanes pass through a digital processing block that includes a series of programmable half-band filters, interpolation stages, and FIR filters, including a programmable FIR filter with variable interpolation rates and up to 80 taps. The output of this digital chain is connected to the DAC. The DAC sample rate is adjustable up to 2.5 GHz. The in phase (I) and quadrature (Q) channels are identical in each transmitter signal chain.

After conversion to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. Each transmit chain provides a wide attenuation adjustment range with fine granularity to help designers optimize signal-to-noise ratio (SNR).

RECEIVER

The ADRV9010 provides four independent receiver channels. Each channel contains all the blocks necessary to receive RF signals and to convert these signals to digital data usable by a baseband processor. Each receiver can be configured as a direct conversion system that supports up to a 200 MHz bandwidth. Each channel contains a programmable attenuator stage, followed by matched I and Q mixers that downconvert received signals to baseband for digitization.

Two gain control options are available. Users can implement their own gain control algorithms by using their baseband processor to manage manual gain control mode, or users can use the on-chip automatic gain control (AGC) system. Performance is optimized by mapping each gain control setting to specific attenuation levels at each adjustable gain block in the receive signal path. Additionally, each channel contains independent receive signal strength indication (RSSI) measurement capability, dc offset tracking, and all the circuitry necessary for self-calibration.

The receivers include ADCs and adjustable sample rates that produce data streams from the received signals. The signals can be conditioned further by a series of decimation filters and a programmable FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate. The receiver outputs are all connected to the SERDES block, where the data is formatted and serialized for transmission to the baseband processor.

OBSERVATION RECEIVER

The ADRV9010 provides four independent observation receiver inputs. These inputs are similar in implementation to the standard receiver channels in terms of the mixers, ADCs, and filtering blocks. The main difference is that these receivers are designed to operate with an observation bandwidth up to 450 MHz, allowing the receivers to receive all the transmitter channel information needed for implementing digital correction algorithms.

Each input is used as the feedback monitor channel for a corresponding transmitter channel. Table 11 shows the possible combinations of transmitter and observation channels.

Table 11. Possible Transmitter/Observation Channel Combinations

Transmitter Channel	Observation Channel
TX1±	ORX1± or ORX2±
TX2±	ORX1± or ORX2±
TX3±	ORX3± or ORX4±
TX4±	ORX3± or ORX4±

The observation receiver channels can either share a common frequency synthesizer with the transmitters or use the auxiliary synthesizer to offset the LO frequency from the transmitter channel being monitored.

CLOCK INPUT

The ADRV9010 requires a differential clock connected to the DEVCLK± pins. The frequency of the clock input signal must be between 15 MHz and 1000 MHz and must have low phase noise because this signal generates the RF LO and internal sampling clocks.

SYNTHESIZERS

The ADRV9010 contains four fractional-N PLLs to generate the RF LO for the signal paths and all internal clock sources. This group of PLLs includes two RF PLLs for the transmit and receive LO generation, an auxiliary PLL that can be used by the observation receivers, and a clock PLL. Each PLL is independently controlled with no need for external components to set frequencies.

RF Synthesizers

The two RF synthesizers use fractional-N PLLs to generate RF LOs for the multiple receiver and transmitter channels. This PLL incorporates a four-core internal VCO and loop filter, capable of generating low phase noise signals with no external components required. An internal LO multiplexer (mux) enables each PLL to supply LOs to any or all receivers and transmitters (for example, LO1 to all transmitters and LO2 to all receivers), resulting in maximum flexibility when configuring the device for TDD operation. The LOs on multiple devices can be phase synchronized to support active antenna systems and beam forming applications.

Auxiliary Synthesizer

The auxiliary synthesizer uses a single core VCO fractional-N PLL to generate the signals necessary to calibrate the device. The output of this block uses a separate mux system to route LOs for calibrating different functions during initialization. The auxiliary synthesizer can also be used to generate LO signals for the observation receivers or as an offset LO used in the receiver signal chains.

Clock Synthesizer

The ADRV9010 contains a single core VCO fractional-N PLL synthesizer that generates all baseband related clock signals and SERDES clocks. This PLL is programmed based on the data rate and sample rate requirements of the system, which typically require the synthesizer to operate in integer mode.

For JESD204B configurations with Np = 12 and JESD204C configurations, a dedicated PLL included in the SERDES block generates the SERDES clocks.

External LO Inputs

The ADRV9010 provides two external LO inputs to allow an external synthesizer to be used with the device. These inputs must be 2× the desired LO frequency. One input is multiplexed with the RF1 PLL, and the other input is multiplexed with the RF2 PLL. Each observation receiver can obtain the LO from either the same input as the associated transmitter channel or the corresponding, dedicated PLL.

SPI INTERFACE

The ADRV9010 uses a SPI to communicate with the baseband processor. This interface can either be configured as a 4-wire interface with dedicated receive and transmit ports, or as a 3-wire interface with a bidirectional data communications port. This SPI allows the baseband processor to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first bit sets the bus direction of the bus transfer. The next 15 bits set the address where data is written. The final eight bits are the data being transferred to the specific register address.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DIO pin, and the final eight bits are read from the ADRV9010, either on the SPI_DO pin in 4-wire mode or on the SPI_DIO pin in 3-wire mode.

POWER SUPPLY SEQUENCE

The ADRV9010 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDIG_1P0 supply is activated first. If the same supply is used to power the VDDA_1P0 supply, then all 1.0 V supplies can be powered on at the same time.

If the VDIG_1P0 supply is isolated, all VDDA_1P8, VDDA_1P3, and VDDA_1P0 supplies must be powered up after the VDIG_1P0 supply is activated. The VIF supply can be powered up at any time.

It is also recommended to toggle the $\overline{\text{RESET}}$ signal after power has stabilized prior to configuration.

If a power-down sequence is followed, avoid any back biasing of the digital control lines by removing the VDIG_1P0 supply last. If no sequencing is used, it is recommended to power down all supplies simultaneously.

GPIO_x PINS

The ADRV9010 provides 19 GPIOs referenced to VIF that can be configured for numerous functions. When configured as outputs, certain pins can provide real-time signal information to the baseband processor, allowing the baseband processor to determine receiver performance. A pointer register selects what information is output to these pins.

Signals used for manual gain mode, calibration flags, state machine status, and various receiver parameters are among the outputs that can be monitored on these pins. Additionally, certain pins can be configured as inputs and used for various functions such as setting the receiver gain in real time.

AUXILIARY CONVERTERS

GPIO_ANA_x/AUXDAC_x

The ADRV9010 contains eight analog GPIOs (the GPIO_ANA_x pins) that are multiplexed with eight identical auxiliary DACs (AUXDAC_x). The analog GPIO ports can be used to control other analog devices or receive control inputs referenced to the VDDA_1P8 supply. The auxiliary DACs are 12-bit converters capable of supplying up to 10 mA. These outputs are typically used to supply bias current or variable control voltages for other related components with analog control inputs.

AUXADC_x

The ADRV9010 contains two auxiliary ADCs with four total input pins (AUXADC_x). These auxiliary ADCs provide 10-bit monotonic outputs with an input voltage range of 0.05 V to 0.95 V. When enabled, each auxiliary ADC is free running. An application programing interface (API) command latches the ADC output value to a register. The ADRV9010 also contains an ADC that supports a built-in diode-based temperature sensor.

JTAG BOUNDARY SCAN

The ADRV9010 provides support for a JTAG boundary scan. There are five dual-function pins associated with the JTAG interface. These pins, listed in Table 12, are used to access the on-chip test access port. To enable the JTAG functionality, set the GPIO_0 through GPIO_2 pins according to Table 13 depending on how the desired JESD204B sync signals are configured in the software (differential or single-ended mode). Pull the TEST_EN pin high to the VIF supply to enable the JTAG mode.

Table 12. Dual-Function Boundary Scan Test Pins

Mnemonic	JTAG Mnemonic	Description
GPIO_14	$\overline{\text{TRST}}$	Test access port reset
GPIO_15	TDO	Test data output
GPIO_16	TDI	Test data input
GPIO_17	TMS	Test access port mode select
GPIO_18	TCK	Test clock

Table 13. JTAG Modes

Test Pin Level	GPIO_2 to GPIO_0	Description
0	xxx[1]	Normal operation
1	000	JTAG mode with differential JESD204B sync signals
1	011	JTAG mode with single-ended JESD204B sync signals

[1] x means any combination.

APPLICATIONS INFORMATION

POWER SUPPLY SEQUENCE

The ADRV9010 requires a specific power-up sequence to avoid undesired power-up currents. In the optimal power-up sequence, the VDIG_1P0 supply is activated first. When VDIG_1P0 powers VDDA_1P0, all 1.0 V supplies can be powered on at the same time.

When VDIG_1P0 is isolated, all VDDA_1P8, VDDA_1P3, and VDDA_1P0 supplies must be powered up after VDIG_1P0 is activated. The VIF supply can be powered up at any time.

It is also recommended prior to configuration to toggle the $\overline{\text{RESET}}$ signal after power has stabilized.

If a power-down sequence is followed, to avoid any back biasing of the digital control lines, remove the VDIG_1P0 supply last. If no sequencing is used, it is recommended to power down all supplies simultaneously.

DATA INTERFACE

The digital data interface for the ADRV9010 implements the JEDEC Standard JESD204B Subclass 1 and JESD204C. The serial interface operates at speeds of up to 14.7456 Gbps in JESD204B mode and 16.22016 Gbps in JESD204C mode.

Table 14, Table 15, and Table 16 list example parameters for various JESD204x interface settings.

Table 14. Example Receiver Interface Rates with Four Channels Active (M = 8)[1]

Bandwidth (MHz)	Output Rate (MSPS)	JESD204x Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
40	61.44	16	16	9830.4	1	16	8110.08	1
60	76.8	16	16	12288	1	16	10137.6	1
100	122.88	16	8	9830.4	2	16	16220.16	1
150	184.32	16	8	14745.6	2	8	12165.12	2
200	245.76	16	4	9830.4	4	8	16220.16	2
200	245.76	12	6	14745.6	2	6	12165.12	2

[1] Other output rates, bandwidth, and number of lanes also supported.

Table 15. Transmitter Interface Rates with Four Channels Active (M = 8)[1]

Primary Signal Bandwidth (MHz)	Total Bandwidth (MHz)	Input Rate (MSPS)	JESD204x Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
50	113	122.88	16	8	9830.4	2	16	16220.16	1
75	150	184.32	16	8	14745.6	2	8	12165.12	2
100	225	245.76	16	4	9830.4	4	4	16220.16	2
150	300	368.64	16	4	14745.6	4	4	12165.12	4
200	450	491.52	16	2	9830.4	8	4	16220.16	4

[1] Other output rates, bandwidth, and number of lanes also supported.

Table 16. Observation Path Interface Rates with 1 Channel Active (M = 2)[1]

Total Bandwidth (MHz)	Output Rate (MSPS)	JESD204x Np Parameter	JESD204B F Parameter	JESD204B Lane Rate (Mbps)	JESD204B Number of Lanes	JESD204C F Parameter	JESD204C Lane Rate (Mbps)	JESD204C Number of Lanes
150	184.32	16	4	7372.8	1	4	6082.56	1
220	245.76	16	4	9830.4	1	4	8110.08	1
250	307.2	16	4	12288	1	4	10137.6	1
300	368.64	16	4	14745.6	1	2	6082.56	2
450	491.52	16	2	9830.4	2	2	8110.08	2
450	491.52	12	3	14745.6	1	3	12165.12	1

[1] Other output rates, bandwidth, and number of lanes also supported.

OUTLINE DIMENSIONS

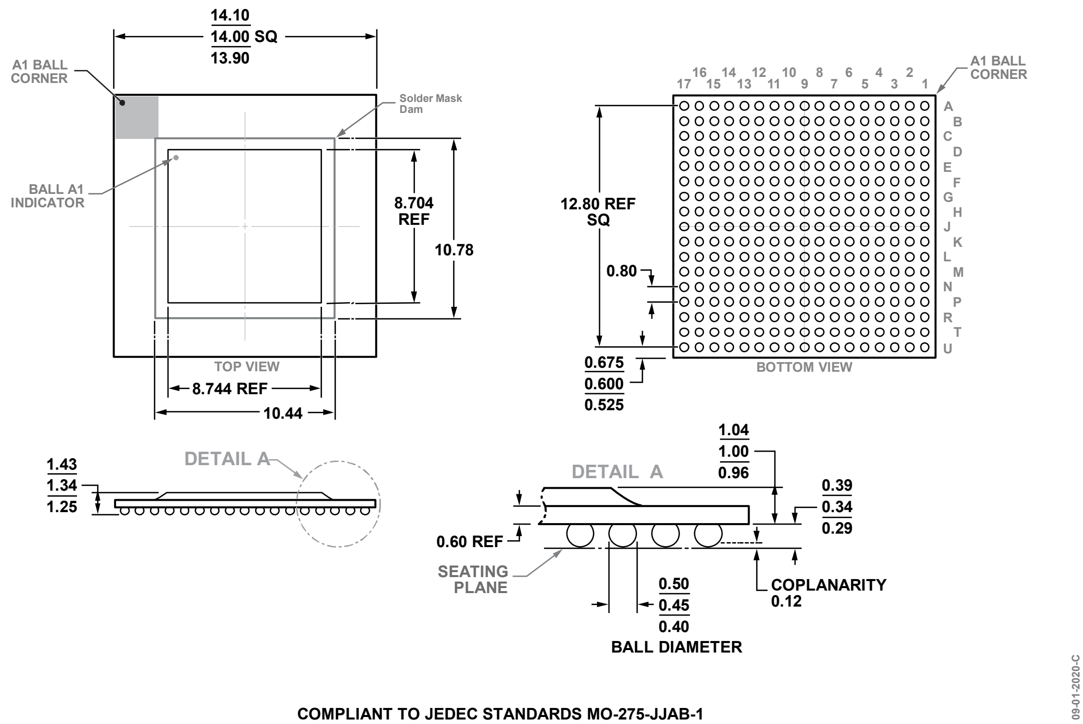


Figure 489. 289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-289-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRV9010BBCZ	−40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-3
ADRV9010BBCZ-REEL	−40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-3
ADRV9010BBCZ-A	−40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-3
ADRV9010BBCZ-A-RL	−40°C to +110°C	289-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-289-3
ADRV9026-HB/PCBZ		High Band Evaluation Board for 2.8 GHz to 6 GHz	
ADRV9026-MB/PCBZ		Mid Band Evaluation Board for 650 MHz to 2.8 GHz	

[1] Z = RoHS Compliant Part.