



**ANALOG  
DEVICES**

# 2 pF Off Capacitance, 1 pC Charge Injection, $\pm 15$ V/12 V *i*CMOS™ Dual SPDT Switch

Preliminary Technical Data

**ADG1236**

## FEATURES

- 2 pF off capacitance
- 1 pC charge injection
- 33 V supply range
- 120  $\Omega$  on resistance
- Fully specified at +12 V,  $\pm 15$  V
- No  $V_L$  supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 16-lead TSSOP and 12-lead LFCSP packages
- Typical power consumption:  $<0.03 \mu\text{W}$

## APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Communication systems

## GENERAL DESCRIPTION

The ADG1236 is a monolithic CMOS device containing two independently selectable SPDT switches. It is designed on an *i*CMOS process. *i*CMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 30 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages, while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of the part make it an ideal solution for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the part suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

### Rev. PrD

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## FUNCTIONAL BLOCK DIAGRAM

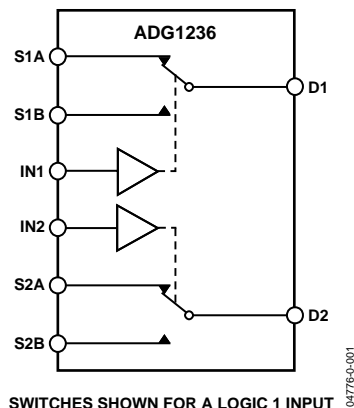


Figure 1.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

## PRODUCT HIGHLIGHTS

- 2 pF off capacitance ( $\pm 15$  V supply).
- 1 pC charge injection.
- 3 V logic-compatible digital inputs:  $V_{IH} = 2.0$  V,  $V_{IL} = 0.8$  V.
- No  $V_L$  logic power supply required.
- Ultralow power dissipation:  $<0.03 \mu\text{W}$ .
- 16-lead TSSOP and 12-lead 3 mm  $\times$  3 mm LFCSP packages.

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**REVISION HISTORY**

11/04—Revision PrD: Preliminary Version

## SPECIFICATIONS

### DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameters	25°C	85°C	Y Version <sup>1</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance ( $R_{ON}$ )	120	220	260	$\Omega$ typ $\Omega$ max	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ ; Figure 21
On Resistance Match between Channels ( $\Delta R_{ON}$ )	5			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )	25		50	$\Omega$ max $\Omega$ typ $\Omega$ max	$V_S = -5\text{ V}/0\text{ V}/+5\text{ V}$ ; $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$			nA typ	$V_{DD} = +10\text{ V}$ , $V_{SS} = -10\text{ V}$ $V_S = 0\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/0\text{ V}$ ; Figure 22
Drain Off Leakage, $I_D$ (Off)	$\pm 0.01$	$\pm 1$	$\pm 5$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.04$	$\pm 1$	$\pm 5$	nA typ	$V_S = 0\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/0\text{ V}$ ; Figure 22
	$\pm 1$	$\pm 2$	$\pm 5$	nA max	$V_S = V_D = 0\text{ V}$ or $10\text{ V}$ ; Figure 23
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
Digital Input Capacitance, $C_{IN}$	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	50			ns typ ns max	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ ; Figure 24
$t_{OFF}$	20		100	ns typ ns max	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$ ; Figure 24
Break-before-Make Time Delay, $t_D$	15		40 1	ns typ ns min	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$ ; Figure 25
Charge Injection	1			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Figure 26
Off Isolation	75			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 27
Channel-to-Channel Crosstalk	85			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Figure 28
Total Harmonic Distortion + Noise	0.002			% typ	$R_L = 600\ \Omega$ , $5\text{ V rms}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$
-3 dB Bandwidth	700			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 29
$C_S$ (Off)	2			pF typ	
$C_D$ (Off)	2			pF typ	
$C_D$ , $C_S$ (On)	5			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Digital Inputs = $0\text{ V}$ or $V_{DD}$
$I_{DD}$	150		5.0	$\mu\text{A}$ max	
$I_{DD}$			300	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital Input = $5\text{ V}$
$I_{SS}$	0.001			$\mu\text{A}$ typ	Digital Inputs = $0\text{ V}$ or $V_{DD}$
			5.0	$\mu\text{A}$ max	

Parameters	25°C	85°C	Y Version <sup>1</sup>	Unit	Test Conditions/Comments
I <sub>GND</sub>	0.001		5.0	μA typ	Digital Inputs = 0 V or V <sub>DD</sub>
I <sub>GND</sub>	150	300		μA max μA typ μA max	Digital Input = 5 V

<sup>1</sup> Temperature range for Y Version is –40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## SINGLE SUPPLY

V<sub>DD</sub> = 12 V ± 10%, V<sub>SS</sub> = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameters	25°C	85°C	Y Version <sup>1</sup>	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to V <sub>DD</sub>	V	
On Resistance (R <sub>ON</sub> )	220			Ω typ Ω max	V <sub>S</sub> = +10 V, I <sub>S</sub> = –10 mA; Figure 21
On Resistance Match between Channels (ΔR <sub>ON</sub> )	10			Ω typ Ω max	V <sub>S</sub> = +10 V, I <sub>S</sub> = –10 mA
On Resistance Flatness (R <sub>FLAT(ON)</sub> )	40			Ω typ	V <sub>S</sub> = +3 V/+6 V/+9 V, I <sub>S</sub> = –10 mA
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, I <sub>S</sub> (Off)	±0.01			nA typ nA max	V <sub>DD</sub> = 12 V V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V; Figure 22
Drain Off Leakage, I <sub>D</sub> (Off)	±0.01	±1	±5	nA typ nA max	V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V; Figure 22
Channel On Leakage, I <sub>D</sub> , I <sub>S</sub> (On)	±0.04	±1	±5	nA typ nA max	V <sub>S</sub> = V <sub>D</sub> = 1 V or 10 V, Figure 23
	±1	±2	±5	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, V <sub>INH</sub>		2.0		V min	
Input Low Voltage, V <sub>INL</sub>		0.8		V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.001		±0.5	μA typ μA max	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Digital Input Capacitance, C <sub>IN</sub>	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
t <sub>ON</sub>	50			ns typ ns max	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 8 V; Figure 24
t <sub>OFF</sub>	15			ns typ ns max	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 8 V; Figure 24
Break-before-Make Time Delay, t <sub>D</sub>	15			ns typ ns min	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> = V <sub>S2</sub> = 8 V; Figure 25
Charge Injection	5		1	pC typ pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF; Figure 26
Off Isolation	75			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Figure 27;
Channel-to-Channel Crosstalk	85			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; Figure 28
–3 dB Bandwidth	700			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; Figure 29
C <sub>S</sub> (Off)	2			pF typ	
C <sub>D</sub> (Off)	2			pF typ	
C <sub>D</sub> , C <sub>S</sub> (On)	5			pF typ	

Parameters	25°C	85°C	Y Version <sup>1</sup>	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = 13.2\text{ V}$
$I_{DD}$	0.001		5.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital Inputs = 0 V or $V_{DD}$
$I_{DD}$	150		300	$\mu\text{A typ}$ $\mu\text{A max}$	Digital Inputs = 5 V

<sup>1</sup> Temperature range for Y Version is  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .  
<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Ratings
$V_{DD}$ to $V_{SS}$	38 V
$V_{DD}$ to GND	-0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to -25 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V
Digital Inputs	GND - 0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Automotive (Y Version)	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance	150.4°C/W
12-Lead LFCSP, $\theta_{JA}$ Thermal Impedance	TBD°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

<sup>1</sup> Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TRUTH TABLE FOR SWITCHES

**Table 4.**

IN	Switch A	Switch B
0	Off	On
1	On	Off

### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

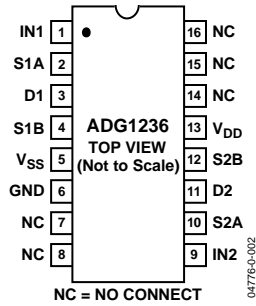


Figure 2. TSSOP Pin Configuration

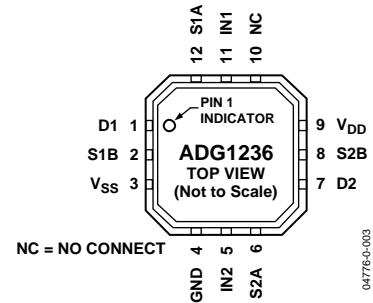


Figure 3. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.		Mnemonic	Function
TSSOP	LFCSP		
1	11	IN1	Logic Control Input.
2	12	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V <sub>SS</sub>	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14–16	10	NC	No Connect.
9	5	IN2	Logic Control Input.
10	6	S2A	Source Terminal. Can be an input or output.
11	7	D2	Drain Terminal. Can be an input or output.
12	8	S2B	Source Terminal. Can be an input or output.
13	9	V <sub>DD</sub>	Most Positive Power Supply Potential.

## TERMINOLOGY

**I<sub>DD</sub>**

The positive supply current.

**I<sub>SS</sub>**

The negative supply current.

**V<sub>D</sub> (V<sub>S</sub>)**

The analog voltage on Terminals D and S.

**R<sub>ON</sub>**

The ohmic resistance between D and S.

**R<sub>FLAT(ON)</sub>**

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

**I<sub>S</sub> (Off)**

The source leakage current with the switch off.

**I<sub>D</sub> (Off)**

The drain leakage current with the switch off.

**I<sub>D</sub>, I<sub>S</sub> (On)**

The channel leakage current with the switch on.

**V<sub>INL</sub>**

The maximum input voltage for Logic 0.

**V<sub>INH</sub>**

The minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

The input current of the digital input.

**C<sub>S</sub> (Off)**

The off switch source capacitance, measured with reference to ground.

**C<sub>D</sub> (Off)**

The off switch drain capacitance, measured with reference to ground.

**C<sub>D</sub>, C<sub>S</sub> (On)**

The on switch capacitance, measured with reference to ground.

**C<sub>IN</sub>**

The digital input capacitance.

**t<sub>ON</sub>**

The delay between applying the digital control input and the output switching on. See Figure 24.

**t<sub>OFF</sub>**

The delay between applying the digital control input and the output switching off.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation**

A measure of unwanted signal coupling through an off switch.

**Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth**

The frequency at which the output is attenuated by 3 dB.

**On Response**

The frequency response of the on switch.

**Insertion Loss**

The loss due to the on resistance of the switch.



### TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply



Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply



Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply



Figure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply



Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply



Figure 9. Leakage Current as a Function of  $V_D$  ( $V_S$ )



Figure 10. Leakage Currents as a Function of  $V_D$  ( $V_S$ )



Figure 13. Leakage Currents as a Function of Temperature



Figure 11. Leakage Current as a Function of  $V_D$  ( $V_S$ )



Figure 14. Supply Currents vs. Input Switching Frequency



Figure 12. Leakage Currents as a Function of Temperature



Figure 15. Charge Injection vs. Source Voltage



Figure 16.  $t_{ON}/t_{OFF}$  Times vs. Temperature



Figure 19. On Response vs. Frequency



Figure 17. Off Isolation vs. Frequency



Figure 20. THD + N vs. Frequency



Figure 18. Crosstalk vs. Frequency

TEST CIRCUITS

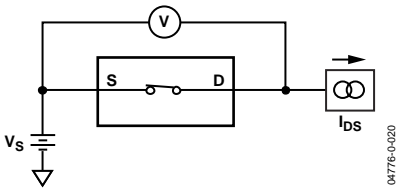


Figure 21. Test Circuit 1—On Resistance

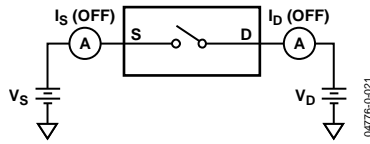


Figure 22. Test Circuit 2—Off Resistance

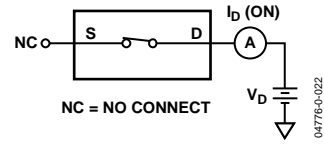


Figure 23. Test Circuit 3—On Leakage

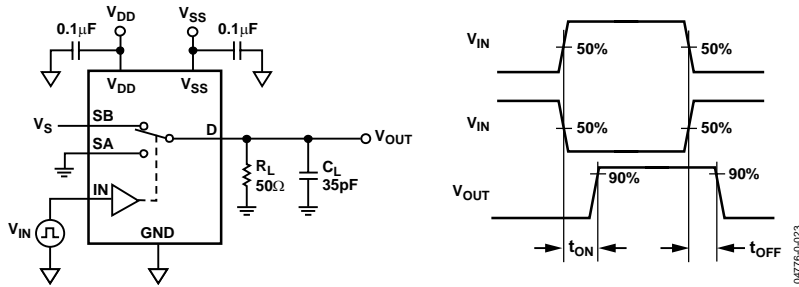


Figure 24. Test Circuit 4—Switching Times

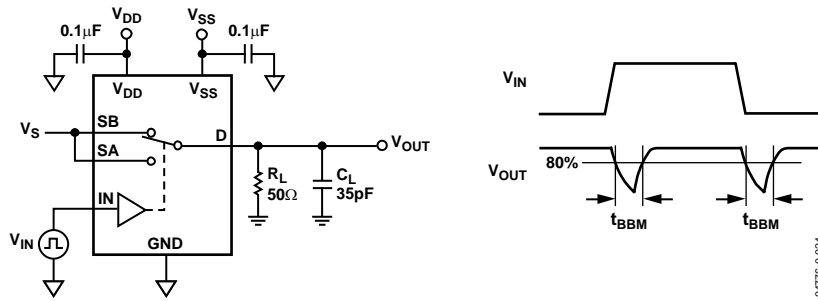


Figure 25. Test Circuit 5—Break-before-Make Time Delay

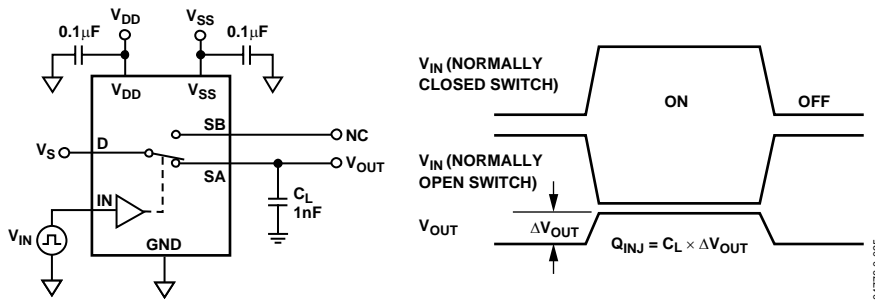


Figure 26. Test Circuit 6—Charge Injection

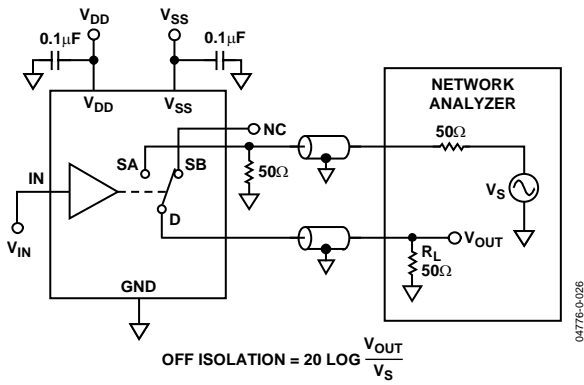


Figure 27. Test Circuit 7—Off Isolation

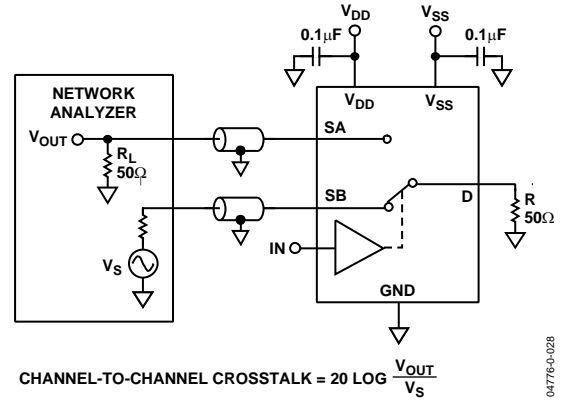


Figure 29. Test Circuit 9—Bandwidth

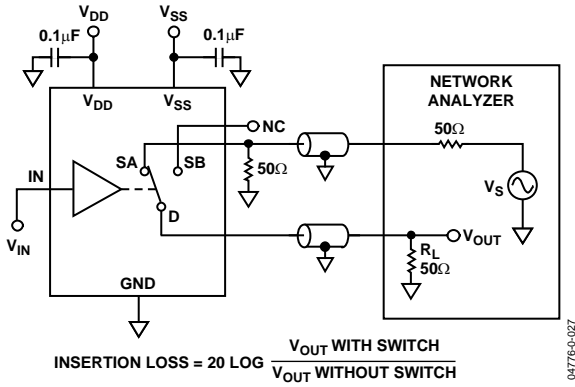


Figure 28. Test Circuit 8—Channel-to-Channel Crosstalk

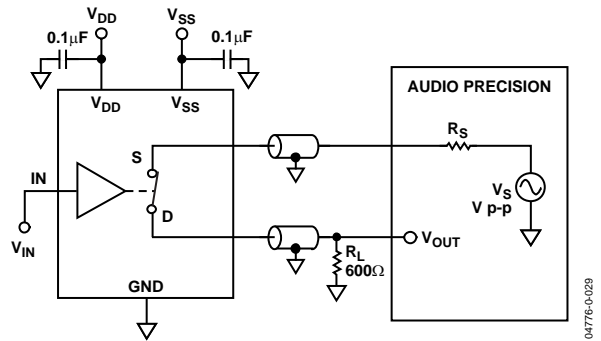


Figure 30. Test Circuit 10—THD + Noise

OUTLINE DIMENSIONS

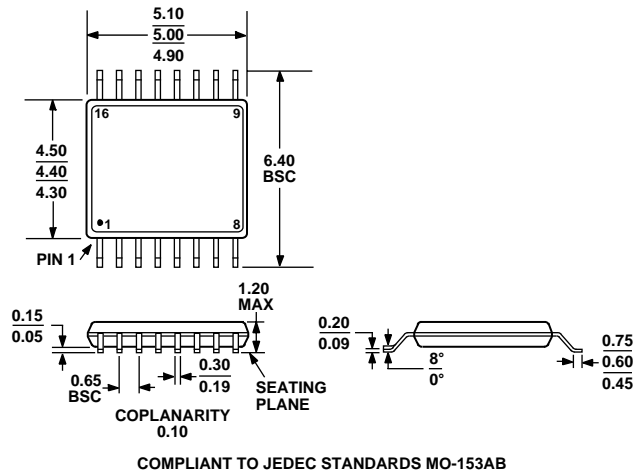


Figure 31. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in inches and (millimeters)

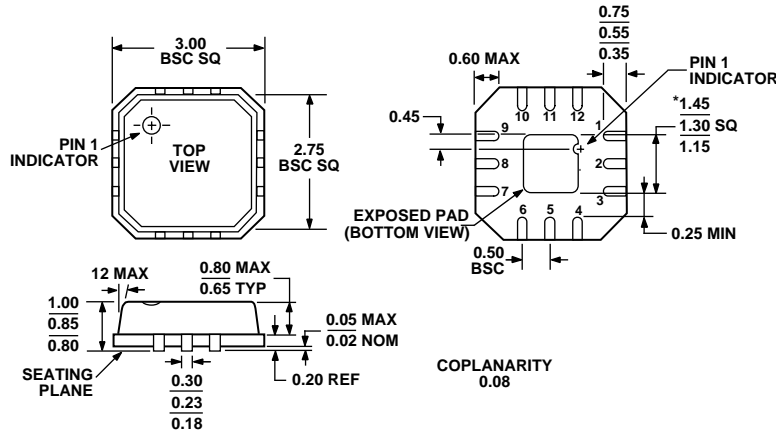


Figure 32. 12-Lead Lead Frame Chip Scale Package [VQ\_LFCSP] 3 mm × 3 mm Body, Very Thin Quad (CP-12-1)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1236YRU	-40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1236YCP	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-12-1

**NOTES**

**NOTES**