30 V Zero-Drift, Rail-to-Rail Output Precision Amplifier

Data Sheet

ADA4638-1

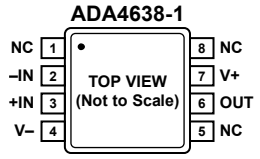
FEATURES

- Single supply operation: 4.5 V to 30 V
- Dual supply operation: ±2.25 V to ±15 V
- Low offset voltage: 4 µV maximum
- Input offset voltage drift: 0.05 µV/°C maximum
- High gain: 130 dB minimum
- High PSRR: 120 dB minimum
- High CMRR: 130 dB minimum
- Input common-mode range includes lower supply rail
- Rail-to-rail output
- Low supply current: 0.95 mA maximum

APPLICATIONS

- Electronic weigh scale
- Pressure and position sensors
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers

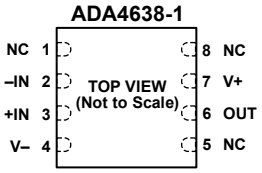
PIN CONFIGURATIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

10072-001

Figure 1. 8-Lead SOIC



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V–.

10072-002

Figure 2. 8-Lead LFCSP

GENERAL DESCRIPTION

The ADA4638-1 is a high voltage, high precision, zero-drift amplifier featuring rail-to-rail output swing. It is guaranteed to operate from 4.5 V to 30 V single supply or ±2.25 V to ±15 V dual supplies while consuming less than 0.95 mA of supply current at ±5 V.

With an offset voltage of 4 µV, offset drift less than 0.05 µV/°C, no 1/f noise, and input voltage noise of only 1.2 µV p-p (0.1 Hz to 10 Hz), the ADA4638-1 is suited for high precision applications where large error sources cannot be tolerated. Pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over the wide operating temperature range. Many applications can take advantage of the rail-to-rail output swing provided by the ADA4638-1 to maximize the signal-to-noise ratio (SNR).

The ADA4638-1 is specified for the extended industrial (−40°C to +125°C) temperature range and is available in 8-lead LFCSP (3 mm × 3 mm) and SOIC packages.

Table 1. Analog Devices, Inc., Zero-Drift Op Amp Portfolio

Operating Voltage	Type	Product	Offset Voltage (µV) Max	Offset Voltage Drift (µV/°C) Max
30 V	Single	ADA4638-1	4.5	0.08
16 V	Single	AD8638	9	0.06
	Dual	AD8639	9	0.06
5 V	Single	ADA4528-1	2.5	0.015
		AD8628	5	0.02
		AD8538	13	0.1
		ADA4051-1	15	0.1
	Dual	AD8629	5	0.02
		AD8539	13	0.1
		ADA4051-2	15	0.1
	Quad	AD8630	5	0.02

Rev. 0

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ADA4638-1* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- EVAL-OPAMP-1 Evaluation Board

Documentation

Data Sheet

- ADA4638-1: 30V Auto-zero, Rail-to-Rail Output Precision Amplifier Data Sheet

Technical Books

- Op Amp Applications Handbook, 2005
- Practical Design Techniques for Sensor Signal Conditioning, 1999

Tools and Simulations

- Analog Filter Wizard
- Analog Photodiode Wizard
- ADA4638-1 SPICE Macro Model

Reference Designs

- CN0359

Reference Materials

Technical Articles

- MS-2062: To Chop or Auto-Zero: That Is the Question.

Tutorials

- MT-055: Chopper Stabilized (Auto-Zero) Precision Op Amps

Design Resources

- ADA4638-1 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all ADA4638-1 EngineerZone Discussions

Sample and Buy

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Technical Support

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REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—30 V OPERATION

V_S = 30 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.5	4.5	µV
		−40°C ≤ T_A ≤ +125°C; SOIC			12.5	µV
		−40°C ≤ T_A ≤ +125°C; LFCSP			14.5	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C; SOIC			0.08	µV/°C
		−40°C ≤ T_A ≤ +125°C; LFCSP			0.1	µV/°C
Input Bias Current	I_B			45	90	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Offset Current	I_{OS}			25	105	pA
		−40°C ≤ T_A ≤ +125°C			170	pA
Input Voltage Range			0		27	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 27 V	130	142		dB
		−40°C ≤ T_A ≤ +125°C	130			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 1 V to 29 V	140	165		dB
		−40°C ≤ T_A ≤ +125°C	140			dB
Input Resistance, Common Mode	R_{INCM}			330		GΩ
Input Capacitance, Differential Mode	C_{INDM}			4		pF
Input Capacitance, Common Mode	C_{INCM}			9		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	29.90	29.92		V
		−40°C ≤ T_A ≤ +125°C	29.85			V
		R_L = 2 kΩ to V_{CM}	29.50	29.58		V
		−40°C ≤ T_A ≤ +125°C	29.35			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		50	60	mV
		−40°C ≤ T_A ≤ +125°C			95	mV
		R_L = 2 kΩ to V_{CM}		235	270	mV
		−40°C ≤ T_A ≤ +125°C			445	mV
Short-Circuit Current	I_{SC}			±38		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		220		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 30 V	120	143		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		0.85	1.05	mA
		−40°C ≤ T_A ≤ +125°C			1.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.5		V/µs
Overload Recovery Time		R_L = 10 kΩ, C_L = 20 pF, A_V = −100		8		µs
Settling Time to 0.1%	t_S	V_{IN} = 5 V step, R_L = 10 kΩ, C_L = 20 pF, A_V = −1		4		µs
Unity-Gain Crossover	UGC	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.3		MHz
Phase Margin	Φ_M	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		69		Degrees
Gain-Bandwidth Product	GBP	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +100		1.5		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		2.5		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		66		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—10 V OPERATION

V_S = 10 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.1	4	µV
		−40°C ≤ T_A ≤ +125°C; SOIC			9	µV
		−40°C ≤ T_A ≤ +125°C; LFCSP			12	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C; SOIC			0.05	µV/°C
		−40°C ≤ T_A ≤ +125°C; LFCSP			0.08	µV/°C
Input Bias Current	I_B			20	50	pA
		−40°C ≤ T_A ≤ +125°C			250	pA
Input Offset Current	I_{OS}			20	80	pA
		−40°C ≤ T_A ≤ +125°C			140	pA
Input Voltage Range			0		7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 7 V	130	155		dB
		−40°C ≤ T_A ≤ +125°C	130			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 1 V to 9 V	130	160		dB
		−40°C ≤ T_A ≤ +125°C	130			dB
Input Resistance, Common Mode	R_{INCM}			250		GΩ
Input Capacitance, Differential Mode	C_{INDM}			4		pF
Input Capacitance, Common Mode	C_{INCM}			9		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	9.96	9.97		V
		−40°C ≤ T_A ≤ +125°C	9.95			V
		R_L = 2 kΩ to V_{CM}	9.85	9.86		V
		−40°C ≤ T_A ≤ +125°C	9.75			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		20	25	mV
		−40°C ≤ T_A ≤ +125°C			40	mV
		R_L = 2 kΩ to V_{CM}		80	90	mV
		−40°C ≤ T_A ≤ +125°C			145	mV
Short-Circuit Current	I_{SC}			±22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		300		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 30 V	120	143		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		0.8	0.95	mA
		−40°C ≤ T_A ≤ +125°C			1.15	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.5		V/µs
Overload Recovery Time		R_L = 10 kΩ, C_L = 20 pF, A_V = −100		14		µs
Settling Time to 0.1%	t_S	V_{IN} = 2 V step, R_L = 10 kΩ, C_L = 20 pF, A_V = −1		3		µs
Unity-Gain Crossover	UGC	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.1		MHz
Phase Margin	Φ_M	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		67		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +100		1.4		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 30 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		66		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.1		pA/√Hz

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_S = 5 V, V_{CM} = V_{SY}/2 V, T_A = 25°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	13	µV
		−40°C ≤ T_A ≤ +125°C; SOIC			18	µV
		−40°C ≤ T_A ≤ +125°C; LFCSP			21	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C; SOIC			0.05	µV/°C
		−40°C ≤ T_A ≤ +125°C; LFCSP			0.08	µV/°C
Input Bias Current	I_B			30	90	pA
		−40°C ≤ T_A ≤ +125°C			230	pA
Input Offset Current	I_{OS}			60	170	pA
		−40°C ≤ T_A ≤ +125°C			200	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	118	140		dB
		−40°C ≤ T_A ≤ +125°C	118			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to +4.5 V	125	150		dB
		−40°C ≤ T_A ≤ +125°C	125			dB
Input Resistance, Common Mode	R_{INCM}			75		GΩ
Input Capacitance, Differential Mode	C_{INDM}			4		pF
Input Capacitance, Common Mode	C_{INCM}			9		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.98	4.984		V
		−40°C ≤ T_A ≤ +125°C	4.97			V
		R_L = 2 kΩ to V_{CM}	4.90	4.92		V
		−40°C ≤ T_A ≤ +125°C	4.87			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		7.5	10	mV
		−40°C ≤ T_A ≤ +125°C			15	mV
		R_L = 2 kΩ to V_{CM}		37	45	mV
		−40°C ≤ T_A ≤ +125°C			70	mV
Short-Circuit Current	I_{SC}			±22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		340		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 4.5 V to 30 V	120	143		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		0.8	0.95	mA
		−40°C ≤ T_A ≤ +125°C			1.15	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.5		V/µs
Overload Recovery Time		R_L = 10 kΩ, C_L = 20 pF, A_V = −100		22		µs
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 20 pF, A_V = −1		3		µs
Unity-Gain Crossover	UGC	V_{IN} = 20 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.0		MHz
Phase Margin	Φ_M	V_{IN} = 20 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		64		Degrees
Gain Bandwidth Product	GBP	V_{IN} = 20 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +100		1.3		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 20 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		1.8		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		1.2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		70		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.015		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	33 V
Input Voltage[1]	$\pm V_{SY}$
Input Current	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Input voltage should always be limited to less than 30 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on a 4-layer JEDEC standard board with zero airflow. For LFCSP packages, the exposed pad is soldered to the board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	120	45	°C/W
8-Lead LFCSP	75	12	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

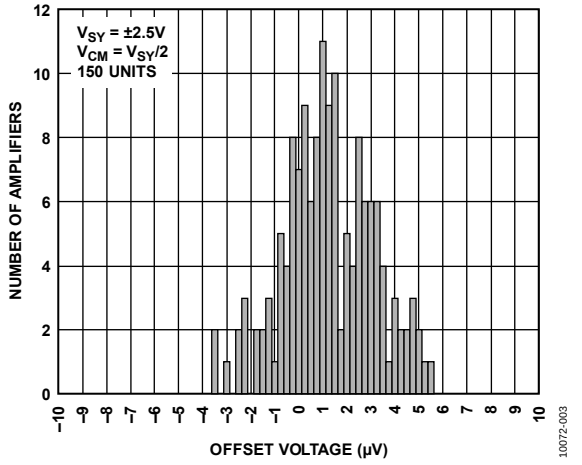

Figure 3. Input Offset Voltage Distribution

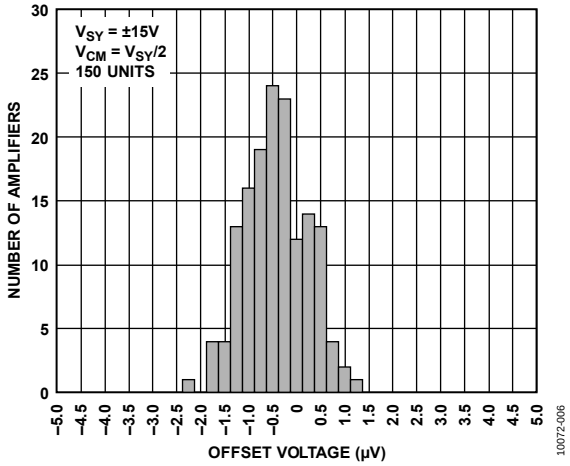

Figure 6. Input Offset Voltage Distribution

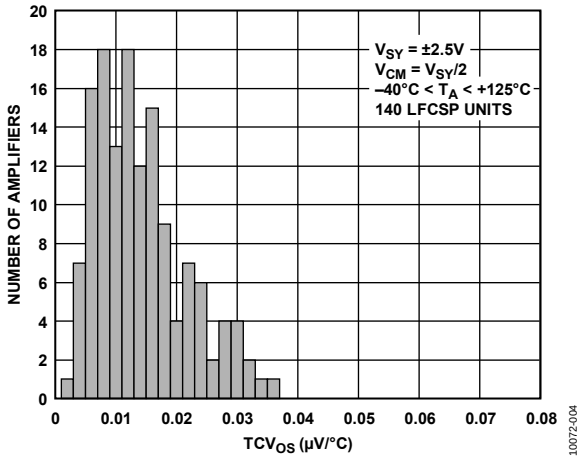

Figure 4. Input Offset Voltage Drift Distribution

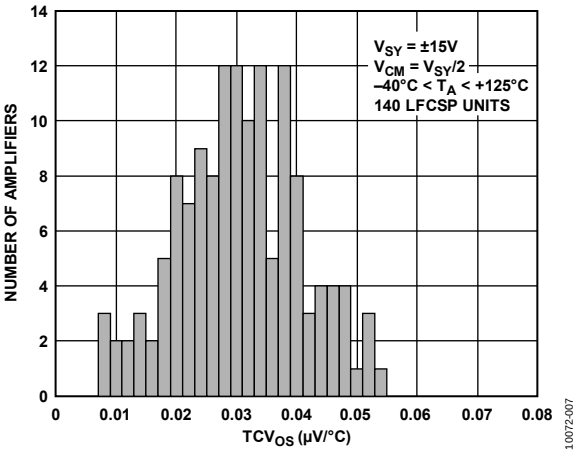

Figure 7. Input Offset Voltage Drift Distribution

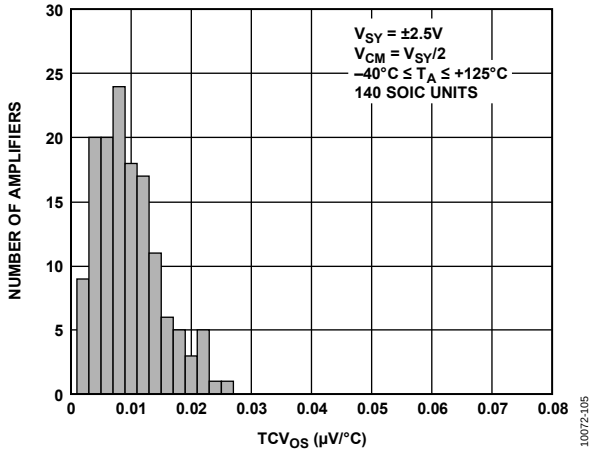

Figure 5. Input Offset Voltage Drift Distribution

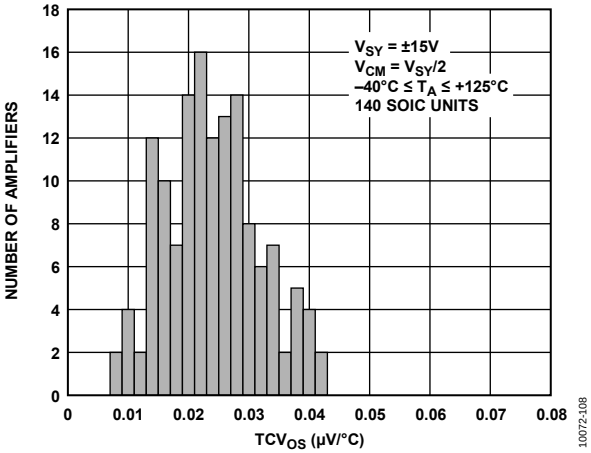

Figure 8. Input Offset Voltage Drift Distribution

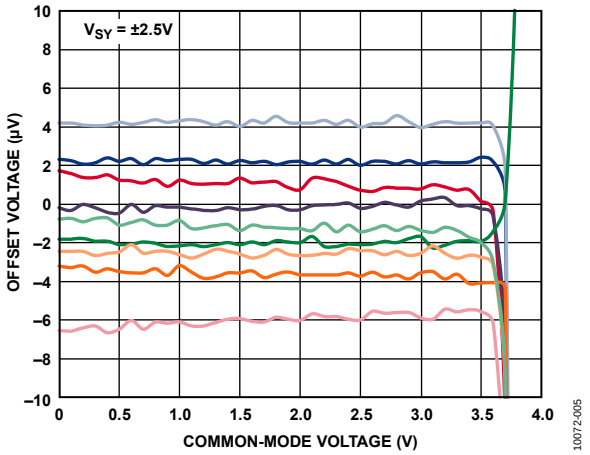

Figure 9. Input Offset Voltage vs. Common-Mode Voltage

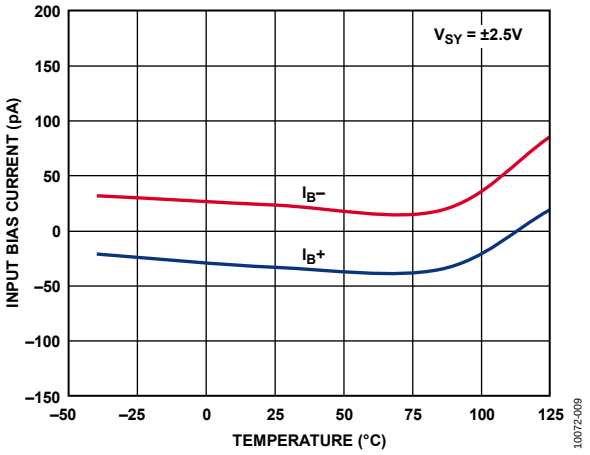

Figure 10. Input Bias Current vs. Temperature

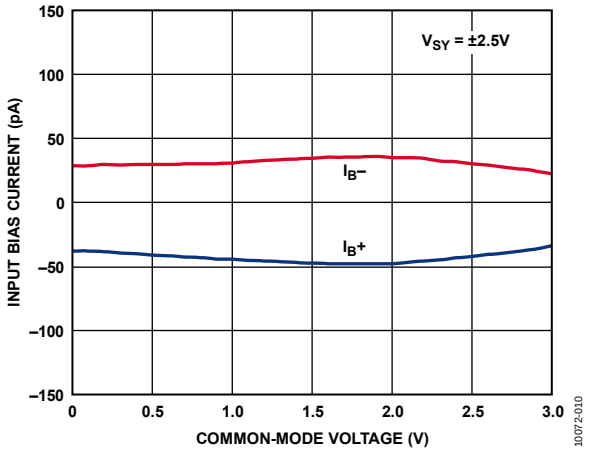

Figure 11. Input Bias Current vs. Common-Mode Voltage

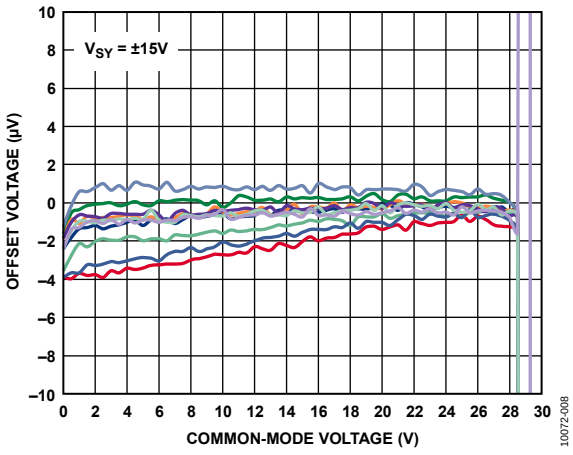

Figure 12. Input Offset Voltage vs. Common-Mode Voltage

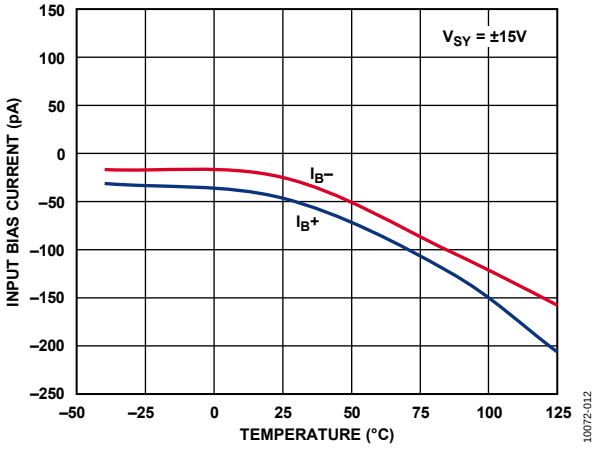

Figure 13. Input Bias Current vs. Temperature

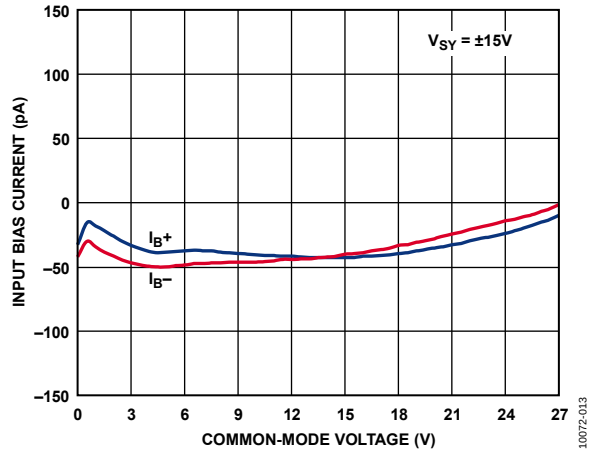

Figure 14. Input Bias Current vs. Common-Mode Voltage

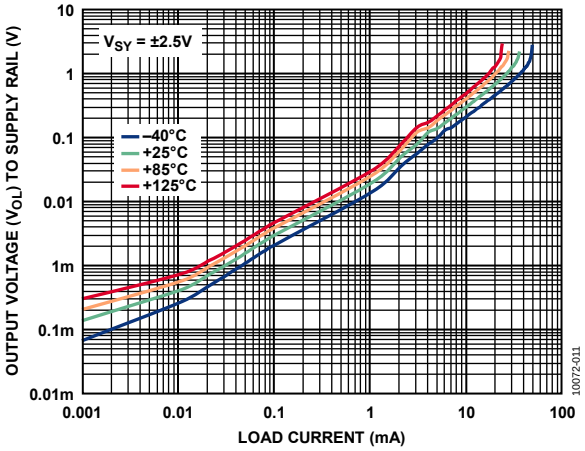

Figure 15. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

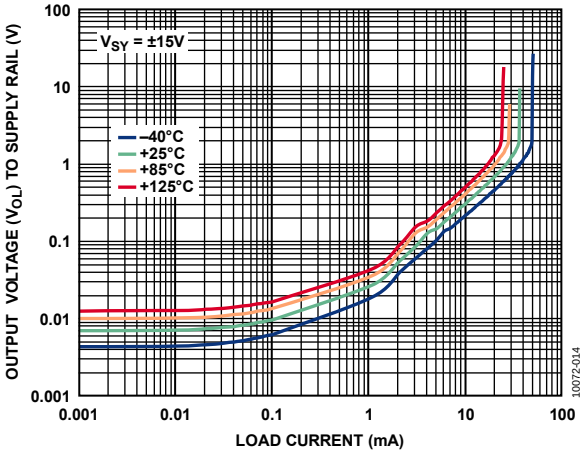

Figure 18. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

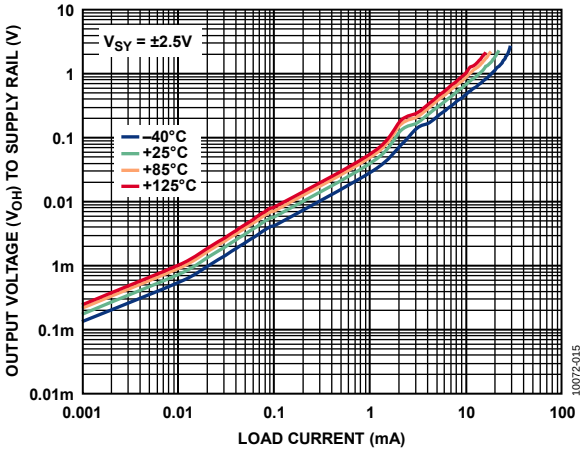

Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

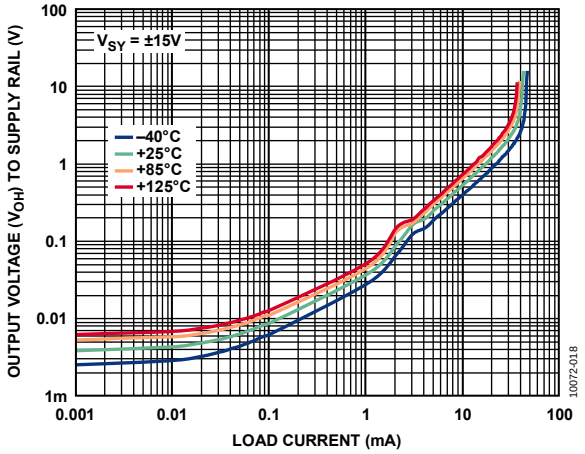

Figure 19. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

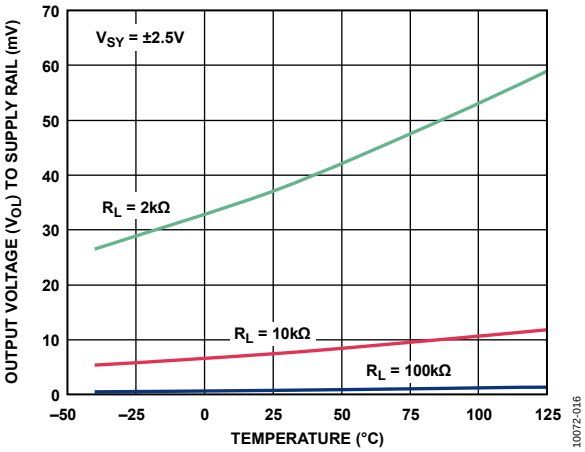

Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

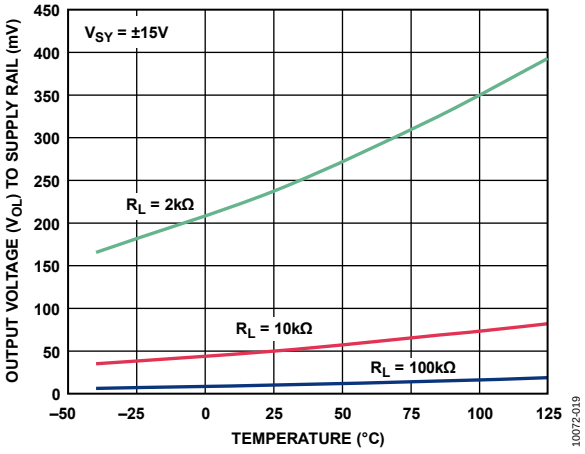

Figure 20. Output Voltage (V_{OL}) to Supply Rail vs. Temperature

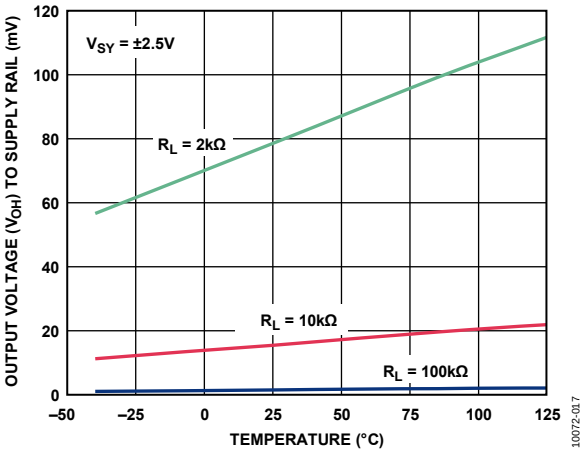

Figure 21. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

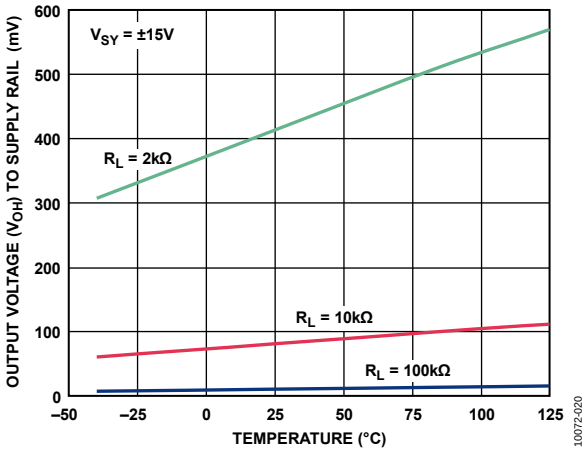

Figure 24. Output Voltage (V_{OH}) to Supply Rail vs. Temperature

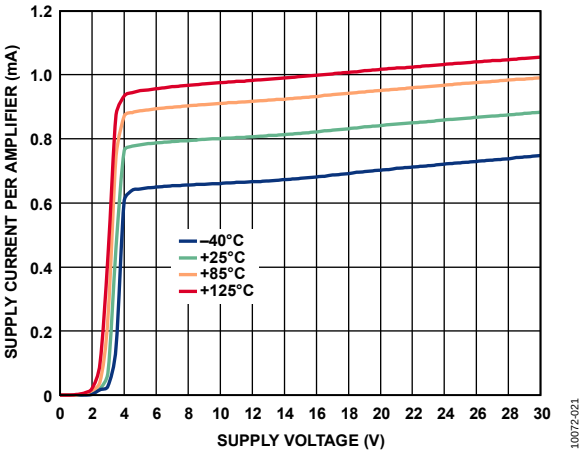

Figure 22. Supply Current vs. Supply Voltage

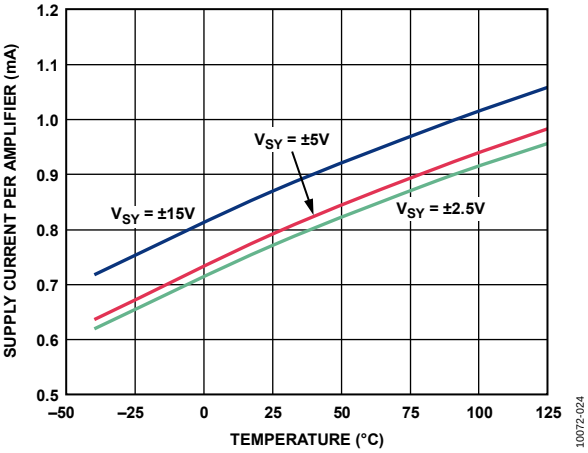

Figure 25. Supply Current vs. Temperature

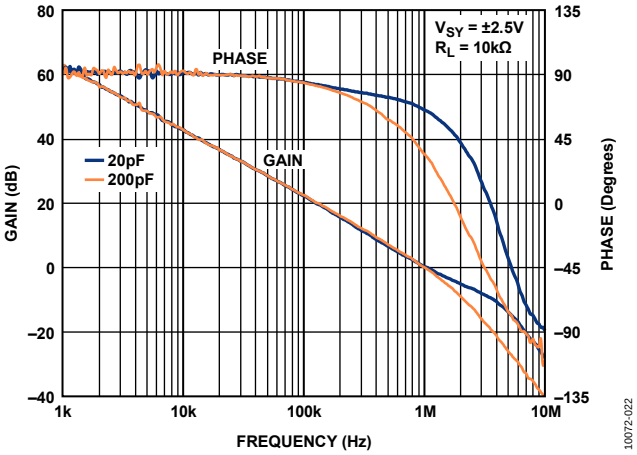

Figure 23. Open-Loop Gain and Phase vs. Frequency

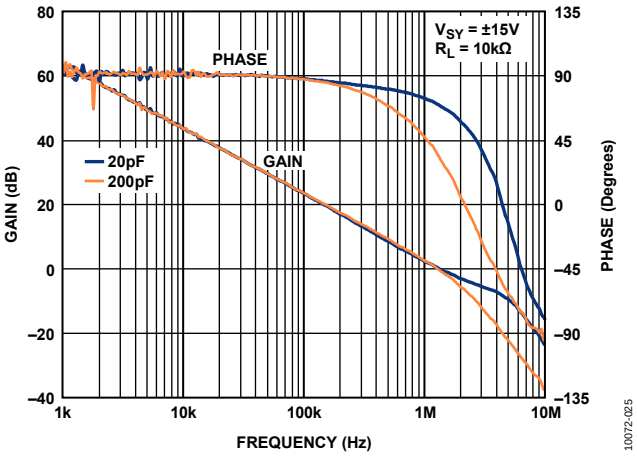

Figure 26. Open-Loop Gain and Phase vs. Frequency

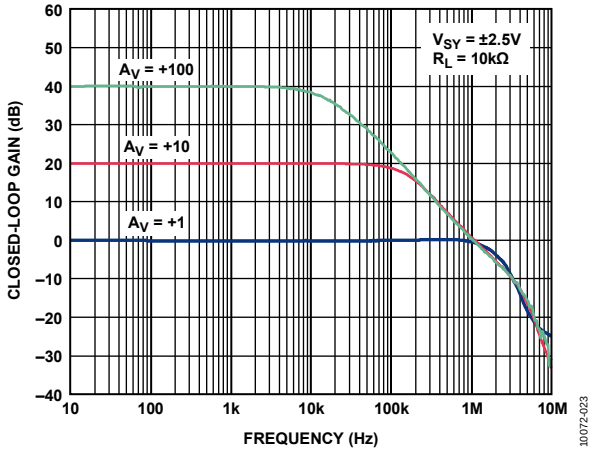

Figure 27. Closed-Loop Gain vs. Frequency

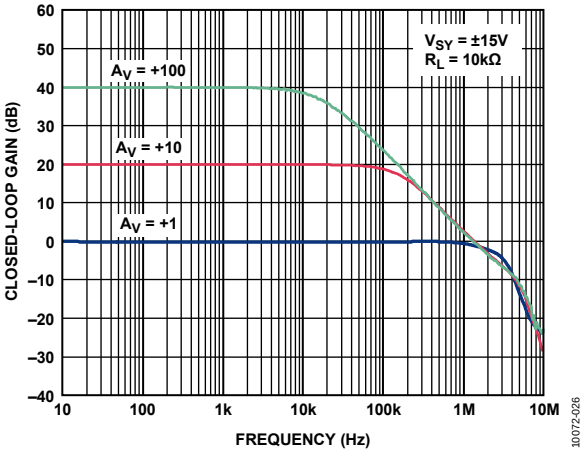

Figure 30. Closed-Loop Gain vs. Frequency

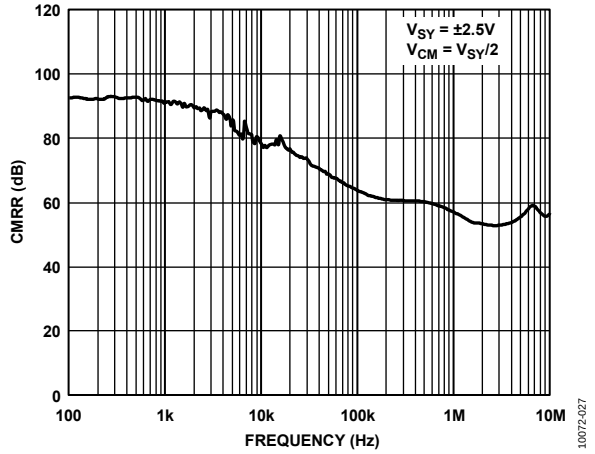

Figure 28. CMRR vs. Frequency

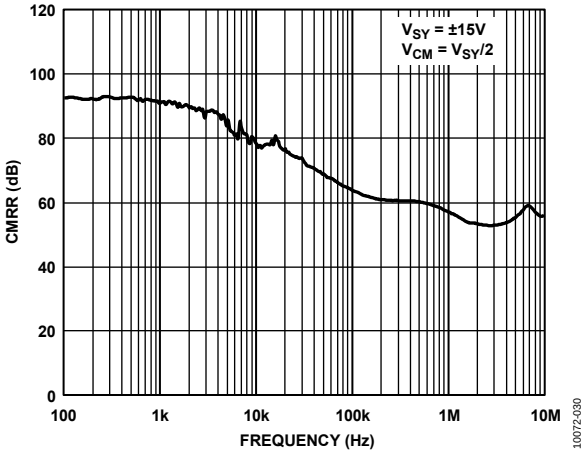

Figure 31. CMRR vs. Frequency

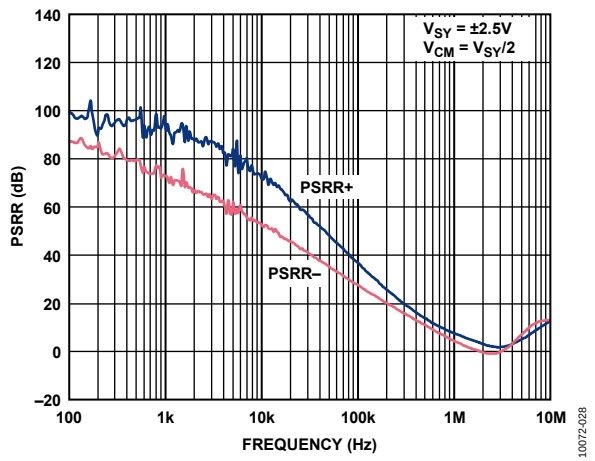

Figure 29. PSRR vs. Frequency

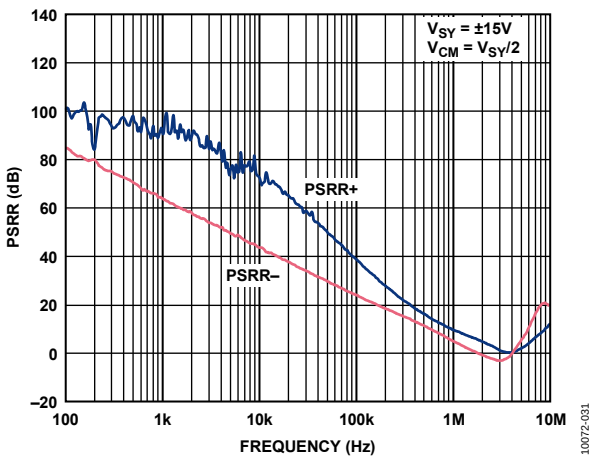

Figure 32. PSRR vs. Frequency

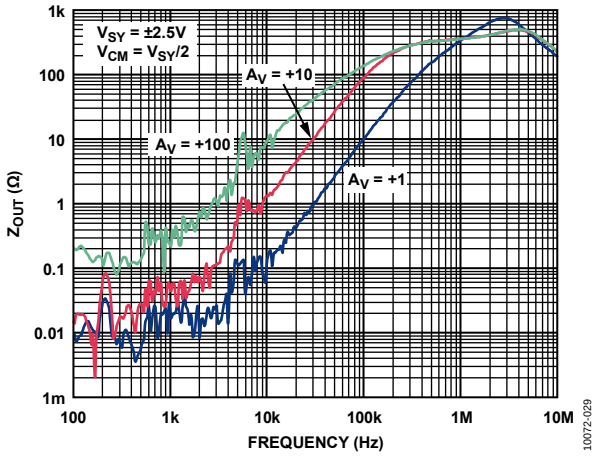

Figure 33. Closed-Loop Output Impedance vs. Frequency

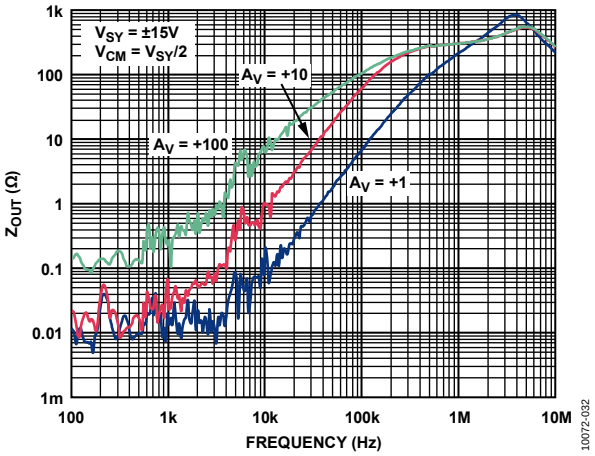

Figure 36. Closed-Loop Output Impedance vs. Frequency

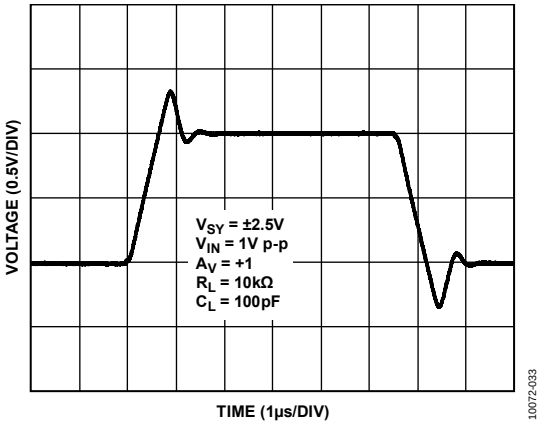

Figure 34. Large Signal Transient Response

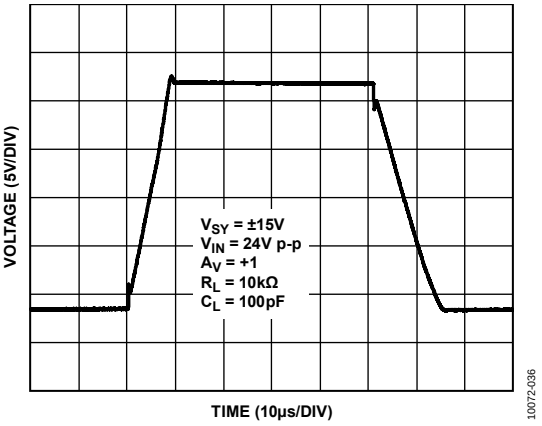

Figure 37. Large Signal Transient Response

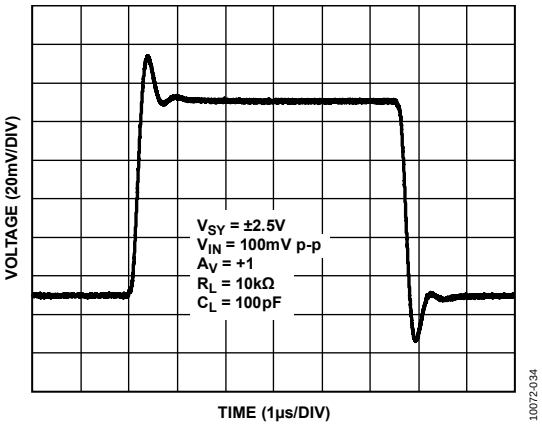

Figure 35. Small Signal Transient Response

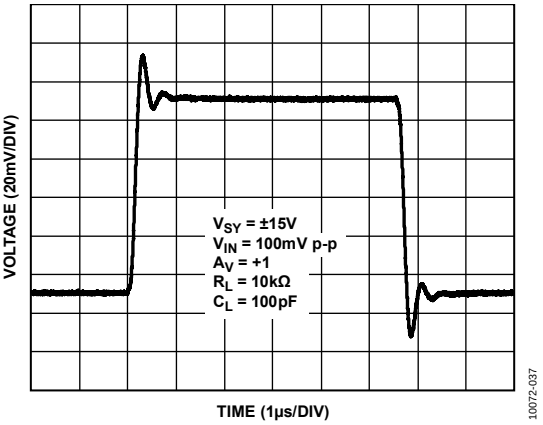

Figure 38. Small Signal Transient Response

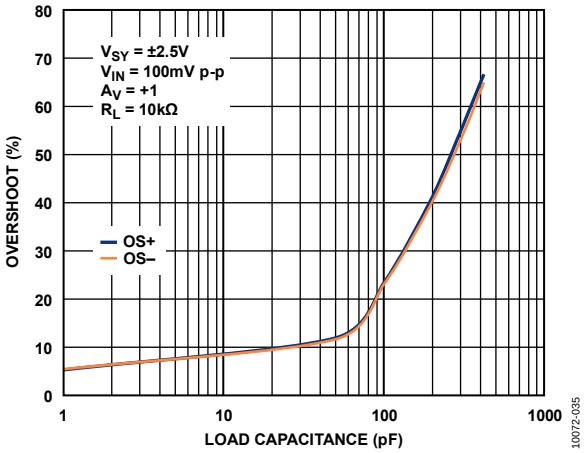

Figure 39. Small Signal Overshoot vs. Load Capacitance

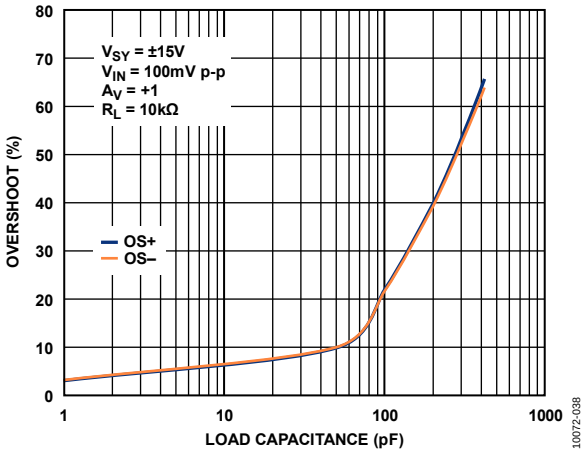

Figure 42. Small Signal Overshoot vs. Load Capacitance

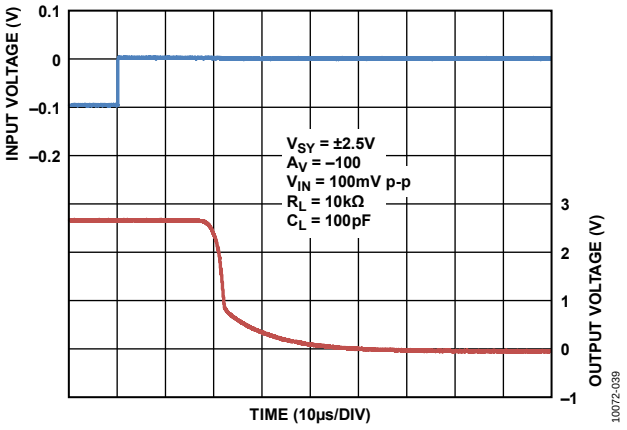

Figure 40. Positive Overload Recovery

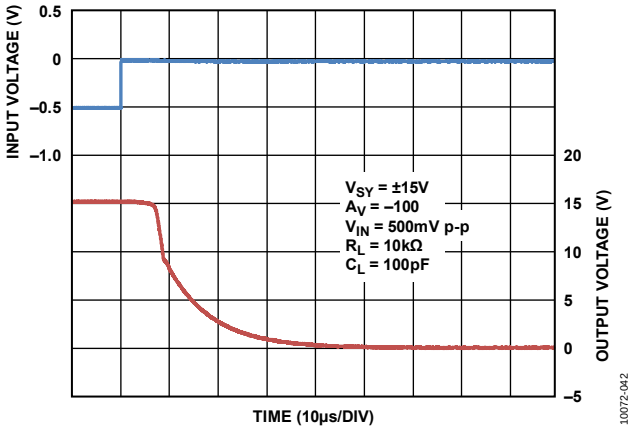

Figure 43. Positive Overload Recovery

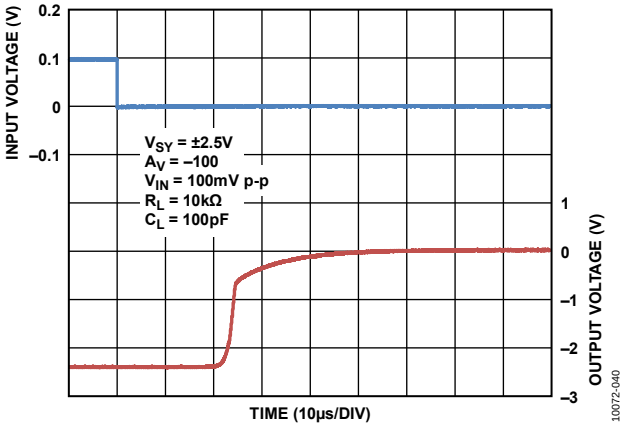

Figure 41. Negative Overload Recovery

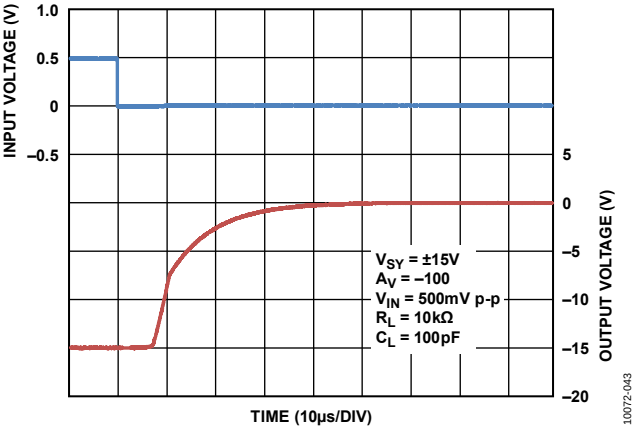

Figure 44. Negative Overload Recovery

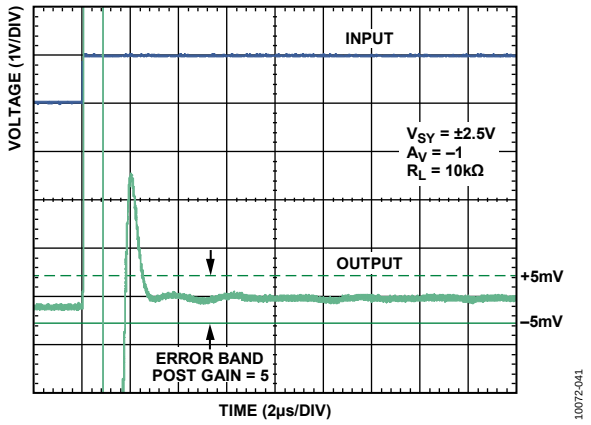

Figure 45. Positive Settling Time to 0.1%

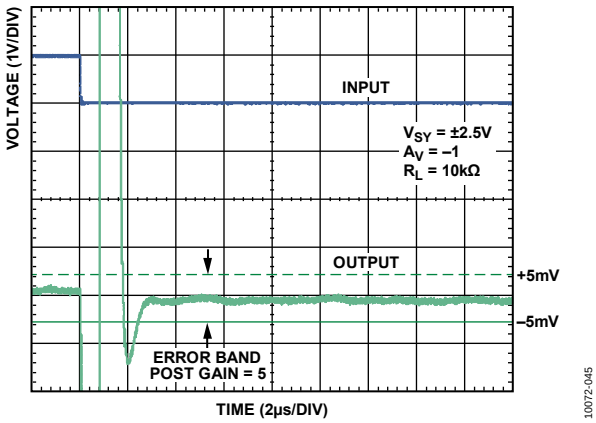

Figure 46. Negative Settling Time to 0.1%

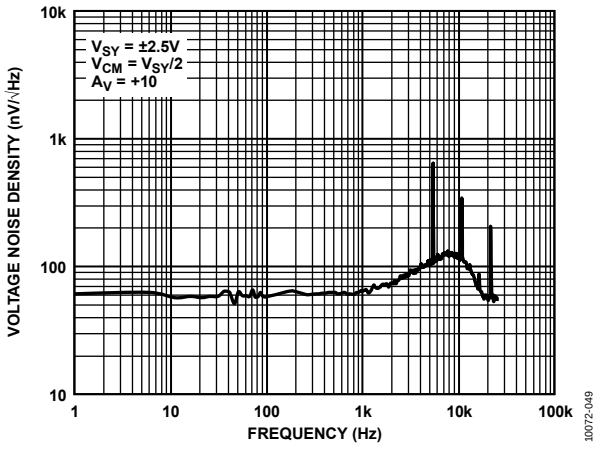

Figure 47. Voltage Noise Density vs. Frequency

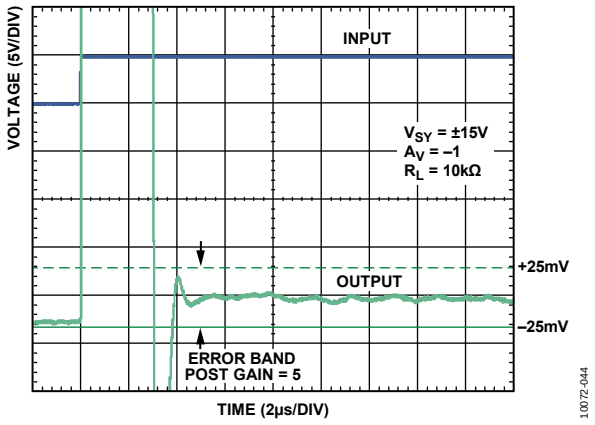

Figure 48. Positive Settling Time to 0.1%

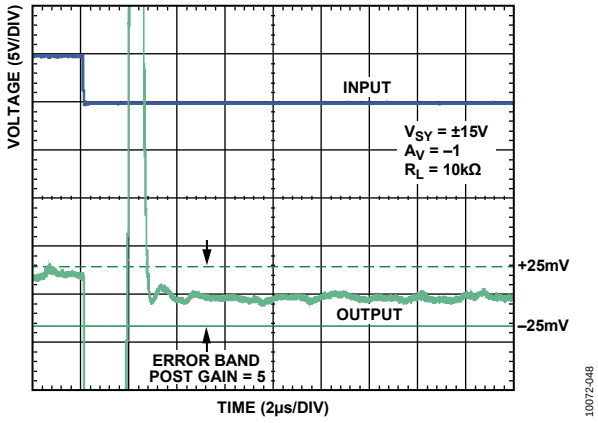

Figure 49. Negative Settling Time to 0.1%

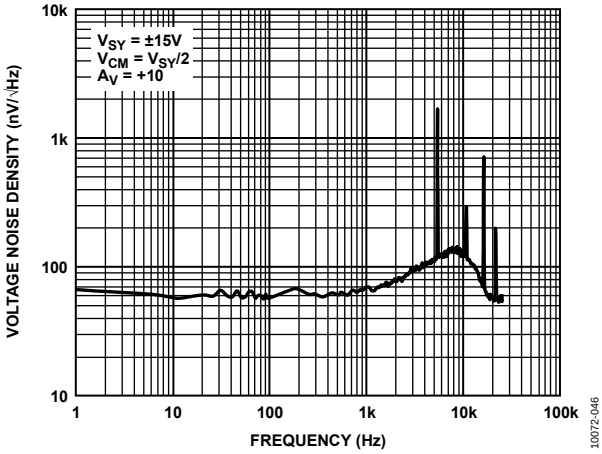

Figure 50. Voltage Noise Density vs. Frequency

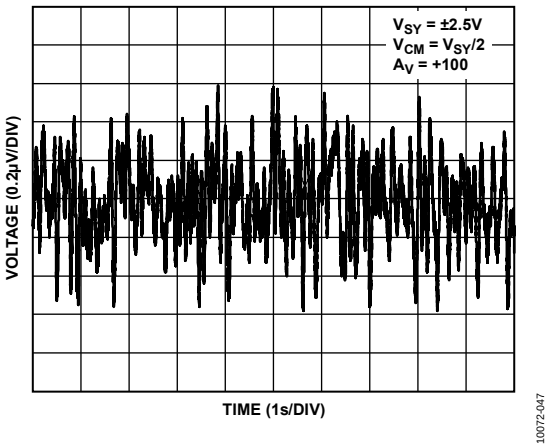

Figure 51. 0.1 Hz to 10 Hz Noise

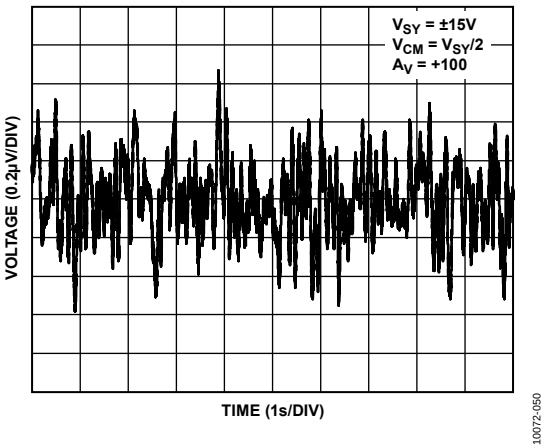

Figure 54. 0.1 Hz to 10 Hz Noise

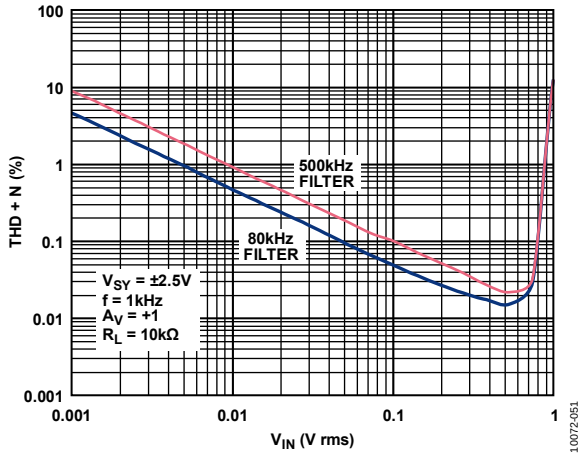

Figure 52. THD + N vs. Amplitude

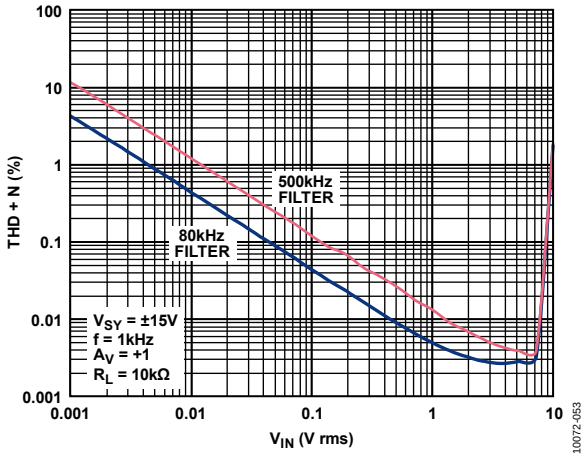

Figure 55. THD + N vs. Amplitude

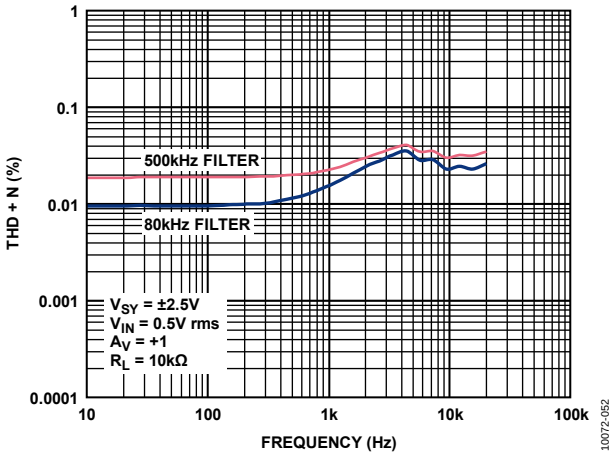

Figure 53. THD + N vs. Frequency

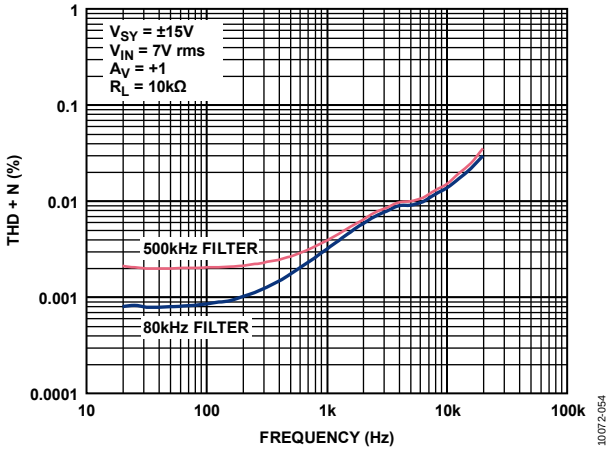

Figure 56. THD + N vs. Frequency

APPLICATIONS INFORMATION

The ADA4638-1, with its wide supply voltage range of 4.5 V to 30 V, is a precision, rail-to-rail output, zero-drift operational amplifier that features a patented combination of auto-zeroing and chopping technique. This unique topology allows the ADA4638-1 to maintain its low offset voltage over a wide temperature range and over its operating lifetime. This amplifier offers ultralow input offset voltage of 4.5 µV maximum and an input offset voltage drift of 80 nV/°C maximum. Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the auto-zeroing and chopping technique, resulting in a superb typical CMRR figure of 142 dB and a PSRR figure of 143 dB at a ±15 V supply voltage. With ultrahigh dc accuracy and no 1/f noise component, the ADA4638-1 is ideal for high gain amplification of low level signals in dc or low frequency applications without the risk of excessive output voltage errors.

DIFFERENTIATION

Traditionally, zero-drift amplifiers are designed using either the auto-zeroing or chopping technique. Each technique has its benefits and drawbacks. Auto-zeroing usually results in low noise energy at the auto-zeroing frequency, at the expense of higher low frequency noise due to aliasing of wideband noise into the auto-zeroed frequency band. Chopping results in lower low frequency noise at the expense of larger noise energy at the chopping frequency. The ADA4638-1 uses both auto-zeroing and chopping in a patented ping-pong arrangement to obtain lower low frequency noise together with lower energy at the chopping and auto-zeroing frequencies, maximizing the signal-to-noise ratio for the majority of applications. The relatively high chopping frequency of 16 kHz and auto-zeroing frequency of 8 kHz simplifies filter requirements for a wide, useful bandwidth.

THEORY OF OPERATION

Figure 57 shows the ADA4638-1 amplifier block diagram. The noninverting and inverting amplifier inputs are +IN and –IN, respectively. The transconductance amplifiers, A1 and A2, are the two input gain stages; the A3 and A4 transconductance amplifiers are the nulling amplifiers used to correct the offsets of A1 and A2, and A_{OUT} is the output amplifier. A four-phase cycle (φ1 to φ4) controls the switches. In Phase 1 (φ1), A1 is auto-zeroed where both the inputs of A1 are connected to +IN. A1 produces a differential output current of $V_{OS1} \times gm1$, where V_{OS1} is the input offset voltage of A1, and gm1 is the differential transconductance of A1. The outputs of A1 are then connected to the inputs and outputs of A3. A3 is designed to have an equivalent resistance of 1/gm3, where gm3 is the transconductance of A3. The amplified version of V_{OS1}, which is $V_{OS1} \times gm1/gm3$, is stored on Capacitors C1 and C2. These capacitors, together with A3, are used to null out the offset of A1 when A1 amplifies the signal during the φ3 and φ4 phases.

While A1 is being auto-zeroed, A2 (nulled by A4, C3, and C4) is used for signal amplification. The ADA4638-1 differs from traditional auto-zero amplifiers in that the input offset voltage is also chopped during signal amplification. During φ1, +IN and –IN are applied to the noninverting and inverting inputs, respectively, of A2. However, during φ2, both the inputs and outputs of A2 are inverted, and the input offset voltage of A2 is chopped.

The combination of auto-zeroing and chopping offers two major benefits. First, any residual offset following the auto-zeroing process is reduced. During φ1, the output offset voltage of A2 is $+V_{OSAZ2}$ and during φ2, it is $-V_{OSAZ2}$, producing a theoretical average of zero. Second, the aliased noise spectrum density at dc due to auto-zeroing is modulated up to the chopping frequency, and the prechopped noise spectrum density at the chopping frequency is modulated down to dc. This noise transformation lowers the noise spectrum density at dc, thus making zero-drift amplifiers ideal for low frequency signal amplification.

During φ3 and φ4, the roles of A1 and A2 are reversed. A2 offset is nulled, and the input signal is chopped and amplified using A1.

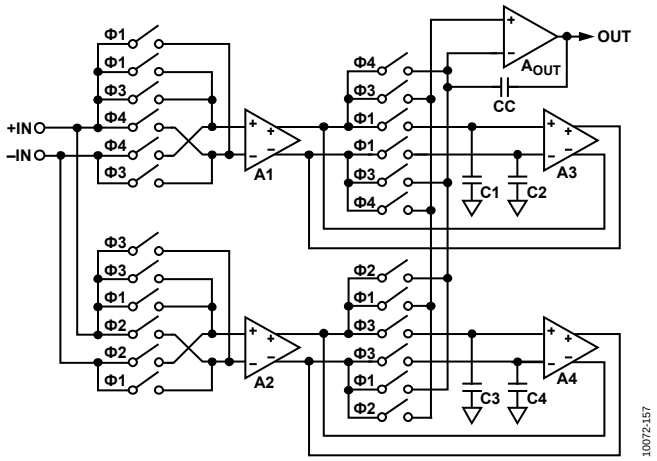

Figure 57. ADA4638-1 Amplifier Block Diagram

INPUT PROTECTION

The ADA4638-1 has internal ESD protection diodes that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse-biased during normal operation. However, if either input exceeds one of the supply rails, these ESD diodes become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, insert a resistor in series with each input to limit the input current to 10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

NO OUTPUT PHASE REVERSAL

An undesired phenomenon, phase reversal (also known as phase inversion) occurs in many amplifiers when one or both of the inputs are driven beyond the specified input common-mode voltage range, in effect reversing the polarity of the output. In some cases, phase reversal can induce lockups and cause equipment damage as well as self destruction.

The ADA4638-1 has been carefully designed to prevent any output phase reversal, provided that both inputs are maintained within the supply voltages. If either one or both inputs may exceed either supply voltage, place resistors in series with the inputs to limit the current to less than 10 mA.

The ADA4638-1 features rail-to-rail output with a supply voltage from 4.5 V to 30 V. Figure 58 shows the input and output waveforms of the ADA4638-1 configured as a unity-gain buffer with a supply voltage of ±15 V and a resistive load of 10 kΩ. The ADA4638-1 does not exhibit phase reversal.

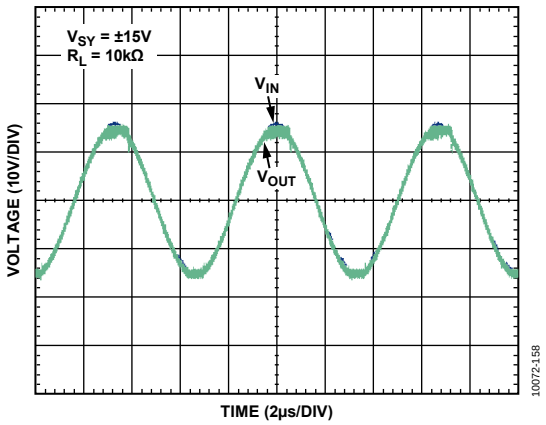

Figure 58. No Phase Reversal

NOISE CONSIDERATIONS

1/f Noise

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, the ADA4638-1 eliminates the 1/f noise internally, thus making it an excellent choice for dc or low frequency high precision applications. The 0.1 Hz to 10 Hz voltage noise is only 1.2 µV p-p at ±15 V of supply voltage.

The low frequency 1/f noise appears as a slow varying offset to the ADA4638-1 and is greatly reduced by the combination of auto-zeroing and chopping technique. This allows the ADA4638-1 to have a much lower noise at dc and low frequency in comparison to standard low noise amplifiers that are susceptible to 1/f noise. Figure 47 and Figure 50 show the voltage noise density of the ADA4638-1 with no 1/f noise.

COMPARATOR OPERATION

Op amps are designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 59 shows the ADA4638-1 configured as a voltage follower with an input voltage, which is kept at midpoint of the power supplies. A1 and A2 indicate the placement of ammeters to measure supply currents. I_{SY}+ refers to the current flowing into the positive supply pin of the op amp, and I_{SY}− refers to the current flowing out of the negative supply pin of the op amp. From Figure 60, as expected in normal operating condition, the current flowing into the op amp is equivalent to the current flowing out of the op amp, where I_{SY}+ = I_{SY}−.

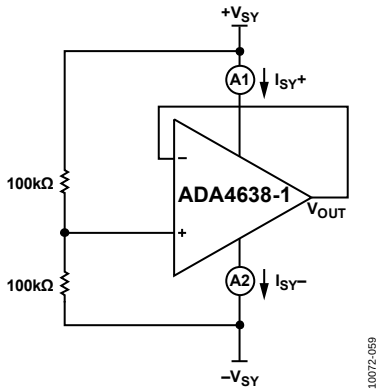

Figure 59. Voltage Follower

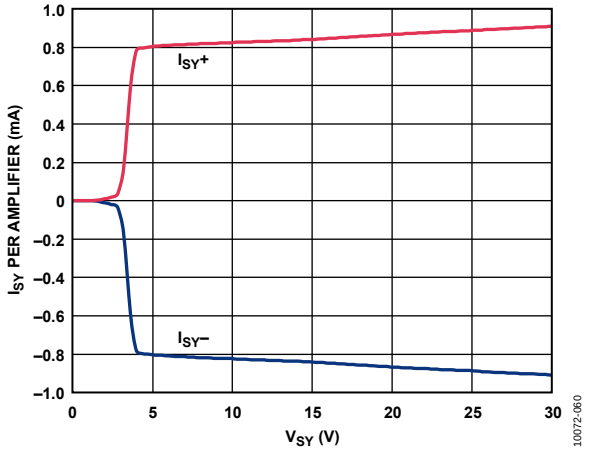

Figure 60. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 61 and Figure 62 show the ADA4638-1 configured as a comparator, with resistors R_{IN1} and R_{IN2} in series with the input pins.

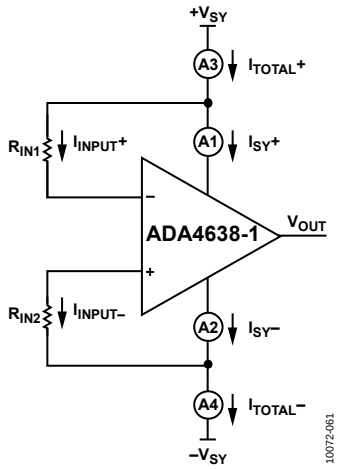

Figure 61. Comparator A

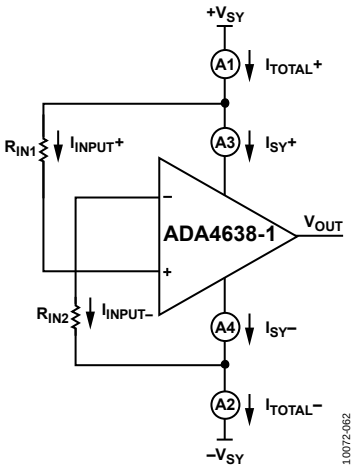

Figure 62. Comparator B

Figure 63 and Figure 64 show the total supply current of the system, I_{TOTAL}, and the actual currents, I_{SY}, that flow into and out of the supply pins of the ADA4638-1. With $R_{IN1} = R_{IN2} =$ 100 kΩ and supply voltage of 30 V, the total supply current of the system is 800 µA to 900 µA.

With smaller input series resistors, total supply current of the system increases much more. Figure 65 and Figure 66 show the supply currents with $R_{IN1} = R_{IN2} = 0$ Ω. The total current of the system increases to 10 mA.

$$I_{TOTAL} = I_{SY} + I_{INPUT}$$

Note that, at 30 V of supply voltage, 8 mA to 9 mA of current flows through the input pins. This is undesirable. The ADA4638-1 is not recommended to be used as a comparator. If absolutely necessary, place resistors in series with the inputs of the amplifier to limit input current to less than 10 mA.

For more details on op amps as comparators, refer to the AN-849 Application Note, *Using Op Amps as Comparators*.

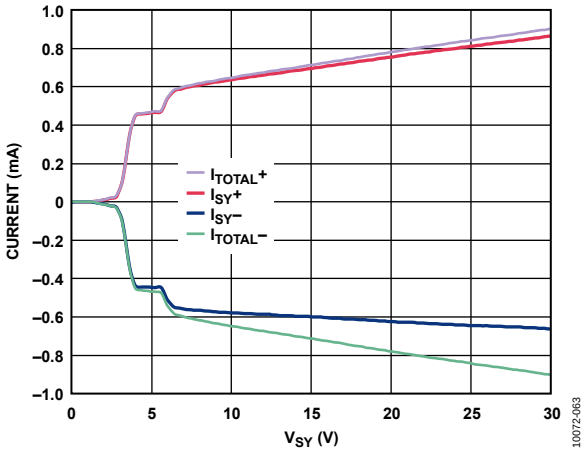

Figure 63. Supply Current vs. Supply Voltage (Comparator A, $R_{IN1} = R_{IN2} = 100$ kΩ)

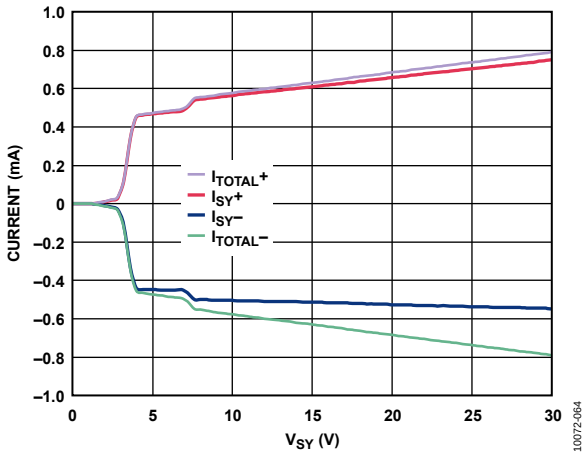

Figure 64. Supply Current vs. Supply Voltage (Comparator B, $R_{IN1} = R_{IN2} = 100$ kΩ)

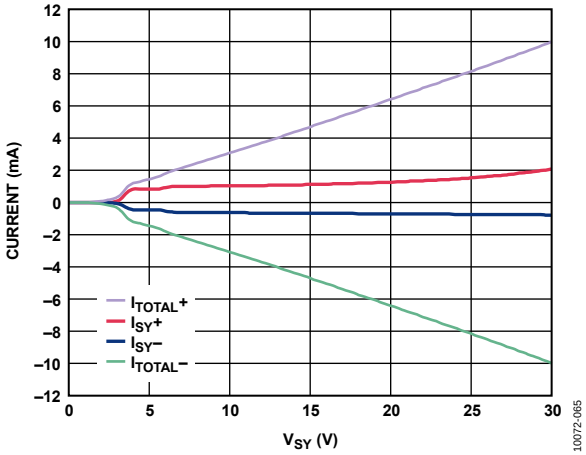

Figure 65. Supply Current vs. Supply Voltage (Comparator A, $R_{IN1} = R_{IN2} = 0$ kΩ)

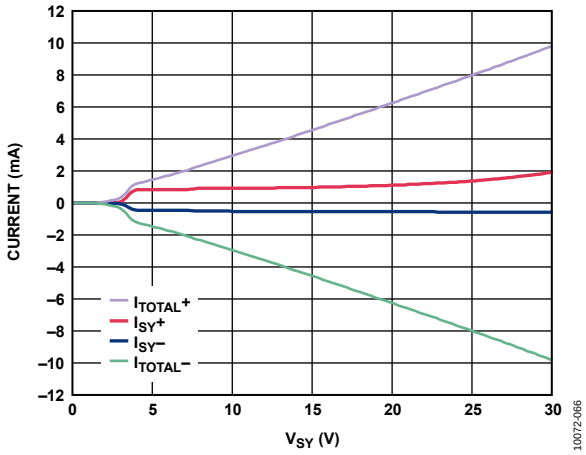

Figure 66. Supply Current vs. Supply Voltage (Comparator B, $R_{IN1} = R_{IN2} = 0$ kΩ)

PRECISION LOW-SIDE CURRENT SHUNT SENSOR

Many applications require the sensing of signals near the positive or negative rails. Current shunt sensors are one such application and are mostly used for feedback control systems. They are also used in a variety of other applications, including power metering, battery fuel gauging and feedback controls in electrical power steering. In such application, it is desirable to use a shunt with very low resistance to minimize series voltage drop. This not only minimizes wasted power, but also allows the measurement of high currents while saving power. A typical shunt may be 100 mΩ. At a measured current of 1 A, the voltage produced from the shunt is 100 mV, and the amplifier error sources are not critical. However, at low measured current in the 1 mA range, the 100 μV generated across the shunt demands a very low offset voltage and drift amplifier to maintain absolute accuracy. The unique attributes of a zero-drift amplifier provides a solution. The ADA4638-1, with its input common-mode voltage that includes the lower supply rail, can be used for implementing low-side current shunt sensors.

Figure 67 shows a low-side current sensing circuit using the ADA4638-1. The ADA4638-1 is configured as a difference amplifier with a gain of 1000. Although the ADA4638-1 has high common-mode rejection, the CMR of the system is limited by the external resistors. Therefore, the key to high CMR for the system are resistors that are well matched from both the resistive ratio and relative drift, where R1/R2 = R3/R4. The resistors are important in determining the performance over manufacturing tolerances, time, and temperature.

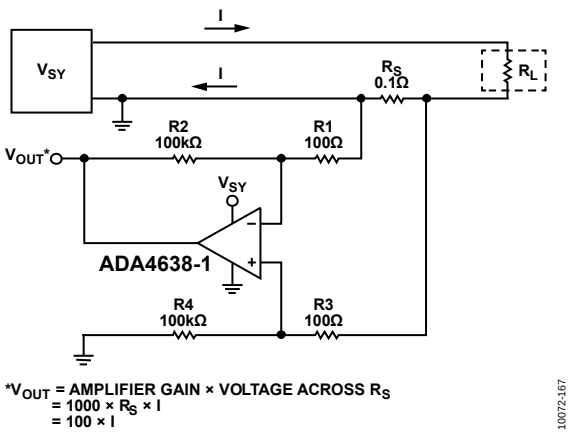

Figure 67. Low-Side Current Sensing Circuit

PRINTED CIRCUIT BOARD LAYOUT

The ADA4638-1 is a high precision device with ultralow offset voltage and offset voltage drift. Therefore, care must be taken in the design of the printed circuit board (PCB) layout to achieve optimum performance of the ADA4638-1 at board level.

To avoid leakage currents, keep the surface of the board clean and free of moisture. Coating the board surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

Properly bypassing the power supplies and keeping the supply traces short minimizes power supply disturbances caused by output current variation. Connect bypass capacitors as close as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at a distance of at least 5 mm from supply lines to minimize coupling.

A potential source of offset error is the Seebeck voltage on the circuit board. The Seebeck voltage occurs at the junction of two dissimilar metals and is a function of the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. Figure 68 shows a cross section of a surface-mount component soldered to a PCB. A variation in temperature across the board (where $T_{A1} \neq T_{A2}$) causes a mismatch in the Seebeck voltages at the solder joints thereby resulting in thermal voltage errors that degrade the performance of the ADA4638-1.

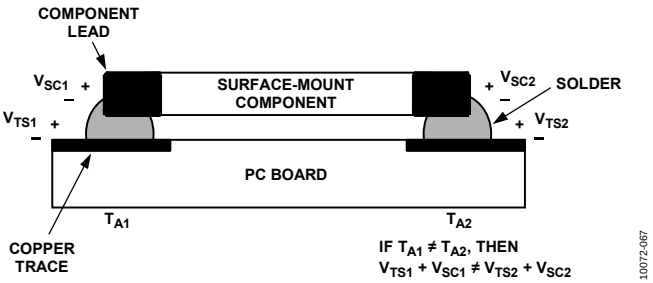

Figure 68. Mismatch in Seebeck Voltages Causes Seebeck Voltage Error

To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Where possible, the input signal paths should contain matching numbers and types of components to match the number and type of thermocouple junctions. For example, dummy components, such as zero value resistors, can be used to match the thermoelectric error source (real resistors in the opposite input path). Place matching components in close proximity and orient them in the same manner to ensure equal Seebeck voltages, thus cancelling thermal errors. Additionally, use leads that are of equal length to keep thermal conduction in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

It is highly recommended to use a ground plane. A ground plane helps distribute heat throughout the board, maintains a constant temperature across the board, and reduces EMI noise pickup.

OUTLINE DIMENSIONS

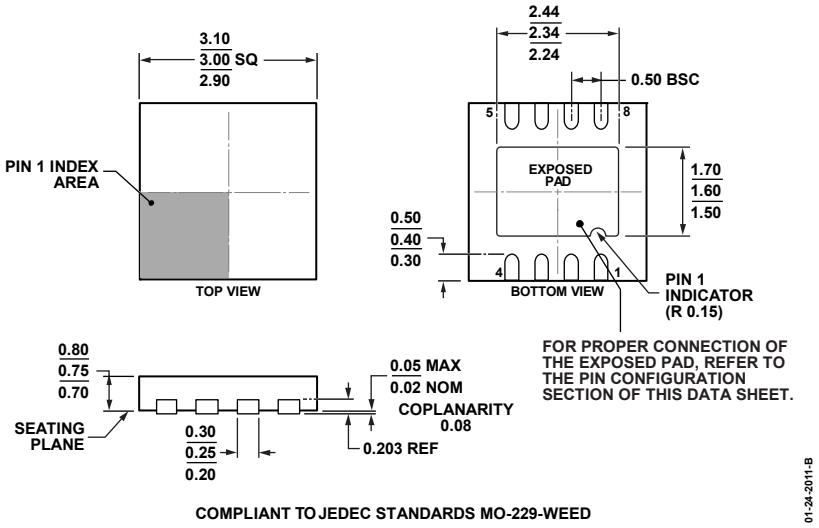

Figure 69. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-11)
Dimensions shown in millimeters

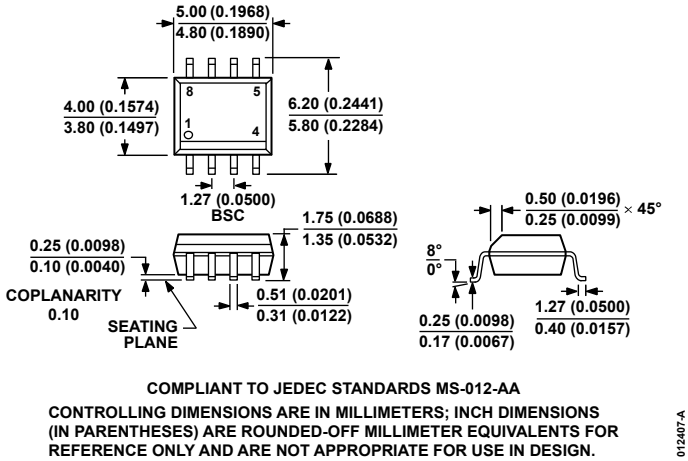

Figure 70. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4638-1ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2W
ADA4638-1ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2W
ADA4638-1ARZ	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4638-1ARZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4638-1ARZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

[1] Z = RoHS Compliant Part.

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