

FEATURES

- 1.8 V analog and digital core supply voltage**
- Correlated double sampler (CDS) with -3 dB, 0 dB, +3 dB, and +6 dB gain**
- 6 dB to 42 dB 10-bit variable gain amplifier (VGA)**
- 14-bit 65 MHz analog-to-digital converter**
- Black-level clamp with variable level control**
- Complete on-chip timing generator**
- Precision Timing™* core with 240 ps resolution @ 65 MHz**
- On-chip 3 V horizontal and RG drivers**
- General-purpose outputs (GPOs) for shutter and system support**
- 7 mm × 7 mm, 48-lead LFCSP**
- Internal LDO regulator circuitry**

APPLICATIONS

- Professional HDTV camcorders**
- Professional/high end digital cameras**
- Broadcast cameras**
- Industrial high speed cameras**

GENERAL DESCRIPTION

The AD9979 is a highly integrated CCD signal processor for high speed digital video camera applications. Specified at pixel rates of up to 65 MHz, the AD9979 consists of a complete analog front end with analog-to-digital conversion, combined with a programmable timing driver. The *Precision Timing* core allows adjustment of high speed clocks with approximately 240 ps resolution at 65 MHz operation.

The analog front end includes black-level clamping, CDS, VGA, and a 65 MSPS, 14-bit analog-to-digital converter (ADC). The timing driver provides the high speed CCD clock drivers for RG, HL, and H1 to H4. Operation is programmed using a 3-wire serial interface.

Available in a space-saving, 7 mm × 7 mm, 48-lead LFCSP, the AD9979 is specified over an operating temperature range of -25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

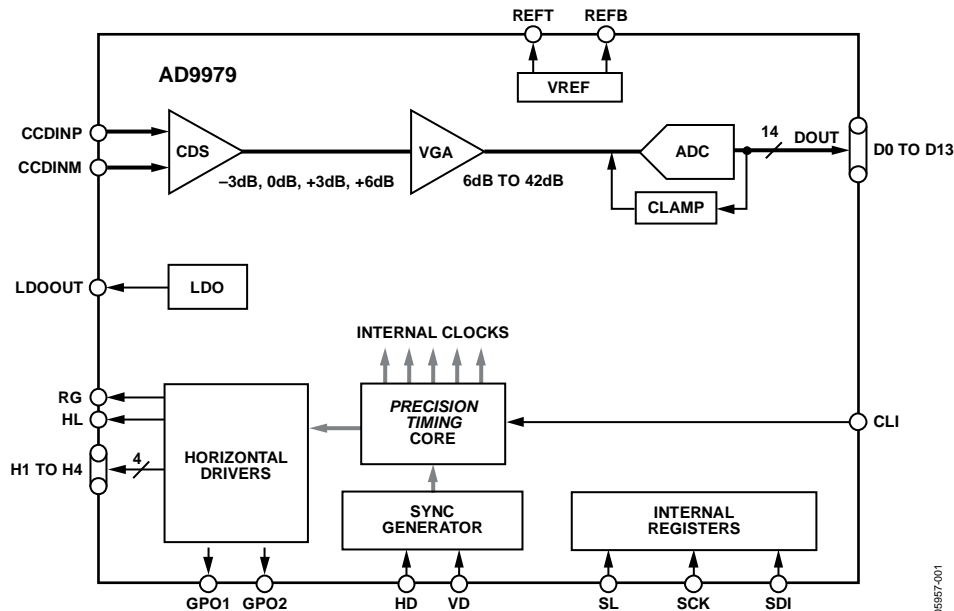


Figure 1.

Rev. C

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

| | | | |
|--|----|--|----|
| Features | 1 | Complete Field—Combining H-Patterns | 23 |
| Applications | 1 | Mode Registers | 24 |
| General Description | 1 | Horizontal Timing Sequence Example | 26 |
| Functional Block Diagram | 1 | General-Purpose Outputs (GPO) | 27 |
| Revision History | 2 | GP Look-Up Tables (LUT) | 30 |
| Specifications | 3 | Analog Front-End Description and Operation | 31 |
| Timing Specifications | 4 | Applications Information | 35 |
| Digital Specifications | 5 | Recommended Power-Up Sequence | 35 |
| Analog Specifications | 6 | Standby Mode Operation | 37 |
| Absolute Maximum Ratings | 7 | CLI Frequency Change | 37 |
| Thermal Resistance | 7 | Circuit Configuration | 38 |
| ESD Caution | 7 | Grounding and Decoupling Recommendations | 38 |
| Pin Configuration and Function Descriptions | 8 | 3-Wire Serial Interface Timing | 40 |
| Typical Performance Characteristics | 10 | Layout of Internal Registers | 41 |
| Equivalent Input/Output Circuits | 11 | Updating of New Register Values | 42 |
| Theory of Operation | 12 | Complete Register Listing | 43 |
| Programmable Timing Generation | 13 | Outline Dimensions | 54 |
| <i>Precision Timing</i> High Speed Timing Core | 13 | Ordering Guide | 54 |
| Horizontal Clamping and Blanking | 16 | | |

REVISION HISTORY

10/09—Rev. B to Rev. C

| | |
|--|---|
| Changes to Clock Rate (CLI) Parameter, Table 1 | 3 |
|--|---|

9/09—Rev. A to Rev. B

| | |
|---|----|
| Changed SCK Falling Edge to SDATA Valid Hold Parameter to SCK Rising Edge to SDATA Hold | 4 |
| Changes to Individual HBLK Patterns Section | 18 |

6/09—Rev. Sp0 to Rev. A

| | |
|---|---|
| Changes to Table 1 | 3 |
| Changes to Table 2 | 4 |
| Changes to Table 3 | 5 |
| Changes to Figure 2 | 6 |
| Changes to Table 5 and Thermal Resistance Section | 7 |

| | |
|---|----|
| Changes to Figure 3 and Table 7 | 8 |
| Changes to Figure 22 | 16 |
| Added GP_LINE_MODE Name, Table 16 | 28 |
| Changes to Figure 42 | 31 |
| Added Example Register Settings for Power-Up Section | 36 |
| Changes to Additional Restriction Section | 37 |
| Changes to Table 22, 3 V System Compatibility Section, and Grounding and Decoupling Recommendations Section | 38 |
| Changes to Table 33 | 51 |
| Changes to Table 34 | 52 |
| Added Exposed Paddle Notation to Outline Dimensions | 54 |

2/07—Revision Sp0: Initial Version

SPECIFICATIONS

Table 1.

| Parameter | Min | Typ | Max | Unit |
|--|-----|------|------|------|
| TEMPERATURE RANGE | | | | |
| Operating | −25 | | +85 | °C |
| Storage | −65 | | +150 | °C |
| POWER SUPPLY VOLTAGE | | | | |
| AVDD (AFE, Timing Core) | 1.6 | 1.8 | 2.0 | V |
| RGVDD (RG, HL Drivers) | 2.7 | 3.3 | 3.6 | V |
| HVDD (H1 to H4 Drivers) | 2.7 | 3.3 | 3.6 | V |
| DVDD (Internal Digital Supply) | 1.6 | 1.8 | 2.0 | V |
| DRVDD (Parallel Data Output Drivers) | 1.6 | 3.0 | 3.6 | V |
| IOVDD (I/O Supply Without the Use of LDO) | 1.6 | 1.8 | 3.6 | V |
| POWER SUPPLY CURRENTS—65 MHz OPERATION | | | | |
| AVDD (1.8 V) | | 48 | | mA |
| RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load) | | 8 | | mA |
| HVDD ¹ (3.3 V, 200 pF Total Load on H1 to H4) | | 40 | | mA |
| DVDD (1.8 V) | | 13 | | mA |
| DRVDD (3.0 V) | | 4 | | mA |
| IOVDD (1.8 V) | | 2 | | mA |
| POWER SUPPLY CURRENTS—STANDBY MODE OPERATION | | | | |
| Reference Standby | | 10 | | mA |
| Total Shutdown | | 0.5 | | mA |
| LDO ² | | | | |
| IOVDD (I/O Supply When Using LDO) | 2.5 | 3.0 | 3.6 | V |
| Output Voltage | 1.8 | 1.85 | 1.9 | V |
| Output Current | 60 | | | mA |
| CLOCK RATE (CLI) | 8 | | 65 | MHz |

¹The total power dissipated by the HVDD (or RGVDD) supply can be approximated using the equation

$$\text{Total HVDD Power} = [C_{\text{LOAD}} \times \text{HVDD} \times \text{Pixel Frequency}] \times \text{HVDD}$$

where C_{LOAD} is the total capacitance seen by all H outputs.

Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation.

² LDO can be used to supply AVDD and DVDD only.

AD9979

TIMING SPECIFICATIONS

$C_L = 20$ pF, $AVDD = DVDD = 1.8$ V, $f_{CLI} = 65$ MHz, unless otherwise noted.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Comments |
|---|---------------|------------------------|-----|------------------------|--------|---------------|
| MASTER CLOCK (CLI) | | | | | | See Figure 15 |
| CLI Clock Period | t_{CONV} | 15.38 | | | ns | |
| CLI High/Low Pulse Width | t_{ADC} | 6.9 | 7.7 | 8.9 | ns | |
| Delay from CLI Rising Edge to Internal Pixel Position 0 | t_{CLIDLy} | | 5 | | ns | |
| AFE | | | | | | |
| SHP Rising Edge to SHD Rising Edge | t_{S1} | 6.9 | 7.7 | 8.5 | ns | See Figure 19 |
| AFE Pipeline Delay | | | 16 | | Cycles | See Figure 20 |
| CLPOB Pulse Width (Programmable) ¹ | t_{COB} | 2 | 20 | | Pixels | |
| HD Pulse Width | t_{CONV} | | | | ns | |
| VD Pulse Width | | 1 HD period | | | ns | |
| SERIAL INTERFACE | | | | | | See Figure 56 |
| Maximum SCK Frequency | f_{SCLK} | 40 | | | MHz | |
| SL to SCK Setup Time | t_{LS} | 10 | | | ns | |
| SCK to SL Hold Time | t_{LH} | 10 | | | ns | |
| SDATA Valid to SCK Rising Edge Setup | t_{DS} | 10 | | | ns | |
| SCK Rising Edge to SDATA Hold | t_{DH} | 10 | | | ns | |
| H-COUNTER RESET SPECIFICATIONS | | | | | | See Figure 53 |
| HD Pulse Width | | t_{CONV} | | | ns | |
| VD Pulse Width | | 1 HD period | | | ns | |
| VD Falling Edge to HD Falling Edge | t_{VDHD} | 0 | | VD period – t_{CONV} | ns | |
| HD Falling Edge to CLI Rising Edge | t_{HDCLI} | 3 | | $t_{CONV} - 2$ | ns | |
| CLI Rising Edge to SHPLOC (Internal Sample Edge) | t_{CLISHP} | 3 | | $t_{CONV} - 2$ | ns | |
| TIMING CORE SETTING RESTRICTIONS | | | | | | |
| Inhibited Region for SHP Edge Location ² (See Figure 19) | t_{SHPINH} | 50 | | 64/0 | | Edge location |
| Inhibited Region for SHP or SHD with Respect to H-Clocks(See Figure 19) ^{3, 4, 5, 6} | | | | | | |
| RETIME = 0, MASK = 0 | t_{SHDINH} | $H \times NEGLOC - 15$ | | $H \times NEGLOC - 0$ | | Edge location |
| RETIME = 0, MASK = 1 | t_{SHDINH} | $H \times POSLOC - 15$ | | $H \times POSLOC - 0$ | | Edge location |
| RETIME = 1, MASK = 0 | t_{SHPINH} | $H \times NEGLOC - 15$ | | $H \times NEGLOC - 0$ | | Edge location |
| RETIME = 1, MASK = 1 | t_{SHPINH} | $H \times POSLOC - 15$ | | $H \times POSLOC - 0$ | | Edge location |
| Inhibited Region for DOUTPHASE Edge Location (See Figure 19) | $t_{DOUTINH}$ | SHDLOC + 0 | | SHDLOC + 15 | | Edge location |

¹ Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

² Only applies to slave mode operation. The inhibited area for SHP is needed to meet the timing requirements for t_{CLISHP} for proper H-counter reset operation.

³ When 0x34[2:0] HxBLKRETIME bits are enabled, the inhibit region for SHD location changes to inhibit region for SHP location.

⁴ When sequence register 0x09[23:21] HBLK masking registers are set to 0, the H-edge reference becomes $H \times NEGLOC$.

⁵ The H-clock signals that have SHP/SHD inhibit regions depends on the HCLK mode: Mode 1 = H1, Mode 2 = H1, H2, and Mode 3 = H1, H3.

⁶ These specifications apply when H1POL, H2POL, RGPOL, and HLPOL are all set to 1 (default setting).

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, $C_L = 20$ pF, t_{MIN} to t_{MAX} , unless otherwise noted.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/ Comments |
|--|-------------|---------------|-----|---------------|---------|------------------------------|
| LOGIC INPUTS | | | | | | |
| High Level Input Voltage | V_{IH} | IOVDD – 0.6 | | | V | |
| Low Level Input Voltage | V_{IL} | | | 0.6 | V | |
| High Level Input Current | I_{IH} | | 10 | | μ A | |
| Low Level Input Current | I_{IL} | | 10 | | μ A | |
| Input Capacitance | C_{IN} | | 10 | | pF | |
| LOGIC OUTPUTS | | | | | | |
| High Level Output Voltage | V_{OH} | IOVDD – 0.5 | | | V | $I_{OH} = 2$ mA |
| Low Level Output Voltage | V_{OL} | | | 0.5 | V | $I_{OL} = 2$ mA |
| CLI INPUT (CLI_BIAS = 0) | | | | | | |
| High Level Input Voltage | V_{IHCLI} | IOVDD/2 + 0.5 | | | V | |
| Low Level Input Voltage | V_{ILCLI} | | | IOVDD/2 – 0.5 | V | |
| H-DRIVER OUTPUTS | | | | | | |
| High Level Output Voltage at Maximum Current | V_{OH} | HVDD – 0.5 | | | V | |
| Low Level Output Voltage at Maximum Current | V_{OL} | | | 0.5 | V | |
| Maximum Output Current (Programmable) | | | 30 | | mA | |
| Maximum Load Capacitance | | 100 | | | pF | |

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 65 MHz, typical timing specifications, t_{MIN} to t_{MAX} , unless otherwise noted.

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|------------|------|---------|--|
| CDS¹ | | | | | |
| Allowable CCD Reset Transient | | 0.5 | 0.8 | V | |
| CDS Gain Accuracy | | | | | |
| -3.0 dB CDS Gain | -3.7 | -3.2 | -2.7 | dB | |
| 0 dB CDS Gain (Default) | -0.9 | -0.4 | +0.1 | dB | |
| +3 dB CDS Gain | +1.9 | +2.4 | +2.9 | dB | |
| +6 dB CDS Gain | +4.3 | +4.8 | +5.3 | dB | |
| Maximum Input Voltage | | | | | VGA gain = 6.3 dB, Code 15 (default value) |
| -3 dB CDS Gain | | 1.4 | | V p-p | |
| 0 dB CDS Gain (Default) | | 1.0 | | V p-p | |
| +3 dB CDS Gain | | 0.7 | | V p-p | |
| +6 dB CDS Gain | | 0.5 | | V p-p | |
| Allowable Optical Black Pixel Amplitude | | | | | |
| 0 dB CDS Gain (Default) | -100 | | +200 | mV | |
| +6 dB CDS Gain | -50 | | +100 | mV | |
| VARIABLE GAIN AMPLIFIER (VGA) | | | | | |
| Gain Control Resolution | | 1024 | | Steps | |
| Gain Monotonicity | | Guaranteed | | | |
| Low Gain Setting | | 6 | | dB | VGA Code 15 (default) |
| Maximum Gain Setting | | 42 | | dB | VGA Code 1023 |
| BLACK LEVEL CLAMP | | | | | |
| Clamp Level Resolution | | 1024 | | Steps | |
| Minimum Clamp Level (Code 0) | | 0 | | LSB | Measured at ADC output |
| Maximum Clamp Level (Code 1023) | | 1023 | | LSB | Measured at ADC output |
| ANALOG-TO-DIGITAL CONVERTER (ADC) | | | | | |
| Resolution | 14 | | | Bits | |
| Differential Nonlinearity (DNL) | -1.0 | ± 0.5 | +1.2 | LSB | |
| No Missing Codes | | Guaranteed | | | |
| Integral Nonlinearity (INL) | | 5 | 16 | LSB | |
| Full-Scale Input Voltage | | 2.0 | | V | |
| VOLTAGE REFERENCE | | | | | |
| Reference Top Voltage (REFT) | | 1.4 | | V | |
| Reference Bottom Voltage (REFB) | | 0.4 | | V | |
| SYSTEM PERFORMANCE | | | | | |
| VGA Gain Accuracy | | | | | Specifications include entire signal chain |
| Low Gain (Code 15) | 5.1 | 5.6 | 6.1 | dB | 0 dB CDS gain (default) |
| Maximum Gain (Code 1023) | 41.3 | 41.8 | 42.3 | dB | Gain = (0.0359 × code) + 5.1 dB |
| Peak Nonlinearity, 500 mV Input Signal | | 0.1 | 0.4 | % | 12 dB total gain applied |
| Total Output Noise | | 2 | | LSB rms | AC grounded input, 6 dB gain applied |
| Power Supply Rejection (PSR) | | 45 | | dB | Measured with step change on supply |

¹ Input signal characteristics are defined as shown in Figure 2.

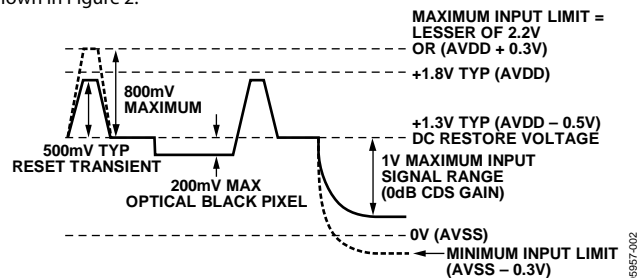


Figure 2. Input Signal Characteristics

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | With Respect To | Rating |
|----------------------------|-----------------|-------------------------|
| AVDD | AVSS | -0.3 V to +2.2 V |
| DVDD | DVSS | -0.3 V to +2.2 V |
| DRVDD | DRVSS | -0.3 V to +3.9 V |
| IOVDD | DVSS | -0.3 V to +3.9 V |
| HVDD | HVSS | -0.3 V to +3.9 V |
| RGVDD | RGVSS | -0.3 V to +3.9 V |
| Any VSS | Any VSS | -0.3 V to +0.3 V |
| RG Output | RGVSS | -0.3 V to RGVDD + 0.3 V |
| H1 to H4, HL Output | HVSS | -0.3 V to HVDD + 0.3 V |
| SCK, SL, SDI | DVSS | -0.3 V to IOVDD + 0.3 V |
| REFT, REFB, CCDINM, CCDINP | AVSS | -0.2 V to AVDD + 0.2 V |
| Junction Temperature | | 150°C |
| Lead Temperature (10 sec) | | 350°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is measured using a 4-layer printed circuit board (PCB) with the exposed paddle soldered to the board.

Table 6.

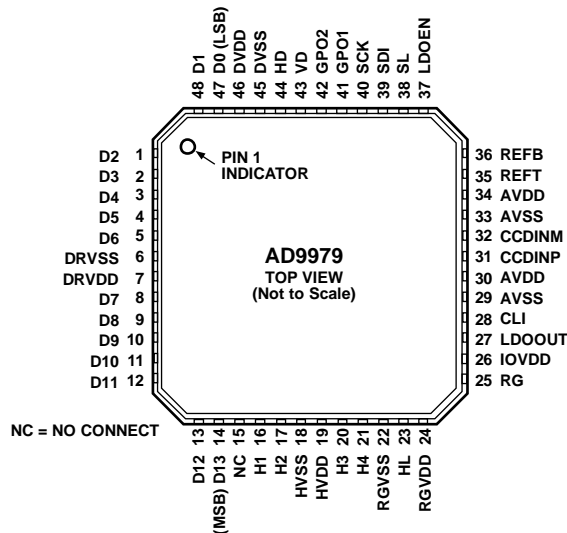
| Package Type | θ_{JA} | Unit |
|----------------------------|---------------|------|
| 48-Lead, 7 mm × 7 mm LFCSP | 25.8 | °C/W |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
 1. THE EXPOSED PAD MUST BE CONNECTED TO GND.

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|-----------|-------------------|---|
| 1 | D2 | DO | Data Output |
| 2 | D3 | DO | Data Output |
| 3 | D4 | DO | Data Output |
| 4 | D5 | DO | Data Output |
| 5 | D6 | DO | Data Output |
| 6 | DRVSS | P | Digital Driver Ground |
| 7 | DRVDD | P | Digital Driver Supply (1.8 V or 3 V) |
| 8 | D7 | DO | Data Output |
| 9 | D8 | DO | Data Output |
| 10 | D9 | DO | Data Output |
| 11 | D10 | DO | Data Output |
| 12 | D11 | DO | Data Output |
| 13 | D12 | DO | Data Output |
| 14 | D13 (MSB) | DO | Data Output |
| 15 | NC | | Not Connected |
| 16 | H1 | DO | CCD Horizontal Clock 1 |
| 17 | H2 | DO | CCD Horizontal Clock 2 |
| 18 | HVSS | P | H1 to H4 Driver Ground |
| 19 | HVDD | P | H1 to H4 Driver Supply (3 V) |
| 20 | H3 | DO | CCD Horizontal Clock 3 |
| 21 | H4 | DO | CCD Horizontal Clock 4 |
| 22 | RGVSS | P | RG Driver Ground |
| 23 | HL | DO | CCD Last Horizontal Clock |
| 24 | RGVDD | P | RG Driver Supply (3 V) |
| 25 | RG | DO | CCD Reset Gate Clock |
| 26 | IOVDD | P | Digital I/O Supply (1.8 V or 3 V)/LDO Input Voltage (3 V) |
| 27 | LDOOUT | P | LDO Output Voltage (1.8 V) |

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|----------|-------------------|---|
| 28 | CLI | DI | Master Clock Input |
| 29 | AVSS | P | Analog Ground for AFE |
| 30 | AVDD | P | Analog Supply for AFE (1.8 V) |
| 31 | CCDINP | AI | CCD Signal Positive Input |
| 32 | CCDINM | AI | CCD Signal Negative Input; Normally Tied to AVSS |
| 33 | AVSS | P | Analog Ground for AFE |
| 34 | AVDD | P | Analog Supply for AFE (1.8 V) |
| 35 | REFT | AO | Reference Top Decoupling (Decouple with 1.0 μ F to AVSS) |
| 36 | REFB | AO | Reference Bottom Decoupling (Decouple with 1.0 μ F to AVSS) |
| 37 | LDOEN | DI | LDO Output Enable; 3 V = LDO Enabled, GND = LDO Disabled |
| 38 | SL | DI | 3-Wire Serial Load |
| 39 | SDI | DI | 3-Wire Serial Data Input |
| 40 | SCK | DI | 3-Wire Serial Clock |
| 41 | GPO1 | DIO | General-Purpose Input/Output 1 |
| 42 | GPO2 | DIO | General-Purpose Input/Output 2 |
| 43 | VD | DI | Vertical Sync Pulse |
| 44 | HD | DI | Horizontal Sync Pulse |
| 45 | DVSS | P | Digital Ground |
| 46 | DVDD | P | Digital Supply (1.8 V) |
| 47 | D0 (LSB) | DO | Data Output |
| 48 | D1 | DO | Data Output |
| | EPAD | | The exposed pad must be connected to GND. |

¹ AI = analog input, AO = analog output, DI = digital input, DO = digital output, DIO = digital input/output, P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

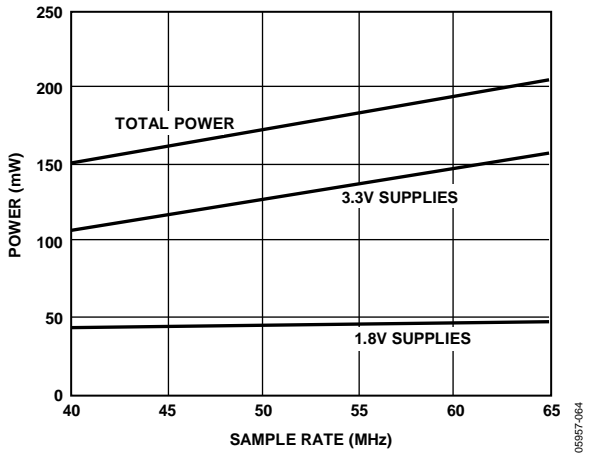


Figure 4. Power vs. Sample Rate

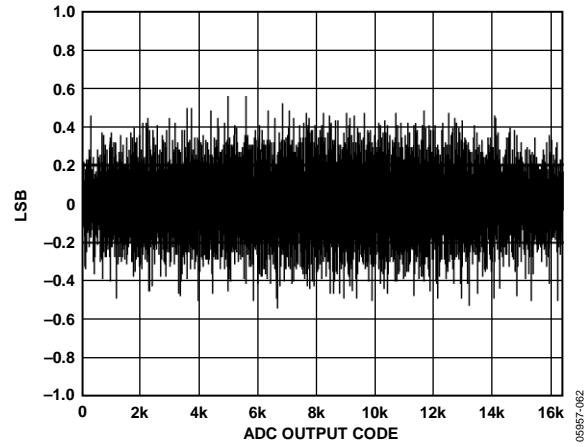


Figure 6. Differential Nonlinearity (DNL)

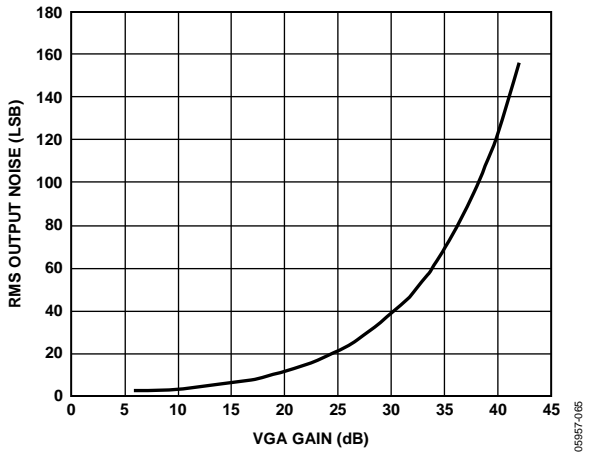


Figure 5. RMS Output Noise vs. VGA Gain

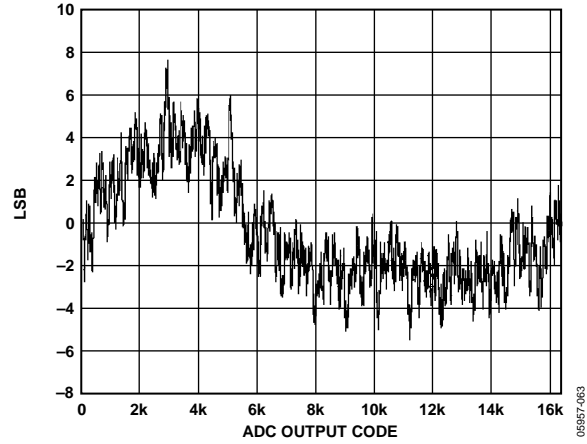


Figure 7. System Integral Nonlinearity (INL)

EQUIVALENT INPUT/OUTPUT CIRCUITS

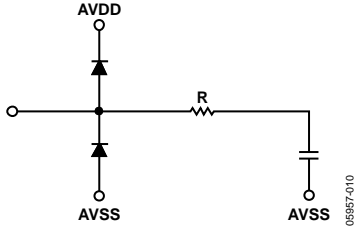


Figure 8. CCD Input

06957-010

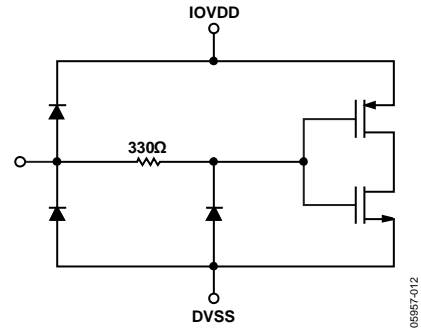


Figure 10. Digital Inputs

06957-012

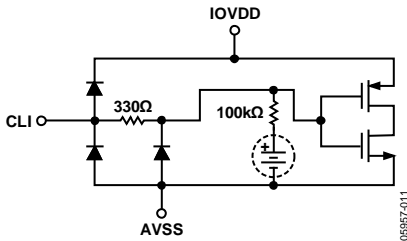


Figure 9. CLI Input, Register 0x15[0] = 1 Enables the Bias Circuit

06957-011

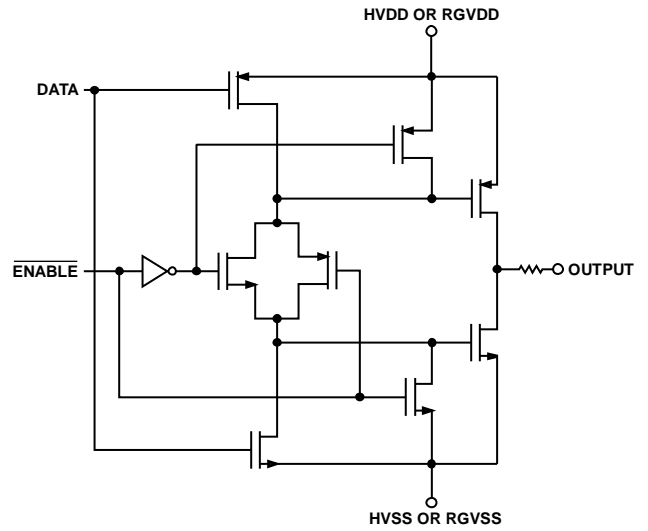


Figure 11. H1 to H4, HL, and RG Outputs

06957-013

THEORY OF OPERATION

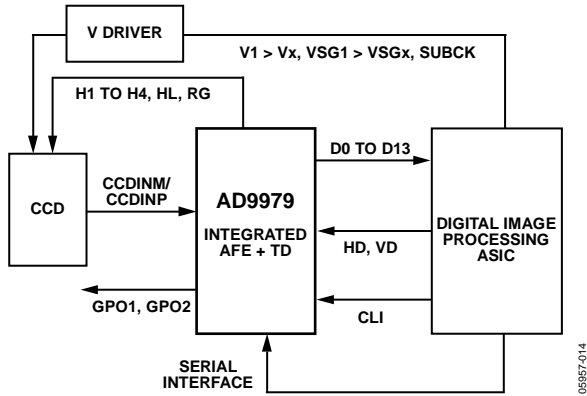


Figure 12. Typical Application

Figure 12 shows the typical application for the AD9979. The CCD output is processed by the AFE circuitry of the AD9979, which consists of a CDS, a VGA, a black-level clamp, and an ADC. The digitized pixel information is sent to the digital image processor chip, which performs the post-processing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9979 from the system ASIC, through the 3-wire serial interface. From the system master clock, CLI, provided by the image processor or an external crystal, the AD9979 generates the horizontal clocks of the CCD and all internal AFE clocks.

All AD9979 clocks are synchronized with VD and HD inputs. All of the horizontal pulses (CLPOB, PBLK, and HBLK) of the AD9979 are programmed and generated internally.

The H drivers for H1 to H4 and RG are included in the AD9979, allowing these clocks to be directly connected to the CCD. The H-drive voltage of 3 V is supported in the AD9979.

Figure 13 and Figure 14 show the maximum horizontal and vertical counter dimensions for the AD9979. These counters control all internal horizontal and vertical clocking, to specify line and pixel locations. The maximum HD length is 8191 pixels per line, and the maximum VD length is 8192 lines per field.

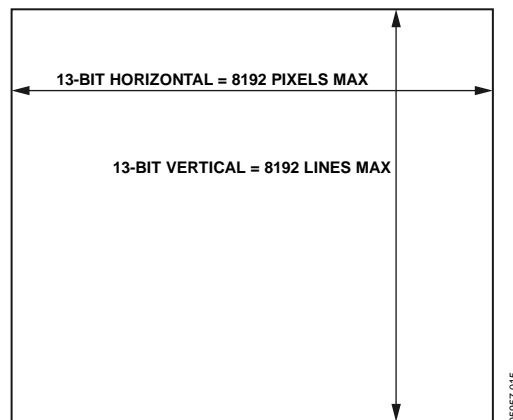


Figure 13. Maximum Dimensions for Vertical and Horizontal Counters

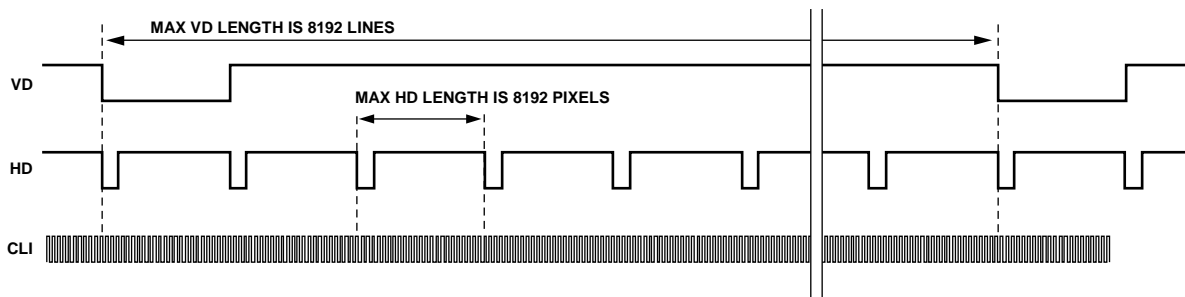


Figure 14. Maximum VD and HD Dimensions

PROGRAMMABLE TIMING GENERATION

PRECISION TIMING HIGH SPEED TIMING CORE

The AD9979 generates flexible high speed timing signals using the *Precision Timing* core. This core is the foundation for generating the timing for both the CCD and the AFE; the reset gate (RG), the HL, Horizontal Driver H1 to Horizontal Driver H4, and the SHP and SHD sample clocks. A unique architecture makes it routine for the system designers to optimize image quality by providing precise control over the horizontal CCD readout and the AFE-correlated double sampling.

Timing Resolution

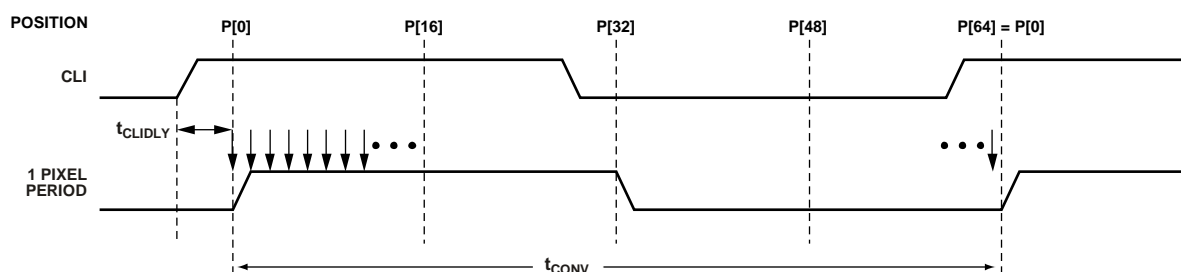
The *Precision Timing* core uses a master clock input (CLI) as a reference. This clock is recommended to be the same as the CCD pixel clock frequency. Figure 15 illustrates how the internal timing core divides the master clock period into 64 steps, or edge positions. Therefore, the edge resolution of the *Precision Timing* core is $t_{CLI}/64$. (For more information on using the CLI input, refer to the Applications Information section.)

Using a 65 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 240 ps. If a 1x system clock is not available, it is also possible to use a 2x reference clock, by programming the CLIDIVIDE register (Address 0x0D). The AD9979 then internally divides the CLI frequency by 2.

High Speed Clock Programmability

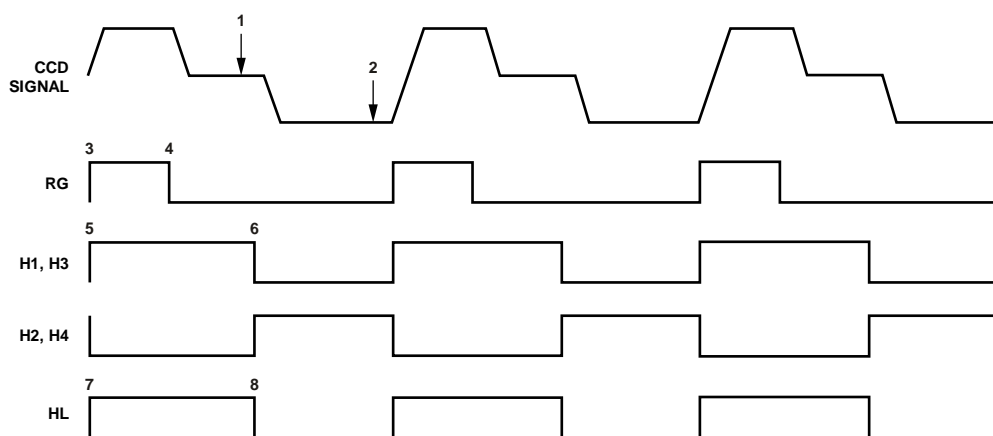
Figure 16 shows how the high speed clocks, RG, HL, H1 to H4, SHP, and SHD, are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. The HL, H1, and H2 horizontal clocks have separate programmable rising and falling edges and polarity control. The AD9979 provides additional HCLK mode programmability, see Table 8.

The edge location registers are each six bits wide, allowing the selection of all 64 edge locations. Figure 19 shows the default timing locations for all of the high speed clock signals.



- NOTES
 1. THE PIXEL CLOCK PERIOD IS DIVIDED INTO 64 POSITIONS, PROVIDING FINE EDGE RESOLUTION FOR HIGH SPEED CLOCKS.
 2. THERE IS A FIXED DELAY FROM THE CLI INPUT TO THE INTERNAL PIXEL PERIOD POSITION (t_{CLIDLy}).

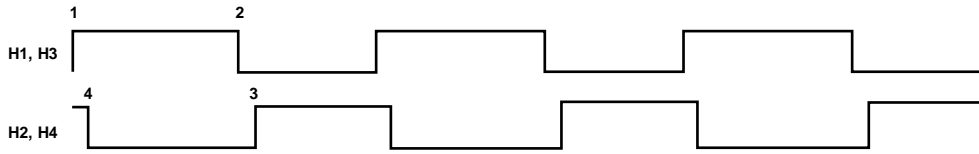
Figure 15. High Speed Clock Resolution From CLI Master Clock Input



- PROGRAMMABLE CLOCK POSITIONS:
 1 SHP SAMPLE LOCATION.
 2 SHD SAMPLE LOCATION.
 3 RG RISING EDGE.
 4 RG FALLING EDGE.
 5 H1 RISING EDGE.
 6 H1 FALLING EDGE.
 7 HL RISING EDGE.
 8 HL FALLING EDGE.

Figure 16. High Speed Clock Programmable Locations (HCLKMODE = 1)

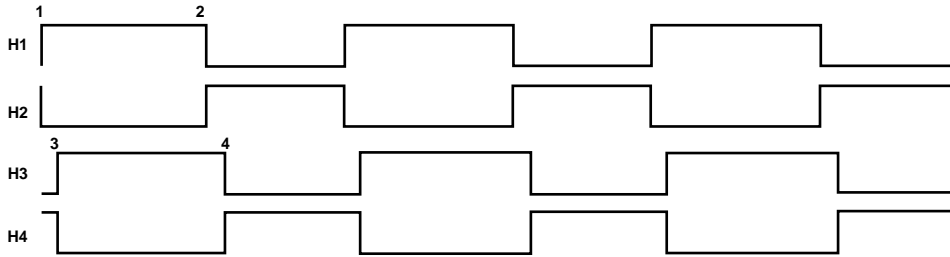
06957-018



H1 TO H4 PROGRAMMABLE LOCATIONS:
 1H1 RISING EDGE.
 2H1 FALLING EDGE.
 3H2 RISING EDGE.
 4H2 FALLING EDGE.

05957-019

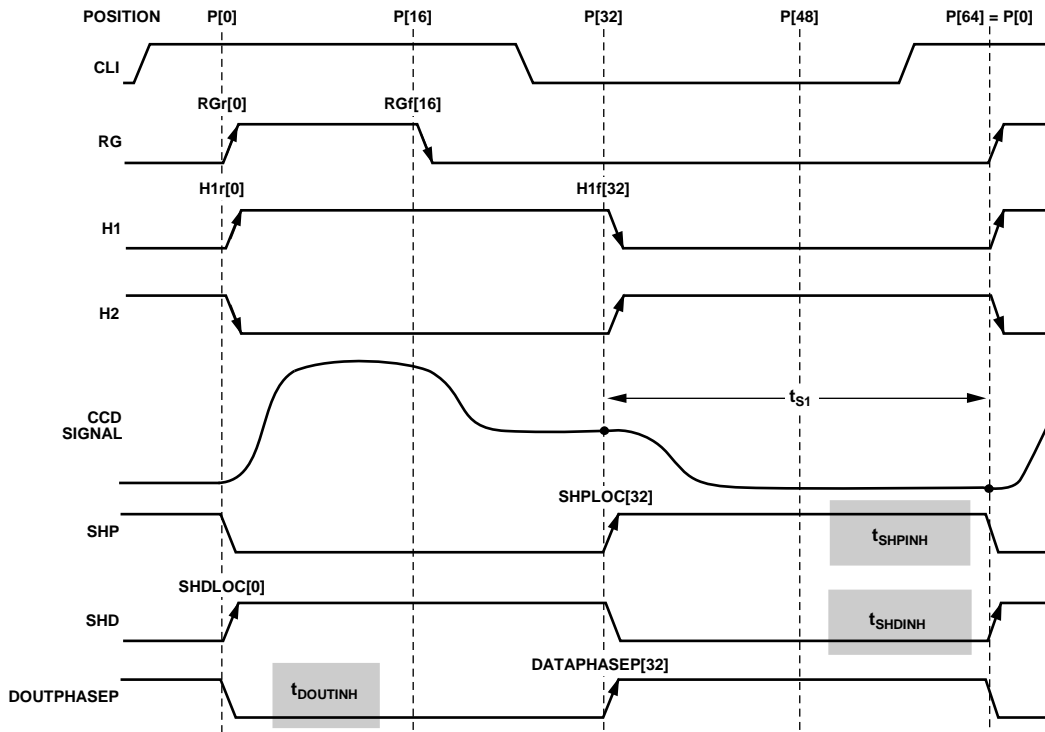
Figure 17. HCLK Mode 2 Operation



H1 TO H4 PROGRAMMABLE LOCATIONS:
 1H1 RISING EDGE.
 2H1 FALLING EDGE.
 3H3 RISING EDGE.
 4H3 FALLING EDGE.

05957-020

Figure 18. HCLK Mode 3 Operation



NOTES
 1. ALL SIGNAL EDGES ARE FULLY PROGRAMMABLE TO ANY OF THE 64 POSITIONS WITHIN 1 PIXEL PERIOD. TYPICAL POSITIONS FOR EACH SIGNAL ARE SHOWN. HCLK MODE 1 IS SHOWN.
 2. CERTAIN POSITIONS MUST BE AVOIDED FOR EACH SIGNAL, SHOWN ABOVE AS INHIBIT REGIONS.
 3. IF A SETTING IN THE INHIBIT REGION IS USED, AN UNSTABLE PIXEL SHIFT CAN OCCUR IN THE HBLK LOCATION OR AFE PIPELINE.

05957-021

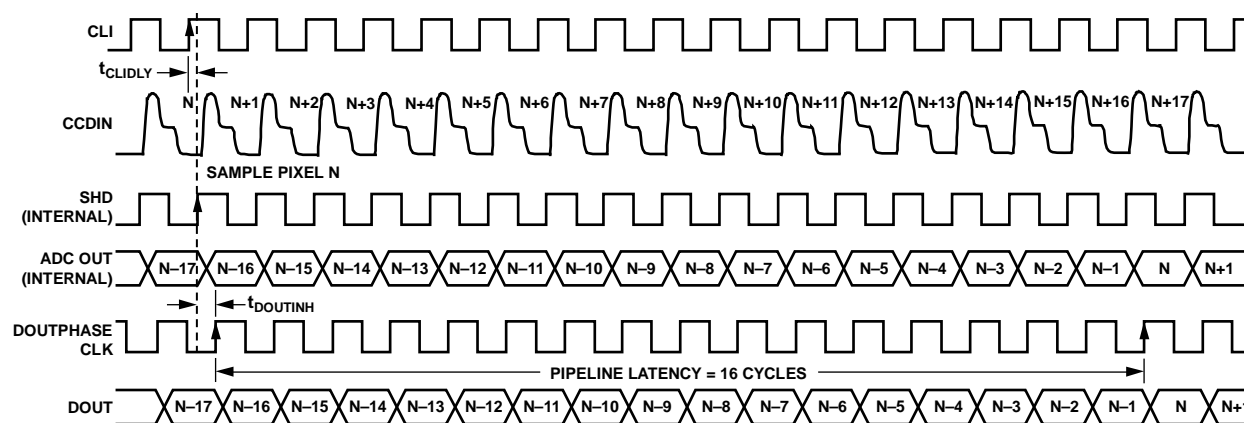
Figure 19. High Speed Timing Default Locations

Table 8. HCLK Modes (Selected by Register Address 0x23, Bits[7:5])

| HCLK Mode | Register Value | Description |
|-------------------|-------------------------|--|
| Mode 1 | 001 | H1 edges are programmable; H3 = H1, H2 = H4 = inverse of H1. |
| Mode 2 | 010 | H1 edges are programmable; H3 = H1. H2 edges are programmable; H4 = H2. |
| Mode 3 | 100 | H1 edges are programmable; H2 = inverse of H1. H3 edges are programmable; H4 = inverse of H3. |
| Invalid Selection | 000, 011, 101, 110, 111 | Invalid register settings. |

Table 9. Horizontal Clock, RG, Drive, and Sample Control Registers Parameters

| Name | Length | Range | Description |
|-----------------|--------|-------------------------|--|
| Polarity | 1 bit | High/low | Polarity control for H1/H3 and RG; 0 = no inversion, 1 = inversion |
| Positive Edge | 6 bits | 0 to 63 edge location | Positive edge location for H1/H3 and RG |
| Negative Edge | 6 bits | 0 to 63 edge location | Negative edge location for H1/H3 and RG |
| Sample Location | 6 bits | 0 to 63 sample location | Sampling location for SHP and SHD |
| Drive Control | 3 bits | 0 to 7 current steps | Drive current for H1 to H4 and RG outputs (4.3 mA steps) |



NOTES

- EXAMPLE SHOWN FOR SHDLOC = 0.
- HIGHER VALUES OF SHD AND/OR DOUTPHASE SHIFT DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.

Figure 20. Pipeline Delay of AFE Data Outputs

06987-022

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9979 features on-chip output drivers for the HL, RG, and H1 to H4 outputs. These drivers are powerful enough to directly drive the CCD inputs. The H-driver and RG-driver currents can be adjusted for optimum rise/fall times into a particular load by using the drive strength control register (Address 0x35). Use the register to adjust the drive strength in 4.3 mA increments. The minimum setting of 0 is equal to off or three-state, and the maximum setting of 7 is equal to 30.1 mA.

Digital Data Outputs

For maximum system flexibility, the AD9979 uses DOUTPHASEN and DOUTPHASEP (Address 0x37, Bits[11:0]) to select the location for the start of each new pixel data value. Any edge location from 0 to 63 can be programmed. Register 0x37 determines the start location of the data output and the DOUTPHASEx clock rising edge with respect to the master clock input CLI.

The pipeline delay through the AD9979 is shown in Figure 20. After the CCD input is sampled by SHD, there is a 16-cycle delay before the data is available.

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9979 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK during the different regions of each field. This allows the dark-pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate the different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 21. These two signals are independently programmed using the registers in Table 10. The start polarity for the CLPOB (PBLK) signal is CLPOB_POL (PBLK_POL), and the first and second toggle positions of the pulse are CLPOBx_TOG1 (PBLKx_TOG1) and CLPOBx_TOG2 (PBLKx_TOG2), respectively. Both signals are active low and need to be programmed accordingly.

Two separate patterns for CLPOB and PBLK can be programmed for each H-pattern, CLPOB0, CLPOB1, PBLK0, and PBLK1. The CLPOB_PAT and PBLK_PAT field registers select which of the two patterns are used in each field.

Figure 32 shows how the sequence change positions divide the readout field into different regions. By assigning a different H-pattern to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Area

Additionally, the AD9979 allows the CLPOB and PBLK signals to be disabled during certain lines in the field, without changing any of the existing pattern settings. There are three sets of start and end registers for both CLPOB and PBLK that allows the creation of up to three masking areas for each signal.

For example, to use the CLPOB masking, program the CLPOBMASKSTARTx and CLPOBMASKENDx registers to specify the starting and ending lines in the field where the CLPOB patterns are to be ignored. Figure 22 illustrates this feature.

The masking registers are not specific to a certain H-pattern; they are always active for any existing field of timing. To disable the CLPOB and PBLK masking feature, set these registers to the maximum value of 0x1FFF.

Note that to disable CLPOB and PBLK masking during power-up, it is recommended to set CLPOBMASKSTARTx (PBLKMASKSTARTx) to 8191 and CLPOBMASKENDx (PBLKMASKENDx) to 0. This prevents any accidental masking caused by different register update events.

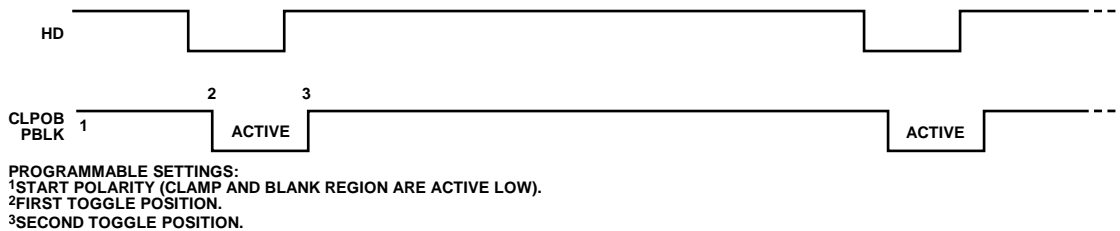


Figure 21. Clamp and Preblank Pulse Placement

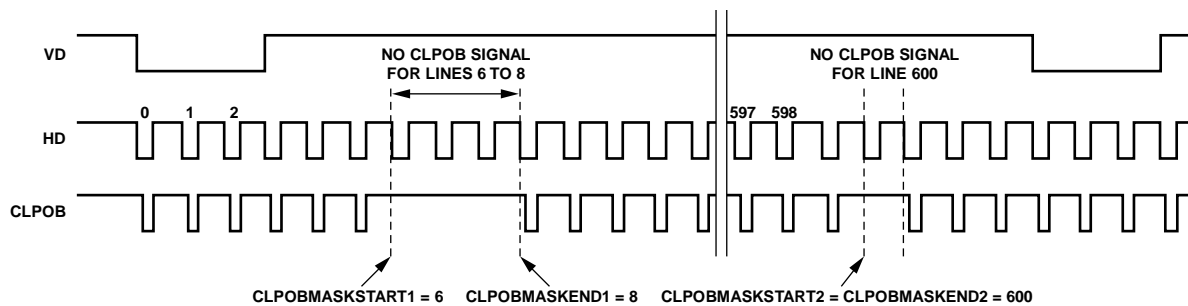


Figure 22. CLPOB Masking Example

Table 10. CLPOB and PBLK Registers

| Name | Length | Range | Description |
|-----------------|---------|--------------------------|---|
| CLPOB0_TOG1 | 13 bits | 0 to 8191 pixel location | First CLPOB0 toggle position within the line for each V-sequence. |
| CLPOB0_TOG2 | 13 bits | 0 to 8191 pixel location | Second CLPOB0 toggle position within the line for each V-sequence. |
| CLPOB1_TOG1 | 13 bits | 0 to 8191 pixel location | First CLPOB1 toggle position within the line for each V-sequence. |
| CLPOB1_TOG2 | 13 bits | 0 to 8191 pixel location | Second CLPOB1 toggle position within the line for each V-sequence. |
| CLPOB_POL | 9 bits | High/low | Starting polarity of CLPOB for each V-sequence[8:0] (in field registers). |
| CLPOB_PAT | 9 bits | 0 to 9 settings | CLPOB pattern selection for each V-sequence[8:0] (in field registers). |
| CLPOBMASKSTARTx | 13 bits | 0 to 8191 pixel location | CLPOB mask start position. Three values available (in field registers). |
| CLPOBMASKENDx | 13 bits | 0 to 8191 pixel location | CLPOB mask end position. Three values available (in field registers). |
| PBLK0_TOG1 | 13 bits | 0 to 8191 pixel location | First PBLK0 toggle position within the line for each V-sequence. |
| PBLK0_TOG2 | 13 bits | 0 to 8191 pixel location | Second PBLK0 toggle position within the line for each V-sequence. |
| PBLK1_TOG1 | 13 bits | 0 to 8191 pixel location | First PBLK1 toggle position within the line for each V-sequence. |
| PBLK1_TOG2 | 13 bits | 0 to 8191 pixel location | Second PBLK1 toggle position within the line for each V-sequence. |
| PBLK_POL | 9 bits | High/low | Starting polarity of PBLK for each V-sequence[8:0] (in field registers). |
| PBLK_PAT | 9 bits | 0 to 9 settings | PBLK pattern selection for each V-sequence[8:0] (in field registers). |
| PBLKMASKSTARTx | 13 bits | 0 to 8191 pixel location | PBLK mask start position. Three values available (in field registers). |
| PBLKMASKENDx | 13 bits | 0 to 8191 pixel location | PBLK mask end position. Three values available (in field registers). |

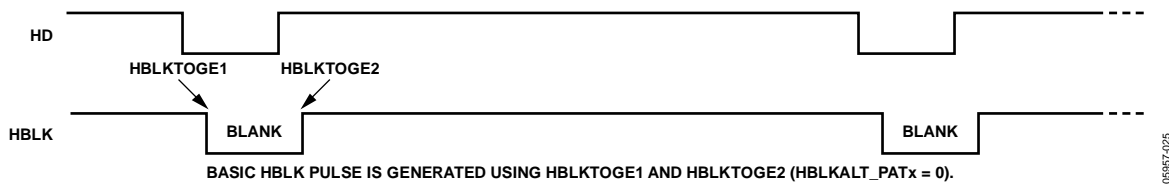


Figure 23. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

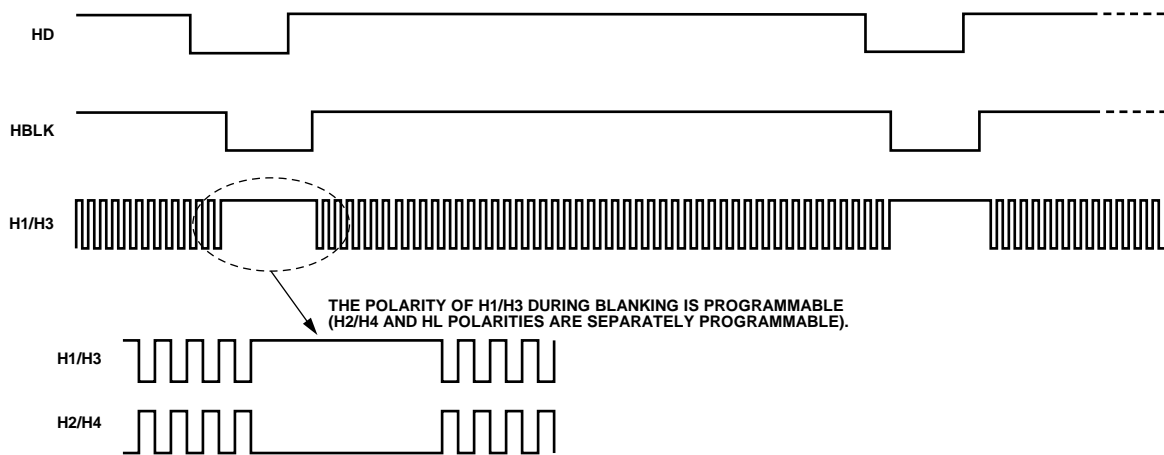


Figure 24. HBLK Masking Control

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 23 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions designate the start and the stop positions of the blanking period. Additionally, as shown in Figure 24, there is a polarity control, HBLKMASK, for H1/H3 and H2/H4 that designates the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 low sets H1 = H3 = low and HBLKMASK_H2 high sets H2 = H4 = high during the blanking. As with the CLPOB and PBLK signals, HBLK registers are available in each H-pattern group, allowing unique blanking signals to be used with different vertical timing sequences.

The AD9979 supports three different modes for HBLK operation. HBLK Mode 0 supports basic operation and offers some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode. Register names are detailed in Table 11.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 25. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns are created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, load the same values into both the HBLKTOGEx and HBLKTOGOx registers.

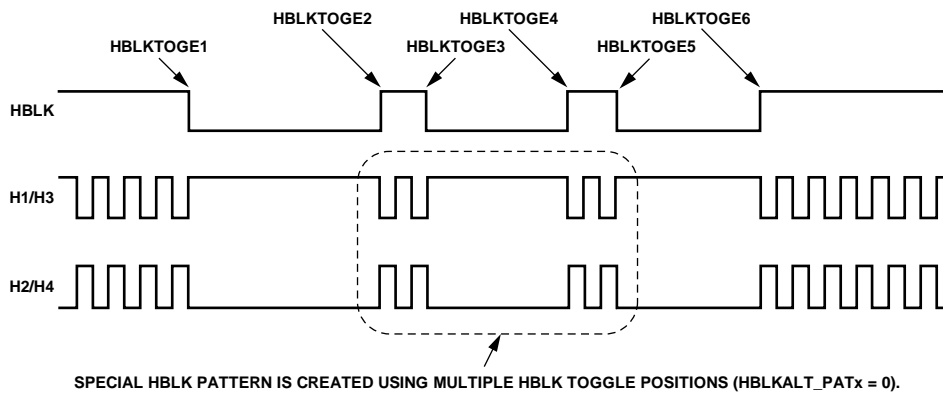


Figure 25. Generating Special HBLK Patterns

Table 11. HBLK Pattern Registers

| Name | Length | Range | Description |
|-------------|---------|--------------------------|--|
| HBLKMODE | 2 bits | 0 to 2 | Enables different HBLK toggle position operation. 0 = normal mode. Six toggle positions are available for even and odd lines. If even/odd alternation is not need, set the toggle positions for the even/odd the same. 1 = pixel mixing mode. Instead of only six toggle positions, use the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers, along with HBLKTOGOx and HBLKTOGEx. If even/odd alternation is not need, set the even/odd toggles the same. 2 = advanced HBLK mode. It divides HBLK interval into six different repeat areas. It uses HBLKSTARTA, HBLKSTARTB, HBLKSTARTC, and RAXHyREPA/RAXHyREPB/RAXHyREPC registers. 3 = test mode. Do not access. |
| HBLKSTART | 13 bits | 0 to 8191 pixel location | Start location for HBLK in HBLK Mode 1 and HBLK Mode 2. |
| HBLKEND | 13 bits | 0 to 8191 pixel location | End location for HBLK in HBLK Mode 1 and HBLK Mode 2. |
| HBLKLEN | 13 bits | 0 to 8191 pixels | HBLK length in HBLK Mode 1 and HBLK Mode 2. |
| HBLKREP | 13 bits | 0 to 8191 repetitions | Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2. |
| HBLKMASK_H1 | 1 bit | High/low | Masking polarity for H1/H3 during HBLK. |
| HBLKMASK_H2 | 1 bit | High/low | Masking polarity for H2/H4 during HBLK. |
| HBLKMASK_HL | 1 bit | High/low | Masking polarity for HL during HBLK. |

| Name | Length | Range | Description |
|---------------------------|---------|--------------------------|---|
| HBLKTOGO1 | 13 bits | 0 to 8191 pixel location | First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO2 | 13 bits | 0 to 8191 pixel location | Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO3 | 13 bits | 0 to 8191 pixel location | Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO4 | 13 bits | 0 to 8191 pixel location | Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO5 | 13 bits | 0 to 8191 pixel location | Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGO6 | 13 bits | 0 to 8191 pixel location | Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE1 | 13 bits | 0 to 8191 pixel location | First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE2 | 13 bits | 0 to 8191 pixel location | Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE3 | 13 bits | 0 to 8191 pixel location | Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE4 | 13 bits | 0 to 8191 pixel location | Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE5 | 13 bits | 0 to 8191 pixel location | Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| HBLKTOGE6 | 13 bits | 0 to 8191 pixel location | Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1. |
| RAXHyREPz ¹ | 12 bits | 0 to 15 HCLK pulses | HBLK Mode 2 even field Repeat Area x. Number of Hy repetitions for HBLKSTARTz even lines. ² Bits[3:0]: number of Hy pulses following HBLKSTARTA. Bits[7:4]: number of Hy pulses following HBLKSTARTB. Bits[11:8]: number of Hy pulses following HBLKSTARTC. |
| HBLKSTARTA | 13 bits | 0 to 8191 pixel location | HBLK Repeat Area Start Position A for HBLK Mode 2. |
| HBLKSTARTB | 13 bits | 0 to 8191 pixel location | HBLK Repeat Area Start Position B for HBLK Mode 2. |
| HBLKSTARTC | 13 bits | 0 to 8191 pixel location | HBLK Repeat Area Start Position C for HBLK Mode 2. |
| HBLKALT_PATx ³ | 3 bits | 0 to 5 even repeat area | HBLK Mode 2 odd field Repeat Area x pattern. Selected from even field repeat areas. ⁴ |

¹ The variable x represents the repeat area, from 0 to 5. The variable y represents the horizontal driver, 1 or 2. The variable z represents the HBLK repeat area start position for HBLK Mode 2, A, B, or C.

² Odd lines defined using HBLKALT_PATx.

³ The variable x represents the repeat area, from 0 to 5.

⁴ Even lines defined using RAXHyREPz; also see Note 1.

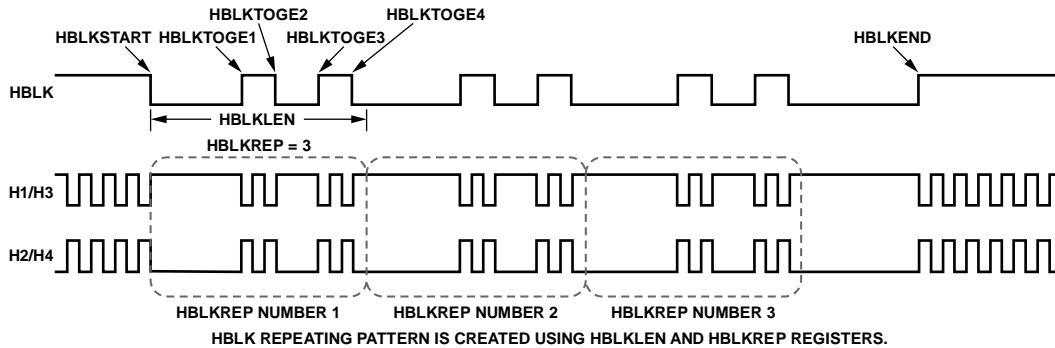


Figure 26. HBLK Repeating Pattern Using HBLK Mode 1 (Register Value = 1)

06957-028

HBLK Mode 1 Operation

Multiple repeats of the HBLK signal can be enabled by setting HBLKMODE to 1. In this mode, the HBLK pattern is generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 26).

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate HBLK toggle positions on even and odd lines for which separate toggle positions are available. If even/odd line alternation is not required, load the same values into the registers for the even lines (HBLKTOGEx) as the odd (HBLKTOGOx) lines.

Increasing Horizontal Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H4 pulse width to increase during the HBLK interval. As shown in Figure 27, the horizontal clock frequency can reduce by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30 (see Table 12). To enable this feature, the HCLK_WIDTH register (Address 0x34, Bits[7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled.

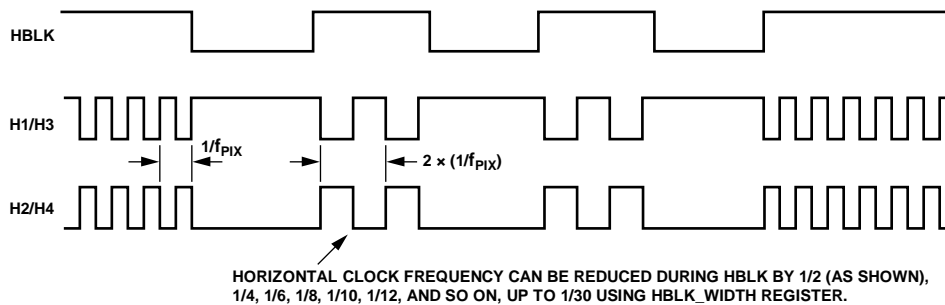
The reduced frequency occurs only for H1 to H4 pulses that are located within the HBLK area.

The HCLK_WIDTH feature is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1, and not in HBLK Mode 2.

Table 12. HCLK Width Register

| Name | Length | Description |
|------------|--------|--|
| HCLK_WIDTH | 4 bits | <p>Controls H1 to H4 width during HBLK as a fraction of pixel rate.</p> <p>0 = same frequency as pixel rate</p> <p>1 = 1/2 pixel frequency, that is, doubles the HCLK pulse width</p> <p>2 = 1/4 pixel frequency</p> <p>3 = 1/6 pixel frequency</p> <p>4 = 1/8 pixel frequency</p> <p>5 = 1/10 pixel frequency</p> <p>6 = 1/12 pixel frequency</p> <p>7 = 1/14 pixel frequency</p> <p>8 = 1/16 pixel frequency</p> <p>9 = 1/18 pixel frequency</p> <p>10 = 1/20 pixel frequency</p> <p>11 = 1/22 pixel frequency</p> <p>12 = 1/24 pixel frequency</p> <p>13 = 1/26 pixel frequency</p> <p>14 = 1/28 pixel frequency</p> <p>15 = 1/30 pixel frequency</p> |



HORIZONTAL CLOCK FREQUENCY CAN BE REDUCED DURING HBLK BY 1/2 (AS SHOWN), 1/4, 1/6, 1/8, 1/10, 1/12, AND SO ON, UP TO 1/30 USING HCLK_WIDTH REGISTER.

Figure 27. Generating Wide Horizontal Clock Pulses During HBLK Interval

05957 4/23

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If unevenly spaced, multiple areas of HCLK pulses are needed; therefore, use HBLK Mode 2. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six different repeat areas (see Table 11). As shown in Figure 28, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC position can be unique in each repeat area by using RAXHyREPz, where x represents the repeat area, from 0 to 5, y represents the horizontal driver, 1 or 2, and z represents the HBLK repeat area start position for HBLK Mode 2, A, B, or C. As shown in Figure 29, setting the RAXH1REPA/RAXH1REPB/RAXH1REPC or RAXH2REPA/RAXH2REPB/RAXH2REPC registers to 0 masks the HCLK groups from appearing in a particular repeat area. Figure 28 shows only two repeat areas being used, although up to six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally, the same value is used for both H1 and H2.

Figure 28 shows the example

RA0H1REPA/RA0H1REPB/RA0H1REPC =
 RA0H2REPA/RA0H2REPB/RA0H2REPC =
 RA1H1REPA/RA1H1REPB/RA1H1REPC =
 RA1H2REPA/RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC, as well as RAXH1REPA/RAXH1REPB/RAXH1REPC and RAXH2REPA/RAXH2REPB/RAXH2REPC, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PATx registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

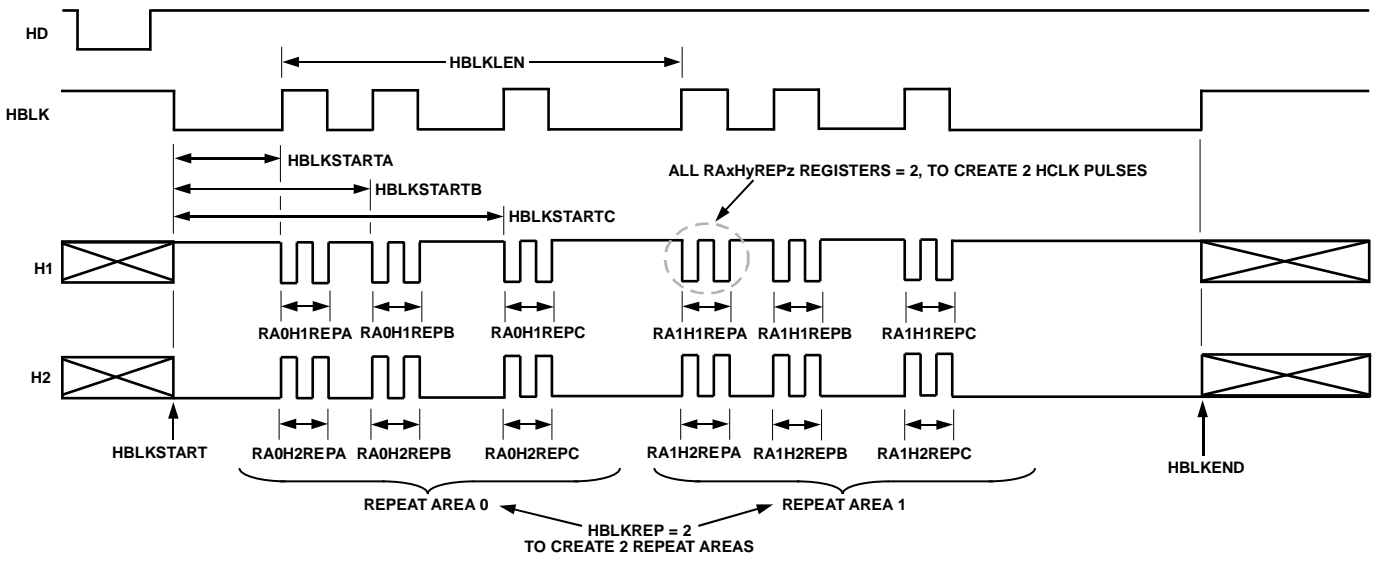


Figure 28. HBLK Mode 2 Registers

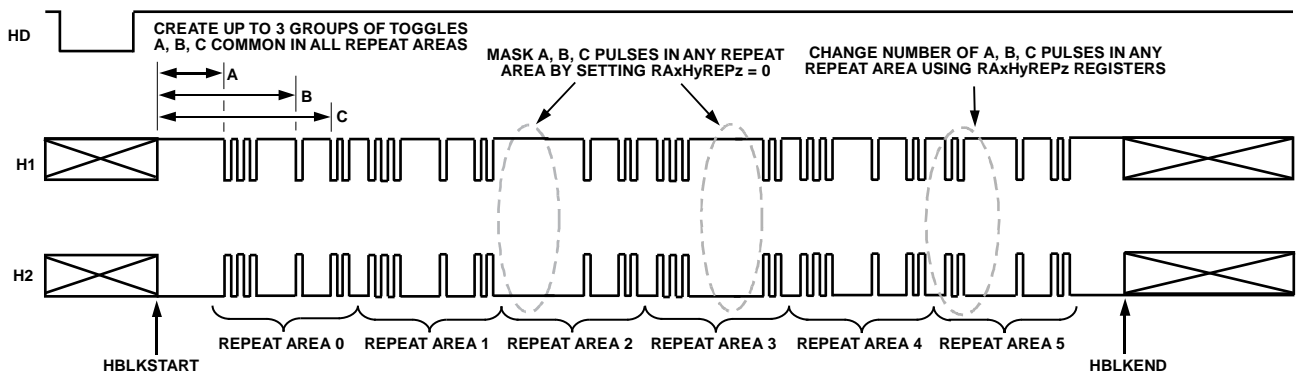


Figure 29. HBLK Mode 2 Operation

HBLK, PBLK, and CLPOB Toggle Positions

The AD9979 uses an internal horizontal pixel counter to position the HBLK, PBLK, and CLPOB toggle positions. The horizontal counter does not reset to 0 until 12 CLI periods after the falling edge of HD. This 12-cycle pipeline delay must be considered when determining the register toggle positions. For example, if CLPOBx_TOGy is 100 and the pipeline delay is not considered, the final toggle position is applied at 112. To obtain the correct toggle positions, the toggle position registers must be set to the desired toggle position minus 12. For example, if the desired toggle position is 100, CLPOBx_TOGy needs to be set to 88, that is, 100 minus 12. Figure 53 shows the 12-cycle pipeline delay referenced to the falling edge of HD.

Note that toggle positions cannot be programmed during the 12-cycle delay from the HD falling edge until the horizontal counter has reset. See Figure 31 for an example of this restriction.

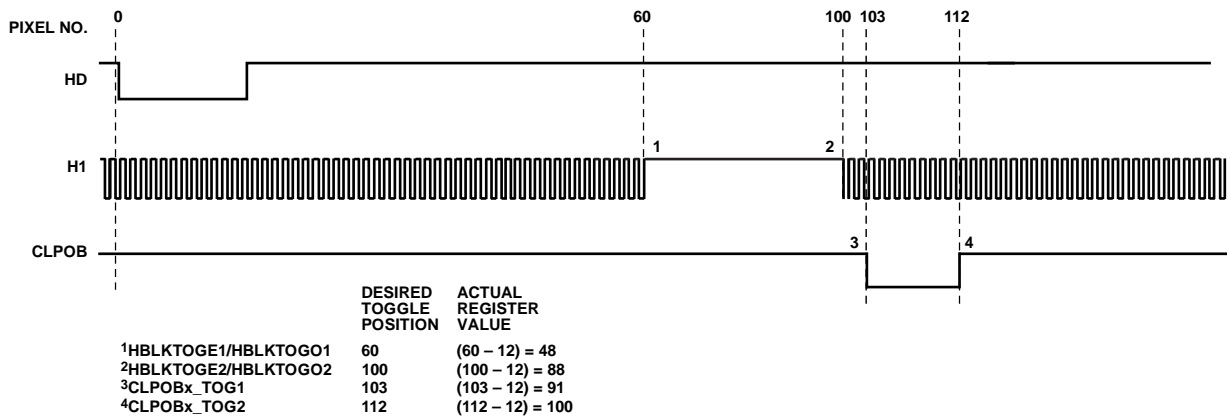


Figure 30. Example of Register Setting to Obtain Desired Toggle Positions

05957-032

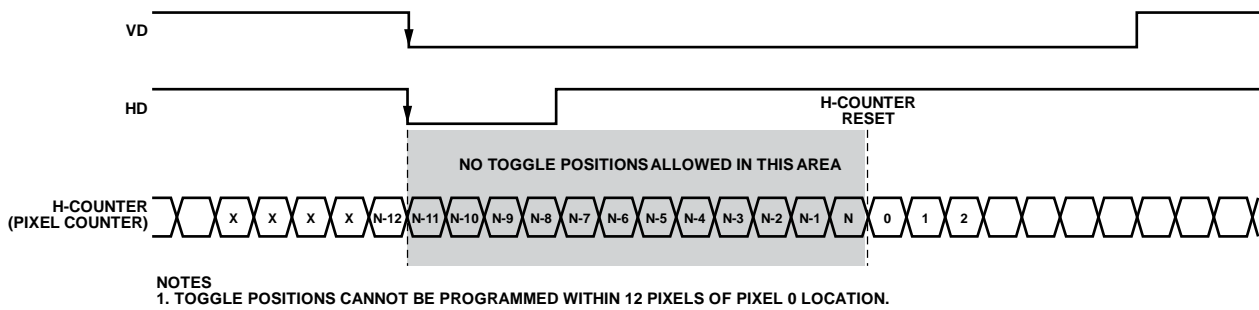


Figure 31. Restriction for Toggle Position Placement

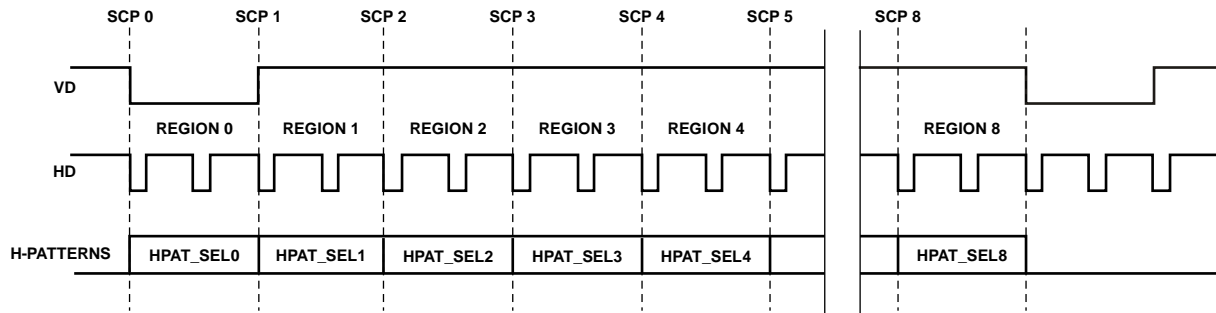
05957-033

COMPLETE FIELD—COMBINING H-PATTERNS

After creating the H-patterns, they combine to create different readout fields. A field consists of up to nine different regions determined by the SCP registers, and within each region, a different H-pattern group can be selected, up to a maximum of 32 groups. Registers to control the H-patterns are located in the field registers. Table 13 describes the field registers.

H-Pattern Selection

The H-patterns are stored in the HPAT memory, as described in Table 33. The user decides how many H-pattern groups are required, up to a maximum of 32, and then uses the HPAT_SELx registers to select which H-pattern group is output in each region of the field. Figure 32 shows how to use the HPAT_SELx and SCPx registers. The SCPx registers create the line boundaries for each region.



FIELD SETTINGS:
 1. SEQUENCE CHANGE POSITIONS (SCP0 TO SCP8) DEFINE EACH OF THE NINE AVAILABLE REGIONS IN THE FIELD.
 2. HPAT_SEL SELECTS THE DESIRED H-PATTERN FOR EACH REGION.

Figure 32. Complete Field Divided into Regions

065871034

Table 13. Field Registers

| Name | Length | Range | Description |
|-----------------------------------|---------|-----------------------|--|
| SCPx | 13 bits | 0 to 8191 line number | Sequence change position for each region; selects an individual line |
| HPAT_SELx | 5 bits | 0 to 31 H-patterns | Selected H-pattern for each region of the field |
| CLPOB_POL | 9 bits | High/low | CLPOB start polarity settings for each region of the field |
| CLPOB_PAT | 9 bits | 0 to 9 patterns | CLPOB pattern selector for each region of the field |
| CLPOBMASKSTARTx, CLPOBMASKENDx | 13 bits | Number of lines | CLPOB mask positions for up to three masking configurations |
| PBLK_POL | 9 bits | High/low | PBLK start polarity settings for each region of the field |
| PBLK_PAT | 9 bits | 0 to 9 patterns | PBLK pattern selector for each region of the field |
| PBLKMASKSTARTx, PBLKMASKENDx | 13 bits | Number of lines | PBLK mask positions for up to three masking configurations |

AD9979

MODE REGISTERS

To select the final field timing of the AD9979, use the mode registers. Typically, all of the field and H-pattern group information is programmed into the AD9979 at startup. During operation, the mode registers allows the user to select any combination of field timing to meet the current requirements of the system. The advantage of using the mode registers in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to write in all of the vertical timing information with each camera mode change.

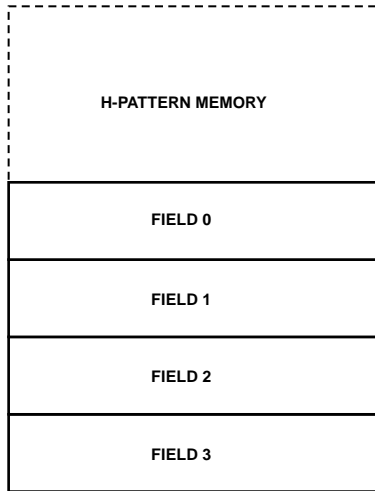
A basic still camera application can require five different fields of horizontal timing: one for draft mode operation, one for auto focusing, and three for still-image readout. With the AD9979, all register timing information for the five fields is loaded at startup. Then, during camera operation, the mode registers selects which field timing to activate depending on how the camera is being used.

The AD9979 supports up to seven field sequences, selected from up to 31 preprogrammed field groups, using the FIELD_SELx registers. When FIELDNUM is greater than 1, the AD9979 starts with Field 1 and increments to each Field N at the start of each VD.

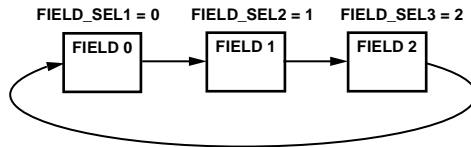
Figure 33 provides examples of the mode configuration settings. This example assumes having four field groups, Field Group 0 to Field Group 3, stored in memory.

Table 14. Mode Registers

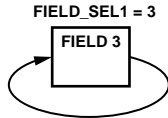
| Name | Length | Range | Description |
|------------|--------|--------------------------|---|
| HPATNUM | 5 bits | 0 to 31 H-pattern groups | Total number of H-pattern groups starting at Address 0x800 |
| FIELDNUM | 3 bits | 0 to 7 fields | Total number of applied fields (1 = single-field operation) |
| FIELD_SEL1 | 5 bits | 0 to 31 field groups | Selected first field |
| FIELD_SEL2 | 5 bits | 0 to 31 field groups | Selected second field |
| FIELD_SEL3 | 5 bits | 0 to 31 field groups | Selected third field |
| FIELD_SEL4 | 5 bits | 0 to 31 field groups | Selected fourth field |
| FIELD_SEL5 | 5 bits | 0 to 31 field groups | Selected fifth field |
| FIELD_SEL6 | 5 bits | 0 to 31 field groups | Selected sixth field |
| FIELD_SEL7 | 5 bits | 0 to 31 field groups | Selected seventh field |



EXAMPLE 1:
TOTAL FIELDS = 3, FIRST FIELD = FIELD 0, SECOND FIELD = FIELD 1, THIRD FIELD = FIELD 2



EXAMPLE 2:
TOTAL FIELDS = 1, FIRST FIELD = FIELD 3



EXAMPLE 3:
TOTAL FIELDS = 4, FIRST FIELD = FIELD 5, SECOND FIELD = FIELD 1, THIRD FIELD = FIELD 4, FOURTH FIELD = FIELD 2

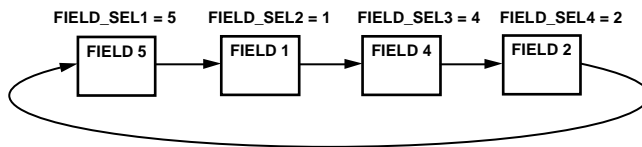


Figure 33. Example of Mode Configurations

06957-035

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 34 shows an example of a CCD layout. The horizontal register contains 28 dummy pixels, which occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and 2 OB lines at the back of the readout. The horizontal direction has 4 OB pixels in the front and 48 in the back.

Figure 35 shows the basic sequence layout to use during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the HBLK time. HBLK is used during the vertical shift interval.

Because PBLK is used to isolate the CDS input (see the Analog Front-End Description and Operation section), the PBLK signal cannot be used during CLPOB operation. The change in the offset behavior that occurs during PBLK impacts the accuracy of the CLPOB circuitry.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes can be used, such as adding in a separate sequence to clamp in the entire shield OB lines. This requires configuring a separate V-sequence for clocking out the OB lines.

The CLPOB mask registers are also useful for disabling the CLPOB on a few lines without affecting the setup of the

clamping sequences. It is important to use CLPOB only during valid OB pixels. During other portions on the frame timing, such as during vertical blanking or SG line timing, the CCD does not output valid OB pixels. Any CLPOB pulses that occur during this time cause errors in clamping operation, and therefore, cause changes in the black level of the image.

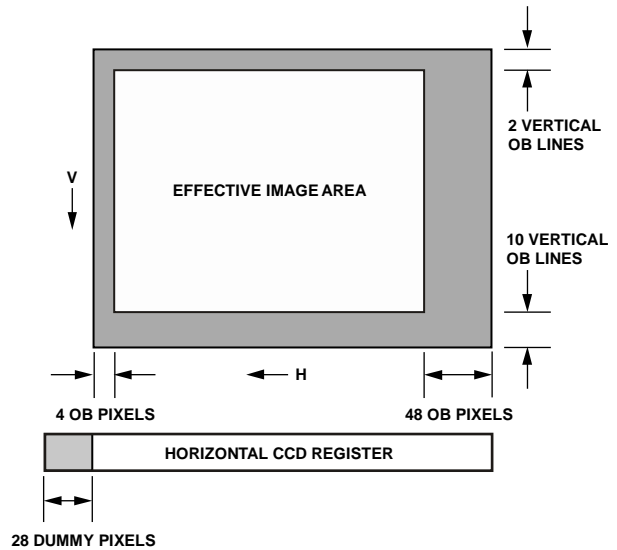
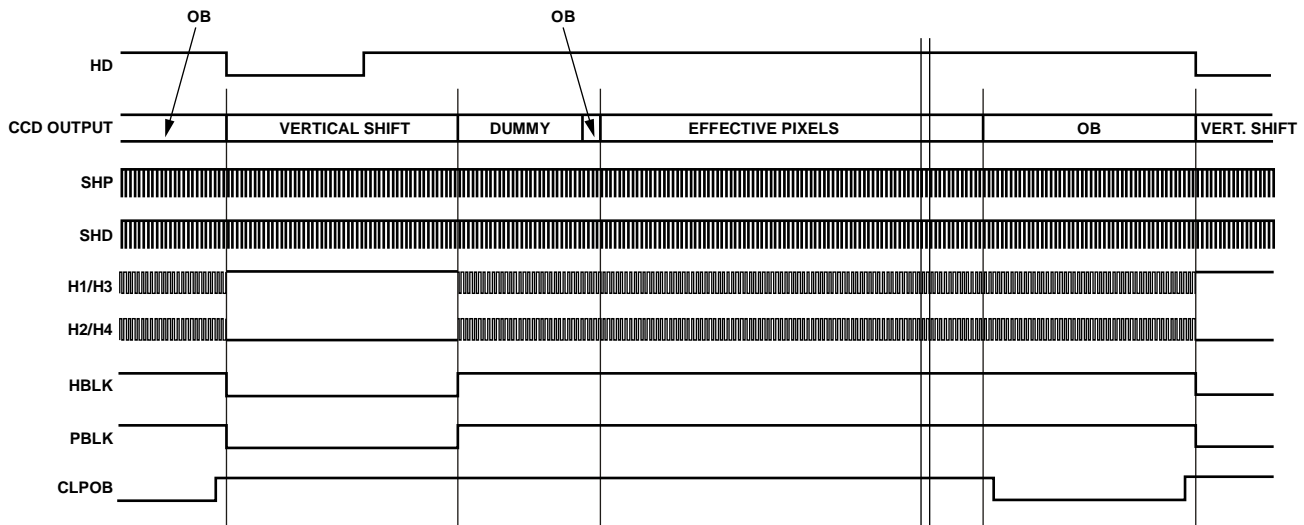


Figure 34. Example CCD Configuration



NOTES
1. IT IS RECOMMENDED THAT PBLK ACTIVE (LOW) NOT BE USED DURING CLPOB ACTIVE (LOW).

Figure 35. Horizontal Sequence Example

GENERAL-PURPOSE OUTPUTS (GPO)

The AD9979 provides programmable outputs to control a mechanical shutter, strobe/flash, the CCD bias select signal, or any other external component with general-purpose (GP) signals. Two GP signals are available, with up to two toggles each, that can be programmed and assigned to GPO1 and GPO2. These pins are bidirectional and also allow visibility of CLPOB, PBLK, and internal high speed signals (as an output) and external control of HBLK (as an input). The registers introduced in this section are described in Table 16.

Primary Field Counter

The AD9979 contains a primary field counter that is used to count multiple fields when using the GPO output signals. This counter is incremented on each VD cycle. The primary counter has several modes of operation controlled by Address 0x50, including the following:

- Activate counter (single count)
- RapidShot (repeating count)
- ShotTimer (delayed count)
- Force to idle

The primary counter regulates the placement of the GP toggle positions. In addition, if the RapidShot feature is used with the primary counter, the counter automatically repeats as necessary for multiple expose/read cycles.

GP Toggles

When configured as an output, each GPO can deliver a signal that is the result of programmable toggle positions. The GP signals are independent and can be linked to a specific VD period or over a range of VD periods, via the primary field counter, through the GP protocol register (Address 0x52). As a result of their associations with the field counters, the GP toggles inherit the characteristics of the field counter, such as RapidShot and ShotDelay. To use the GP toggles

1. Program the toggle positions (Address 0x54 to Address 0x59)
2. Program the protocol (Address 0x52)
3. Program the counter parameters (Address 0x51)
4. Activate the counter (Address 0x50)

For Protocol 1 (no counter association), skip Step 3 and Step 4.

With these four steps, the GP signals can be programmed to accomplish many common tasks. Careful protocol selection and application of the primary counter yields efficient results to allow the GP signals smooth integration with system operation.

Several simple examples of GPO application using only one GPO and one field counter follow. These examples can be used as building blocks for more complex GPO activity. In addition, specific GPO signals can be passed through a four-input LUT to realize combinational logic between them. For example, GPO1 and GPO2 can be sent through an XOR look-up table, and the result can be delivered on GPO1, GPO2, or both. In addition, either GPO1 or GPO2 can deliver its original toggles.

Table 15. Primary Field Counter Registers (Address 0x50 and Address 0x51)

| Name | Length | Description |
|----------------|--------|--|
| PRIMARY_ACTION | 3 bits | 0x0 = idle (no counter action). GPO signals still can be controlled using polarity or GPx_PROTOCOL = 1. 0x1 = activate counter. Single cycle of counter from 1 to counter maximum value; then returns to idle state. 0x2 = RapidShot. After reaching maximum counter value, counter wraps and repeats until reset. 0x3 = ShotTimer. Active single cycle of counter after added delay of N fields (use PRIMARY_DELAY register). 0x4 = test mode only. 0x5 = test mode only. 0x6 = test mode only. 0x7 = force to idle. |
| PRIMARY_MAX | 4 bits | Primary counter maximum value. |
| PRIMARY_DELAY | 4 bits | ShotTimer. Number of fields to delay before the next primary count starts. |

AD9979

Table 16. GPO Registers (Address 0x52 to Address 0x59)

| Name | Length | Range | Description |
|--------------------------------|---------|---------------|---|
| GP1_PROTOCOL | 2 bits | 0 to 3 | 0x0 = idle. |
| GP2_PROTOCOL | 2 bits | 0 to 3 | 0x1 = manual, no counter association. 0x2 = link to primary counter. 0x3 = primary repeat. Allows GP signals to repeat with RapidShot. |
| GP_LINE_MODE | 2 bits | Off/on | Enables general-purpose output signals on every line. 0 = disable. 1 = enable. |
| GPx_POL ¹ | 2 bits | Low/high | Starting polarity for general-purpose signals. Only updated during PROTOCOL = 1. |
| GPO_OUTPUT_EN | 2 bits | Off/on | 0 = disable GPOx. Output pins are in high-Z state (default). 1 = enable GPO1 to GPO2 outputs (1 bit per output). |
| SEL_GPOx ¹ | 2 bits | 0 to 3 | Select signal for GPO output. 0 = use GP toggles. 1 = use CLPOB. 2 = use PBLK. 3 = use high speed timing signal. |
| SEL_HS_GPOx ¹ | 2 bits | 0 to 3 | Select GPO output high speed timing signal used. 0 = use delayed CLI. 1 = use delayed ADC output latch clock. 2 = use delayed SHD sample clock. 3 = use delayed SHP sample clock. |
| HBLK_EXT | 1 bit | Off/on | 1 = enable external HBLK signal to be input to GPO2 pin. |
| GP_LUT_EN | 2 bits | | 0 = disabled. |
| GP12_LUT | 4 bits | Logic setting | Desired logic to be realized on GPO1 combined with GPO2. Example logic settings for GP12_LUT: 0x6 = GPO1 XOR GPO2 (See Figure 41). 0x7 = GPO1 NAND GPO2. 0x8 = GPO1 AND GPO2. 0xE = GPO1 OR GPO2. |
| GPTx_TOGy_FIELD ^{1,2} | 4 bits | 0 to 15 | Field of activity, relative to primary counter for toggle. |
| GPTx_TOGy_LINE ^{1,2} | 13 bits | 0 to 8191 | Line of activity for toggle. |
| GPTx_TOGy_PIXEL ^{1,2} | 13 bits | 0 to 8191 | Pixel of activity for toggle. |

¹ The variable x represents the general-purpose output, 1 or 2.

² The variable y represents the toggle, 1 or 2.

Single-Field Toggles

Single-field toggles begin in the field following the register write. There can be up to two toggles in the field. The mode is set with GPx_PROTOCOL equal to 1. In this mode, the field toggle settings must be set to 1. Toggles repeat for each field until GPx_PROTOCOL is set to 0. GPx_PROTOCOL must be reset to 0 for one field before it can be active again.

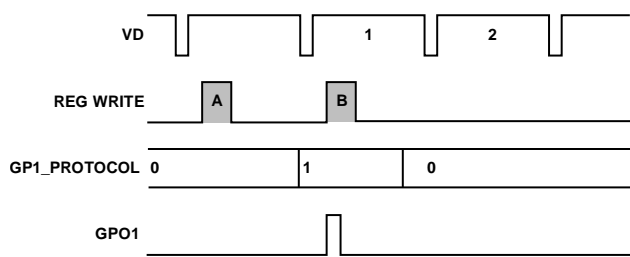
Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x054 ← 0x000A001
0x055 ← 0x0002000
0x056 ← 0x000000F
```

Details

- A) Field 0: 0x052 ← 0x0000001
- B) Field 1: 0x052 ← 0x0000000



NOTES
 1. THE FIELD TOGGLE POSITION IS IGNORED WHEN THE GPO PROTOCOL IS 1. TOGGLE POSITIONS REPEAT FOR EACH FIELD UNTIL GPO PROTOCOL IS RESET.

Figure 36. Single-Field Toggles Using GP1_PROTOCOL = 1

Scheduled Toggles

Scheduled toggles are programmed to occur during any upcoming field. For example, there can be one toggle in Field 1 and the next toggle in Field 3. The mode is set with GPx_PROTOCOL = 2, which tells the GPO to obey the primary field counter.

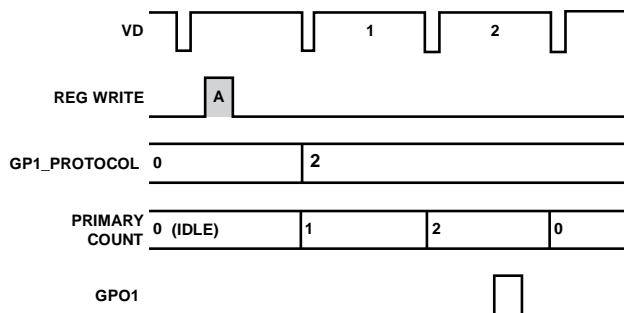
Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x054 ← 0x00C4002
0x055 ← 0x0004000
0x056 ← 0x00000B3
```

Details

- A) Field 0: 0x050 ← 0x0000001
- 0x052 ← 0x0000002



THE PRIMARY COUNTER REGULATES THE SUBCK AND VSG ACTIVITY; LINK A GPO TO THE PRIMARY COUNTER ONLY IF IT IS TO HAPPEN DURING EXPOSURE/READ.

Figure 37. Scheduled Toggles Using GP1_PROTOCOL = 2

RapidShot Sequences

RapidShot technology provides continuous repetition of scheduled toggles. As in the case of scheduled toggles, a pulse can traverse multiple fields. The mode is set with GPx_PROTOCOL = 3, which tells the GPO to obey the repeating primary field counter. GPx_PROTOCOL must be reset to 0 for one field before it can be active again.

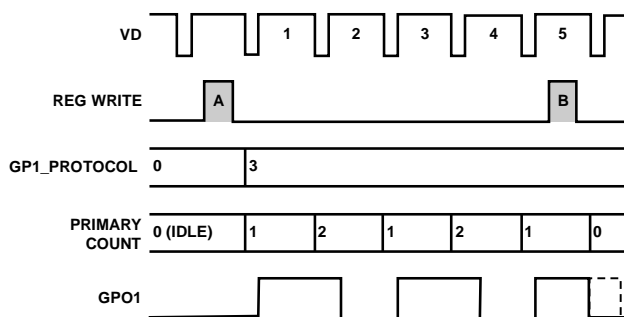
Preparation

The GPO toggle positions can be programmed any time prior to use. For example,

```
0x051 ← 0x0000002
0x054 ← 0x000A001
0x055 ← 0x0004000
0x056 ← 0x000000F
0x052 ← 0x0000003
```

Details

- A) Field 0: 0x050 ← 0x0000002
- B) Field 2: 0x050 ← 0x0000007



NOTES
 1. THE GPO PROTOCOLS ARE THE SAME AS THE SCHEDULED TOGGLES, EXCEPT THE TOGGLES CAN BE EXCLUDED FROM REPETITION BY CHOOSING GPO PROTOCOL 2.
CAUTION! THE FIELD COUNTER MUST BE FORCED INTO IDLE STATE TO TERMINATE REPETITIONS.

Figure 38. RapidShot Toggle Operation Using GP1_PROTOCOL = 3

ShotTimer Sequences

ShotTimer technology provides internal delay of scheduled toggles. The delay is in terms of fields.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

```
0x051 ← 0x0000032
0x054 ← 0x000A001
0x055 ← 0x0004000
0x056 ← 0x000000F
0x052 ← 0x0000002
```

Details

A) Field 0: 0x050 ← 0x0000003

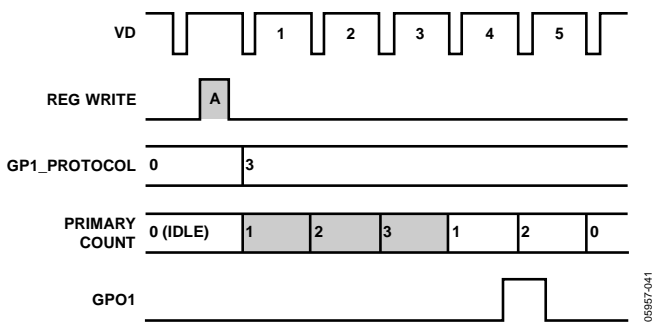


Figure 39. ShotDelay Toggle Operation Using GP1_PROTOCOL = 3

GP LOOK-UP TABLES (LUT)

The AD9979 includes a LUT for each pair of consecutive GP signals when configured as outputs. The external GPO outputs from the GPO1 pair can output the result of the LUT or the original GPO internal signal.

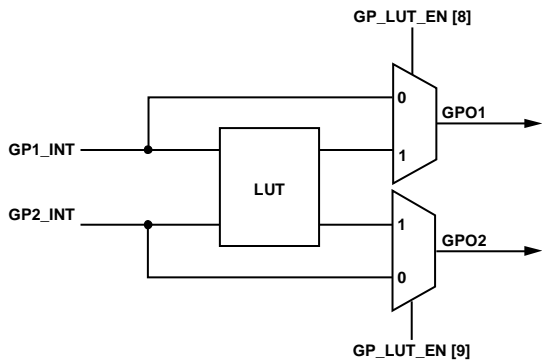


Figure 40. Internal LUT for GPO1 and GPO2 Signals

Address 0x52 dictates the behavior of the LUT and identifies which signals receive the result. Each 4-bit register can realize any logic combination of GPO1 and GPO2. Table 17 shows how the register values of GP12_LUT[13:10] are determined. XOR, NAND, AND, and OR results are shown, but any 4-bit combination is possible. A simple example of XOR gating is shown in Figure 41.

Table 17. LUT Results Based on GPO1, GPO2 Values

| GPO2 | GPO1 | LUT | | | |
|------|------|-----|------|-----|----|
| | | XOR | NAND | AND | OR |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |

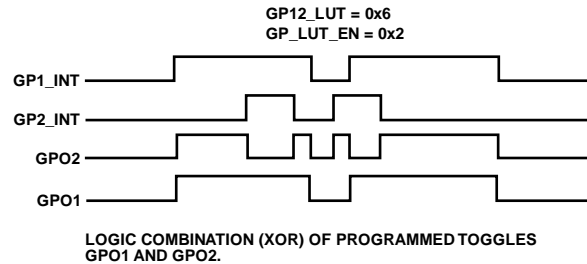
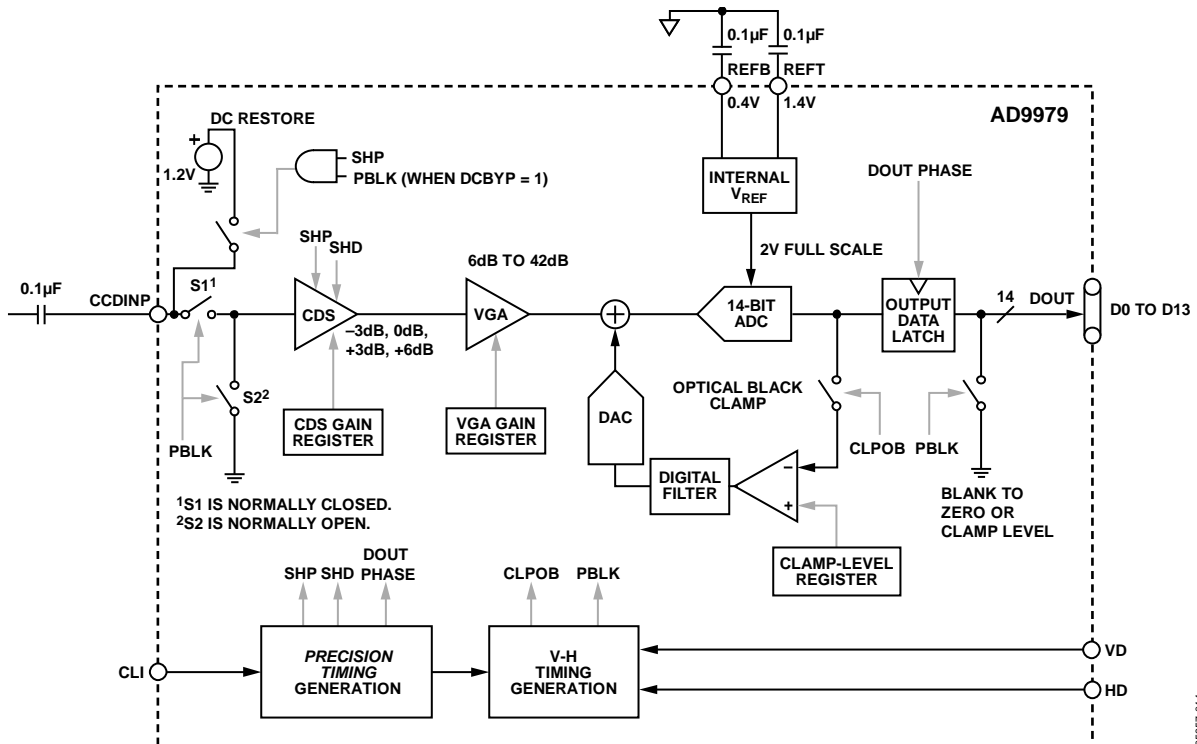


Figure 41. LUT Example for GPO1 XOR GPO2

Field Counter and GPO Limitations

1. The following is a summary of the known limitations of the field counters and GPO signals that dictate usability.
2. The field counter trigger (Address 0x50) is self-reset at the start of every VD period. Therefore, there must be one VD period between sequential programming to that address.
3. If the protocol is set to 1, the toggles repeat for each field until the protocol is set to idle.

ANALOG FRONT-END DESCRIPTION AND OPERATION



06957-044

The AD9979 signal processing chain is shown in Figure 42. Each processing step is essential in achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external $0.1\ \mu\text{F}$ series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.2 V, to be compatible with the 1.8 V core supply voltage of the AD9979. The dc restore switch is active during the SHP sample pulse time.

The dc restore circuit can be disabled when the optional PBLK signal is used to isolate large signal swings from the CCD input (see the Analog Preblanking section). Bit 6 of Address 0x00 controls whether the dc restore is active during the PBLK interval (see Table 24).

Analog Preblanking

During certain CCD blanking or substrate clocking intervals, the CCD input signal to the AD9979 can increase in amplitude beyond the recommended input range. The PBLK signal can be used to isolate the CDS input from large signal swings. As shown in Figure 42, when PBLK is active (low), the CDS input is isolated from the CCDINx pin (S1 open) and is internally shorted to ground (S2 closed).

During the PBLK active time, the ADC outputs can be programmed to output all zeros or the programmed clamp level.

Note that because the CDS input is shorted during PBLK, the CLPOB pulse must not be used during the same active time as the PBLK pulse.

Correlated Double Sampler (CDS)

The CDS circuit samples each CCD pixel twice to extract the video information and to reject low frequency noise. The timing shown in Figure 19 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and to sample the CCD signal level, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC and SHDLOC registers, located at Address 0x36. Placement of these two clock signals is critical in achieving the best performance from the CCD.

The CDS gain is variable in four steps, set by using CDSGAIN (Address 0x04): $-3\ \text{dB}$, $0\ \text{dB}$ (default), $+3\ \text{dB}$, and $+6\ \text{dB}$ (see Table 24). Improved noise performance results from using the $+3\ \text{dB}$ and $+6\ \text{dB}$ settings, but the input range is reduced with these settings (see Table 4).

Input Configurations

The CDS circuit samples each CCD pixel twice to extract the video information and to reject the low frequency noise (see Figure 43). There are three possible configurations for the CDS: inverting CDS mode, noninverting CDS mode, and SHA mode. CDSMODE (Address 0x00[9:8]) selects which configuration is used (see Table 24).

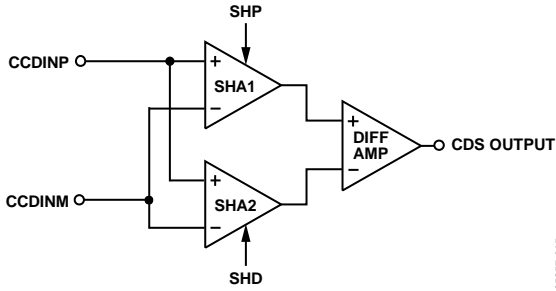
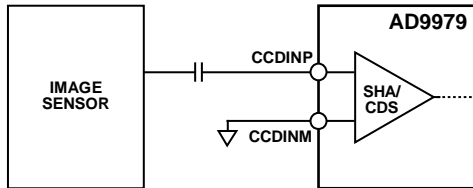


Figure 43. CDS Block Diagram (Conceptual)

Inverting CDS Mode

For this configuration, the signal from the CCD is applied to the positive input of the CDS system (CCDINP) and the negative side (CCDINM) is grounded (see Figure 44). The CDSMODE setting for this configuration is 0x00. Traditional CCD applications use this configuration with the reset level established below the AVDD supply level, by the AD9979 dc restore circuit, at approximately 1.5 V. The maximum saturation level is 1.0 V below the reset level, as shown in Figure 45 and Table 18. A maximum saturation voltage of 1.4 V is also possible when using the minimum CDS gain setting.



NOTES
1. COUPLING CAPACITOR IS NOT REQUIRED FOR CERTAIN BLACK-LEVEL REFERENCE VOLTAGES.

Figure 44. Single-Input CDS Configuration

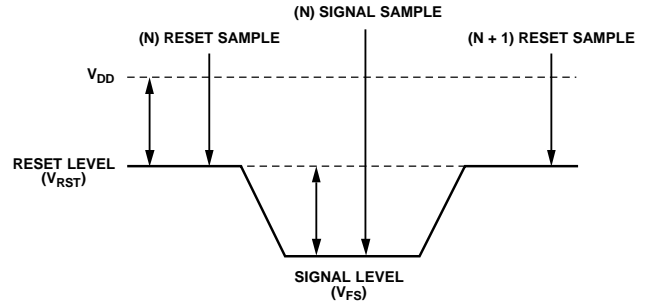


Figure 45. Traditional Inverting CDS Signal

Table 18. Inverting Voltage Levels

| Signal Level | Symbol | Min | Typ | Max | Unit |
|----------------|-----------|----------------|----------------|----------|------|
| Saturation | V_{FS} | | 1000 | 1400 | mV |
| Reset | V_{RST} | $V_{DD} - 500$ | $V_{DD} - 300$ | V_{DD} | mV |
| Supply Voltage | V_{DD} | 1600 | 1800 | 2000 | mV |

Noninverting CDS Mode

If the noninverting input is desired, the reset level signal (or black level signal) is established at a voltage above ground potential. Saturation level (or white level) is approximately 1 V. Samples are taken at each signal level (see Figure 46 and Table 19).

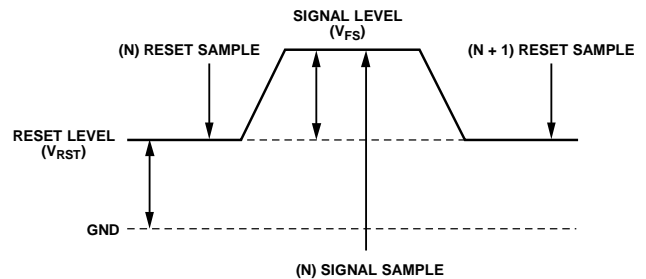


Figure 46. Noninverting CDS Signal

Table 19. Noninverting Voltage Levels

| Signal Level | Symbol | Min | Typ | Max | Unit |
|--------------|-----------|-----|------|------|------|
| Saturation | V_{FS} | | 1000 | 1400 | mV |
| Reset | V_{RST} | 0 | 250 | 500 | mV |

SHA Mode—Differential Input Configuration

In this configuration, which uses a differential input sample-and-hold amplifier (SHA), a signal is applied to the CCDINP input, while an inverse signal is applied simultaneously to the CCDINM input (see Figure 47). Sampling occurs on both signals at the same time, creating the differential output for amplification and for the ADC (see Figure 48 and Table 20).

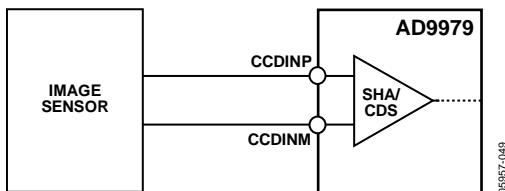


Figure 47. SHA Mode—Differential Input Configuration

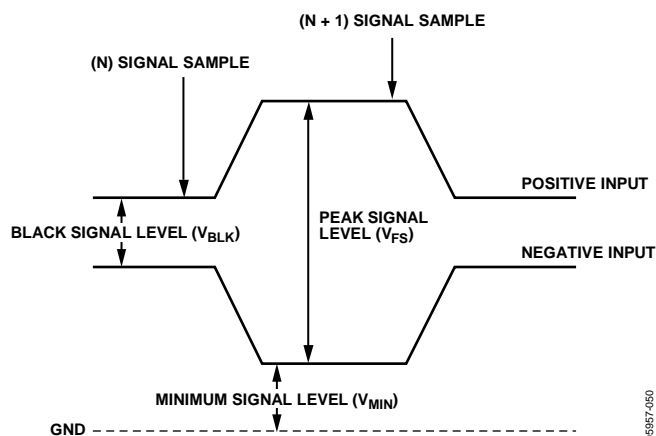


Figure 48. SHA Mode—Differential Input Signal

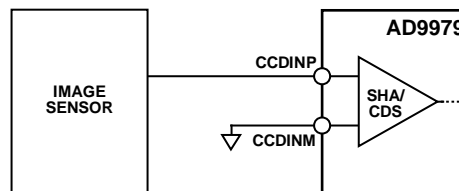
Table 20. SHA Mode—Differential Voltage Levels

| Signal Level | Symbol | Min | Typ | Max | Unit |
|-------------------------|-----------|------|----------------|------|------|
| Black Signal Level | V_{BLK} | | 0 | | mV |
| Saturation Signal Level | V_{FS} | 1000 | $V_{DD} - 300$ | 1400 | mV |
| Minimum Signal Level | V_{MIN} | 0 | 1800 | | mV |

SHA Mode—DC-Coupled, Single-Ended Input

The SHA mode can also be used in a single-ended fashion, with the signal from the image sensor applied to the CDS/SHA using a single input, CCDINP. This is similar to the differential configuration, except in this case, the CCDINM line is held at a constant dc voltage. This establishes a reference level that matches the image sensor reference voltage (see Figure 49).

Referring to Figure 50 and Table 21, the CCDINM signal is a constant dc voltage set at a level above ground potential. The sensor signal is applied to the other input, and samples are taken at the signal minimum and at a point of signal maximum. The resulting differential signal is the difference between the signal and the reference voltage.



NOTES
1. DC VOLTAGE ABOVE GROUND CAN BE USED TO MATCH THE SENSOR REFERENCE LEVEL.

Figure 49. SHA Mode—DC-Coupled, Single-Ended Input Configuration

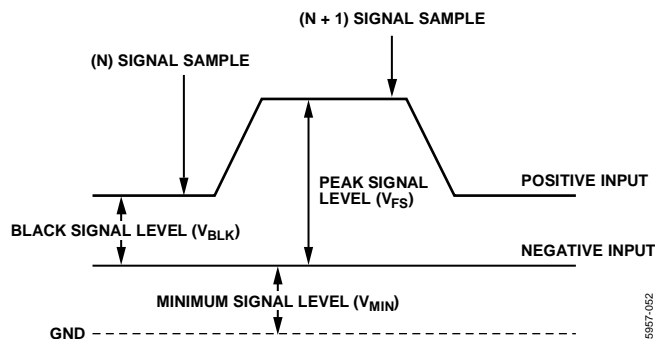


Figure 50. SHA Mode—DC-Coupled, Single-Ended Input Signal

Table 21. SHA Mode—Single-Ended, Input Voltage Levels

| Signal Level | Symbol | Min | Typ | Max | Unit |
|-------------------------|-----------|-----|------|------|------|
| Black Signal Level | V_{BLK} | | 0 | | mV |
| Saturation Signal Level | V_{FS} | | 1000 | 1400 | mV |
| Minimum Signal Level | V_{MIN} | 0 | | | mV |

CDS Timing Control

The timing shown in Figure 19 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and the data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of SHPLOC and SHDLOC, located at Address 0x36. Placement of these two clock signals is critical in achieving the best performance from the CCD.

SHA Timing Control

When SHA mode is selected, only the SHPLOC setting is used to sample the input signal, but the SHDLOC signal still needs to be programmed to an edge setting of SHPLOC + 32.

Variable Gain Amplifier (VGA)

The VGA stage provides a gain range of approximately 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. A gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain is calculated for any gain register value by

$$\text{Gain (dB)} = (0.0358 \times \text{Code}) + 5.75 \text{ dB}$$

where *Code* is the range of 0 to 1023.

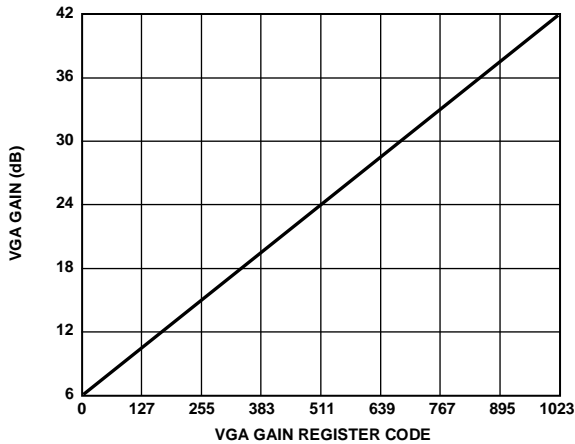


Figure 51. VGA Gain Curve

Analog-to-Digital Converter

The AD9979 uses a high performance ADC architecture, optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. (See Figure 5 to Figure 7 for the typical linearity and noise performance plots of the AD9979.)

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The value can be programmed between 0 LSB and 255 LSB, in 256 steps. The resulting error signal is filtered to reduce noise, and the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during the postprocessing, the AD9979 optical black clamping can be disabled using CLAMPENABLE, Bit 3 in Address 0x00. When the loop is disabled, the clamp level register can still be used to provide fixed offset adjustment.

Note that if the CLPOB loop is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is gained up.

It is recommended to align the CLPOB pulse with the CCD optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths can be used, but the ability for the loop to track low frequency variations in the black level is reduced. See the Horizontal Clamping and Blanking section for more timing information.

Digital Data Outputs

The AD9979 digital output data is latched using the DOUTPHASEx value, as shown in Figure 42. (Output data timing is shown in Figure 20.) The switching of the data outputs can couple noise back into the analog signal path. To minimize any switching noise while using default register settings, it is recommended that DOUTPHASEPx be set to a value between 15 and 31. Other settings can produce good results, but experimentation is necessary.

The data output coding is normally straight binary, but the coding can be changed to gray coding by setting Bit 2 of Address 0x01 to 1.

APPLICATIONS INFORMATION

RECOMMENDED POWER-UP SEQUENCE

When the AD9979 is powered up, the following sequence is recommended (refer to Figure 52 for each step).

1. Turn on the power supplies for the AD9979 and apply CLI clock. There is no required order for bringing up each supply.
2. Although the AD9979 contains an on-chip, power-on reset, a software reset of the internal registers is recommended. Write 1 to SW_RST (Address 0x10, Bit [0], which resets all the internal registers to their default values. This bit is self-clearing and automatically resets back to 0.
3. Write to the desired registers to configure high speed timing and horizontal timing. Note that all TESTMODE registers must be written as described in the register maps.

4. To place the part into normal power operation, write 0 to STANDBY (Address 0x00, Bits[1:0]) and REFBUF_PWRDN (Address 0x00, Bit 2).
5. The *Precision Timing* core must be reset by writing 1 to TGCORE_RST (Address 0x14, Bit 0). This starts the internal timing core operation.
6. Write 1 to OUT_CONTROL (Address 0x11, Bit 0).

The next VD/HD falling edge allows register updates to occur, including OUT_CONTROL (Address 0x11, Bit [0]), which enables all clock outputs.

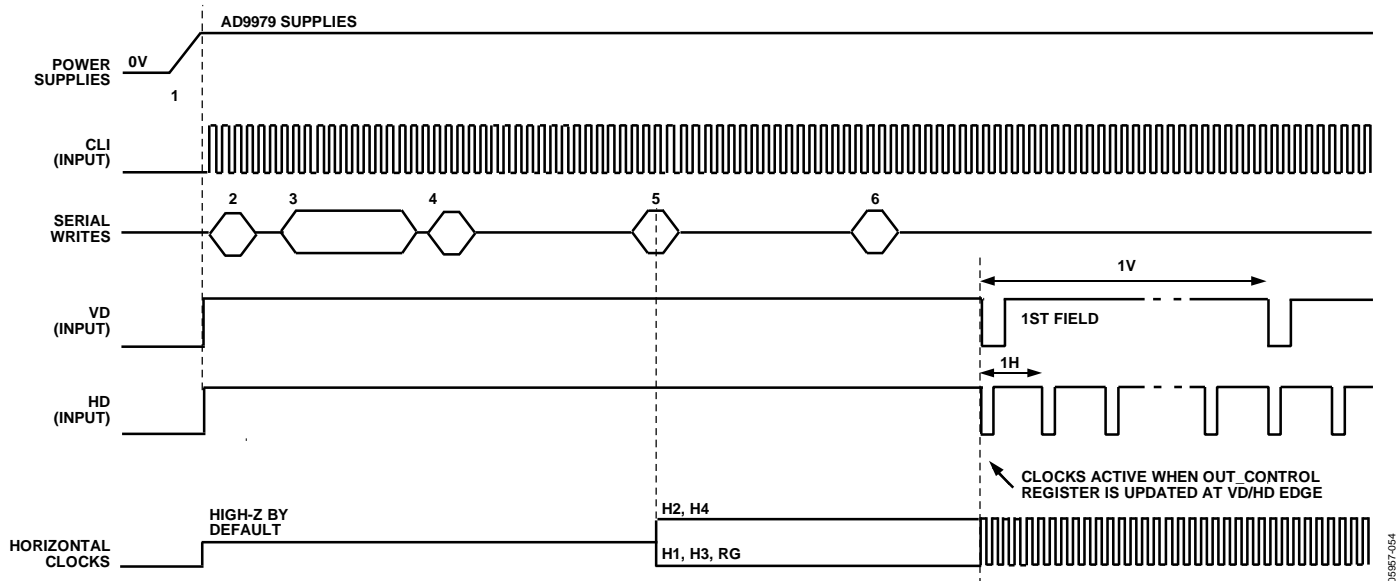


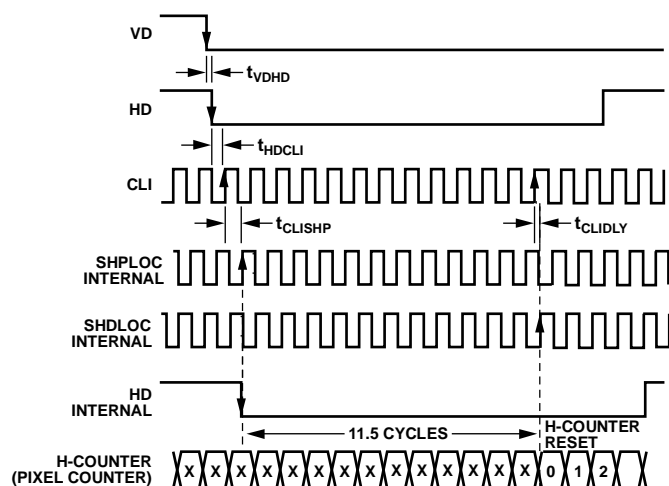
Figure 52. Recommended Power-Up Sequence

08967-054

Example Register Settings for Power-Up

The following settings can be used for basic operation. A single CLPOB pulse is used with only H-pattern and one field. Additional HPATS and FIELDS can be added, as needed, along with different CLPOB toggle positions.

```
010 0000001 //Software Reset
028 0000001 //total number of H-Pattern groups = 1
800 0064000 //HPAT0 HBLKTOG01, TOG02 settings
801 3fffffff //unused HBLK Odd toggles set to zero or max value
802 3fffffff //unused HBLK Odd toggles set to zero or max value
803 0064000 //HPAT0 HBLKTOGE1, TOGE2 settings
804 3fffffff //unused HBLK Even toggles set to zero or max value
805 3fffffff //unused HBLK Even toggles set to zero or max value
806 0000000 //HBLK StartA, B are not used
807 0000000 //HBLK StartC is not used
808 0000000 //HBLK Alternation Patterns are not used
809 0000000 //HBLKLEN, HBLKREP not used, HBLK masking pol = 0
80a 0000000 //HBLKSTART, END not used
80b 0000000 //Test, set to zero
80c 00dc05a //CLPOB pat 0 toggles
80d 3fffffff //CLPOB pat 1 toggles not used, set to max
80e 3fffffff //PBLK pat 0 toggles not used, set to max
80f 3fffffff //PBLK pat 1 toggles not used, set to max
810 1000000 //FIELD0 SCP0, SCP1
811 1000800 //SCP2, SCP3 set same as SCP1
812 1000800 //SCP4, SCP5 set same as SCP1
813 1000800 //SCP6, SCP7 set same as SCP1
814 0000800 //SCP8 set same as SCP1
815 0000000 //Select HPAT0 for all regions
816 0000000 //Select HPAT0 for all regions
817 0000000 //Test, set to zero
818 0000001 //CLPOB start polarity = HIGH
819 1000800 //CLPOB masking set to highest SCP value (no mask)
81a 1000800 //CLPOB masking set to highest SCP value (no mask)
81b 1000800 //CLPOB masking set to highest SCP value (no mask)
81c 0000001 //PBLK start polarity = HIGH
81d 1000800 //PBLK masking set to highest SCP value (no mask)
81e 0000000 //PBLK masking set to highest SCP value (no mask)
81f 0000000 //PBLK masking set to highest SCP value (no mask)
02a 0000001 //total number of Fields = 1
02b 0000000 //field select = FIELD0
02c 0000000 //field select = FIELD0
000 0000008 //AFE settings
014 0000001 //reset TGCORE
011 0000001 //enable outputs
```



NOTES

- EXTERNAL HD FALLING EDGE IS LATCHED BY CLI RISING EDGE, THEN LATCHED AGAIN BY SHPLOC (INTERNAL SAMPLING EDGE).
- INTERNAL H-COUNTER IS ALWAYS RESET 11.5 CLOCK CYCLES AFTER THE INTERNAL HD FALLING EDGE, AT SHDLOC (INTERNAL SAMPLING EDGE).
- DEPENDENT ON THE VALUE OF SHDLOC, H-COUNTER RESET CAN OCCUR 13 OR 14 CLI CLOCK EDGES AFTER THE EXTERNAL HD FALLING EDGE.
- SHPLOC = 32, SHDLOC = 0 IS SHOWN IN ABOVE EXAMPLE. IN THIS CASE, THE H-COUNTER RESET OCCURS 13 CLI RISING EDGES AFTER HD FALLING EDGE.
- HD FALLING EDGE MUST OCCUR COINCIDENT WITH VD FALLING EDGE (WITHIN SAME CLI CYCLE) OR AFTER VD FALLING EDGE. HD FALLING EDGE MUST NOT OCCUR WITHIN 1 CLI CYCLES IMMEDIATELY BEFORE VD FALLING EDGE.

Figure 53. Horizontal Counter Pipeline Delay

09987-955

Additional Restrictions

When operating, note the following restrictions:

- The HD falling edge should be located in the same CLI clock cycle as the VD falling edge or later than the VD falling edge. The HD falling edge should not be located within 1 cycle prior to the VD falling edge.
- If possible, perform all start-up serial writes with VD and HD disabled. This prevents unknown behavior caused by partial updating of registers before all information is loaded.

The internal horizontal counter is reset 12 CLI cycles after the falling edge of HD. See Figure 53 for details on how the internal counter is reset.

STANDBY MODE OPERATION

The AD9979 contains two different standby modes to optimize the overall power dissipation in a particular application. Bits[1:0] of Address 0x00 control the power-down state of the device.

- STANDBY[1:0] = 00 = normal operation (full power)
- STANDBY[1:0] = 01 = reference standby mode
- STANDBY[1:0] = 10 or 11 = total shut-down mode (lowest power)

Table 22 summarizes the operation of each power-down mode. OUT_CONTROL (Address 0x11, Bit [0]) takes priority over the reference standby mode in determining the digital output states, but total shutdown mode takes priority over OUT_CONTROL. Total shutdown mode has the lowest power consumption. When returning from total shutdown mode to normal operation, the timing core must be reset at least 100 μ s after STANDBY (Address 0x00, Bits[1:0]) is written to.

There is an additional register to independently disable the internal voltage reference buffer, REFBUF_PWRDN (Bit 2, (Address 0x00)). By default, the buffer is disabled. It must be enabled for normal operation.

CLI FREQUENCY CHANGE

If the input clock (CLI) is interrupted or changes to a different frequency, the timing core must be reset for proper operation. After the CLI clock has settled to the new frequency, or the previous frequency is resumed, write 0 and then 1 to TGCORE_RST (Address 0x14). This guarantees proper timing core operation.

Table 22. Standby Mode Operation

| I/O Block | Total Shutdown (Default) ^{1,2} | OUT_CONTROL = Low ² | Reference Standby |
|-------------|---|--------------------------------|--------------------|
| AFE | Off | No change | Only REFT, REFB on |
| Timing Core | Off | No change | On |
| H1 | High-Z | Low | Low (4.3 mA) |
| H2 | High-Z | High | High (4.3 mA) |
| H3 | High-Z | Low | Low (4.3 mA) |
| H4 | High-Z | High | High (4.3 mA) |
| HL | High-Z | Low | Low (4.3 mA) |
| RG | High-Z | Low | Low (4.3 mA) |
| DOUT | Low ³ | Low | Low |

¹ To exit total shutdown, write 00 to STANDBY (Address 0x00, Bits[1:0]), then reset the timing core after 100 μ s to guarantee proper settling.

² Total shutdown mode takes priority over OUT_CONTROL for determining the output polarities.

³ The status of the DOUT pins is unknown at power-up. Low status is guaranteed in total shutdown mode after the power-up sequence is completed.

CIRCUIT CONFIGURATION

The AD9979 recommended circuit configurations are shown in Figure 54 and Figure 55. Achieving good image quality from the AD9979 requires careful attention to PCB layout. Route all signals to maintain low noise performance. Directly route the CCD output signal through a 0.1 μ F capacitor to Pin 31. To minimize interference with the CCDINM, CCDINP, REFT, and REFB signals, carefully route the master clock (CLI) to Pin 28.

The H1 to H4, HL, and RG traces need low inductance to avoid excessive distortion of the signals. Heavier traces are recommended because of the large transient current demands on H1 to H4 and HL from the capacitive load of the CCD. If possible, physically locating the AD9979 closer to the CCD reduces the inductance on these lines. Make the routing path as direct as possible from the AD9979 to the CCD.

3 V System Compatibility

The AD9979 typical circuit connections for a 3 V system are shown in Figure 54. This application uses an external 3.3 V supply connected to the IOVDD input of the AD9979, which also serves as the LDO input. The LDO generates a 1.8 V output for the AD9979 core supply voltages, AVDD and DVDD. The LDOOUT pin can then be connected directly to the AVDD and DVDD pins. In this configuration, the LDOEN pin is tied high to enable the LDO.

Alternatively, a separate 1.8 V regulated supply voltage may be used to power the AVDD and DVDD pins. In this case, the LDOOUT pin needs to be left floating, and the LDOEN pin needs to be grounded. A typical circuit configuration for a 1.8 V system is shown in Figure 55.

GROUNDING AND DECOUPLING RECOMMENDATIONS

As shown in Figure 54 and Figure 55, a single ground plane is recommended for the AD9979. This ground plane needs to be as continuous as possible, particularly around the P-type, AI-type, and A-type pins to ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All high frequency decoupling capacitors need to be located as close as possible to the package pins.

All the supply pins must be decoupled to ground with good quality, high frequency chip capacitors. There also needs to be a 4.7 μ F or larger bypass capacitor for each main supply, that is, AVDD, RGVDD, HVDD, and DRVDD, although this is not necessary for each individual pin. In most applications, it is easier to share the supply for RGVDD and HVDD, which can be done as long as the individual supply pins are separately bypassed. A separate 3 V supply can be used for DRVDD, but this supply pin still needs to be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The reference bypass pins (REFT, REFB) must be decoupled to ground as close as possible to their respective pins. The bridge capacitor between REFT and REFB is recommended for pixel rates greater than 40 MHz. The analog input capacitor (CCDINM, CCDINP) also needs to be located close to the pin.

The GND connections should be tied to the lowest impedance ground plane on the PCB. Performance does not degrade if several of these GND connections are left unconnected for routing purposes.

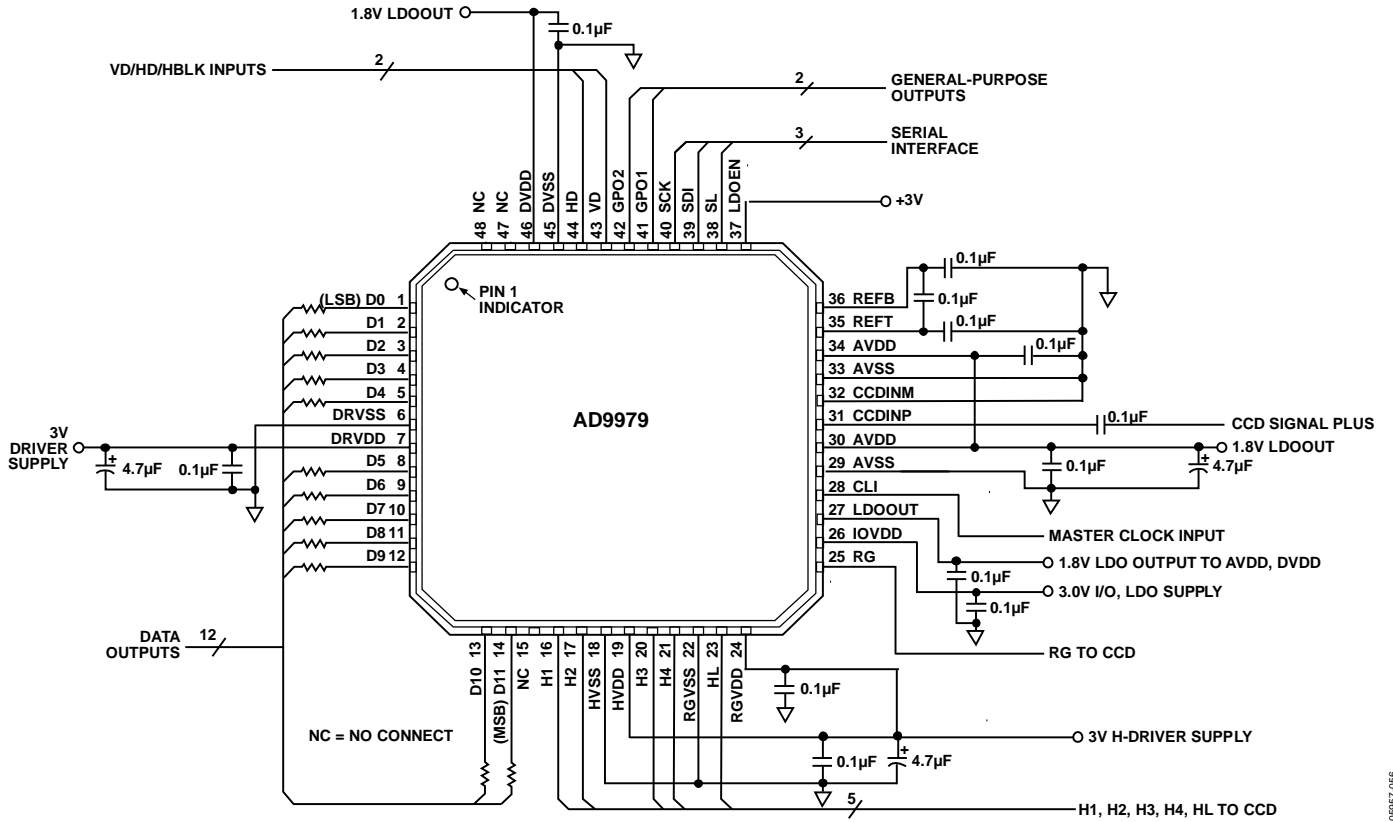


Figure 54. Typical 3 V Circuit Configuration

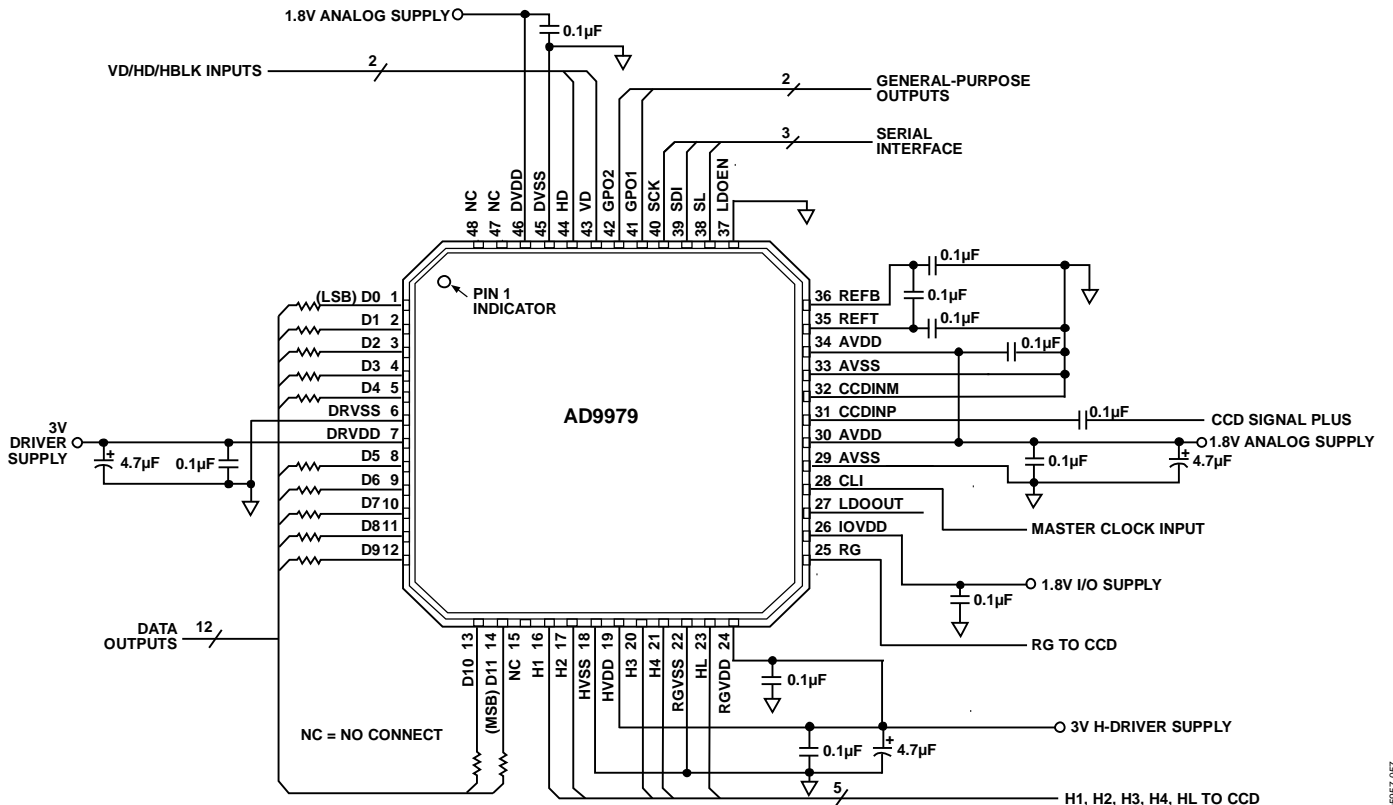
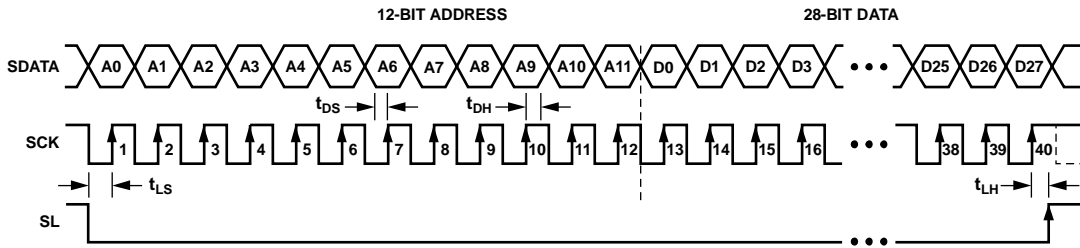


Figure 55. Typical 1.8 V Circuit Configuration

3-WIRE SERIAL INTERFACE TIMING

All of the internal registers of the AD9979 are accessed through a 3-wire serial interface. Each register consists of a 12-bit address and a 28-bit data-word. Both the 12-bit address and the 28-bit data-words are written starting with the LSB. To write to each register, a 40-bit operation is required, as shown in Figure 56. Although many registers are fewer than 28-bits wide, all 28 bits must be written for each register. For example, if the register is only 20-bits wide, the upper 8 bits are don't care bits and must be filled with zeros during the serial write operation. If fewer than 28 data bits are written, the register does not update with new data.

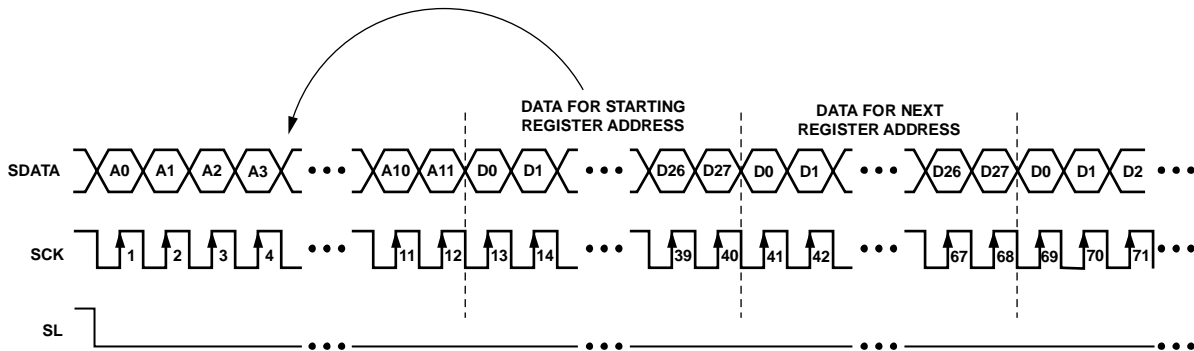
Figure 57 shows a more efficient way to write to the registers, using the AD9979 address auto-increment capability. Using this method, the lowest desired address is written first, followed by multiple 28-bit data-words. Each new 28-bit data-word is automatically written to the next highest register address. By eliminating the need to write to each 12-bit address, faster register loading is achieved. Continuous write operations can be used starting with any register location.



- NOTES:
1. SDATA BITS ARE LATCHED ON SCK RISING EDGES. SCK MAY IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
 2. ALL 40 BITS MUST BE WRITTEN: 12 BITS FOR ADDRESS AND 28 BITS FOR DATA.
 3. IF THE REGISTER LENGTH IS <28 BITS, THEN ZEROS MUST BE USED TO COMPLETE THE 28-BIT DATA LENGTH.
 4. NEW DATA VALUES ARE UPDATED IN THE SPECIFIED REGISTER LOCATION AT DIFFERENT TIMES, DEPENDING ON THE PARTICULAR REGISTER WRITTEN TO. SEE THE UPDATING OF NEW REGISTER VALUES SECTION FOR MORE INFORMATION.

Figure 56. Serial Write Operation

05957-059



- NOTES:
1. MULTIPLE SEQUENTIAL REGISTERS MAY BE LOADED CONTINUOUSLY.
 2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 28-BIT DATA-WORDS.
 3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 28-BIT DATA-WORD (ALL 28 BITS MUST BE WRITTEN).
 4. SL IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.

Figure 57. Continuous Serial Write Operation

05957-059

LAYOUT OF INTERNAL REGISTERS

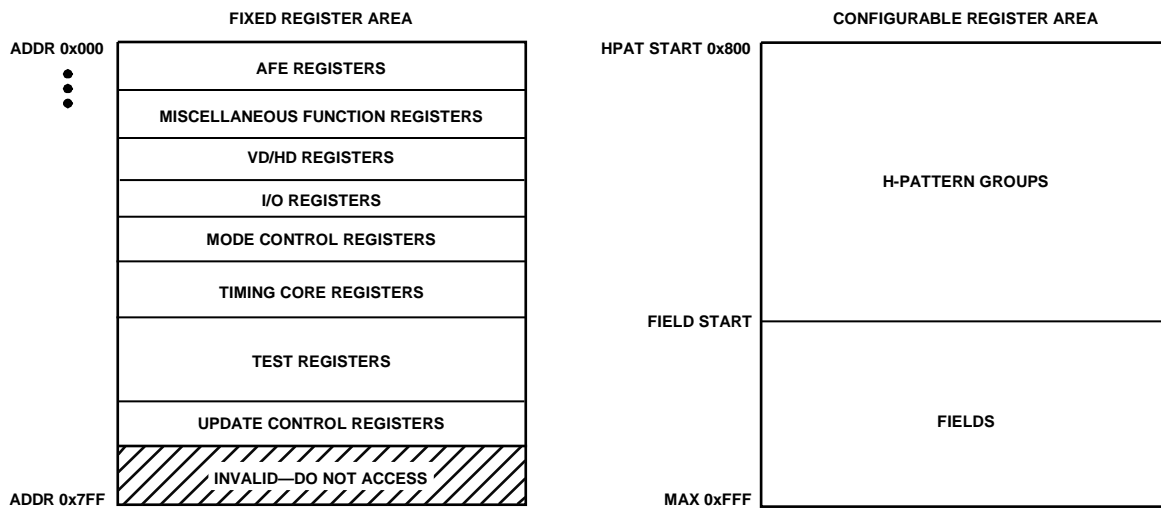
The AD9979 address space is divided into two different register areas, as illustrated in Figure 58. In the first area, Address 0x000 to Address 0x7FF contain the registers for the AFE, miscellaneous functions, VD/HD parameters, input/output control, mode control, timing core, test, and update control functions. The second area of the address space, beginning at Address 0x800, consists of the registers for the H-pattern groups and fields. This is a configurable set of register space; the user can decide how many H-pattern groups and fields are used in a particular design. The AD9979 supports up to 32 H-patterns.

Register 0x28 specifies the total number of H-pattern groups. The starting address for the H-pattern group registers is always 0x800, and the starting address for the field registers is determined by the number of H-pattern groups, and it is equal to 0x800 plus the number of H-pattern groups times 16. Each H-pattern group and field occupies 16 register addresses.

It is important to note that the H-pattern group and field registers must always occupy a continuous block of addresses.

Figure 59 shows an example using three H-pattern groups and two fields. The starting address for the H-pattern groups is always 0x800. Because HPATNUM is set to 3, the H-pattern groups occupy 48 address locations, that is, 16 registers times 3 H-pattern groups. The starting address of the field registers for this example is 0x830, or 0x800 plus 48 (decimal). Note the decimal value must be converted to a hexadecimal number before adding it to 0x800.

The AD9979 address space contains many unused addresses. Undefined addresses between Address 0x00 and Address 0xFF must not be written to; otherwise, the AD9979 can operate incorrectly. Continuous register writes needs to be performed carefully to avoid writing to undefined registers.



NOTES
1. THE H-PATTERN GROUP AND FIELD REGISTERS MUST OCCUPY A CONTINUOUS BLOCK OF ADDRESSES.

Figure 58. Layout of AD9979 Registers

05957-060

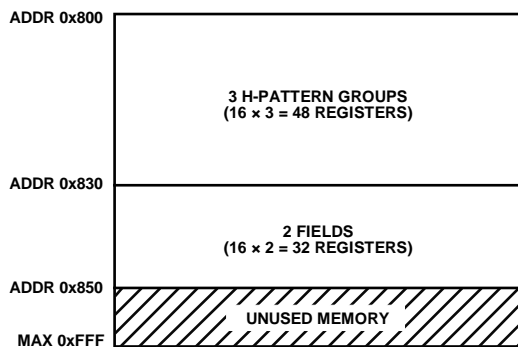


Figure 59. Example Register Configuration

05957-061

UPDATING OF NEW REGISTER VALUES

The internal registers of the AD9979 are updated at different times, depending on the register. Table 23 summarizes the three different types of register updates. The register listing tables also contain a column with update type to identify when each register is updated (see Table 24 to Table 34).

SCK Updated (SCK)

Some of the registers are updated immediately, as soon as the 28th data bit (D27) is written. These registers are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions.

Table 23. Register Update Locations

| Update Type | Description |
|-------------|---|
| SCK | Register is immediately updated when the 28th data bit (D27) is clocked in. |
| VD | Register is updated at the VD falling edge. VD-updated registers can be delayed further, using UPDATE (Address 0x17, Bits[12:0]). Field registers are not affected by UPDATE. |
| SCP | Register is updated at the next SCP in which the register is used. |

VD Updated (VD)

Many of the registers are updated at the next VD falling edge. By updating these values at the next VD edge, the current field is not corrupted and the new register values are applied to the next field. The VD update can be further delayed past the VD falling edge, using UPDATE (Address 0x17, Bits[12:0]), which delays the VD-updated register updates to any HD line in the field. Note that the field registers are not affected by UPDATE.

SCP Updated (SCP)

All of the H-pattern group registers are updated at the next SCP in which the registers are used.

COMPLETE REGISTER LISTING

All addresses and default values are expressed in hexadecimal. When an address contains less than 28 data bits, all remaining bits must be written as 0s.

Table 24. AFE Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|--------------------|---------------|-------------|--------------------|---|
| 00 | [1:0] | 3 | SCK | STANDBY | Standby modes. 0 = normal operation (full power). 1 = reference standby mode. 2 = total shutdown mode (lowest power). 3 = total shutdown mode (lowest power). |
| | [2] | 1 | | REFBUF_PWRDN | Reference buffer for REFT and REFB power control. 0 = REFT/REFB internally driven. 1 = REFT/REFB not driven. |
| | [3] | 1 | | CLAMPENABLE | Clamp enable control. 0 = disable black clamp. 1 = enable black clamp. |
| | [5:4] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [6] | 0 | | PBLK_LVL | PBLK level control. 0 = blank to 0. 1 = blank to clamp level. |
| | [7] | 0 | | DCBYP | DC restore circuit control. 0 = enable dc restore circuit during PBLK. 1 = bypass dc restore circuit during PBLK. |
| | [9:8] | 0 | | CDSMODE | CDS operation. 0 = normal (inverting) CDS mode. 1 = sample/hold amplifier (SHA) mode. 2 = positive (noninverting) CDS mode. 3 = invalid. Do not use. |
| | [16:10] [27:17] | 0 | | TESTMODE Unused | Test operation only. Set to 0. Set unused bits to 0. |
| 01 | [1:0] | 0 | SCK | TESTMODE | Test operation only. Set to 0. |
| | [2] | 0 | | GRAYENCODE | Gray coding ADC outputs. 0 = disable. 1 = enable. |
| | [3] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [4] | 1 | | TESTMODE | Test operation only. Set to 0. |
| | [27:5] | | | Unused | Set unused bits to 0. |
| 02 | [0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 03 | [23:0] | FFFFFF | | TESTMODE | Test operation only. Set to FFFFFFFF. |
| | [27:24] | | | Unused | Set unused bits to 0. |
| 04 | [1:0] | 1 | VD | CDSGAIN | CDS gain setting. 0 = -3 dB. 1 = 0 dB (default). 2 = +3 dB. 3 = +6 dB. |
| | [27:2] | | | Unused | Set unused bits to 0. |
| 05 | [9:0] | F | VD | VGAGAIN | VGA gain. 6 dB to 42 dB in 0.035 dB per step. |
| | [27:10] | | | Unused | Set unused bits to 0. |
| 06 | [9:0] | 1EC | VD | CLAMPLEVEL | Optical black clamp level; 0 LSB to 1023 LSB (1 LSB per step). |
| | [27:10] | | | Unused | Set unused bits to 0. |

AD9979

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|------------------|---------------|-------------|-----------|---|
| 07 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 08 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 09 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 0A | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 0B | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 0C | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 0D | [0] | 0 | VD | CLIDIVIDE | CLI divide. 1 = divide CLI input frequency by 2. |
| | [3:1] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [27:4] | | | Unused | Set unused bits to 0. |
| 0E | [27:0] | | | Unused | Set unused register to 0, if accessed. |
| 0F | [27:0] | | | Unused | Set unused register to 0, if accessed. |

Table 25. Miscellaneous Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|----------|------------------|---------------|-------------|-------------|--|
| 10 | [0] | 0 | SCK | SW_RST | Software reset. Bit self-clears to 0 when a reset occurs. 1 = reset Address 0x00 to Address 0xFF to default values. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 11 | [0] | 0 | VD | OUT_CONTROL | Output control. 0 = make all outputs dc inactive. 1 = enable outputs at next VD edge. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 12 | [1:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [27:2] | | | Unused | Set unused bits to 0. |
| 13 | [0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 14 | [0] | 0 | SCK | TGCORE_RST | Timing core reset bar. 0 = hold in reset. 1 = resume operation. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 15 | [0] | 0 | SCK | CLI_BIAS | Enable bias for CLI input (see Figure 9). 0 = disable bias (CLI input is dc-coupled). 1 = enable bias (CLI input is ac-coupled). |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 16 | [0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [27:1] | | | Unused | Set unused bits to 0. |
| 17 | [12:0] | 0 | SCK | UPDATE | Serial interface update line. Sets the line (HD) within the field to update the VD-updated registers. Disabled when PREVENTUP = 1. |
| | [13] | 0 | | PREVENTUP | Prevents normal update of VD-updated registers. 0 = normal update at VD. 1 = prevent update of VD-updated registers. |
| | [27:14] | | | Unused | Set unused bits to 0. |
| 18 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 19 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 1A to 1F | [27:0] | | | Unused | Set unused registers to 0. |

Table 26. VD/HD Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|----------------------------|---------------|-------------|-----------------------------------|--|
| 20 | [0] [27:1] | 0 | | TESTMODE Unused | Test operation only. Set to 0. Set unused bits to 0. |
| 21 | [0] [2:1] [27:3] | 0 0 | SCK | VDHDPOL TESTMODE Unused | VD/HD active polarity. 0 = active low. 1 = active high. Test operation only. Set to 0. Set unused bits to 0. |
| 22 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |

Table 27. I/O Control Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|--|--------------------------------|-------------|--|---|
| 23 | [0] [1] [2] [3] [4] [7:5] [27:8] | 0 0 0 0 0 1 | SCK | TESTMODE TESTMODE IO_NVR DATA_NVR TESTMODE HCLKMODE Unused | Test operation only. Set to 0. Test operation only. Set to 0. IOVDD voltage range for VD, HD, SCK, SDATA, and SL. ¹ 0 = 1.8 V. 1 = 3.3 V. DRVDD voltage range. Test operation only. Set to 0. Selects HCLK output configuration (see Table 8). Set unused bits to 0. |
| 24 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 25 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 26 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |
| 27 | [27:0] | 0 | | TESTMODE | Test operation only. Set to 0. |

¹ The inputs/outputs are 3 V tolerant, so there is no problem having higher than 1.8 V inputs at startup; however, this register needs to be set to 1 at initialization if using higher than 1.8 V supplies.

Table 28. Mode Control Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|--|-----------------------|-------------|--|--|
| 28 | [4:0] [27:5] | 0 | VD | HPATNUM Unused | Total number of H-pattern groups. Set unused bits to 0. |
| 29 | [27:0] | | | Unused | Set unused register to 0, if accessed. |
| 2A | [2:0] [27:3] | 0 | VD | FIELDNUM Unused | Total number of fields (set to 1 for single-field operation). Set unused bits to 0. |
| 2B | [4:0] [9:5] [14:10] [19:15] [24:20] [27:25] | 0 0 0 0 0 | VD | FIELD_SEL1 FIELD_SEL2 FIELD_SEL3 FIELD_SEL4 FIELD_SEL5 Unused | Selected first field. Selected second field. Selected third field. Selected fourth field. Selected fifth field. Set unused bits to 0. |
| 2C | [4:0] [9:5] [27:10] | 0 0 | VD | FIELD_SEL6 FIELD_SEL7 Unused | Selected sixth field. Selected seventh field. Set unused bits to 0. |
| 2D | [27:0] | | | Unused | Set unused register to 0, if accessed. |
| 2E | [27:0] | | | Unused | Set unused register to 0, if accessed. |
| 2F | [27:0] | | | Unused | Set unused register to 0, if accessed. |

Table 29. Timing Core Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|------------------|---------------|-------------|-------------|--|
| 30 | [5:0] | 0 | SCK | H1POSLOC | H1 rising edge location. |
| | [7:6] | | | Unused | Set unused bits to 0. |
| | [13:8] | 20 | | H1NEGLOC | H1 falling edge location. |
| | [15:14] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [16] | 1 | | H1POL | H1 polarity control. 0 = inverse of Figure 19. 1 = no inversion. |
| | [27:17] | | | Unused | Set unused bits to 0. |
| 31 | [5:0] | 0 | SCK | H2POSLOC | H2 rising edge location. |
| | [7:6] | | | Unused | Set unused bits to 0. |
| | [13:8] | 20 | | H2NEGLOC | H2 falling edge location. |
| | [15:14] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [16] | 1 | | H2POL | H2 polarity control. 0 = inverse of Figure 19. 1 = no inversion. |
| | [27:17] | | | Unused | Set unused bits to 0. |
| 32 | [5:0] | 0 | SCK | HLPOSLOC | HL rising edge location. |
| | [7:6] | | | Unused | Set unused bits to 0. |
| | [13:8] | 20 | | HLNEGLOC | HL falling edge location. |
| | [15:14] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [16] | 1 | | HLPOL | HL polarity control. 0 = inverse of Figure 19. 1 = no inversion. |
| | [27:17] | | | Unused | Set unused bits to 0. |
| 33 | [5:0] | 0 | SCK | RGPOSLOC | RG rising edge location. |
| | [7:6] | | | Unused | Set unused bits to 0. |
| | [13:8] | 10 | | RGNEGLOC | RG falling edge location. |
| | [15:14] | 0 | | TESTMODE | Test operation only. Set to 0. |
| | [16] | 1 | | RGPOL | RG polarity control. 0 = inverse of Figure 19. 1 = no inversion. |
| | [27:17] | | | Unused | Set unused bits to 0. |
| 34 | [0] | 0 | SCK | H1BLKRETIME | Retime H1 HBLK to internal clock. ¹ 0 = no retime. 1 = enable retime. |
| | [1] | 0 | | H2BLKRETIME | Retime H2 HBLK to internal clock. ^{1,2} |
| | [2] | 0 | | HLBLKRETIME | Retime HL HBLK to internal clock. ^{1,2} |
| | [3] | 0 | | HL_HBLK_EN | Enables HBLK for HL output. 0 = disable. 1 = enable. |
| | [7:4] | 0 | | HCLK_WIDTH | Enables wide horizontal clocks during HBLK interval. 0 = disable (see Table 12). |
| | [27:8] | | | Unused | Set unused bits to 0. |

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|------------------|---------------|-------------|-------------|--|
| 35 | [2:0] | 1 | SCK | H1DRV | H1 drive strength. 0 = off. 1 = 4.3 mA. 2 = 8.6 mA. 3 = 12.9 mA. 4 = 17.2 mA. 5 = 21.5 mA. 6 = 25.8 mA. 7 = 30.1 mA. |
| | [3] | | | Unused | Set unused bits to 0. |
| | [6:4] | 1 | | H2DRV | H2 drive strength. ³ |
| | [7] | | | Unused | Set unused bits to 0. |
| | [10:8] | 1 | | H3DRV | H3 drive strength. ³ |
| | [11] | | | Unused | Set unused bits to 0. |
| | [14:12] | 1 | | H4DRV | H4 drive strength. ³ |
| | [15] | | | Unused | Set unused bits to 0. |
| | [18:16] | 1 | | HLDRV | HL drive strength. ³ |
| | [19] | | | Unused | Set unused bits to 0. |
| 36 | [22:20] | 1 | SCK | RGDRV | RG drive strength. ³ |
| | [27:23] | | | Unused | Set unused bits to 0. |
| | [5:0] | 0 | | SHDLOC | SHD sampling edge location. |
| | [11:6] | 20 | | SHPLOC | SHP sampling edge location. |
| 37 | [17:12] | 10 | SCK | SHPWIDTH | SHP width. Controls input dc restore switch active time. |
| | [27:18] | | | Unused | Set unused bits to 0. |
| | [5:0] | 0 | | DOUTPHASEP | DOUT positive edge phase control. |
| | [11:6] | 20 | | DOUTPHASEN | DOUT negative edge phase control. Set DOUTPHASEN = DOUTPHASEP + 0x20. |
| | [12] | 0 | | DCLKMODE | 0 = DCLK tracks DOUT phase. 1 = DCLK is CLI post-Schmitt trigger and postdivider when CLIDIVIDE = 1. |
| | [14:13] | 2 | | CLKDATA_SEL | Data output clock selection. 0 = no delay. 1 = ~4 ns. 2 = ~8 ns. 3 = ~12 ns. |
| 38 | [15] | 0 | SCK | INV_DCLK | 0 = no inversion. 1 = invert DCLK to output. |
| | [27:16] | | | Unused | Set unused bits to 0. |
| 39 | [27:0] | | | Unused | Set unused register to 0 if accessed. |
| 3A | [27:0] | | | Unused | Set unused register to 0 if accessed. |
| 3B | [27:0] | | | Unused | Set unused register to 0 if accessed. |
| 3C | [27:0] | | | Unused | Set unused register to 0 if accessed. |
| 3D | [27:0] | | | Unused | Set unused register to 0 if accessed. |

¹ Recommended setting is enable retime. Enabling retime adds one cycle delay to programmed HBLK positions.

² See Address 34, Bit 0 for setting options.

³ See Address 35, Bits[2:0] for setting options.

AD9979

Table 30. Test Registers—Do Not Access

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|----------|---------------------------|---------------|-------------|--------------------------------|--|
| 3E | [18:0] [27:19] | 4B020 | | TESTMODE Unused | Test operation only. Set to 4B020. Set unused bits to 0. |
| 3F | [27:0] | | | Unused | Set unused register to 0, if accessed. |
| 40 | [3:0] [9:4] [27:10] | F 0 | | TESTMODE TESTMODE Unused | Test operation only. Set to F, if accessed. Test operation only. Set to 0. Set unused bits to 0. |
| 41 to 4F | [27:0] | | | Unused | Set unused registers to 0, if accessed. |

Table 31. Shutter and GPIO Registers

| Address | Data Bits | Default Value | Update Type | Name | Description |
|---------|--|---|-------------|---|---|
| 50 | [2:0] [27:3] | 0 | VD | PRIMARY_ACTION Unused | Selects action for primary and secondary counters. 0 = idle (do nothing). Auto-reset on VD. 1 = activate counter. Primary: auto-exposure/read. 2 = RapidShot. Wrap/repeat counter. 3 = ShotTimer. Delay start of count. 4 = test operation only. 5 = test operation only. 6 = test operation only. 7 = force to idle. Set unused bits to 0, if accessed. |
| 51 | [3:0] [7:4] [8] [27:9] | 0 0 0 | VD | PRIMARY_MAX PRIMARY_DELAY TESTMODE Unused | Primary counter maximum value. Number of fields to delay before the next count (exposure) starts. Test operation only. Set to 0. Set unused bits to 0, if accessed. |
| 52 | [1:0] [3:2] [5:4] [6] [7] [9:8] [13:10] [27:14] | 0 0 0 0 0 0 0 | VD | GP1_PROTOCOL GP2_PROTOCOL GP_LINE_MODE GP1_POL GP2_POL GP_LUT_EN GP12_LUT Unused | Selects protocol for general-purpose signal GPO1. 0 = idle. 1 = no counter association. 2 = link to primary. 3 = primary repeat. Selects protocol for general-purpose signal GPO2. ¹ Enables general-purpose output signals on every line. 0 = disable. 1 = enable. GPO1 low/high start polarity. GPO2 low/high start polarity. Use result from LUT or else GPO is unaltered. Bit [8] = GPO1 enable. Bit [9] = GPO2 enable. Two-input LUT results. For example, {GP12_LUT} ← [GPO2:GPO1] {0, 1, 1, 0} = GPO2 XOR GPO1. {1, 1, 1, 0} = GPO2 OR GPO1. {0, 1, 1, 1} = GPO2 NAND GPO1. {1, 0, 0, 0} = GPO2 AND GPO1. Set unused bits to 0, if accessed. |

| Address | Data Bits | Default Value | Update Type | Name | Description |
|----------|-----------|---------------|-------------|-----------------|---|
| 53 | [1:0] | 0 | VD | GPO_OUTPUT_EN | Enable both GPOs. 0 = both disabled. 3 = both enabled. |
| | [3:2] | 0 | | SEL_GPO1 | Select signal for GPO1 output. 0 = GPO. 1 = CLPOB. 2 = PBLK. 3 = DLL_SIGNAL_GPO. |
| | [5:4] | 0 | | SEL_GPO2 | Select signal for GPO2 output. ² |
| | [7:6] | 0 | | SEL_HS_GPO1 | Select which high speed timing signal is used for GPO1 output. 0 = delayed CLI. 1 = delayed ADC output latch clock. 2 = delayed SHD sample clock. 3 = delayed SHP sample clock. |
| | [9:8] | 0 | | SEL_HS_GPO2 | Select which high speed timing signal is used for GPO2 output. ³ |
| | [10] | 0 | | HBLK_EXT | Enable external HBLK signal to be an input to GPO2. |
| | [27:11] | | | Unused | Set unused bits to 0 if accessed. |
| 54 | [3:0] | 0 | VD | GPT1_TOG1_FIELD | General-Purpose Signal 1, first toggle position, field location. |
| | [12:4] | | | Unused | Set unused bits to 0 if accessed. |
| | [25:13] | 0 | | GPT1_TOG1_LINE | General-Purpose Signal 1, first toggle position, line location. |
| | [27:26] | | | Unused | Set unused bits to 0 if accessed. |
| 55 | [12:0] | 0 | VD | GPT1_TOG1_PIXEL | General-Purpose Signal 1, first toggle position, pixel location. |
| | [16:13] | 0 | | GPT1_TOG2_FIELD | General-Purpose Signal 1, second toggle position, field location. |
| | [27:19] | | | Unused | Set unused bits to 0 if accessed. |
| 56 | [12:0] | 0 | VD | GPT1_TOG2_LINE | General-Purpose Signal 1, second toggle position, line location. |
| | [25:13] | 0 | | GPT1_TOG2_PIXEL | General-Purpose Signal 1, second toggle position, pixel location. |
| | [27:25] | | | Unused | Set unused bits to 0 if accessed. |
| 57 | [3:0] | 0 | VD | GPT2_TOG1_FIELD | General-Purpose Signal 2, first toggle position, field location. |
| | [12:4] | | | Unused | Set unused bits to 0 if accessed. |
| | [25:13] | 0 | | GPT2_TOG1_LINE | General-Purpose Signal 2, first toggle position, line location. |
| | [27:26] | | | Unused | Set unused bits to 0 if accessed. |
| 58 | [12:0] | 0 | VD | GPT2_TOG1_PIXEL | General-Purpose Signal 2, first toggle position, pixel location. |
| | [16:13] | 0 | | GPT2_TOG2_FIELD | General-Purpose Signal 2, second toggle position, field location. |
| | [27:19] | | | Unused | Set unused bits to 0 if accessed. |
| 59 | [12:0] | 0 | VD | GPT2_TOG2_LINE | General-Purpose Signal 2, second toggle position, line location. |
| | [25:13] | 0 | | GPT2_TOG2_PIXEL | General-Purpose Signal 2, second toggle position, pixel location. |
| | [27:25] | | | Unused | Set unused bits to 0 if accessed. |
| 5A to 5F | [27:0] | | | Unused | Set unused registers to 0 if accessed. |

¹ See Address 52, Bits[1:0] for setting options.

² See Address 53, Bits[3:2] for setting options.

³ See Address 53, Bits[7:6] for setting options.

Table 32. Update Control Registers

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|---------|------------------|---------------|-------------|-----------------|--|
| 60 | [15:0] | 1803 | SCK | AFE_UPDT_SCK | Enable SCK update of AFE registers. Each bit corresponds to one address location. AFE_UPDT_SCK[0] = 1; update Address 0x00 on SCK rising edge. AFE_UPDT_SCK[1] = 1; update Address 0x01 on SCK rising edge. ... AFE_UPDT_SCK[15] = 1; update Address 0x0F on SCK rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 61 | [15:0] | E7FC | SCK | AFE_UPDT_VD | Enable VD update of AFE registers. Each bit corresponds to one address location. AFE_UPDT_VD[0] = 1; update Address 0x00 on VD rising edge. AFE_UPDT_VD[1] = 1; update Address 0x01 on VD rising edge. ... AFE_UPDT_VD[15] = 1; update Address 0x0F on VD rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 62 | [15:0] | F8FD | SCK | MISC_UPDT_SCK | Enable SCK update of miscellaneous registers. Each bit corresponds to one address location. MISC_UPDT_SCK[0] = 1; update Address 0x10 on SCK rising edge. MISC_UPDT_SCK[1] = 1; update Address 0x11 on SCK rising edge. ... MISC_UPDT_SCK[15] = 1; update Address 0x1F on SCK rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 63 | [15:0] | 0702 | SCK | MISC_UPDT_VD | Enable VD update of miscellaneous registers. Each bit corresponds to one address location. MISC_UPDT_VD[0] = 1; update Address 0x10 on VD rising edge. MISC_UPDT_VD[1] = 1; update Address 0x11 on VD rising edge. ... MISC_UPDT_VD[15] = 1; update Address 0x1F on VD rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 64 | [15:0] | FFF9 | SCK | VDHD_UPDT_SCK | Enable SCK update of VDHD registers. Each bit corresponds to one address location. VDHD_UPDT_SCK[0] = 1; update Address 0x20 on SCK rising edge. VDHD_UPDT_SCK[1] = 1; update Address 0x21 on SCK rising edge. ... VDHD_UPDT_SCK[15] = 1; update Address 0x22 on SCK rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 65 | [15:0] | 0006 | SCK | VDHD_UPDT_VD | Enable VD update of VDHD registers. Each bit corresponds to one address location. VDHD_UPDT_SCK[0] = 1; update Address 0x20 on VD rising edge. VDHD_UPDT_SCK[1] = 1; update Address 0x21 on VD rising edge. ... VDHD_UPDT_SCK[15] = 1; update Address 0x22 on VD rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |
| 66 | [15:0] | FFFF | SCK | TGCORE_UPDT_SCK | Enable SCK update of timing core registers. Each bit corresponds to one address location. TGCORE_UPDT_SCK[0] = 1; update Address 0x30 on SCK rising edge. TGCORE_UPDT_SCK[1] = 1; update Address 0x31 on SCK rising edge. ... TGCORE_UPDT_SCK[15] = 1; update Address 0x37 on SCK rising edge. Set unused bits to 0, if accessed. |
| | [27:16] | | | Unused | |

| Address | Data Bit Content | Default Value | Update Type | Name | Description |
|----------|------------------|---------------|-------------|----------------|---|
| 67 | [15:0] | 0000 | SCK | TGCORE_UPDT_VD | Enable VD update of timing core registers. Each bit corresponds to one address location. TGCORE_UPDT_VD[0] = 1; update Address 0x30 on VD rising edge. TGCORE_UPDT_VD[1] = 1; update Address 0x31 on VD rising edge. ... TGCORE_UPDT_VD[15] = 1; update Address 0x37 on VD rising edge. |
| | [27:16] | | | Unused | Set unused bits to 0, if accessed. |
| 68 to 72 | [27:0] | | | Unused | Set unused registers to 0, if accessed. |

Table 33. HPAT Registers (HPAT Registers Always Start at Address 0x800)

| Address | Data Bit Content | Default Value ¹ | Update Type | Name | Description |
|---------|------------------|----------------------------|-------------|------------|---|
| 00 | [12:0] | X | SCP | HBLKTOGO1 | First HBLK toggle position for odd lines, or RA0H1REPA/RA0H1REPB/RA0H1REPC. |
| | [25:13] | X | | HBLKTOGO2 | Second HBLK toggle position for odd lines, or RA1H1REPA/RA1H1REPB/RA1H1REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 01 | [12:0] | X | SCP | HBLKTOGO3 | Third HBLK toggle position for odd lines, or RA2H1REPA/RA2H1REPB/RA2H1REPC. |
| | [25:13] | X | | HBLKTOGO4 | Fourth HBLK toggle position for odd lines, or RA3H1REPA/RA3H1REPB/RA3H1REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 02 | [12:0] | X | SCP | HBLKTOGO5 | Fifth HBLK toggle position for odd lines, or RA4H1REPA/RA4H1REPB/RA4H1REPC. |
| | [25:13] | X | | HBLKTOGO6 | Sixth HBLK toggle position for odd lines, or RA5H1REPA/RA5H1REPB/RA5H1REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 03 | [12:0] | X | SCP | HBLKTOGE1 | First HBLK toggle position for even lines, or RA0H2REPA/RA0H2REPB/RA0H2REPC. |
| | [25:13] | X | | HBLKTOGE2 | Second HBLK toggle position for even lines, or RA1H2REPA/RA1H2REPB/RA1H2REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 04 | [12:0] | X | SCP | HBLKTOGE3 | Third HBLK toggle position for even lines, or RA2H2REPA/RA2H2REPB/RA2H2REPC. |
| | [25:13] | X | | HBLKTOGE4 | Fourth HBLK toggle position for even lines, or RA3H2REPA/RA3H2REPB/RA3H2REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 05 | [12:0] | X | SCP | HBLKTOGE5 | Fifth HBLK toggle position for even lines, or RA4H2REPA/RA4H2REPB/RA4H2REPC. |
| | [25:13] | X | | HBLKTOGE6 | Sixth HBLK toggle position for even lines, or RA5H2REPA/RA5H2REPB/RA5H2REPC. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 06 | [12:0] | X | SCP | HBLKSTARTA | HBLK Repeat Area Start Position A. Used during HBLK Mode 2. |
| | [25:13] | X | | HBLKSTARTB | HBLK Repeat Area Start Position B. Used during HBLK Mode 2. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 07 | [12:0] | X | SCP | HBLKSTARTC | HBLK Repeat Area Start Position C. Used during HBLK Mode 2. |
| | [27:13] | | | Unused | Set unused bits to 0. |

AD9979

| Address | Data Bit Content | Default Value ¹ | Update Type | Name | Description |
|---------|------------------|----------------------------|-------------|--------------|---|
| 08 | [2:0] | X | SCP | HBLKALT_PAT1 | HBLK Pattern 1 order. Used during pixel mixing mode. |
| | [5:3] | X | | HBLKALT_PAT2 | HBLK Pattern 2 order. Used during pixel mixing mode. |
| | [8:6] | X | | HBLKALT_PAT3 | HBLK Pattern 3 order. Used during pixel mixing mode. |
| | [11:9] | X | | HBLKALT_PAT4 | HBLK Pattern 4 order. Used during pixel mixing mode. |
| | [14:12] | X | | HBLKALT_PAT5 | HBLK Pattern 5 order. Used during pixel mixing mode. |
| | [17:15] | X | | HBLKALT_PAT6 | HBLK Pattern 6 order. Used during pixel mixing mode. |
| | [19:18] | X | | HBLKMODE | HBLK mode selection. 0 = normal HBLK. 1 = pixel mixing mode. 2 = special pixel mixing mode. 3 = not used. |
| | [20] | X | | TESTMODE | Test operation only. Set to 0. |
| | [27:21] | | | Unused | Set unused bits to 0. |
| | [12:0] | X | | SCP | HBLKLEN |
| 09 | [20:13] | X | | HBLKREP | Number of HBLK repetitions in HBLK alternation modes. |
| | [21] | X | | HBLKMASK_H1 | Masking polarity for H1/H3 during HBLK. |
| | [22] | X | | HBLKMASK_H2 | Masking polarity for H2/H4 during HBLK. |
| | [27:23] | | | Unused | Set unused bits to 0. |
| 0A | [12:0] | X | SCP | HBLKSTART | HBLK start position used in pixel mixing modes. |
| | [25:13] | X | | HBLKEND | HBLK end position used in pixel mixing modes. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 0B | [27:0] | X | | TESTMODE | Test operation only. Set to 0. |
| 0C | [12:0] | X | SCP | CLPOB0_TOG1 | CLPOB0 Toggle Position 1. |
| | [25:13] | X | | CLPOB0_TOG2 | CLPOB0 Toggle Position 2. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 0D | [12:0] | X | SCP | CLPOB1_TOG1 | CLPOB1 Toggle Position 1. |
| | [25:13] | X | | CLPOB1_TOG2 | CLPOB1 Toggle Position 2. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 0E | [12:0] | X | SCP | PBLK0_TOG1 | PBLK0 Toggle Position 1. |
| | [25:13] | X | | PBLK0_TOG2 | PBLK0 Toggle Position 2. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 0F | [12:0] | X | SCP | PBLK1_TOG1 | PBLK1 Toggle Position 1. |
| | [25:13] | X | | PBLK1_TOG2 | PBLK1 Toggle Position 2. |
| | [27:26] | | | Unused | Set unused bits to 0. |

¹ X = Don't care.

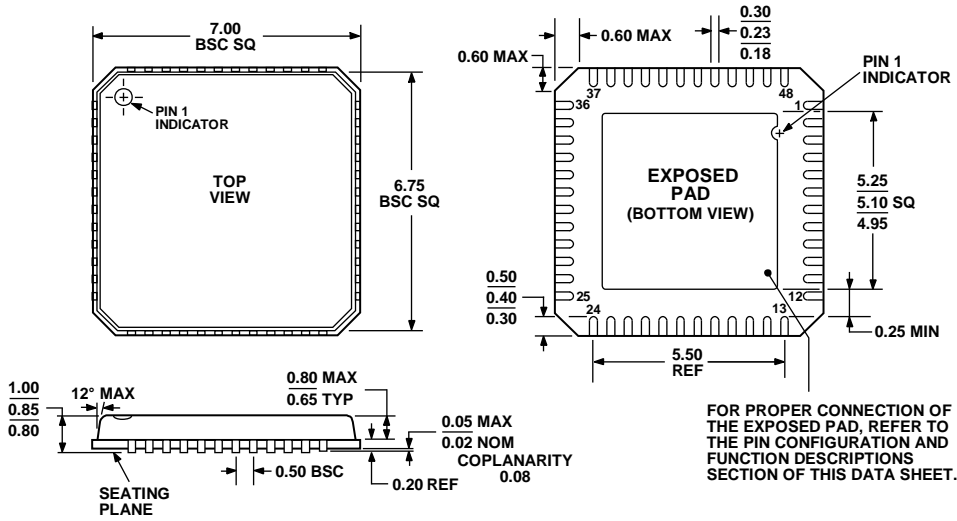
Table 34. Field Registers

| Address | Data Bit Content | Default Value ¹ | Update Type | Name | Description |
|---------|------------------|----------------------------|-------------|--------|-----------------------------|
| 00 | [12:0] | X | VD | SCP0 | Sequence Change Position 0. |
| | [25:13] | X | | SCP1 | Sequence Change Position 1. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 01 | [12:0] | X | VD | SCP2 | Sequence Change Position 2. |
| | [25:13] | X | | SCP3 | Sequence Change Position 3. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 02 | [12:0] | X | VD | SCP4 | Sequence Change Position 4. |
| | [25:13] | X | | SCP5 | Sequence Change Position 5. |
| | [27:26] | | | Unused | Set unused bits to 0. |
| 03 | [12:0] | X | VD | SCP6 | Sequence Change Position 6. |
| | [25:13] | X | | SCP7 | Sequence Change Position 7. |
| | [27:26] | | | Unused | Set unused bits to 0. |

| Address | Data Bit Content | Default Value ¹ | Update Type | Name | Description |
|---------|--|----------------------------|-------------|---|--|
| 04 | [12:0] [27:13] | X | VD | SCP8 Unused | Sequence Change Position 8. Set unused bits to 0. |
| 05 | [4:0] [9:5] [14:10] [19:15] [24:20] [27:25] | X X X X X | VD | HPAT_SEL0 HPAT_SEL1 HPAT_SEL2 HPAT_SEL3 HPAT_SEL4 Unused | Selected H-pattern for first region in field. Selected H-pattern for second region in field. Selected H-pattern for third region in field. Selected H-pattern for fourth region in field. Selected H-pattern for fifth region in field. Set unused bits to 0. |
| 06 | [4:0] [9:5] [14:10] [19:15] [27:20] | X X X X | VD | HPAT_SEL5 HPAT_SEL6 HPAT_SEL7 HPAT_SEL8 Unused | Selected H-pattern for sixth region in field. Selected H-pattern for seventh region in field. Selected H-pattern for eighth region in field. Selected H-pattern for ninth region in field. Set unused bits to 0. |
| 07 | [27:0] | | | Unused | Set unused register to 0. |
| 08 | [8:0] [17:9] [27:18] | X X | VD | CLPOB_POL CLPOB_PAT Unused | CLPOB start polarity settings. CLPOB pattern selector. 0 = CLPOB0_TOGx registers are used. 1 = CLPOB1_TOGx registers are used. Set unused bits to 0. |
| 09 | [12:0] [25:13] [27:26] | X X | VD | CLPOBMASKSTART1 CLOBMASKEND1 Unused | CLPOB Mask Region 1 start position. CLPOB Mask Region 1 end position. Set unused bits to 0. |
| 0A | [12:0] [25:13] [27:26] | X X | VD | CLPOBMASKSTART2 CLOBMASKEND2 Unused | CLPOB Mask Region 2 start position. CLPOB Mask Region 2 end position. Set unused bits to 0. |
| 0B | [12:0] [25:13] [27:26] | X X | VD | CLPOBMASKSTART3 CLOBMASKEND3 Unused | CLPOB Mask Region 3 start position. CLPOB Mask Region 3 end position. Set unused bits to 0. |
| 0C | [8:0] [17:9] [27:18] | X X | VD | PBLK_POL PBLK_PAT Unused | PBLK start polarity settings for Sequence 0 to Sequence 8. PBLK pattern selector. 0 = PBLK0_TOGx registers are used. 1 = PBLK1_TOGx registers are used. Set unused bits to 0. |
| 0D | [12:0] [25:13] [27:26] | X X | VD | PBLKMASKSTART1 PBLKMASKEND1 Unused | PBLK Mask Region 1 start position. PBLK Mask Region 1 end position. Set unused bits to 0. |
| 0E | [12:0] [25:13] [27:26] | X X | VD | PBLKMASKSTART2 PBLKMASKEND2 Unused | PBLK Mask Region 2 start position. PBLK Mask Region 2 end position. Set unused bits to 0. |
| 0F | [12:0] [25:13] [27:26] | X X | VD | PBLKMASKSTART3 PBLKMASKEND3 Unused | PBLK Mask Region 3 start position. PBLK Mask Region 3 end position. Set unused bits to 0. |

¹ X = Don't care.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 60. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
 7 mm × 7 mm Body, Very Thin Quad
 (CP-48-1)
 Dimensions shown in millimeters

080108-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| AD9979BCPZ | -25°C to +85°C | 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-48-1 |
| AD9979BCPZRL | -25°C to +85°C | 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-48-1 |

¹ Z = RoHS Compliant Part.

NOTES

AD9979

NOTES