High Speed Monolithic Pulse Width Modulator

AD9560

FEATURES

Up to 50 MHz Pulse Rate
Autocalibration on Chip
8-Bit Resolution
Center, Leading, Trailing Edge Modulation
Low Power: 335 mW
Single +5 V Operation

APPLICATIONS

Laser Printers
Gray Scale Capability
Resolution Enhancement
Add-In Boards
Digital Copiers (Photo Mode)
Color Copiers
Optical Disk Drives
Precision Pulse Placement

GENERAL DESCRIPTION

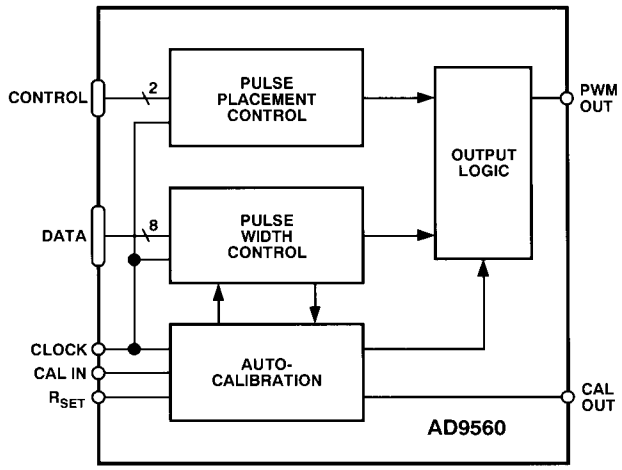
The AD9560 is a high speed, digitally programmable pulse width modulator (PWM). Output pulse width is proportional to an 8-bit DATA input value. Two additional CONTROL inputs determine if the pulse is placed at the beginning, middle, or end of the clock period. Pulse width and placement can be changed every clock cycle up to 50 MHz. All inputs and outputs are CMOS compatible.

Pulse width modulation is a proven and increasingly popular method for controlling gray scale and/or resolution enhancement in laser printers. The AD9560 provides a one chip solution to pixel-by-pixel control which yields much greater true resolution than "super pixel" techniques that are in use in present generation printers. High resolution is possible without significant increase in dot clock frequency which is necessary for "super pixel" methods.

Super pixel graphics, in effect, "trick the eye" by scattering different size pixels in varying densities. At a distance, these images appear to have high quality gray scale characteristics. Upon close inspection, a similar graphic utilizing pixel-by-pixel modulation demonstrates that resolution has been compromised to obtain gray scale.

In a basic laser printer or copier, the laser diode is either "on" or "off" for any pixel period. By utilizing the AD9560 ahead of the laser diode, each pixel can be controlled to increments equal to 1/256 of the pixel period. With the additional on-chip placement control (i.e., center, leading, and trailing edge modulation), 764 different pulse size/position options are theoretically possible.

FUNCTIONAL BLOCK DIAGRAM



For images containing text and graphics, mixed-mode operation may be required. The pulse width modulation feature of the AD9560 is disabled simply by inputting the codes 00_H and FF_H. The output will be logic zero and logic one respectively for the entire clock cycle.

The AD9560 pulse width modulator is fully self-contained, requiring only a single resistor (R_{SET}) to match the nominal full-scale range to the DOT CLOCK. An on-chip autocalibration circuit fine tunes the range and compensates for lot-to-lot variation of on-chip timing circuits.

With autocalibration and SOIC packaging the AD9560 is well suited for volume, automated assembly. In addition to 28-lead SOIC (AD9560KR), 28-pin P-DIP (AD9560KN) is also available. Both devices are rated over the commercial temperature range, 0°C to +70°C.

HIGHLIGHTS

1. Single +5 V power supply.
2. Autocalibration on chip.
3. Complete pulse placement flexibility.
4. High-resolution: 256 pulse widths.
5. Low power: 335 mW.
6. Automatic 00_H and FF_H decoding.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD9560—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; R_{SET} = 2.55 kΩ, CLOCK = 20 MHz, unless otherwise indicated)

Parameter	Temperature	Test Level	AD9560KN Min	AD9560KN Typ	AD9560KN Max	AD9560KR Min	AD9560KR Typ	AD9560KR Max	Units
RESOLUTION			8			8			Bits
ACCURACY (@ 1 MHz)									
Differential Linearity	+25°C	V		0.25			0.25		LSB
Integral Linearity[1]	+25°C	V		0.15			0.15		LSB
Ramp Misalignment	+25°C	V		1.5			1.5		LSB
ACCURACY (@ 20 MHz)									
Differential Linearity	+25°C	I		0.4			0.4	2.0	LSB
Integral Linearity[1]	+25°C	I		1.5			1.5	4.0	LSB
Ramp Misalignment	+25°C	V		1.5			1.5		LSB
DIGITAL INPUTS									
Logic "1" Voltage	Full	II	3.5			3.5			V
Logic "0" Voltage	Full	II			1.0			1.0	V
Input Current	Full	II			±1			±1	μA
Input Capacitance	+25°C	V		5			5		pF
Data Setup Time[2, 3]	+25°C	IV		−11.9	−8		−11.9	−8	ns
Data Hold Time[3]	+25°C	IV		14.4	19.2		14.4	19.2	ns
Data Setup Time[2, 3, 4]	Full	IV			−6			−6	ns
Data Hold Time[3, 4]	Full	IV			24			24	ns
Minimum Clock Pulse Width[3]	Full	V		7			7		ns
DYNAMIC PERFORMANCE[5]									
Maximum Trigger Rate	Full	IV	40	50		40	50		MHz
Minimum Propagation Delay (t_{PD})[6]	Full	II	24	34	44	24	34	44	ns
Minimum Propagation Delay TC	Full	V		98			98		ps/°C
Output Pulse Width @ Code 25	Full	V		5			5		ns
OutputPulse Width @ Code 254	Full	V		90			90		% Clock
Output Rise Time[7]	Full	II		2.1	3.0		2.1	3.0	ns
Output Fall Time[7]	Full	II		1.9	3.0		1.9	3.0	ns
DIGITAL OUTPUT									
Logic "1" Voltage[7]	Full	II	4.6			4.6			V
Logic "0" Voltage[7]	Full	II			0.4			0.4	V
POWER SUPPLY[5]									
Positive Supply Current (+5.0 V)	Full	II		67	87		67	87	mA
Power Dissipation	Full	II		335	435		335	435	mW
Power Supply Rejection Ratio (t_{PD}) Sensitivity (TEM)[8]	+25°C	V		3.5			3.5		ns/V

NOTES

[1]Measured at endpoints.

[2]When operating at or near maximum CLOCK rate, CLOCK edge should lead DATA change, making Data Setup Time negative. See Timing Diagram.

[3]Specified for CMOS logic driver.

[4]The time interval between Data Setup Time and Data Hold Time is relatively constant over the full temperature range. If an appropriate CMOS clock is used, the temperature coefficient of the data window will track the temperature coefficient of the input clock.

[5]Power supply should be maintained at +5 V, ±10% during normal operation.

[6]Measured from rising edge of clock to transition of overdrive codes 00_H and FF_H.

[7]Output load = 10 pF and 2 mA source/sink.

[8]Tested from +4.5 V to +5.5 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . . +7 V
Digital Input Voltage Range . . . . . −0.5 V to +5 V
Minimum R_{SET} . . . . . 500 Ω
Digital Output Current (Sourcing)[2] . . . . . 10 mA
Digital Output Current (Sinking)[2] . . . . . 10 mA
Operating Temperature Range[3]
D9560KN, KR . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
Lead Soldering Temperature (10 sec)[4] . . . . . +300°C

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability may be impaired. Functional operability under any of these conditions is not necessarily implied.
[2]CAL OUT should drive a single high impedance input.
[3]Typical thermal impedance:
28-Pin Plastic DIP θ_{JA} = 37°C/W; θ_{JC} = 10°C/W
28-Pin SOIC (Plastic) θ_{JA} = 46°C/W; θ_{JC} = 10°C/W
[4]When soldering surface mount packages in vapor phase equipment, temperature should not exceed 220°C for more than one minute.

EXPLANATION OF TEST LEVELS

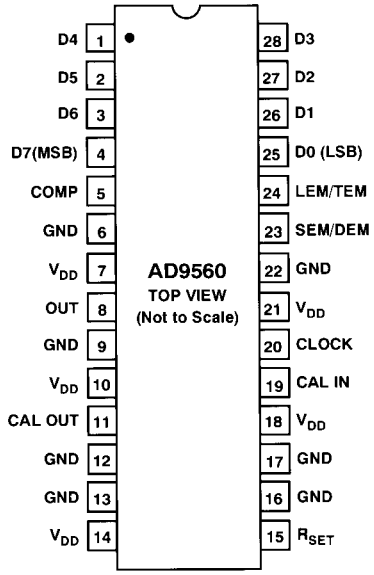
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option
AD9560KN	0°C to +70°C	28-Pin P-DIP	
AD9560KR	0°C to +70°C	28-Lead SOIC	

PIN CONFIGURATION
(P-DIP or SOIC)



PIN DESCRIPTIONS

1–4	D4–D7	Digital Data Bits; D7 is MSB
5	COMP	Bias Supply Bypass (0.47 μF)
6	GND	Ground Return
7	V_{DD}	+5 V Supply
8	PWM OUT	Pulse Width Modulated Output
9	GND	Ground Return
10	V_{DD}	+5 V Supply
11	CAL OUT	Calibration Complete Signal
12	GND	Ground Return
13	GND	Ground Return
14	V_{DD}	+5 V Supply
15	R_{SET}	Ramp Current Set Resistor
16	GND	Ground Return
17	GND	Ground Return
18	V_{DD}	+5 V Supply
19	CAL IN	Initiates Autocalibration
20	CLOCK	Dot Clock Input
21	V_{DD}	+5 V Supply
22	GND	Ground Return
23	SEM/DEM	Controls Single or Dual Edge Modulation
24	LEM/TEM	Controls Leading or Trailing Edge Modulation
25–28	D0–D3	Digital Data Inputs; D0 is LSB

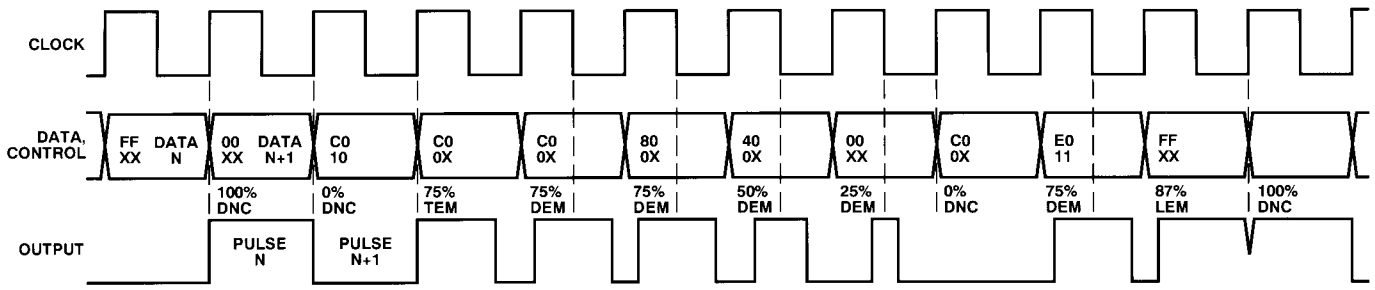


Figure 1. Pulse Pattern Example

THEORY OF OPERATION

General

The AD9560 is a mixed signal IC designed to facilitate high speed pulse width modulation in laser printers and copiers. In order to deliver superior linearity and speed while maintaining low power dissipation, it is fabricated in a BiCMOS process.

The AD9560's 8-bit pulse width resolution and pulse positioning capabilities combine to offer a high level of gray shading flexibility in laser beam printers or copiers. In addition to its pulse control, it also includes an autocalibration circuit to minimize external components and eliminate extra burden on the system microprocessor.

A parallel architecture comprising ramp generators, DACs, and comparators creates a group of pulses. These are combined in the output logic to form OUT pulses whose width and placement are representative of the 8-bit pulse width DATA and the pulse placement CONTROL inputs.

Modulation Modes

Positioning the width-controlled pulses at the beginning, middle, or end of the CLOCK period adds significantly to the flexibility of the AD9560. This is accomplished through CONTROL bits SEM/DEM and LEM/TEM. These acronyms represent single-edge modulation/dual-edge modulation; and leading-edge modulation/trailing-edge modulation. SEM/DEM and LEM/TEM are collectively identified as CONTROL.

Pulse positioning within the DOT CLOCK period is defined by the following CONTROL Truth Table:

SEM/DEM	LEM/TEM	Alignment
1	1	LEM (RHJ)
1	0	TEM (LHJ)
0	X	DEM (CJ)

Single-edge modulation offers two options in which one edge is modulated while the other remains fixed relative to the DOT CLOCK. For leading-edge modulation, the rising edge of the pulse is delayed from the leading edge of the DOT CLOCK proportional to DATA, and the falling edge remains fixed at the end of the DOT CLOCK period. This may also be called "right-hand justified" (RHJ).

Similarly, trailing-edge modulation has the rising edge fixed on the beginning of the DOT CLOCK period, and the falling edge delayed proportional to DATA. This can be called "left-hand justified" (LHJ).

Dual-edge modulation is often called "center justified" (CJ) because the delay of both edges vary relative to the DOT CLOCK. The rising edge is delayed from the leading edge of the CLOCK, and the falling edge is delayed from the center of the CLOCK period. Thus, with increasing values for DATA, pulse width increases with its center remaining constant proportional to the DOT CLOCK.

Like DATA, modulation control inputs SEM/DEM and LEM/TEM can be updated at the DOT CLOCK rate, up to 50 MHz.

Pulse Pattern Example

The diagram at the top of the page illustrates the output of the AD9560 with various DATA (Pins 1–4, 25–28) and CONTROL (Pins 23, 24) inputs. This does not take into account any delays, which will be explained later, but assumes an ideal timing relationship for clarity.

The top line shows the DOT CLOCK; the second shows DATA and CONTROL inputs being updated on the rising edge of CLOCK. DATA and CONTROL values are shown near the beginning of the DATA/CONTROL period. The third line shows the resulting pulse with an explanation of the pulse between the second and third lines.

The first DATA/CONTROL period is indicated as DATA N, and the second as DATA N+1. The second and third pulses are labeled as Pulse N and N+1, illustrating the one CLOCK period pipeline delay. The vertical dashed lines show the relevant point of reference of the CLOCK to each output pulse.

The CONTROL value number one is shown as XX; this means the value is not important because a 100% pulse will be output for any CONTROL value. Likewise, Pulse N is noted as 100%, DNC (do not care) noting that CONTROL value is unimportant.

The fourth DATA/CONTROL value is CO/0X, indicating that the level for LEM/TEM is unimportant when SEM/DEM is logic level zero (LL0).

Selecting R_{SET}

For the AD9560 to provide full range coverage of the CLOCK pulse period, the ramp time must be matched to the CLOCK period. All components for the ramp generators except R_{SET} are integrated in the AD9560. R_{SET} is customer selected, depending upon the DOT CLOCK frequency.

The ramps are generated by constant current sources charging on-chip capacitors. R_{SET} can be chosen in the range from approximately 1 kΩ for 50 MHz operation to 50 kΩ for 1 MHz. Because the absolute value of the on-chip capacitor can vary substantially, an autocalibration circuit is included to fine tune matching of ramp time to the DOT CLOCK period.

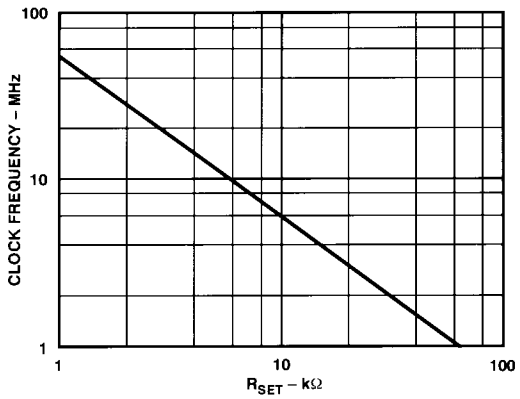


Figure 2. R_{SET} vs. CLOCK Frequency

Figure 2 shows approximate values for R_{SET} over the operating frequency range. For more precise determination, the following equation should be used:

$$R_{SET} = 10^{[10.951-1.033\ log(f)]}$$

where: f = CLOCK Frequency in Hz.

The closest value of 1% metal-film resistor should be used. This resistor will generate a current within the range of the auto-calibration circuit. Thus, the value for R_{SET} calculated for a particular print engine will be correct for device-to-device timing variations, even from different production lots.

Autocalibration

The AD9560 should be calibrated on power-up and any time normal operation is interrupted. The AD9560 will maintain its accuracy over its rated temperature range as long as power is applied.

Some high-precision printing applications may require periodic calibration during normal operation to assure consistency of print contrast from the lightest to the darkest shades. The frequency of calibration depends upon sensitivity of the laser print engine and/or significant ambient temperature variation.

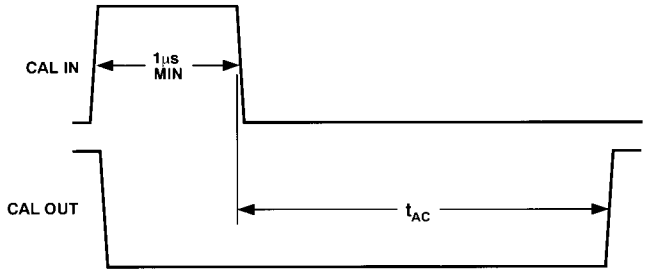


Figure 3. AutoCAL Timing

Autocalibration is initiated by applying a pulse of 1 µs minimum duration to Pin 19, CAL IN. The CLOCK pulse should be applied continuously during calibration. CAL IN should remain high for a minimum of 1 µs to allow the calibration current to settle to its lowest value. Also, during the CAL IN pulse, all internal logic is initialized for calibration and proper synchronization once calibration is complete; the falling edge of CAL IN initiates the Auto-Cal cycle.

Auto-Cal is not affected by the code applied to the DATA or CONTROL inputs. However, to ensure that no OUT pulses are generated during calibration, it is suggested that all digital inputs be held at logic zero.

On the falling edge of CAL IN, the calibration circuit contributes no additional current to the primary charging current controlled by R_{SET}. The calibration current is incremented on each 32nd CLOCK pulse until the full-scale ramp time is equal to the period of the CLOCK. With a maximum of 64 incremental increases, the maximum autocalibration time, t_{AC}, can be calculated by the equation:

$$t_{AC} = (32/f_C) \cdot 64$$

or:

$$t_{AC} = 2048 \cdot t_C$$

where: f_C = CLOCK frequency in hertz
t_C = CLOCK period in seconds

This yields the maximum time from the trailing edge of CAL IN to the rising edge of CAL OUT. As an example, the maximum time required for autocalibration for a system with clock frequency of 10 MHz is 204.8 µs.

APPLICATIONS

DATA Timing

Input DATA to the AD9560 is double buffered, resulting in a one-CLOCK-period delay for a given DATA word until its related output. Figure 4 illustrates timing of DATA relative to the CLOCK for worst case conditions, operating at 50 MHz.

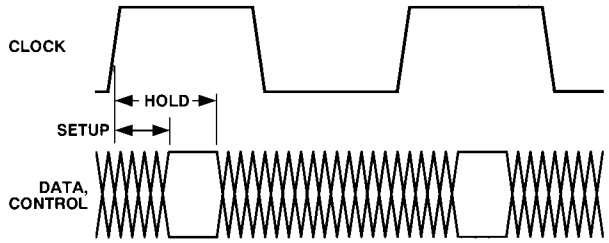


Figure 4. DATA and CONTROL Timing

A longer delay exists from the CLOCK input to the latching circuit than from the DATA inputs. Therefore, setup is a negative number, ranging from −6 ns to −16 ns over temperature. The DATA must remain valid from 12 ns to 24 ns after the rising edge of CLOCK.

At 50 MHz, the CLOCK period is 20 ns. At room temperature, with a worst case setup time of −8 ns, and worst case hold time of 19.2 ns, DATA should be updated in the window from 0 ns to 8 ns after the rising edge of CLOCK. Lower frequencies will have greater tolerance to DATA timing.

OUTPUT Delay

A propagation delay exists between the CLOCK and OUT pulses. The minimum propagation delay can be observed when alternating between codes 00_H and FF_H. OUT pulse transitions will typically occur 34 ns after the rising edge of CLOCK for 20 MHz operation. This delay is due to logic propagation and may vary from 24–44 ns over temperature.

An additional delay is incurred for any value other than 00_H and FF_H. This is due to nonlinear ramp effects. The first and last 5% of the ramp are unusable, so the OUT transition for TEM will be delayed by the logic propagation delay plus 5% of the CLOCK period.

For LEM, the fixed edge will occur after the logic prop delay plus 95% of a clock period. DEM will be centered at a point equal to the logic prop delay plus 50% of the CLOCK period.

Thus, for values other than 00_H and FF_H, the output will typically occur from 34 ns plus 5% to 34 ns plus 95% of CLOCK period at 20 MHz.

PWM Override

For the purposes of printing text, or any time absolute white or black is required, 00_H is decoded, and a 100% LL0 is output in the next CLOCK cycle. Likewise, FF_H is detected and the next pulse is 100% LL1.

Transfer Function

OUT pulse width increases with increasing DATA values. The DATA format is Binary. For convenience, the Hexadecimal format is used in this data sheet; i.e., FF_H represents decimal 255. As the heavy line of Figure 5 shows, the transfer function of the AD9560 is slightly nonideal.

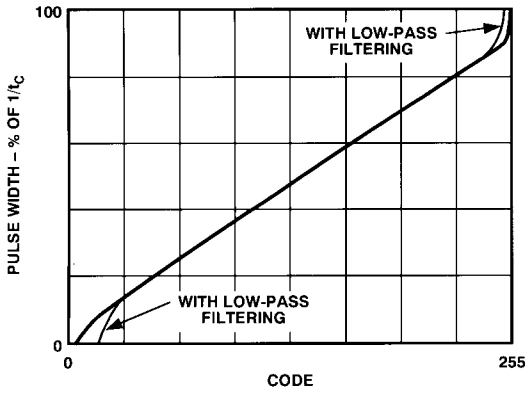


Figure 5. Transfer Function

An ideal transfer would give 0% (or 0 ns) pulse width for a code 00_H. As the code is incremented in steps of one, the pulse width would increase by 0.039% until it reached 100% for code FF_H.

The normal output (heavy line in Figure 5) shows no output for the first several codes. A pulse width approaching 0% would require zero rise and fall time on the pulse.

Finite rise time prevents the very narrow pulses near 00_H from reaching a valid logic level one (LL1) voltage. This produces a slew-rate-limited pulse increasing in width and amplitude, until a pulse of approximately 3–5 ns reaches a proper logic level. Thus, the transfer is nonlinear until about 3–5 ns pulse width (varies as a function of CLOCK frequency, i.e., for 1 MHz operation, an LSB is roughly 4 ns, so an output may be observed on code 01_H).

Attaining 99% or greater duty cycle would require ideal ramp characteristics. In reality, approximately 5% of the ramp is unusable at each end because of nonlinearity and settling characteristics. Even though the errors are at both ends, and affects timing vs. the CLOCK at beginning and end, they affect only the high end of the transfer function, since it is based on a percentage of pulse width. The normal transfer function (heavy line) shows code FE_H generating a 90% pulse and 100% for FF_H.

These nonideal characteristics also affect adjacent pulse relationships when modulation mode is changed pulse-to-pulse. The ramp errors affect both the rising and falling edges of the output. This can result in small gaps between pulses expected to be adjacent.

For example, a leading edge modulated (RHJ) pulse followed by a trailing edge modulated (LHJ) pulse should stay high from the rising edge of the first pulse to the falling edge of the second. However, a gap as much as 10% of the CLOCK period is possible. This is illustrated by the narrow glitch between the last two pulses of the pulse pattern example. The effect of this on image quality is dependent upon laser engine sensitivity.

If 90% maximum pulse width or unexpected 10% gaps prove to be a problem for a particular engine type, the effect can be minimized by low-pass filtering the digital output of the AD9560. This can be accomplished with an RC low-pass filter as shown in Figure 6. The effect on the transfer function is shown by the dashed lines in Figure 5.

The capacitance should be large enough to overcome variations in stray circuit capacitance. A 100 Ω resistor and 47 pF capacitor should produce the desired results at clock rates of 20 MHz or greater. Excessive stray capacitance may lead to overcorrection which reduces overall dynamic range. Reducing the resistor will alleviate this.

Logic Interface

When driving the AD9560 with very high slew rate logic, differential nonlinearity may degrade slightly. A resistor in series with the DATA lines, in conjunction with stray board and device capacitance, will slow down the fast edges. A resistor should not be inserted in the CLOCK line; its transitions should be as fast as possible to minimize jitter.

Circuit Connections

DATA, SEM/DEM, and LEM/TEM as well as the CLOCK must be updated at the DOT frequency of the printer. Thus, Figure 6 assumes these signals originating from a high speed ASIC. CAL IN and CAL OUT operate at speeds that any μP can control. The only support components required are R_{SET} and a 0.47 μF compensation capacitor. Depending upon CLOCK speed and engine sensitivity, an optional RC low-pass filter may be required to smooth the transfer function. This is discussed in more detail in the Transfer Function section.

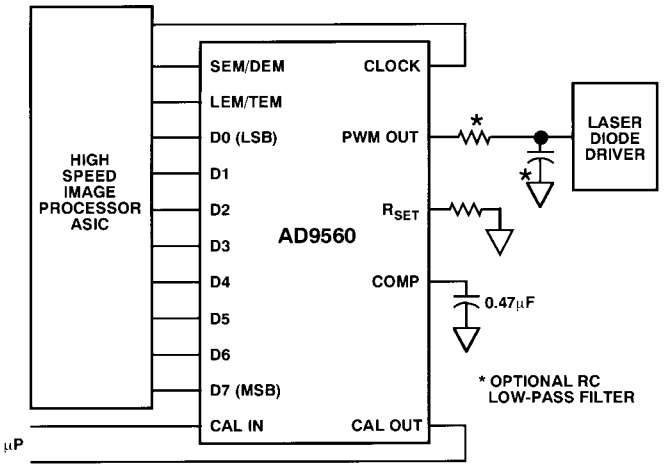


Figure 6. Connection Diagram

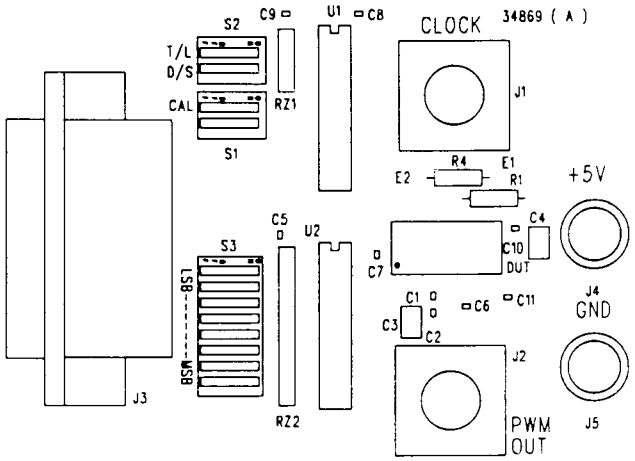


Figure 7. Evaluation Board Component Layout

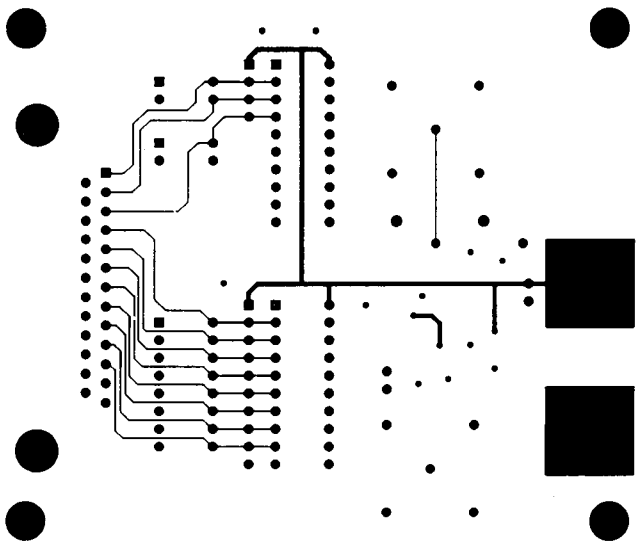


Figure 8. Evaluation Board Circuit Side [Evaluation Board Is 3.8 Inches (96.5 mm)by 3.2 Inches (83.8 mm)]

Grounding and Bypassing

Because the AD9560 utilizes analog circuits to achieve its superb pulse placement, caution must be exercised when incorporating it into the mostly digital controller card of a printer. A ground plane, isolated from the digital ground, is suggested.

Multiple ground and V_{DD} pins are utilized on the AD9560. Optimum performance results when all ground pins are connected to the single ground plane, and all V_{DD} pins are connected together and decoupled individually to the ground plane with 0.1 μF capacitors. In addition, at least one low frequency 10 μF capacitor should decouple V_{DD} near the AD9560.

The bias supply bypass, (COMP) Pin 5, should be decoupled with a 0.47 μF chip capacitor. This controls the frequency response of internal current control circuits. This value should be constant, regardless of the CLOCK frequency.

These specific recommendations along with normal high speed layout techniques will assure maximum performance over the specified clock range.

Evaluation Board

A fully populated and tested evaluation board is available to facilitate initial testing of the AD9560. The component and wiring side layouts are shown in Figure 7.

This board includes DIP switches for manual control of DATA, CONTROL, and CAL IN. It requires only a +5 V power supply, a pulse generator for CLOCK, and an oscilloscope for viewing the output pulses as various switch settings are employed.

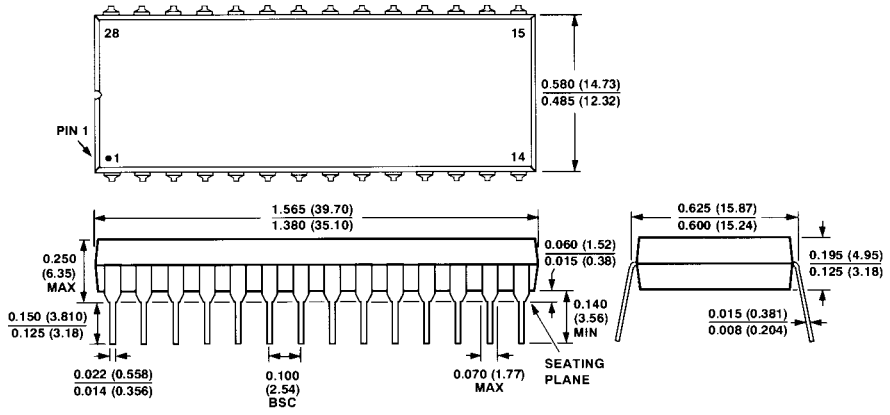
All inputs are also connected to a 25-pin I/O connector. This port can be used to test dynamic performance. On-board switches should all be in the "off" position. The connections are as follows:

Pin	Function
1	LEM/TEM
2	SEM/DEM
3	CAL IN
4	D0 (LSB)
5	D1
6	D2
7	D3
8	D4
9	D5
10	D6
11	D7 (MSB)

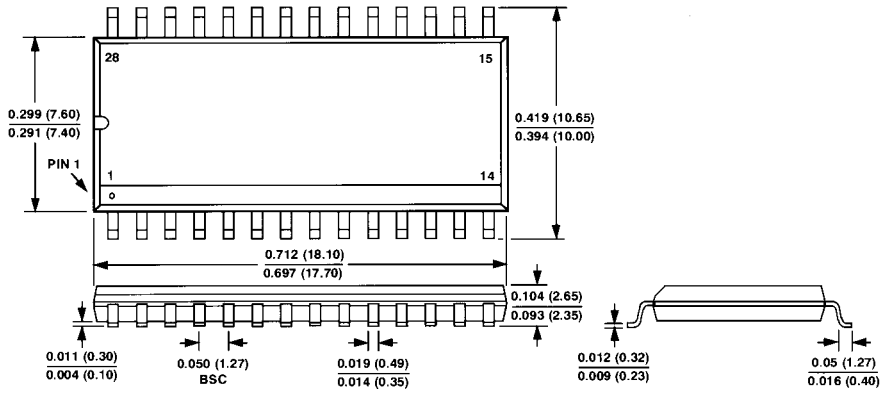
PACKAGE OUTLINE

Dimensions shown in inches and (mm)

28-Lead Plastic DIP
(Suffix N)



28-Lead Wide-Body Plastic SOIC
(Suffix R)



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