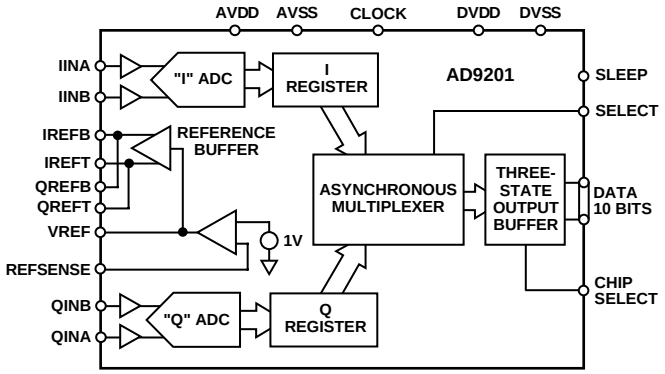
Dual Channel, 20 MHz 10-Bit Resolution CMOS ADC

AD9201

FEATURES

Complete Dual Matching ADCs
Low Power Dissipation: 215 mW (+3 V Supply)
Single Supply: 2.7 V to 5.5 V
Differential Nonlinearity Error: 0.4 LSB
On-Chip Analog Input Buffers
On-Chip Reference
Signal-to-Noise Ratio: 57.8 dB
Over Nine Effective Bits
Spurious-Free Dynamic Range: –73 dB
No Missing Codes Guaranteed
28-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9201 is a complete dual channel, 20 MSPS, 10-bit CMOS ADC. The AD9201 is optimized specifically for applications where close matching between two ADCs is required (e.g., I/Q channels in communications applications). The 20 MHz sampling rate and wide input bandwidth will cover both narrowband and spread-spectrum channels. The AD9201 integrates two 10-bit, 20 MSPS ADCs, two input buffer amplifiers, an internal voltage reference and multiplexed digital output buffers.

Each ADC incorporates a simultaneous sampling sample-and-hold amplifier at its input. The analog inputs are buffered; no external input buffer op amp will be required in most applications. The ADCs are implemented using a multistage pipeline architecture that offers accurate performance and guarantees no missing codes. The outputs of the ADCs are ported to a multiplexed digital output buffer.

The AD9201 is manufactured on an advanced low cost CMOS process, operates from a single supply from 2.7 V to 5.5 V, and consumes 215 mW of power (on 3 V supply). The AD9201 input structure accepts either single-ended or differential signals, providing excellent dynamic performance up to and beyond its 10 MHz Nyquist input frequencies.

PRODUCT HIGHLIGHTS

1. Dual 10-Bit, 20 MSPS ADCs
   A pair of high performance 20 MSPS ADCs that are optimized for spurious free dynamic performance are provided for encoding of I and Q or diversity channel information.
2. Low Power
   Complete CMOS Dual ADC function consumes a low 215 mW on a single supply (on 3 V supply). The AD9201 operates on supply voltages from 2.7 V to 5.5 V.
3. On-Chip Voltage Reference
   The AD9201 includes an on-chip compensated bandgap voltage reference pin programmable for 1 V or 2 V.
4. On-chip analog input buffers eliminate the need for external op amps in most applications.
5. Single 10-Bit Digital Output Bus
   The AD9201 ADC outputs are interleaved onto a single output bus saving board space and digital pin count.
6. Small Package
   The AD9201 offers the complete integrated function in a compact 28-lead SSOP package.
7. Product Family
   The AD9201 dual ADC is pin compatible with a dual 8-bit ADC (AD9281) and has a companion dual DAC product, the AD9761 dual DAC.

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AD9201–SPECIFICATIONS

(AVDD = +3 V, DVDD = +3 V, F_{SAMPLE} = 20 MSPS, VREF = 2 V, INB = 0.5 V, T_{MIN} to T_{MAX}, internal ref, differential input signal, unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Condition
RESOLUTION			10		Bits	
CONVERSION RATE	F_S			20	MHz	
DC ACCURACY						
Differential Nonlinearity	DNL		±0.4		LSB	REFT = 1 V, REFB = 0 V
Integral Nonlinearity	INL		1.2		LSB	
Differential Nonlinearity (SE)	DNL		±0.5	±1	LSB	REFT = 1 V, REFB = 0 V
Integral Nonlinearity (SE)	INL		±1.5	±2.5	LSB	
Zero-Scale Error, Offset Error	E_{ZS}		±1.5	±3.8	% FS	
Full-Scale Error, Gain Error	E_{FS}		±3.5	±5.4	% FS	
Gain Match			±0.5		LSB	
Offset Match			±5		LSB	
ANALOG INPUT						
Input Voltage Range	AIN	–0.5		AVDD/2	V	
Input Capacitance	C_{IN}		2		pF	
Aperture Delay	t_{AP}		4		ns	
Aperture Uncertainty (Jitter)	t_{AJ}		2		ps	
Aperture Delay Match			2		ps	
Input Bandwidth (–3 dB)	BW					
Small Signal (–20 dB)			240		MHz	
Full Power (0 dB)			245		MHz	
INTERNAL REFERENCE						
Output Voltage (1 V Mode)	VREF		1		V	REFSENSE = VREF
Output Voltage Tolerance (1 V Mode)			±10		mV	
Output Voltage (2 V Mode)	VREF		2		V	REFSENSE = GND
Output Voltage Tolerance (2 V Mode)			±15		mV	
Load Regulation (1 V Mode)				±28	mV	1 mA Load Current
Load Regulation (2 V Mode)			±15		mV	1 mA Load Current
POWER SUPPLY						
Operating Voltage	AVDD	2.7	3	5.5	V	AVDD – DVDD ≤ 2.3 V
	DRVDD	2.7	3	5.5	V	
Supply Current	I_{AVDD}		71.6		mA	AVDD = 3 V
	I_{DRVDD}		0.1		mA	
Power Consumption	P_D		215	245	mW	AVDD = DVDD = 3 V
Power-Down			15.5		mW	STBY = AVDD, Clock = AVSS
Power Supply Rejection	PSR		0.8	1.3	% FS	
DYNAMIC PERFORMANCE[1]						
Signal-to-Noise and Distortion	SINAD					
f = 3.58 MHz		55.6	57.3		dB	
f = 10 MHz			55.8		dB	
Signal-to-Noise	SNR					
f = 3.58 MHz		55.9	57.8		dB	
f = 10 MHz			56.2		dB	
Total Harmonic Distortion	THD					
f = 3.58 MHz			–69	–63.3	dB	
f = 10 MHz			–66.3		dB	
Spurious Free Dynamic Range	SFDR					
f = 3.58 MHz		–66	–73		dB	
f = 10 MHz			–70.5		dB	
Two-Tone Intermodulation Distortion[2]	IMD		–62		dB	f = 44.49 MHz and 45.52 MHz
Differential Phase	DP		0.1		Degree	NTSC 40 IRE Mod Ramp
Differential Gain	DG		0.05		%	F_S = 14.3 MHz
Crosstalk Rejection			68		dB	

Parameter	Symbol	Min	Typ	Max	Units	Condition
DYNAMIC PERFORMANCE (SE)[3]						
Signal-to-Noise and Distortion	SINAD					
f = 3.58 MHz			52.3		dB	
Signal-to-Noise	SNR					
f = 3.58 MHz			55.5		dB	
Total Harmonic Distortion	THD					
f = 3.58 MHz			–55		dB	
Spurious Free Dynamic Range	SFDR					
f = 3.58 MHz			–58		dB	
DIGITAL INPUTS						
High Input Voltage	V_{IH}	2.4			V	
Low Input Voltage	V_{IL}			0.3	V	
DC Leakage Current	I_{IN}		±6		µA	
Input Capacitance	C_{IN}		2		pF	
LOGIC OUTPUT (with DVDD = 3 V)						
High Level Output Voltage						
(I_{OH} = 50 µA)	V_{OH}		2.88		V	
Low Level Output Voltage						
(I_{OL} = 1.5 mA)	V_{OL}		0.095		V	
LOGIC OUTPUT (with DVDD = 5 V)						
High Level Output Voltage						
(I_{OH} = 50 µA)	V_{OH}		4.5		V	
Low Level Output Voltage						
(I_{OL} = 1.5 mA)	V_{OL}		0.4		V	
Data Valid Delay	t_{OD}		11		ns	
MUX Select Delay	t_{MD}		7		ns	
Data Enable Delay	t_{ED}		13		ns	C_L = 20 pF. Output Level to 90% of Final Value
Data High-Z Delay	t_{DHZ}		13		ns	
CLOCKING						
Clock Pulsewidth High	t_{CH}	22.5			ns	
Clock Pulsewidth Low	t_{CL}	22.5			ns	
Pipeline Latency			3.0		Cycles	

NOTES
[1]AIN differential 2 V p-p, REFT = 1.5 V, REFB = –0.5 V.
[2]IMD referred to larger of two input signals.
[3]SE is single ended input, REFT = 1.5 V, REFB = –0.5 V.
Specifications subject to change without notice.

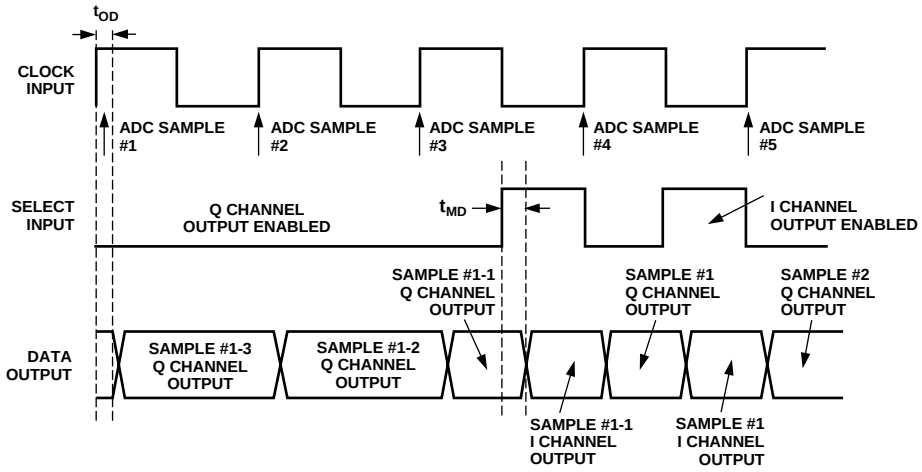


Figure 1. ADC Timing

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
AINA, AINB	AVSS	–1.0	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
REFSENSE	AVSS	–0.3	AVDD + 0.3	V
REFT, REFB	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature 10 sec			+300	°C

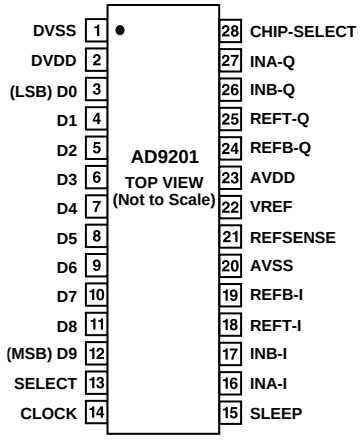
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9201ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9201-EVAL		Evaluation Board	

*RS = Shrink Small Outline.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DVSS	Digital Ground
2	DVDD	Digital Supply
3	D0	Bit 0 (LSB)
4	D1	Bit 1
5	D2	Bit 2
6	D3	Bit 3
7	D4	Bit 4
8	D5	Bit 5
9	D6	Bit 6
10	D7	Bit 7
11	D8	Bit 8
12	D9	Bit 9 (MSB)
13	SELECT	Hi I Channel Out, Lo Q Channel Out
14	CLOCK	Clock
15	SLEEP	Hi Power Down, Lo Normal Operation
16	INA-I	I Channel, A Input
17	INB-I	I Channel, B Input
18	REFT-I	Top Reference Decoupling, I Channel
19	REFB-I	Bottom Reference Decoupling, I Channel
20	AVSS	Analog Ground
21	REFSENSE	Reference Select
22	VREF	Internal Reference Output
23	AVDD	Analog Supply
24	REFB-Q	Bottom Reference Decoupling, Q Channel
25	REFT-Q	Top Reference Decoupling, Q Channel
26	INB-Q	Q Channel, B Input
27	INA-Q	Q Channel, A Input
28	CHIP-SELECT	Hi-High Impedance, Lo-Normal Operation

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSBs beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9201 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.