

### FEATURES

- Offset voltage: 2.5 mV maximum**
- Single-supply operation: 2.7 V to 5.5 V**
- Low noise: 8 nV/√Hz**
- Wide bandwidth: 24 MHz**
- Slew rate: 11 V/μs**
- Short-circuit output current: 120 mA**
- Qualified for automotive applications**
- No phase reversal**
- Low input bias current: 1 pA**
- Low supply current per amplifier: 2 mA maximum**
- Unity gain stable**

### APPLICATIONS

- Battery-powered instruments**
- Multipole filters**
- ADC front ends**
- Sensors**
- Barcode scanners**
- ASIC input or output amplifiers**
- Audio amplifiers**
- Photodiode amplifiers**
- Datapath/mux/switch control**

### GENERAL DESCRIPTION

The [AD8646](#) and the [AD8647](#) are the dual, and the [AD8648](#) is the quad, rail-to-rail, input and output, single-supply amplifiers featuring low offset voltage, wide signal bandwidth, low input voltage, and low current noise. The [AD8647](#) also has a low power shutdown function.

The combination of 24 MHz bandwidth, low offset, low noise, and very low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. The [AD8646/](#)

[AD8647/AD8648](#) offer high output drive capability, which is excellent for audio line drivers and other low impedance applications. The [AD8646](#) and [AD8648](#) are available for automotive applications (see the Ordering Guide).

Applications include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, barcode scanners, and multipole filters. The ability to swing rail to rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

### PIN CONFIGURATIONS

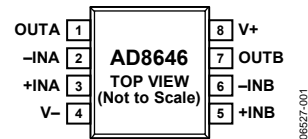


Figure 1. 8-Lead SOIC and MSOP

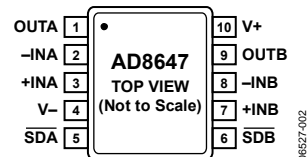


Figure 2. 10-Lead MSOP

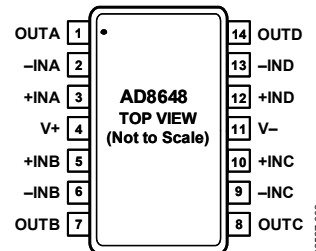


Figure 3. 14-Lead SOIC and TSSOP

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## REVISION HISTORY

### **Revision History: AD8646/AD8647/AD8648**

#### **8/2016—Rev. E to Rev. F**

Changes to Figure 18 and Figure 21 .....	9
Changes to Figure 39 .....	12

#### **3/2014—Rev. D to Rev. E**

Changes to Differential Input Voltage, Table 3 .....	6
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#### **4/2010—Rev. C to Rev. D**

Changes to Features Section and General Description Section .	1
Updated Outline Dimensions .....	16
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#### **2/2009—Rev. B to Rev. C**

Change to Supply Current Shutdown Mode (AD8647 Only) Parameter, Table 1 .....	3
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Added Figure 50; Renumbered Sequentially .....	15
Updated Outline Dimensions .....	16
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#### **10/2007—Revision B: Initial Combined Version**

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### **Revision History: AD8646**

#### **10/2007—Rev. 0 to Rev. B**

Combined with AD8648 .....	Universal
Added AD8647 .....	Universal
Deleted Figure 4 and Figure 7 .....	7
Deleted Figure 33 .....	11

#### **8/2007—Revision 0: Initial Version**

### **Revision History: AD8648**

#### **10/2007—Rev. A to Rev. B**

Combined with AD8646 .....	Universal
Added AD8647 .....	Universal
Deleted Figure 7 .....	6
Deleted Figure 11 .....	7
Deleted Figure 16 and Figure 17 .....	8
Deleted Figure 24 .....	9
Deleted Figure 27, Figure 28, Figure 31, and Figure 32 .....	10

#### **6/2007—Rev. 0 to Rev. A**

Changes to General Description .....	1
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

#### **1/2006—Revision 0: Initial Version**

## SPECIFICATIONS

$V_{SY} = 5\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
<b>INPUT CHARACTERISTICS</b>							
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to }5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.6	2.5	mV	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.8	7.5	$\mu\text{V}/^\circ\text{C}$	
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.3	1	pA	
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	pA	
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			550	pA	
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA	
Input Voltage Range	$V_{CM}$		0		5	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }5\text{ V}$	67	84		dB	
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to }4.5\text{ V}$	104	116		dB	
Input Capacitance	$C_{DIFF}$					pF	
Differential							
Common Mode	$C_{CM}$					6.7	pF
<b>OUTPUT CHARACTERISTICS</b>							
Output Voltage High	$V_{OH}$	$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.98	4.99		V	
Output Voltage Low		$I_{OUT} = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.90			V	
		$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.85	4.92		V	
		$I_{OUT} = 10\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.70			V	
	Output Current	$I_{SC}$				±120	mA
Closed-Loop Output Impedance	$Z_{OUT}$	At 1 MHz, $A_V = 1$				5	$\Omega$
<b>POWER SUPPLY</b>							
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to }5.5\text{ V}$	63	80		dB	
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	2.0	mA	
Supply Current Shutdown Mode (AD8647 Only)	$I_{SD}$	Both amplifiers shut down, $V_{IN\_SDA}$ and $V_{IN\_SDB} = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10		nA	
					1	$\mu\text{A}$	
<b>SHUTDOWN INPUTS (AD8647)</b>							
Logic High Voltage (Enabled)	$V_{INH}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+2.0			V	
Logic Low Voltage (Power-Down)	$V_{INL}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			+0.8	V	
Logic Input Current (Per Pin)	$I_{IN}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1	$\mu\text{A}$	
Output Pin Leakage Current		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ (shutdown active)		1		nA	
<b>DYNAMIC PERFORMANCE</b>							
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		11		V/ $\mu\text{s}$	
Gain Bandwidth Product	GBP			24		MHz	
Phase Margin	$\phi_m$			74		Degrees	
Settling Time	$t_s$	To 0.1%		0.5		$\mu\text{s}$	
Amplifier Turn-On Time (AD8647)	$t_{on}$	$25^\circ\text{C}$ , $A_V = 1$ , $R_L = 1\text{ k}\Omega$ (see Figure 44)		1		$\mu\text{s}$	
Amplifier Turn-Off Time (AD8647)	$t_{off}$	$25^\circ\text{C}$ , $A_V = 1$ , $R_L = 1\text{ k}\Omega$ (see Figure 45)		1		$\mu\text{s}$	

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3		$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1 \text{ kHz}$		8		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		6		$\text{nV}/\sqrt{\text{Hz}}$
Channel Separation	CS	$f = 10 \text{ kHz}$		-115		dB
		$f = 100 \text{ kHz}$		-110		dB
Total Harmonic Distortion Plus Noise	THD + N	$V_{p-p} = 0.1 \text{ V}, R_L = 600 \Omega, f = 25 \text{ kHz}, T_A = 25^\circ\text{C}$				
		$A_V = +1$		0.010		%
		$A_V = -10$		0.021		%

$V_{SY} = 2.7\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.6	2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.8	7.0	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	$V_{CM}$		0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$	62	79		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 2.2\text{ V}$	95	102		dB
Input Capacitance						
Differential	$C_{DIFF}$			2.5		pF
Common Mode	$C_{CM}$			7.8		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65	2.68		V
Output Voltage Low	$V_{OL}$	$I_{OUT} = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.60	11	25	V
Output Current	$I_{SC}$	Short circuit		$\pm 63$	30	mV
Closed-Loop Output Impedance	$Z_{OUT}$	At 1 MHz, $A_V = 1$		5		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to } 5.5\text{ V}$	63	80		dB
Supply Current per Amplifier	$I_{SY}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.6	2.0	mA
Supply Current Shutdown Mode (AD8647 Only)	$I_{SD}$	Both amplifiers shut down, $V_{IN\_SDA}$ and $V_{IN\_SDB} = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	2.5	mA
					1	$\mu\text{A}$
<b>SHUTDOWN INPUTS (AD8647)</b>						
Logic High Voltage (Enabled)	$V_{INH}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+2.0			V
Logic Low Voltage (Power-Down)	$V_{INL}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			+0.8	V
Logic Input Current (Per Pin)	$I_{IN}$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1	$\mu\text{A}$
Output Pin Leakage Current		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$ (shutdown active)		1		nA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		11		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			24		MHz
Phase Margin	$\phi_m$			53		Degrees
Settling Time	$t_s$	To 0.1%		0.3		$\mu\text{s}$
Amplifier Turn-On Time (AD8647)	$t_{on}$	$25^\circ\text{C}$ , $A_V = 1$ , $R_L = 1\text{ k}\Omega$ (see Figure 41)		1.2		$\mu\text{s}$
Amplifier Turn-Off Time (AD8647)	$t_{off}$	$25^\circ\text{C}$ , $A_V = 1$ , $R_L = 1\text{ k}\Omega$ (see Figure 42)		1		$\mu\text{s}$
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3		$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		8	6	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Channel Separation	CS	$f = 10\text{ kHz}$ $f = 100\text{ kHz}$		-115	-110	dB

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to $V_{SY}$
Differential Input Voltage	$\pm 6$ V
Output Short Circuit to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	$300^{\circ}\text{C}$
Junction Temperature	$150^{\circ}\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC_N	125	43	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP	210	45	$^{\circ}\text{C}/\text{W}$
10-Lead MSOP	200	44	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC_N	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP	180	35	$^{\circ}\text{C}/\text{W}$

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### TYPICAL PERFORMANCE CHARACTERISTICS

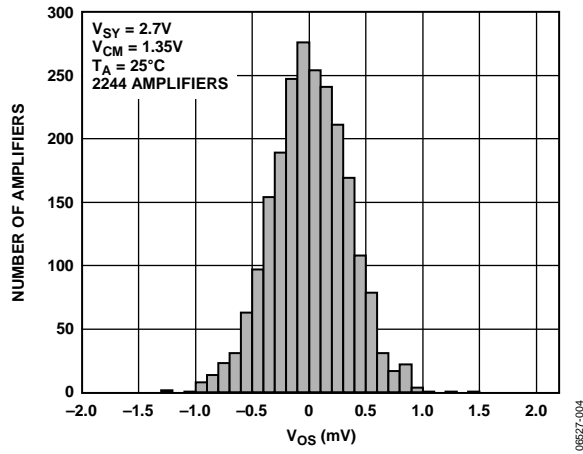


Figure 4. Input Offset Voltage Distribution

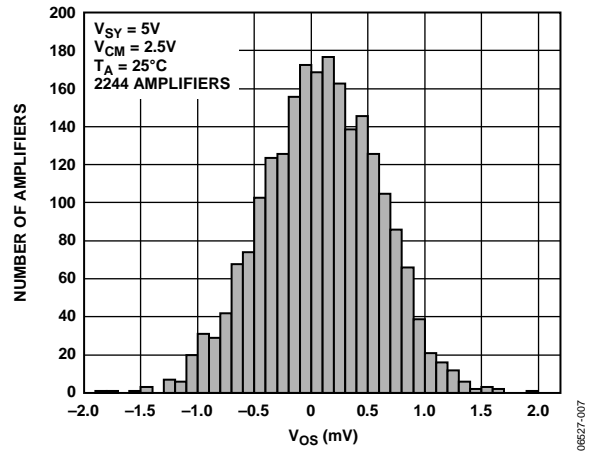


Figure 7. Input Offset Voltage Distribution

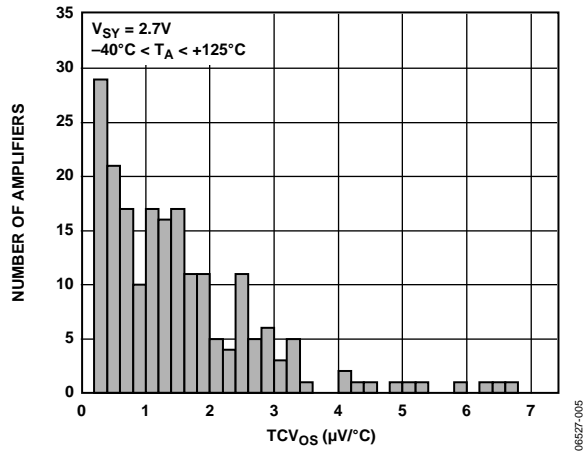


Figure 5.  $V_{OS}$  Drift ( $TCV_{OS}$ ) Distribution

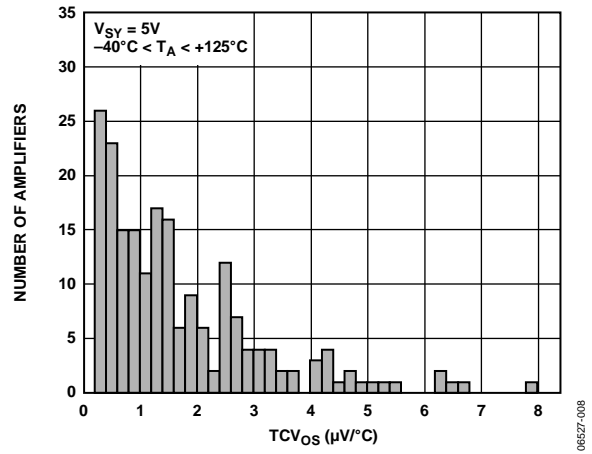


Figure 8.  $V_{OS}$  Drift ( $TCV_{OS}$ ) Distribution

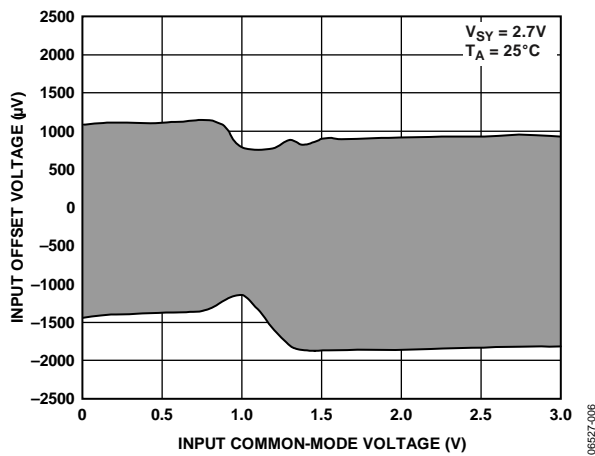


Figure 6. Input Offset Voltage vs. Input Common-Mode Voltage

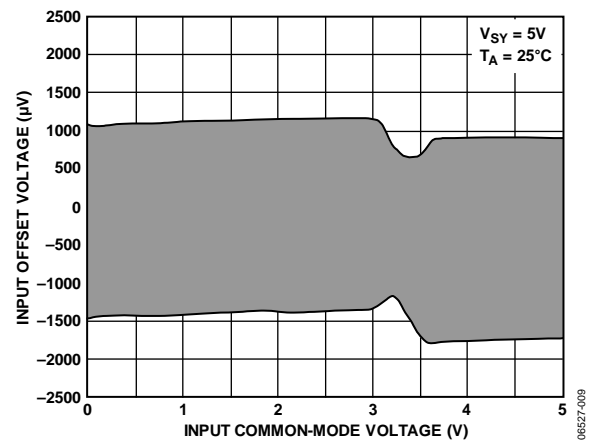


Figure 9. Input Offset Voltage vs. Input Common-Mode Voltage

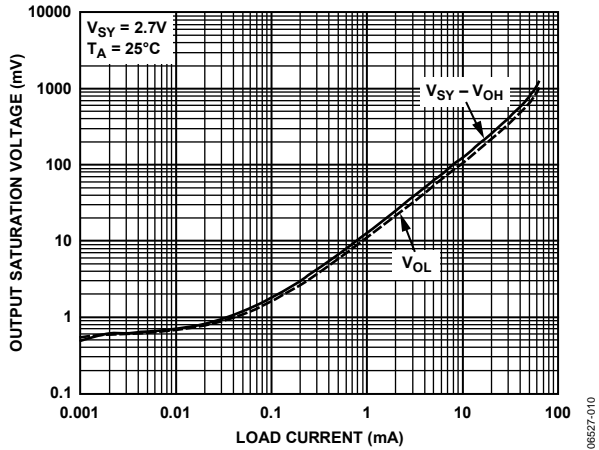


Figure 10. Output Saturation Voltage vs. Load Current

06527-010

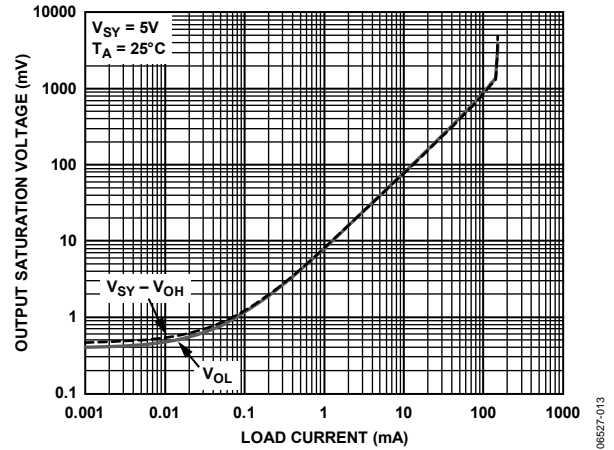


Figure 13. Output Saturation Voltage vs. Load Current

06527-013

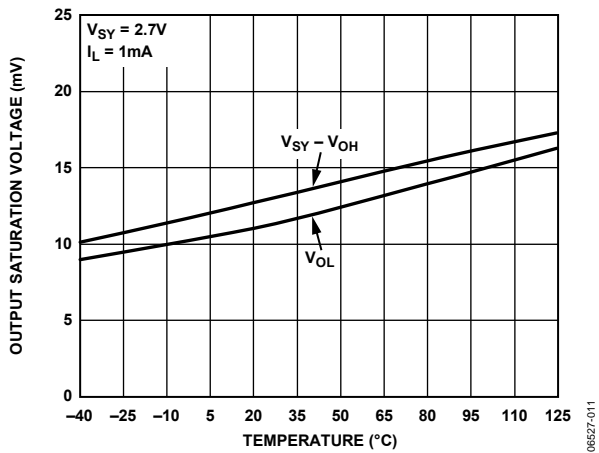


Figure 11. Output Saturation Voltage vs. Temperature

06527-011

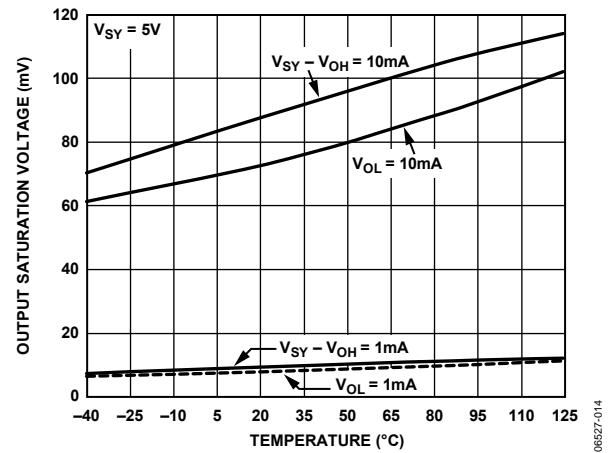


Figure 14. Output Saturation Voltage vs. Temperature

06527-014

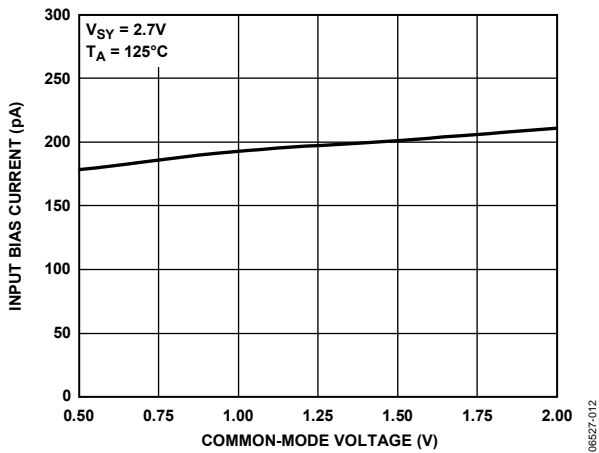


Figure 12. Input Bias Current vs. Common-Mode Voltage

06527-012

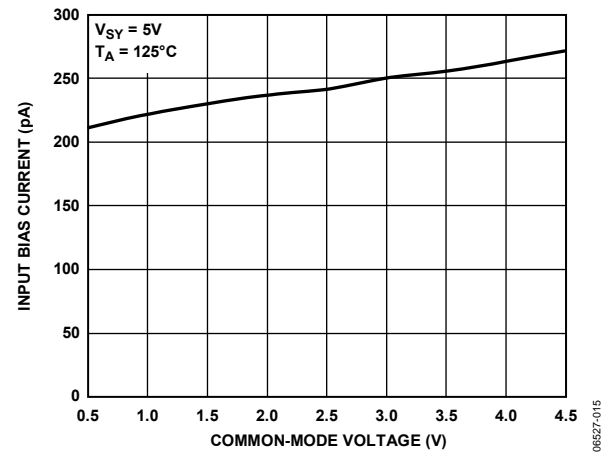


Figure 15. Input Bias Current vs. Common-Mode Voltage

06527-015



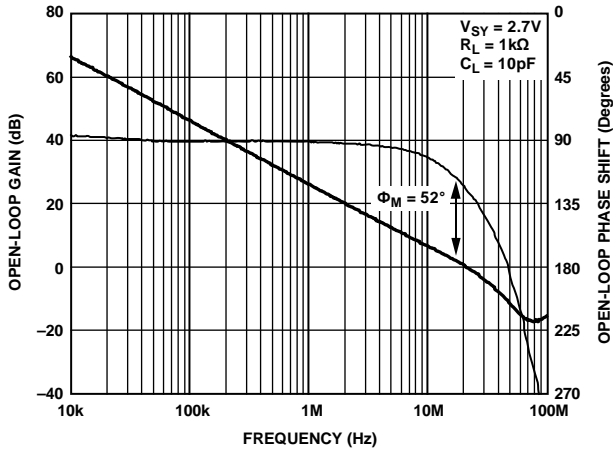


Figure 16. Open-Loop Gain and Phase vs. Frequency

06527-016

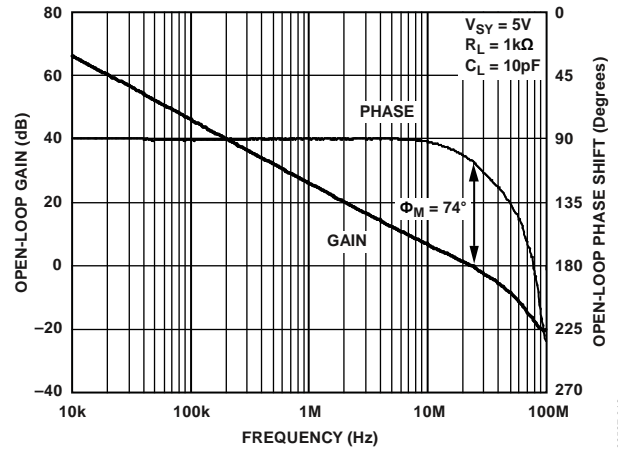


Figure 19. Open-Loop Gain and Phase vs. Frequency

06527-019

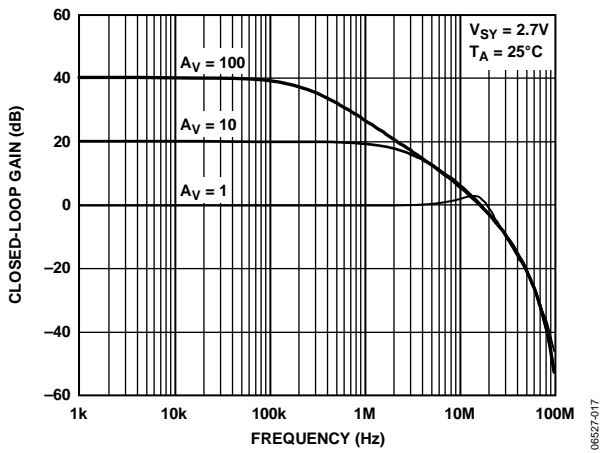


Figure 17. Closed-Loop Gain vs. Frequency

06527-017

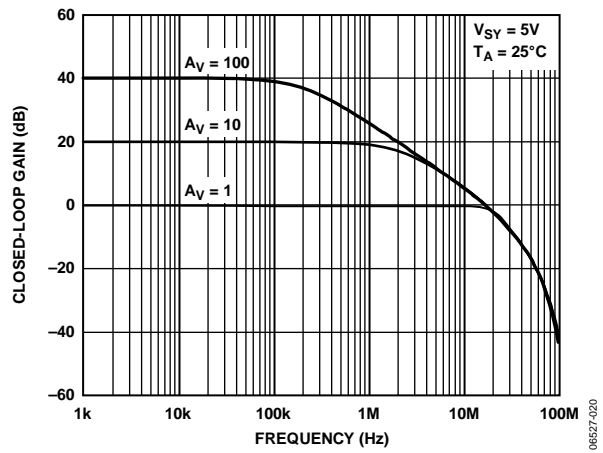


Figure 20. Closed-Loop Gain vs. Frequency

06527-020

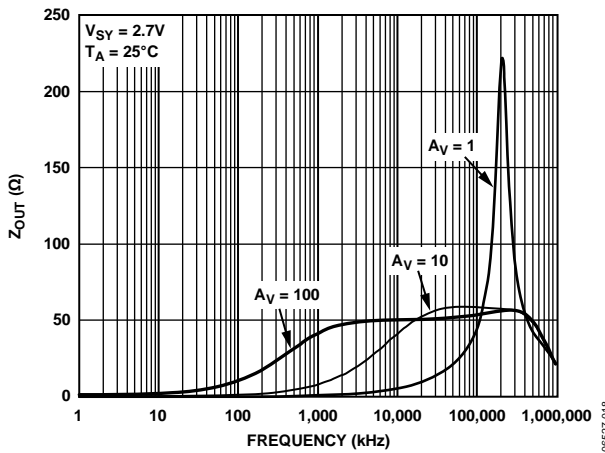


Figure 18.  $Z_{OUT}$  vs. Frequency

06527-018

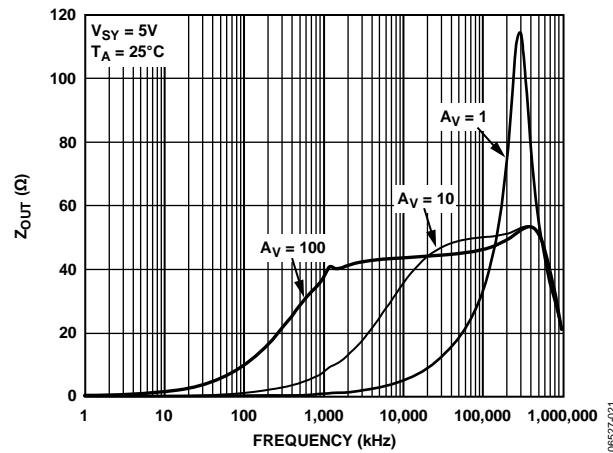


Figure 21.  $Z_{OUT}$  vs. Frequency

06527-021

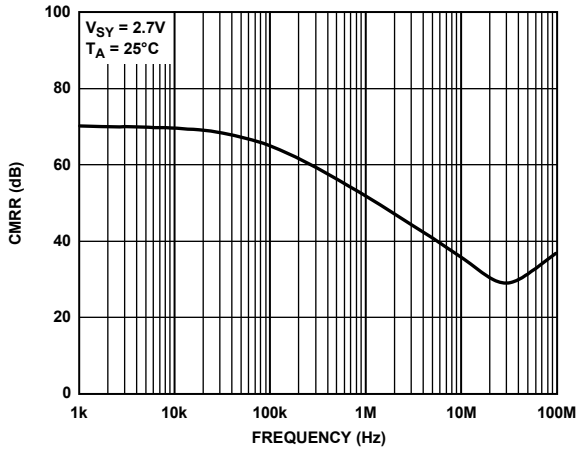


Figure 22. CMRR vs. Frequency

06527-022

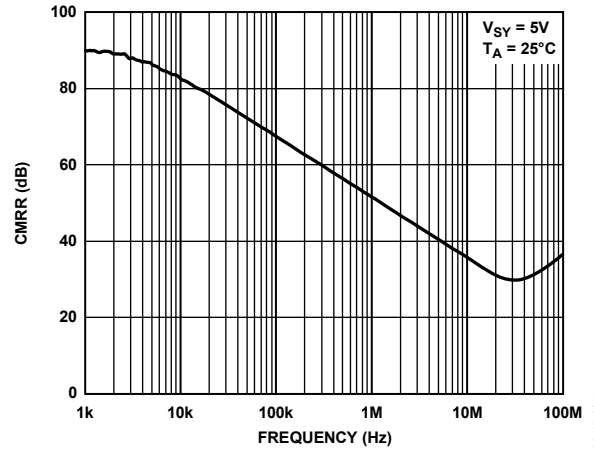


Figure 25. CMRR vs. Frequency

06527-025

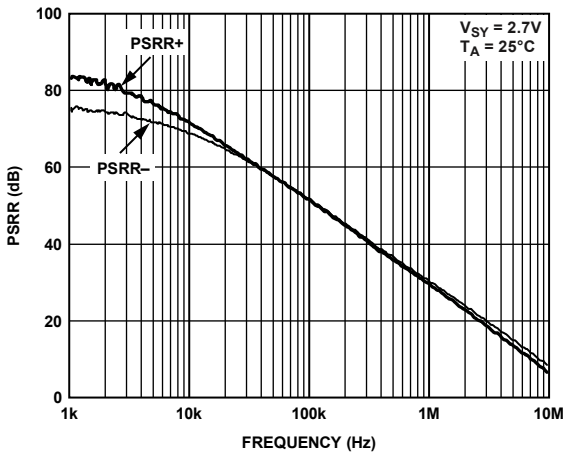


Figure 23. PSRR vs. Frequency

06527-023

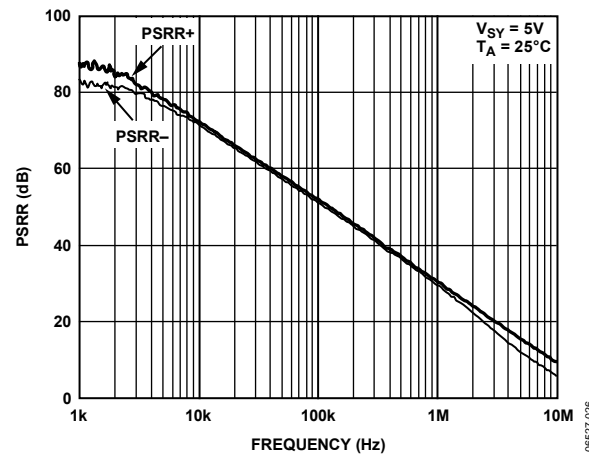


Figure 26. PSRR vs. Frequency

06527-026

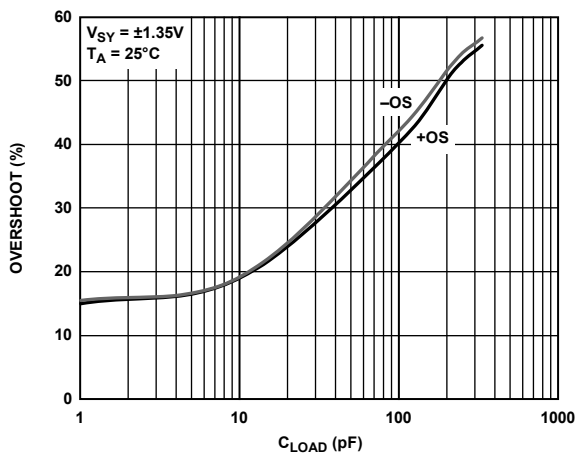


Figure 24. Overshoot vs. Load Capacitance

06527-024

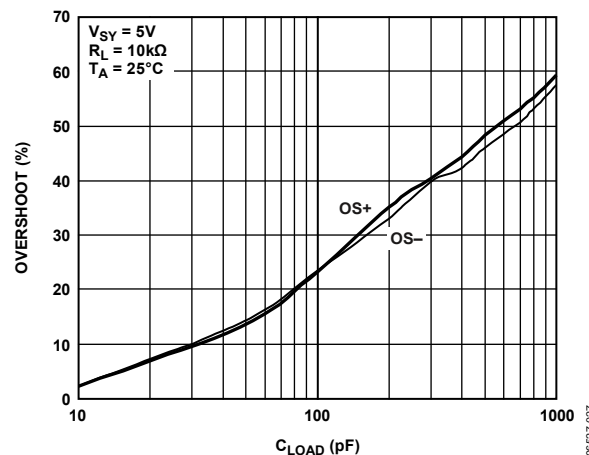


Figure 27. Overshoot vs. Load Capacitance

06527-027

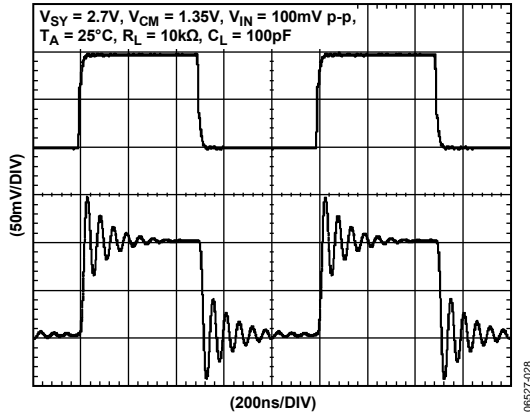


Figure 28. Small-Signal Transient Response

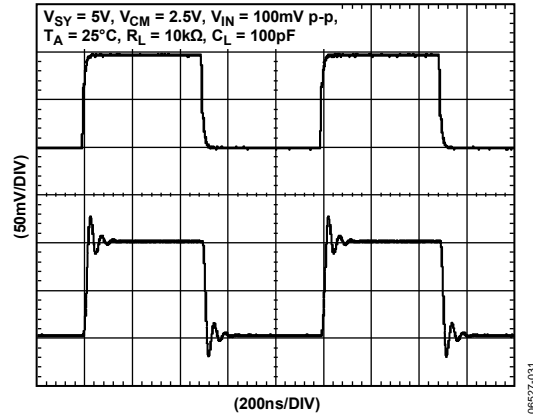


Figure 31. Small-Signal Transient Response

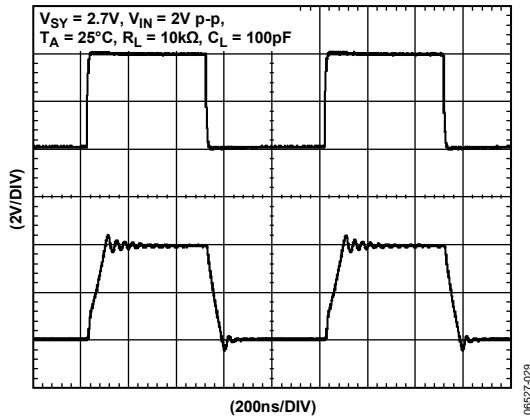


Figure 29. Large-Signal Transient Response

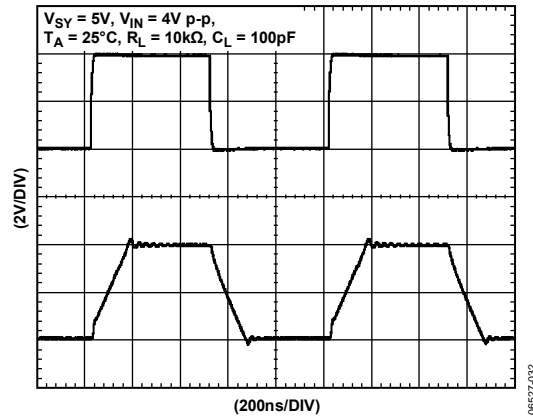


Figure 32. Large-Signal Transient Response

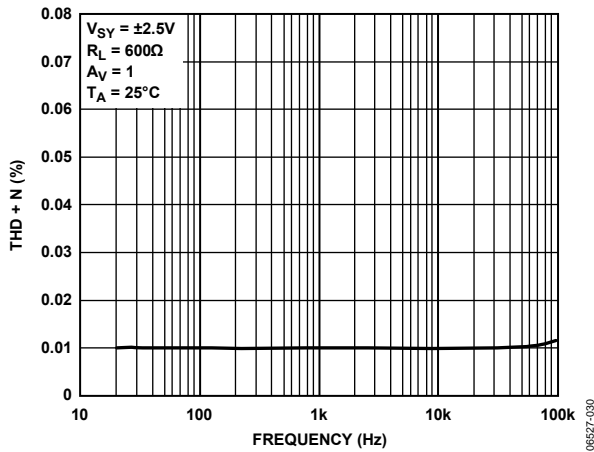


Figure 30. THD + Noise vs. Frequency

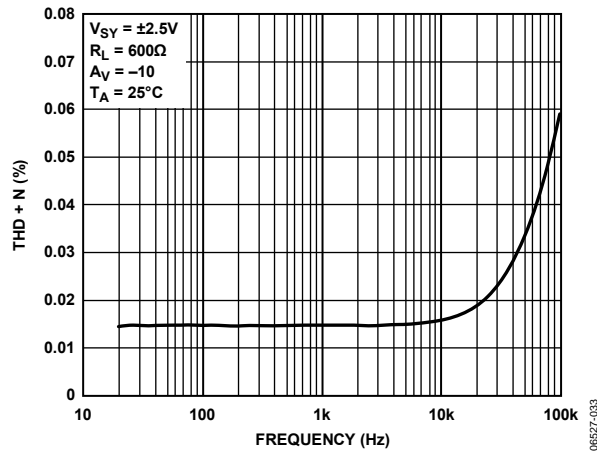


Figure 33. THD + Noise vs. Frequency

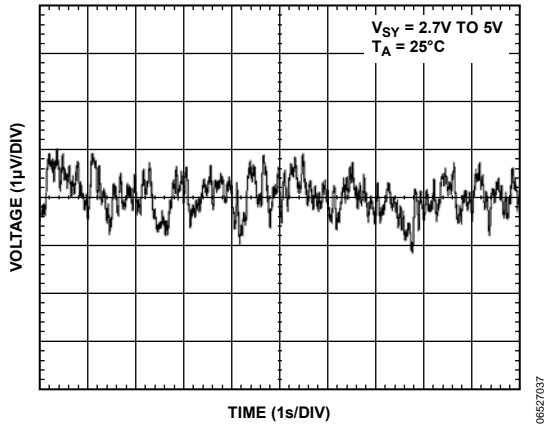


Figure 34. 0.1 Hz to 10 Hz Voltage Noise

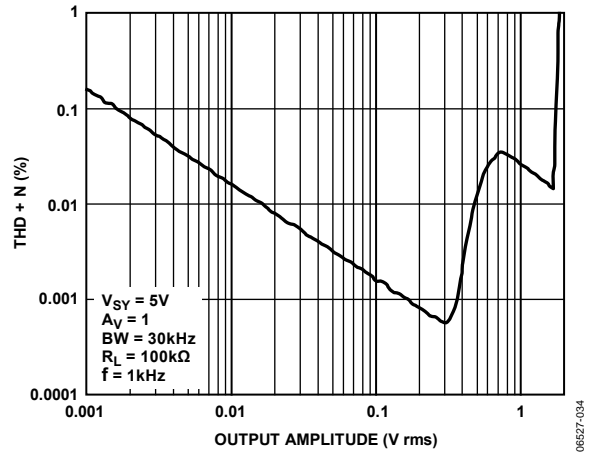


Figure 37. THD + Noise vs. Output Amplitude

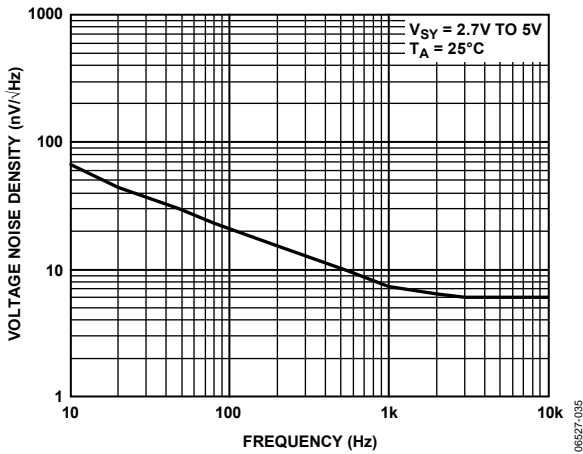


Figure 35. Voltage Noise Density vs. Frequency

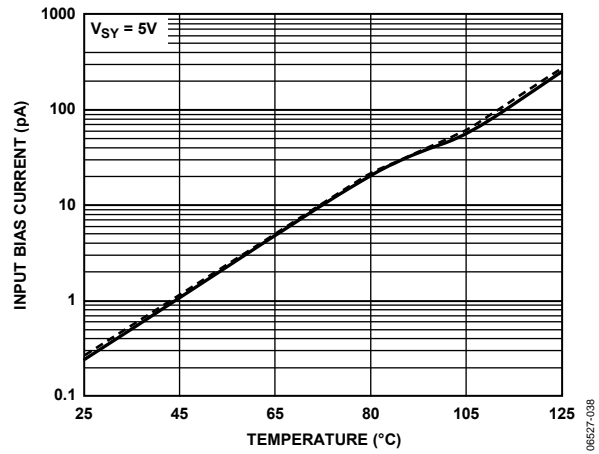


Figure 38. Input Bias Current vs. Temperature

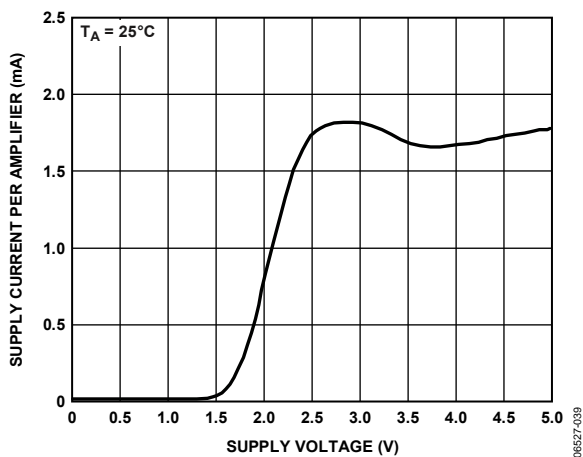


Figure 36. Supply Current per Amplifier vs. Supply Voltage

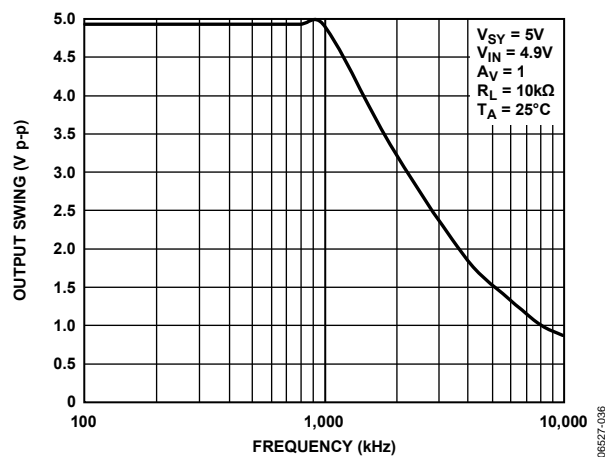


Figure 39. Maximum Output Swing vs. Frequency

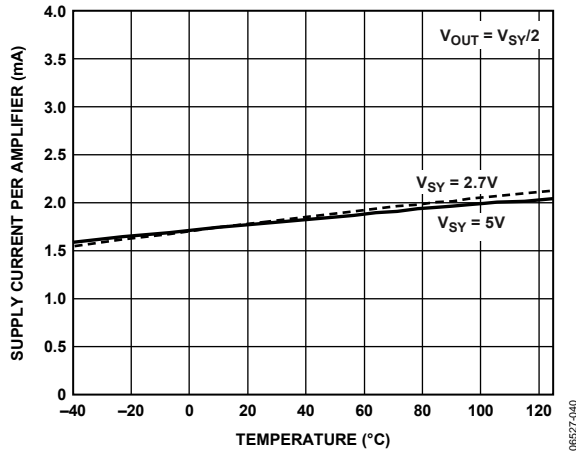


Figure 40. Supply Current per Amplifier vs. Temperature

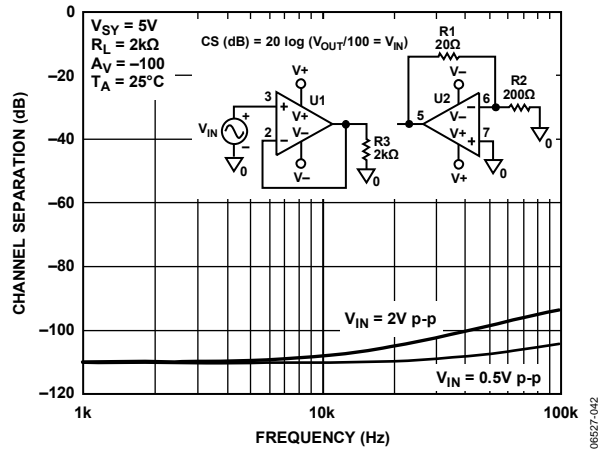


Figure 43. Channel Separation

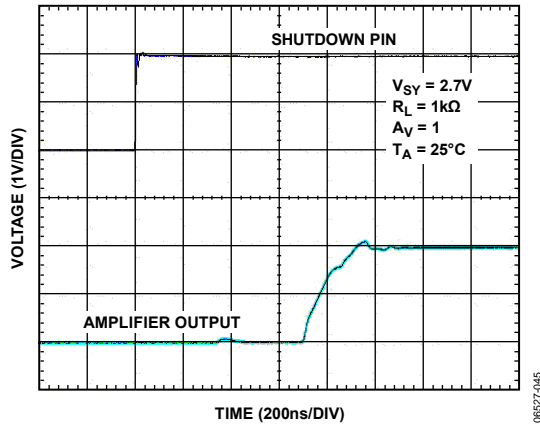


Figure 41. Turn-On Time

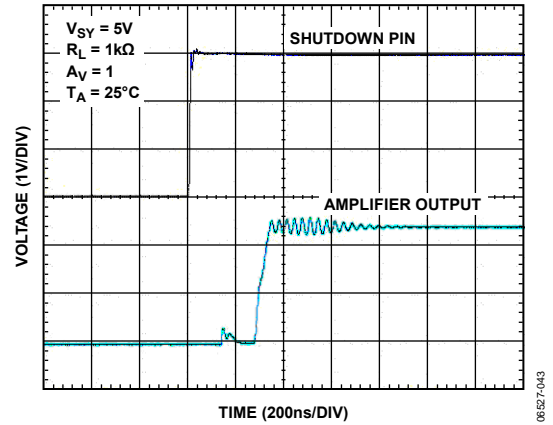


Figure 44. Turn-On Time

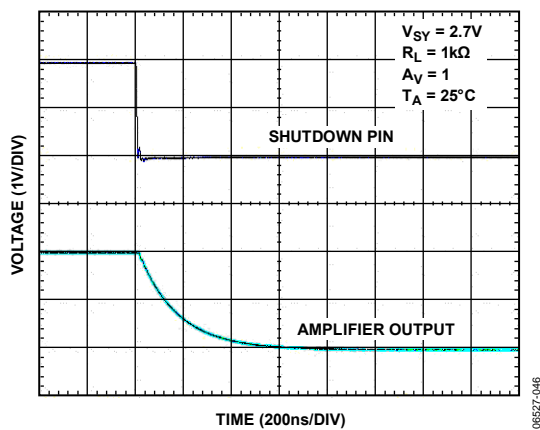


Figure 42. Turn-Off Time

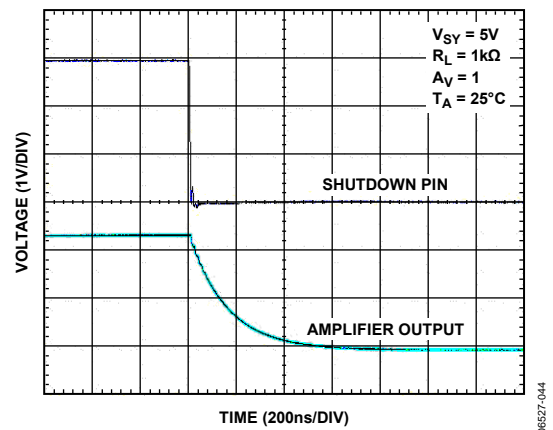


Figure 45. Turn-Off Time

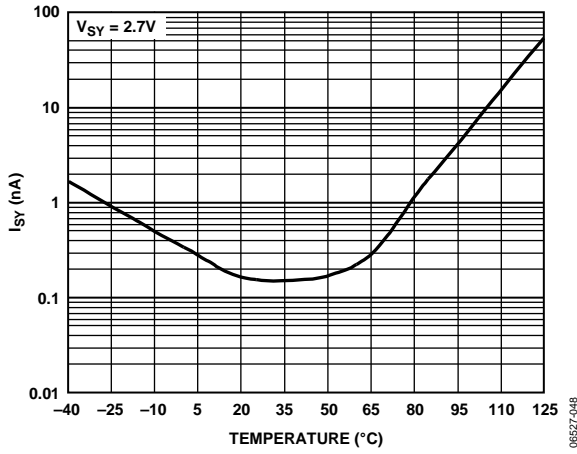


Figure 46. Supply Current with Op-Amp Shutdown vs. Temperature

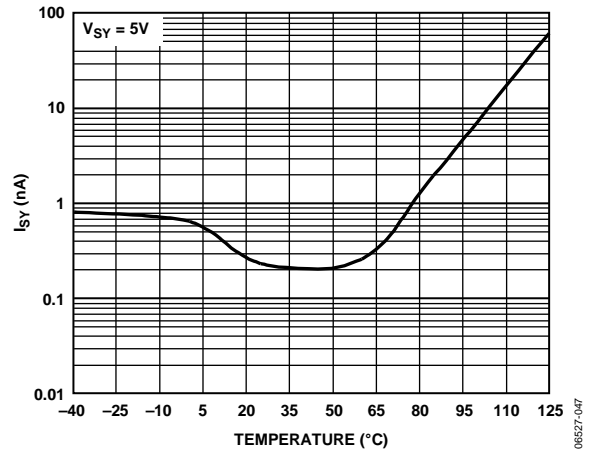


Figure 47. Supply Current with Op-Amp Shutdown vs. Temperature

## THEORY OF OPERATION

### POWER-DOWN OPERATION

The shutdown function of the AD8647 is referenced to the negative supply voltage of the operational amplifier. A logic level high ( $> 2.0\text{ V}$ ) enables the device, while a logic level low ( $< 0.8\text{ V}$ ) disables the device and places the output in a high impedance condition. Several outputs can be wire-ORed, thus eliminating a multiplexer. The logic input is a high impedance CMOS input. If dual or split supplies are used, the logic signals must be properly referred to the negative supply voltage.

### MULTIPLEXING OPERATION

Because each op amp has a separate logic input enable pin, the outputs can be connected together if it can be guaranteed that only one op amp is active at any time. By connecting the op amps as shown in Figure 48, a multiplexer can be eliminated. With the reasonably short turn-on and turn-off times, low frequency signal paths can be smoothly selected. The turn-off time is slightly faster than the turn-on time so, even when using sections from two different packages, the overlap is less than 300 nanoseconds.

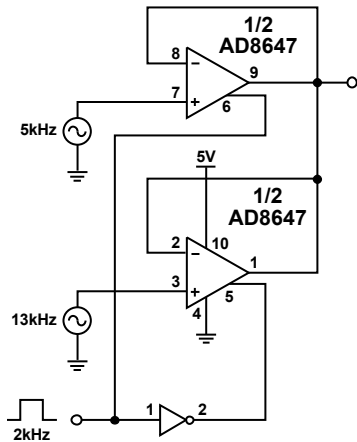


Figure 48. AD8647 Output Switching

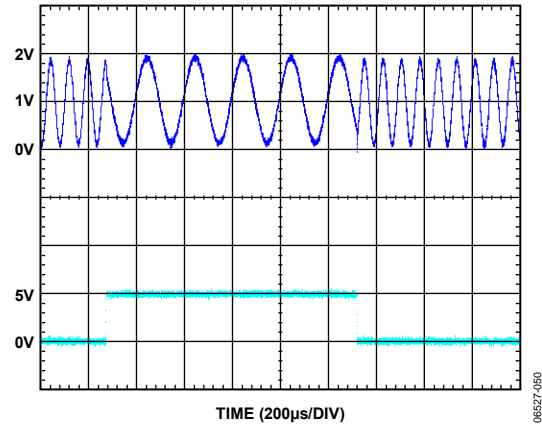


Figure 49. Switching Waveforms

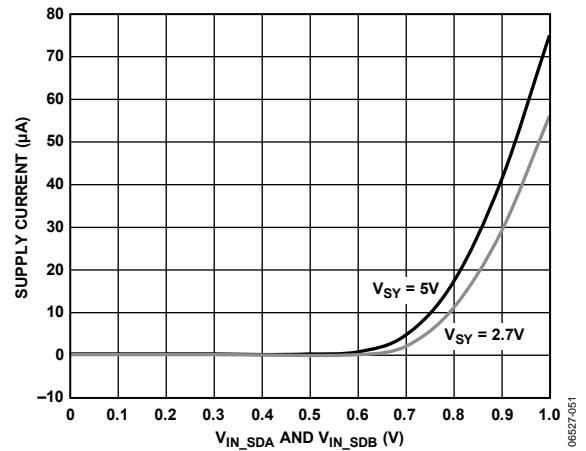
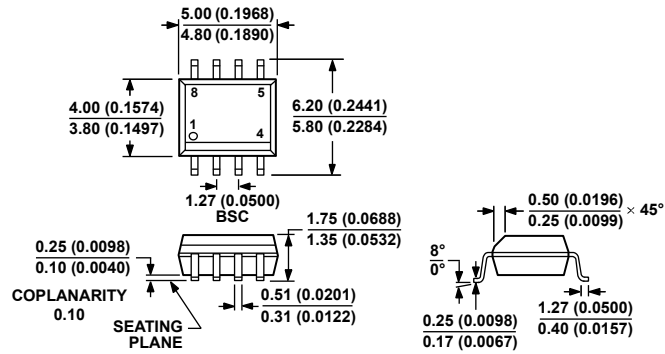


Figure 50. Supply Current Shutdown Mode, AD8647

OUTLINE DIMENSIONS

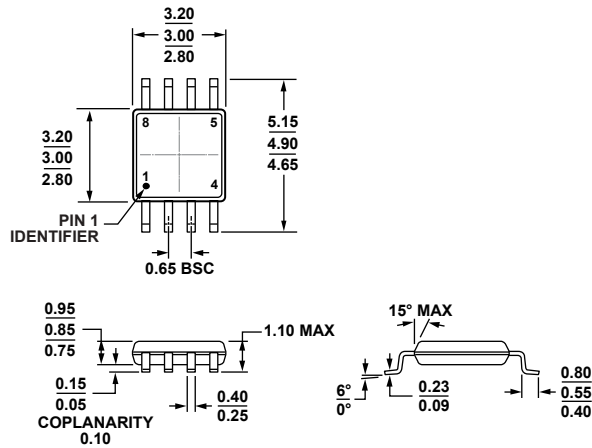


COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

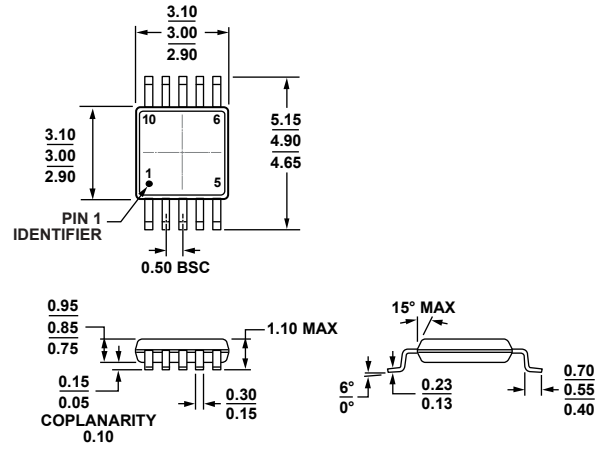


COMPLIANT TO JEDEC STANDARDS MO-187-AA  
 Figure 52. 8-Lead Mini Small Outline Package [MSOP]  
 (RM-8)

Dimensions shown in millimeters

100709-B



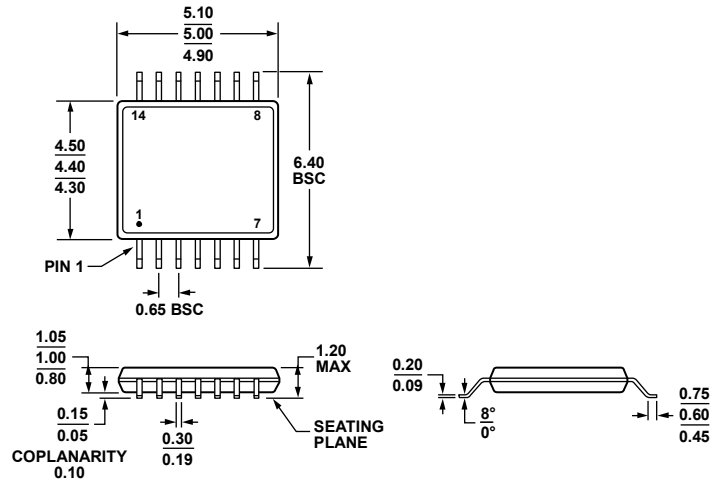


COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 53. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

Dimensions shown in millimeters

091708-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 54. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061988-A

