7 MHz Rail-to-Rail Low Voltage Operational Amplifiers

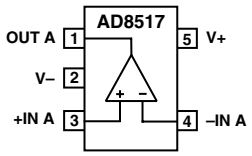
AD8517/AD8527

FEATURES
Single Supply Operation: 1.8 V to 6 V
Space-Saving SOT-23, μSOIC Packaging
Wide Bandwidth: 7 MHz @ 5 V
Low Offset Voltage: 3.5 mV Max
Rail-to-Rail Output Swing and Rail-to-Rail Input
8 V/μs Slew Rate
Only 900 μA Supply Current @ 5 V

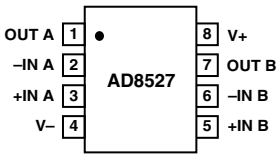
APPLICATIONS
Portable Communications
Portable Phones
Sensor Interface
Active Filters
PCMCIA Cards
ASIC Input Drivers
Wearable Computers
Battery-Powered Devices
New Generation Phones
Personal Digital Assistants

PIN CONFIGURATIONS

5-Lead SOT-23
(RT Suffix)



8-Lead SOIC
(R Suffix)



8-Lead MSOP
(RM Suffix)

GENERAL DESCRIPTION

The AD8517 brings precision and bandwidth to the SOT-23-5 package even at single supply voltages as low as 1.8 V. The small package makes it possible to place the AD8517 next to sensors, reducing external noise pickup. The AD8527 dual amplifier is offered in the space-saving MSOP package.

The AD8517 and AD8527 are rail-to-rail input and output bipolar amplifiers with a gain bandwidth of 7 MHz and typical voltage offset of 1.3 mV from a 1.8 V supply. The low supply current makes these parts ideal for battery-powered applications. The 8 V/μs slew rate makes the AD8517/AD8527 a good match for driving ASIC inputs, such as voice codecs.

The AD8517/AD8527 is specified over the extended industrial (–40°C to +125°C) temperature range. The AD8517 single is available in 5-lead SOT-23 surface-mount packages. The dual AD8527 is available in 8-lead SOIC and MSOP packages.

REV. B

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AD8517/AD8527–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 5.0 V, V– = 0 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
AD8517ART (SOT-23-5)	V_{OS}			1.3	3.5	mV
		–40°C ≤ T_A ≤ +125°C			5	mV
AD8527	V_{OS}			1.3	3.5	mV
		–40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B				450	nA
		–40°C ≤ T_A ≤ +125°C			900	nA
Input Offset Current	I_{OS}				±225	nA
		–40°C ≤ T_A ≤ +125°C			±750	nA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5.0 V,				
		–40°C ≤ T_A ≤ +125°C	60	70		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V < V_{OUT} < 4.5 V		20		V/mV
		R_L = 10 kΩ, 0.5 V < V_{OUT} < 4.5 V	50	100		V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +125°C	30			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			500		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA,				
		–40°C ≤ T_A ≤ +125°C	4.965			V
		I_L = 5 mA	4.70			V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA,				
		–40°C ≤ T_A ≤ +125°C			35	mV
		I_L = 5 mA			200	mV
Short Circuit Current	I_{SC}	Short to Ground, Instantaneous		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.2 V to 6 V		90		dB
		–40°C ≤ T_A ≤ +125°C		65		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V		900	1,200	µA
		–40°C ≤ T_A ≤ +125°C			1,400	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V_{OUT} < 4 V, R_L = 10 kΩ		8		V/µs
Gain Bandwidth Product	GBP			7		MHz
Settling Time	T_S	4 V Step, 0.1%		400		ns
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.2		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 2.2 V, V– = 0 V, V_{CM} = 1.1 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
AD8517ART (SOT-23-5)	V_{OS}			1.3	3.5	mV
		–40°C ≤ T_A ≤ +125°C			5	mV
AD8527	V_{OS}			1.3	3.5	mV
		–40°C ≤ T_A ≤ +125°C			5	mV
Input Bias Current	I_B				450	nA
Input Offset Current	I_{OS}				±225	nA
Input Voltage Range	V_{CM}		0		2.2	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 2.2 V,				
		–40°C ≤ T_A ≤ +125°C	55	70		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V < V_{OUT} < 1.7 V		20		V/mV
		R_L = 10 kΩ	20	50		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA	2.165			V
		I_L = 2.5 mA	1.9			V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA			35	mV
		I_L = 2.5 mA			200	mV
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_{OUT} = 1.1 V		750	1,100	µA
		–40°C ≤ T_A ≤ +125°C			1,300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		8		V/µs
Gain Bandwidth Product	GBP			7		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		15		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		1.2		pA/$\sqrt{Hz}$

Specifications subject to change without notice.

AD8517/AD8527–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 1.8 V, V– = 0 V, V_{CM} = 0.9 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
AD8517ART (SOT-23-5)	V_{OS}			1.3	3.5	mV
		0°C ≤ T_A ≤ 125°C			5	mV
AD8527	V_{OS}			1.3	3.5	mV
		0°C ≤ T_A ≤ 125°C			5	mV
Input Bias Current	I_B				450	nA
Input Offset Current	I_{OS}				±225	nA
Input Voltage Range	V_{CM}		0		1.8	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.8 V,				
		0°C ≤ T_A ≤ 125°C	50	70		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V < V_{OUT} < 1.3 V		20		V/mV
		R_L = 10 kΩ	20	50		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA	1.765			V
		I_L = 2.5 mA	1.5			V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA			35	mV
		I_L = 2.5 mA			200	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 1.7 V to 2.2 V,				
		0°C ≤ T_A ≤ 125°C	50	65		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0.9 V		650	1,100	µA
		0°C ≤ T_A ≤ 125°C			1,300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		7		V/µs
Gain Bandwidth Product	GBP			7		MHz
Phase Margin	ϕ_m			50		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		15		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		1.2		pA/$\sqrt{Hz}$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 6 V
Input Voltage[2] . . . . . GND to V_S
Differential Input Voltage . . . . . ±0.6 V
Internal Power Dissipation
SOT-23 (RT) . . . . . See Thermal Resistance Chart
SOIC (R) . . . . . See Thermal Resistance Chart
µSOIC (RM) . . . . . See Thermal Resistance Chart
Output Short-Circuit Duration
. . . . . Indefinite for T_A < +40°C
Storage Temperature Range
R, RM and RT Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8517, AD8527 . . . . . –40°C to +125°C
Junction Temperature Range
R, RM and RT Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than 6 V the input voltage is limited to less than or equal to the supply voltage.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
5-Lead SOT-23 (RT)	230	146	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead µSOIC (RM)	210	45	°C/W

NOTE
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for SOT-23 and SOIC packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8517ART-REEL	–40°C to +125°C	5-Lead SOT-23	RT-5	ADA
AD8527AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8527ARM-REEL	–40°C to +125°C	8-Lead µSOIC	RM-8	AFA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8517/AD8527 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

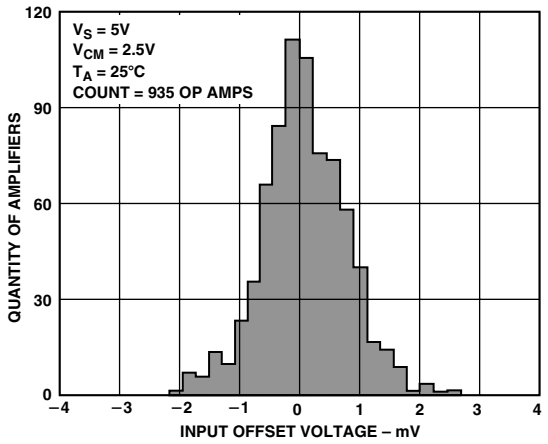


Figure 1. Input Offset Voltage Distribution

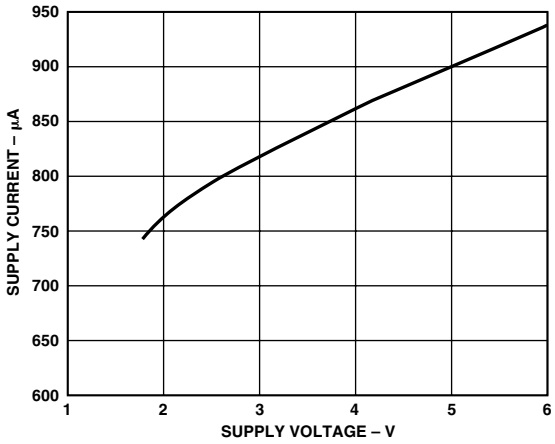


Figure 2. Supply Current per Amplifier vs. Supply Voltage

AD8517/AD8527–Typical Characteristics

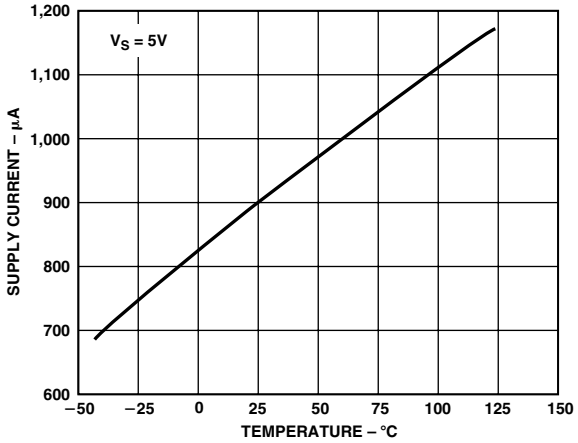


Figure 3. Supply Current per Amplifier vs. Temperature

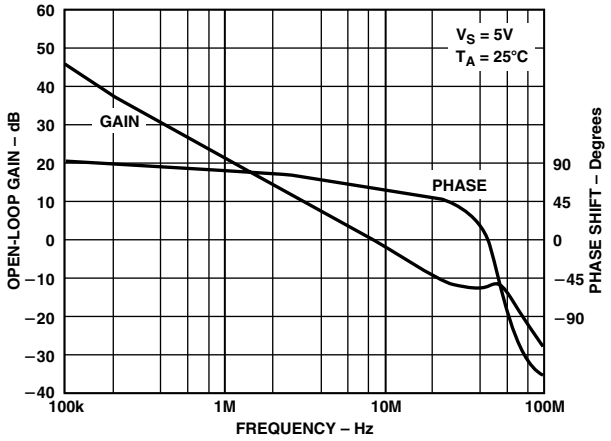


Figure 6. Open-Loop Gain vs. Frequency

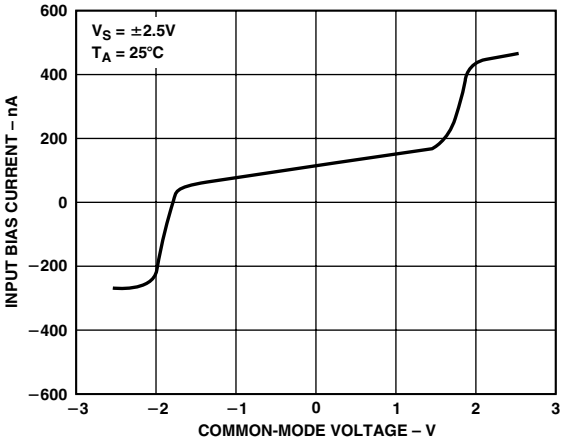


Figure 4. Input Bias Current vs. Common-Mode Voltage

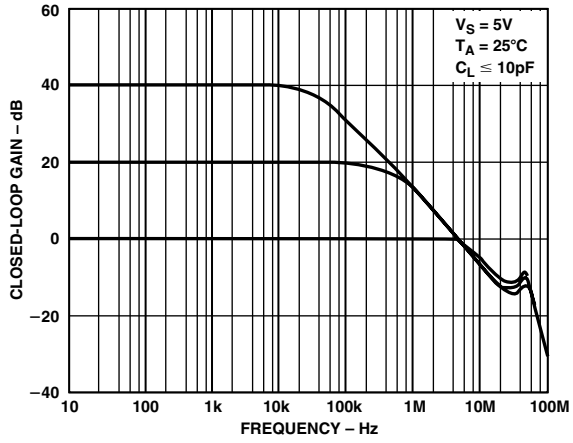


Figure 7. Closed-Loop Gain vs. Frequency

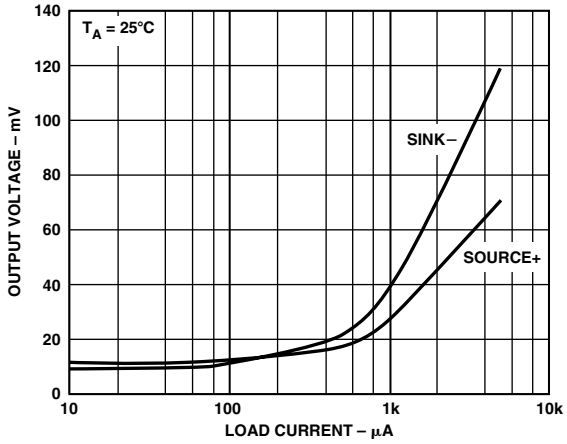


Figure 5. Output Voltage to Supply Rail vs. Load Current

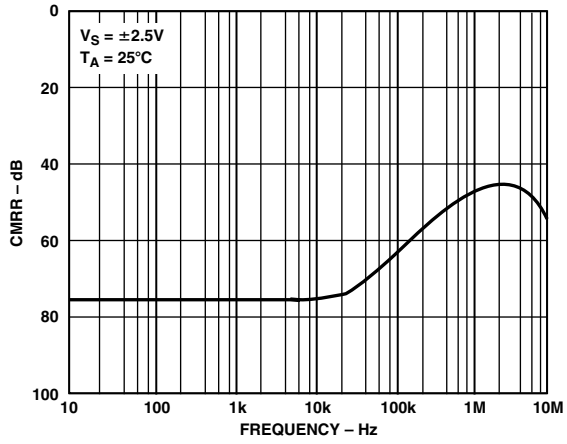


Figure 8. CMRR vs. Frequency

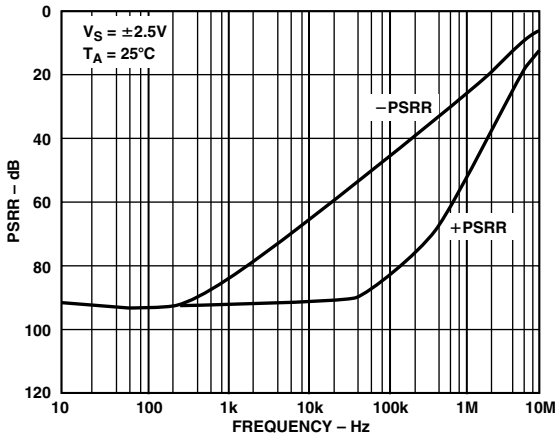


Figure 9. PSRR vs. Frequency

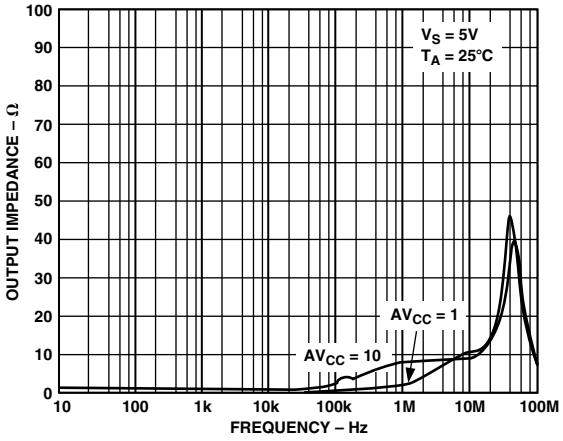


Figure 12. Output Impedance vs. Frequency

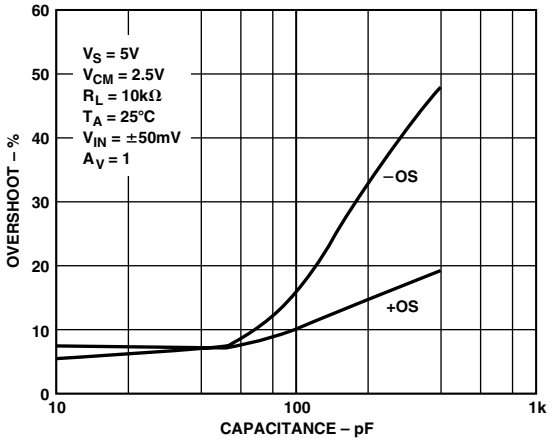


Figure 10. Overshoot vs. Capacitance Load

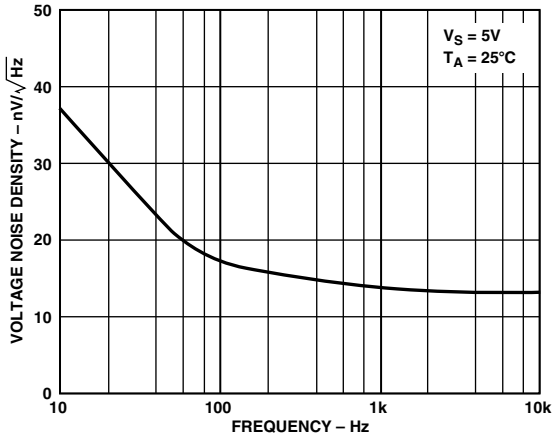


Figure 13. Voltage Noise Density vs. Frequency

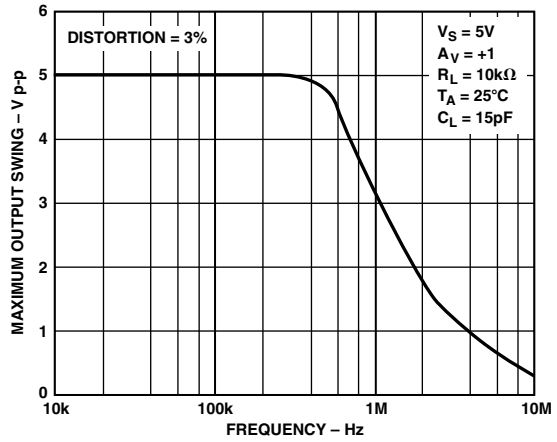


Figure 11. Output Swing vs. Frequency

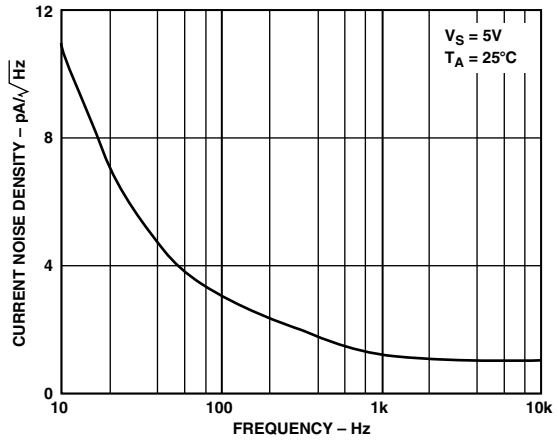


Figure 14. Current Noise Density vs. Frequency

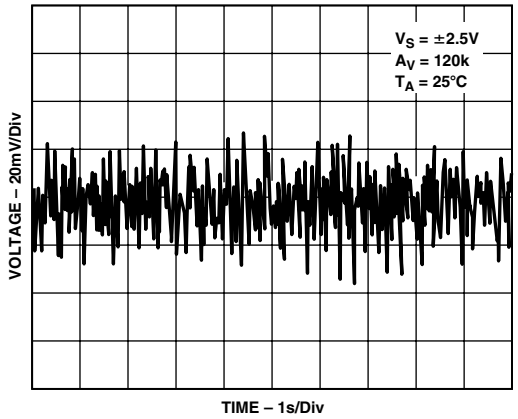


Figure 15. 0.1 Hz to 10 Hz Noise

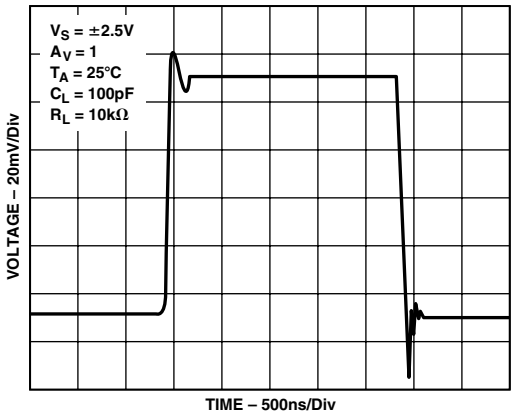


Figure 17. Small Signal Transient Response

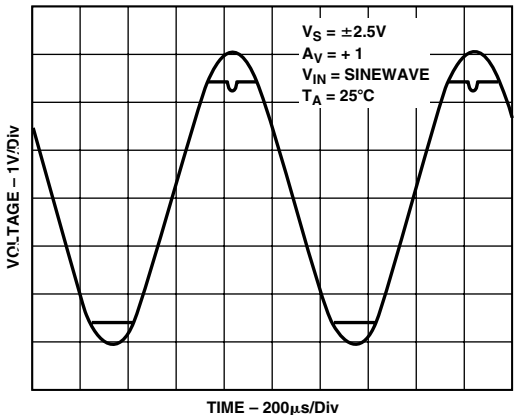


Figure 16. No Phase Reversal

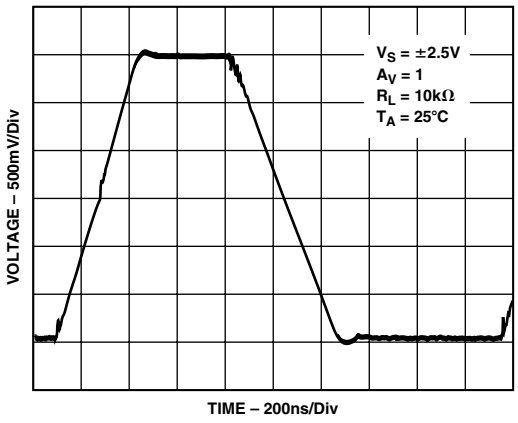


Figure 18. Large Signal Transient Response

THEORY OF OPERATION

The AD85x7 is a rail-to-rail operational amplifier that can operate at supply voltages as low as 1.8 V. This family is fabricated using Analog Devices' high-speed complementary bipolar process, also called XFCB. The process trench isolates each transistor to minimize parasitic capacitance thereby allowing high-speed performance. Figure 19 shows a simplified schematic of the AD85x7 family.

The input stage consists of two parallel complementary differential pair: one NPN pair (Q1 and Q2) and one PNP pair (Q3 and Q4). The voltage drops across R7. R8, R9, and R10 are kept low for rail-to-rail operation. The major gain stage of the op amp is a double-folded cascode consisting of transistors Q5, Q6, Q8, and Q9. The output stage, which also operates rail-to-rail, is driven by Q14. The transistors Q13 and Q10 act as level-shifters to give more headroom during 1.8 V operation.

As the voltage at the base of Q13 increases, Q18 starts to sink current. When the voltage at the base of Q13 decreases, I8 flows through D16 and Q15 increasing the VBE of Q17, then Q20 sources current.

The output stage also furnishes gain, which depends on the load resistance, since the output transistors are in common emitter configuration. The output swing when sinking or sourcing 250 µA is 35 mV from each rail.

The input bias current characteristics depend on the common-mode voltage, see Figure 4. As the input voltage reaches about 1 V below V_{CC}, the PNP pair (Q3 and Q4) turns off.

The 1 kΩ input resistor R1 and R2, together with the diodes D7 and D8, protect the input pairs against avalanche damage.

The AD85x7 family exhibits no phase reversal as the input signal exceeds the supply by more than 0.6 V. Excessive current can flow through the input pins via the ESD diodes D1–D2 or D3–D4, in the event their ~0.6 V thresholds are exceeded. Such fault currents must be limited to 5 mA or less by the use of external series resistance(s).

LOW VOLTAGE OPERATION

Battery Voltage Discharge

The AD8517 operates at supply voltages as low as 1.8 V. This amplifier is ideal for battery-powered applications since it can operate at the end of discharge voltage of most popular batteries. Table I lists the Nominal and End of Discharge Voltages of several typical batteries.

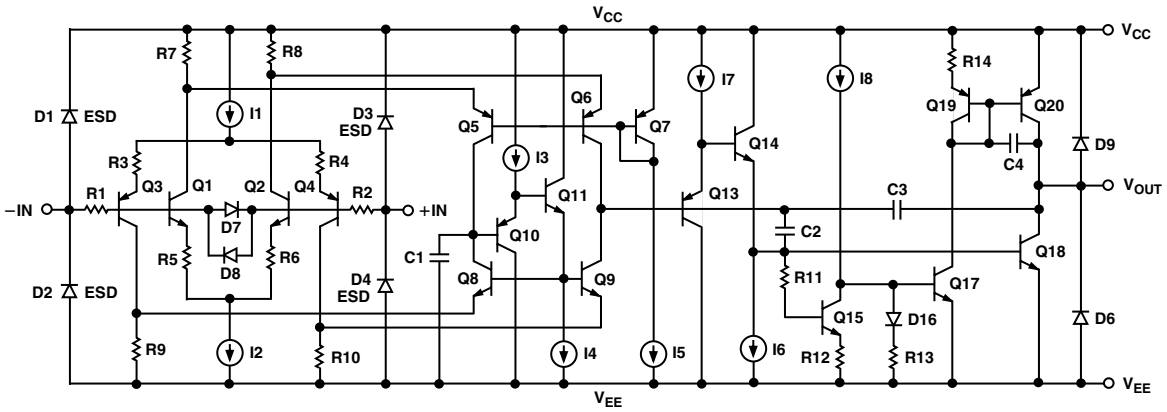


Figure 19. Simplified Schematic

Table I. Typical Battery Life Voltage Range

Battery	Nominal Voltage (V)	End of Voltage Discharge (V)
Lead-Acid	2	1.8
Lithium	2.6-3.6	1.7-2.4
NiMH	1.2	1
NiCd	1.2	1
Carbon-Zinc	1.5	1.1

RAIL-TO-RAIL INPUT AND OUTPUT

The AD8517 features an extraordinary rail-to-rail input and output with supply voltages as low as 1.8 V. With the amplifier's supply range set to 1.8 V, the input can be set to 1.8 V p-p, allowing the output to swing to both rails without clipping. Figure 20 shows a scope picture of both input and output taken at unity gain, with a frequency of 1 kHz, at V_S = 1.8 V and V_{IN} = 1.8 V p-p.

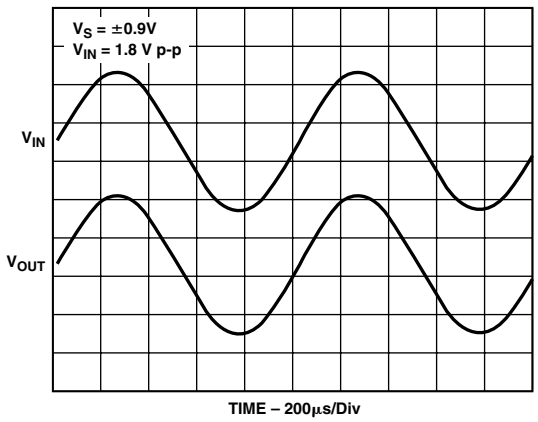


Figure 20. Rail-to-Rail Input Output

The rail-to-rail feature of the AD8517 can be observed over the supply voltage range, 1.8 V to 5 V. Traces are shown offset for clarity.

INPUT BIAS CONSIDERATION

The input bias current (I_B) is a nonideal, real-life parameter that affects all op amps. I_B can generate a somewhat significant offset voltage. This offset voltage is created by I_B when flowing through the negative feedback resistor R_F. If I_B is 500 nA (worst case), and R_F is 100 kΩ, the corresponding generated offset voltage is 50 mV ($V_{OS} = I_B \times R_F$).

Obviously the lower R_F the lower the generated voltage offset. Using a compensation resistor, R_B, as shown in Figure 21, can significantly minimize this effect. With the input bias current minimized, we still need to be aware of the input offset current (I_{OS}) which will generate a slight offset error. Figure 21 shows three different configurations to minimize IB-induced offset errors.

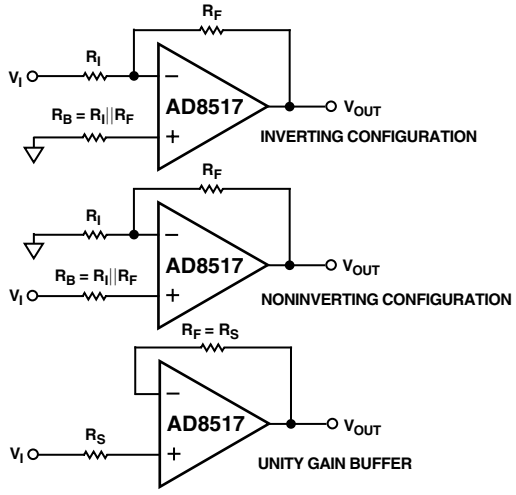


Figure 21. Input Bias Cancellation Circuits

DRIVING CAPACITIVE LOAD

Gain vs. Capacitive Load

Most amplifiers have difficulty driving capacitance due to degradation of phase caused by additional phase lag from the capacitive load. Higher capacitance at the output can increase the amount of overshoot and ringing in the amplifier's step response and could even affect the stability of the device. The value of capacitance load an amplifier can drive before oscillation varies with gain, supply voltage, input signal, temperature, and frequency, among others. Unity gain is the most challenging configuration for driving capacitance load. However, the AD8517 offers good capacitance driving ability. Table II shows the AD8517's ability to capacitance load at different gains before instability occurs. This table is good for all V_{SY}.

Table II. Gain and Capacitance Load

Gain	Max Capacitance
1	400 pF
2	1.5 nF
2.5	8 nF
3	Unconditionally Stable

In-the-Loop Compensation Technique for Driving Capacitive Loads

When driving capacitive loads in unity configuration, the in-the-loop compensation technique is recommended to avoid oscillation as is illustrated in Figure 22.

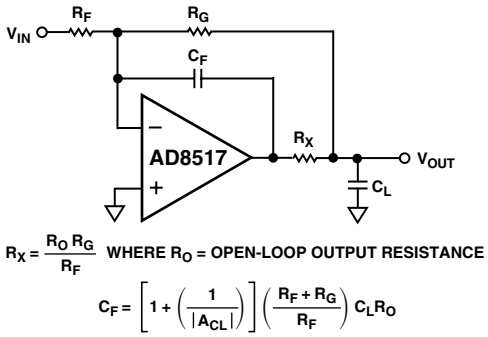


Figure 22. In-the-Loop Compensation Technique for Driving Capacitive Loads

Snubber Network Compensation for Driving Capacitive Loads

As load capacitance increases, the overshoot and settling time will increase and the unity gain bandwidth of the device will decrease. Figure 23 shows an example of the AD8517 configured for unity gain and driving a 10 kΩ resistor and a 680 pF capacitor placed in parallel, with a square wave input set to a frequency of 250 kHz and unity gain.

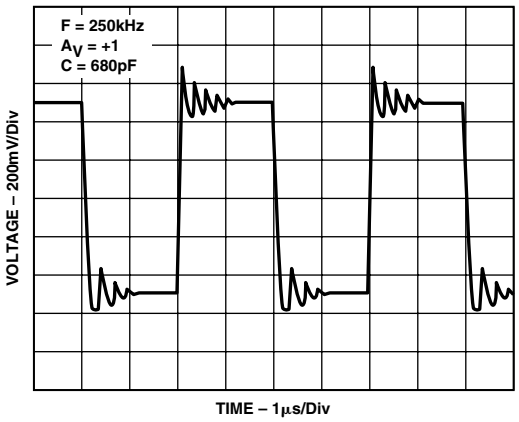


Figure 23. Photo of a Ringing Square Wave

By connecting a series R–C from the output of the device to ground, known as the "snubber" network, this ringing and overshoot can be significantly reduced. Figure 24 shows the network setup, and Figure 25 shows the improvement of the output response with the "snubber" network added.

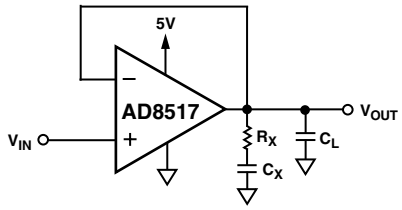


Figure 24. Snubber Network Compensation for Capacitive Loads

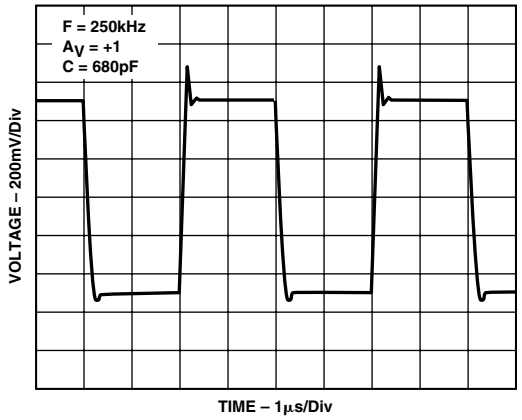


Figure 25. Photo of a Square Wave with the Snubber Network Compensation

The network operates in parallel with the load capacitor, C_L, and provides compensation for the added phase lag. The actual values of the network resistor and capacitor have to be empirically determined. Table III shows some values of snubber network for large capacitance load.

Table III. Snubber Network Values for Large Capacitive Loads

C_{LOAD}	Rx	Cx
680 pF	300 Ω	3 nF
1 nF	100 Ω	10 nF
10 nF	400 Ω	30 nF

TOTAL HARMONIC DISTORTION + NOISE

The AD85x7 family offers a low total harmonic distortion, which makes this amplifier ideal for audio applications. Figure 26 shows a graph of THD + N, for a V_S > 3 V the THD + N is about 0.001% and 0.03% for $V_S \geq 1.8$ V in a noninverting configuration with a gain of 1. In an inverting configuration, the noise is 0.003% for all V_{SY}.

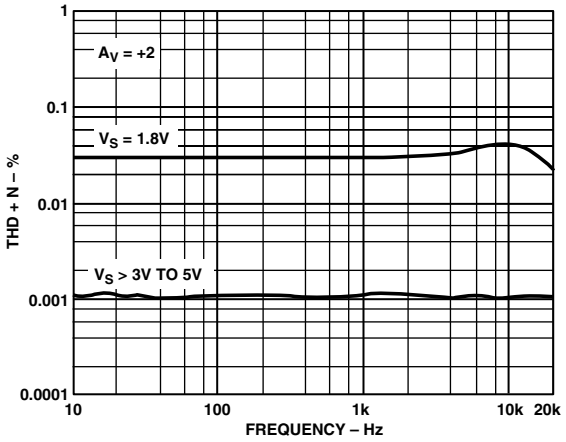


Figure 26. THD + N vs. Frequency Graph

A MICROPOWER REFERENCE VOLTAGE GENERATOR

Many single supply circuits are configured with the circuit-biased to one-half of the supply voltage. In these cases, a false-ground reference can be created by using a voltage divider buffered by an amplifier. Figure 27 shows the schematic for such a circuit.

The two 1 MΩ resistors generate the reference voltages while drawing only 0.9 μA of current from a 1.8 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow for a bypass capacitor to be connected at the reference output. This bypass capacitor helps establish an ac ground for the reference output.

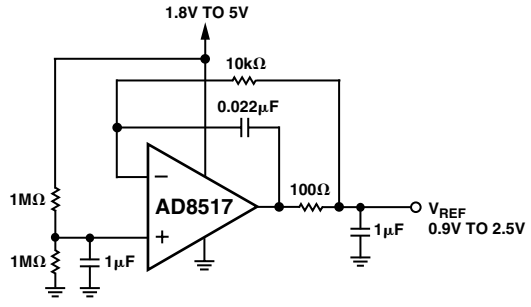


Figure 27. A Micropower Reference Voltage Generator

MICROPHONE PREAMPLIFIER

The AD8517 is ideal to use as a microphone preamplifier. Figure 28 shows this implementation.

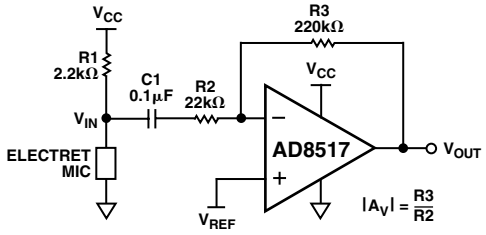


Figure 28. A Microphone Preamplifier

R1 is used to bias an electret microphone and C1 blocks dc voltage from the amplifier. The magnitude of the gain of the amplifier is approximately R3/R2 when R2 ≥ 10 × R1. V_{REF} should be equal to 1/2 1.8 V for maximum voltage swing.

Direct Access Arrangement for Telephone Line Interface

Figure 28 illustrates a 1.8 V transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer-coupled 600 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Amplifier A3 is configured as a difference amplifier for two reasons: (1) It prevents the transmit signal from interfering with the receive signal and (2) it extracts the receive signal from the transmission line for amplification by A4. A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the AD8517/AD8527's 5-lead SOT-23, 8-lead MSOP, and 8-lead SOIC footprint and this circuit offers a compact solution.

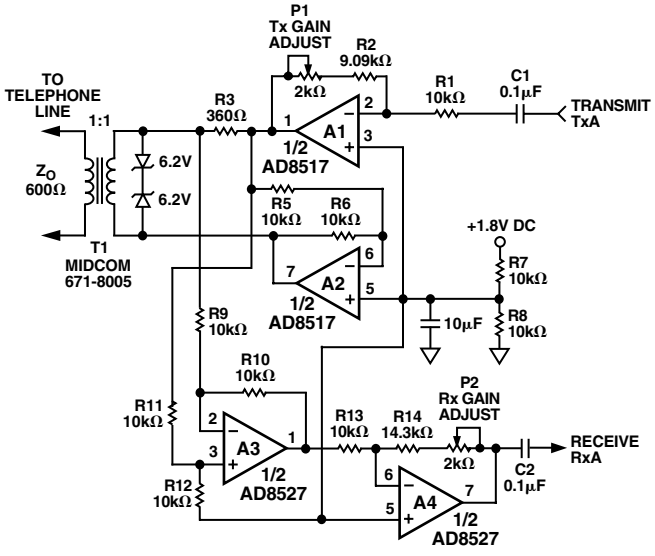


Figure 29. A Single-Supply Direct Access Arrangement for Modems

SPICE Model

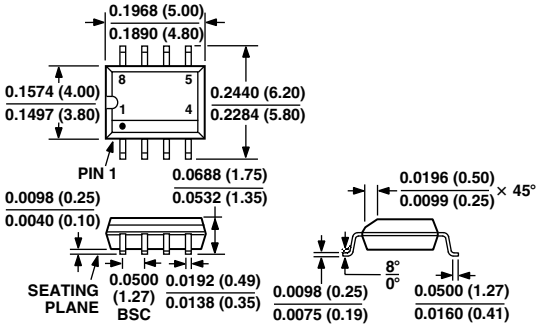
The SPICE model for the AD8517 amplifier is available and can be downloaded from the Analog Devices' web site at **http://www.analog.com**. The macro-model accurately simulates a number of AD8517 parameters, including offset voltage, input common-mode range, and rail-to-rail output swing. The output voltage versus output current characteristics of the macro-model is identical to the actual AD8517 performance, which is a critical feature with a rail-to-rail amplifier model. The model also accurately simulates many ac effects, such as gain-bandwidth product, phase margin, input voltage noise, CMRR and PSRR versus frequency, and transient response. Its high degree of model accuracy makes the AD8517 macro-model one of the most reliable and true-to-life models available for any amplifier.

C3736b–2.5–7/00 (rev. B) 01020

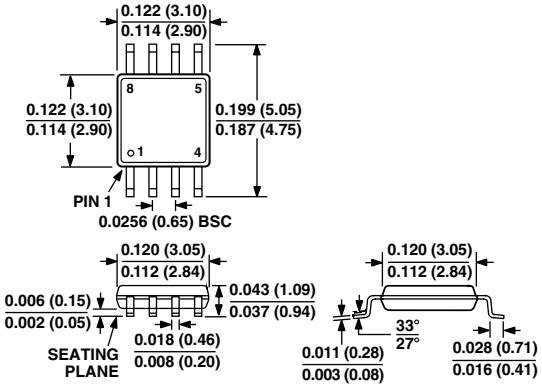
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

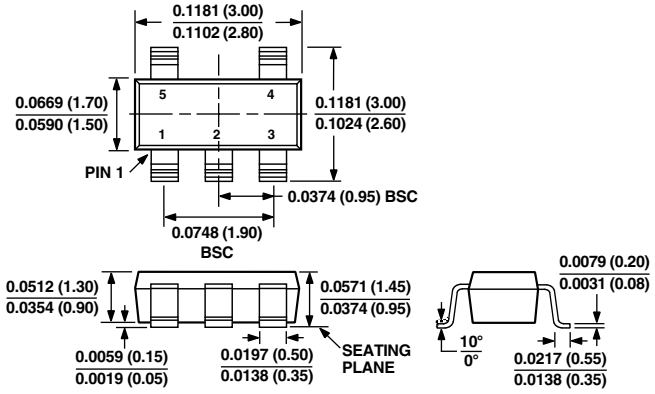
8-Lead Narrow Body SOIC (SO-8)



8-Lead MSOP (RM-8)



5-Lead SOT-23 (RT-5)



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