8-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 20-Lead TSSOP

Data Sheet **AD7927**

FEATURES

Fast throughput rate: 200 kSPS
Specified for AV_{DD} of 2.7 V to 5.25 V
Low power
3.6 mW maximum at 200 kSPS with 3 V supply
7.5 mW maximum at 200 kSPS with 5 V supply
8 (single-ended) inputs with sequencer
Wide input bandwidth
70 dB minimum SINAD at 50 kHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface SPI-, QSPI™-, MICROWIRE™-, DSP-compatible
Shutdown mode: 0.5 µA maximum
20-lead TSSOP
Qualified for automotive applications

GENERAL DESCRIPTION

The AD7927 is a 12-bit, high speed, low power, 8-channel, successive approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 200 kSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 8 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7927 uses advanced design techniques to achieve very low power dissipation at maximum throughput rates. At maximum throughput rates, the AD7927 consumes 1.2 mA maximum with 3 V supplies; with 5 V supplies, the current consumption is 1.5 mA maximum.

Through the configuration of the control register, the analog input range for the part can be selected as 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, with either straight binary or twos complement output coding. The AD7927 features eight single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially.

The conversion time for the AD7927 is determined by the SCLK frequency, as this is also used as the master clock to control the conversion. The conversion time may be as short as 800 ns with a 20 MHz SCLK.

FUNCTIONAL BLOCK DIAGRAM

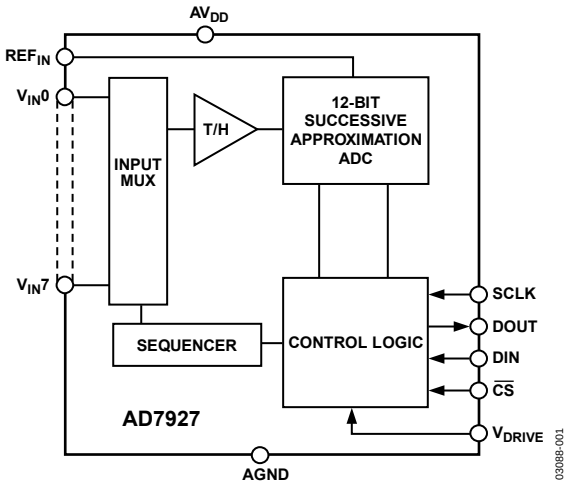

Figure 1.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption.
   The AD7927 offers up to 200 kSPS throughput rates. At the maximum throughput rate with 3 V supplies, the AD7927 dissipates 3.6 mW of power maximum.

2. Eight Single-Ended Inputs with a Channel Sequencer.
   A consecutive sequence of channels can be selected on which the ADC cycles and converts.

3. Single-Supply Operation with V_{DRIVE} Function.
   The AD7927 operates from a single 2.7 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of AV_{DD}.

4. Flexible Power/Serial Clock Speed Management.
   The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The part also features various shutdown modes to maximize power efficiency at lower throughput rates. Current consumption is 0.5 µA maximum when in full shutdown.

5. No Pipeline Delay.
   The part features a standard successive approximation ADC with a $\overline{CS}$ input pin, which allows for accurate control of each sampling instant.

Rev. D Document Feedback

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- AD7927 Evaluation kit

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Data Sheet

- AD7927: 8-Channel, 200 kSPS, 12-Bit ADC with Sequencer in 20-Lead TSSOP Data Sheet

Product Highlight

- 8- to 18-Bit SAR ADCs ... From the Leader in High Performance Analog

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7927 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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SPECIFICATIONS

AV_{DD} = V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK} = 20 MHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz
Signal-to-(Noise + Distortion) (SINAD)[2]	70	dB min	@ 5 V, B models
	69.5	dB min	@ 5 V, W models
	69	dB min	@ 3 V Typically 70 dB
Signal-to-Noise Ratio (SNR)[2]	70	dB min	B models
	69.5	dB min	W models
Total Harmonic Distortion (THD)[2]	−77	dB max	@ 5 V Typically −84 dB
	−73	dB max	@ 3 V Typically −77 dB
Peak Harmonic or Spurious Noise	−78	dB max	@ 5 V Typically −86 dB
(SFDR)[2]	−76	dB max	@ 3 V Typically −80 dB
Intermodulation Distortion (IMD)[2]			f_A = 40.1 kHz, f_B = 41.5 kHz
Second-Order Terms	−90	dB typ	
Third-Order Terms	−90	dB typ	
Aperture Delay	10	ns typ	
Aperture Jitter	50	ps typ	
Channel-to-Channel Isolation[2]	−82	dB typ	f_{IN} = 400 kHz
Full Power Bandwidth	8.2	MHz typ	@ 3 dB
	1.6	MHz typ	@ 0.1 dB
DC ACCURACY[2]			
Resolution	12	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	−0.9/+1.5	LSB max	Guaranteed no missed codes to 12 bits
0 V to REF_{IN} Input Range			Straight binary output coding
Offset Error	±8	LSB max	Typically ±0.5 LSB
Offset Error Match	±0.5	LSB max	
Gain Error	±1.5	LSB max	
Gain Error Match	±0.5	LSB max	
0 V to 2 × REF_{IN} Input Range			−REF_{IN} to +REF_{IN} biased about REF_{IN} with
Positive Gain Error	±1.5	LSB max	Twos complement output coding
Positive Gain Error Match	±0.5	LSB max	
Zero Code Error	±8	LSB max	Typically ±0.8 LSB
Zero Code Error Match	±0.5	LSB max	
Negative Gain Error	±1	LSB max	
Negative Gain Error Match	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to REF_{IN}	V	RANGE bit set to 1
	0 to 2 × REF_{IN}	V	RANGE bit set to 0, AV_{DD}/V_{DRIVE} = 4.75 V to 5.25 V
DC Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	f_{SAMPLE} = 200 kSPS
REFERENCE INPUT			
REF_{IN} Input Voltage	2.5	V	±1% specified performance
DC Leakage Current	±1	µA max	
REF_{IN} Input Impedance	36	kΩ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}	V min	
Input Low Voltage, V_{INL}	0.3 × V_{DRIVE}	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	

Parameter	B Version[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} − 0.2	V min	I_{SOURCE} = 200 µA, AV_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance[3]	10	pF max	
Output Coding			
Straight (Natural) Binary			Coding bit set to 1
Twos Complement			Coding bit set to 0
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time	300	ns max	Sine wave input
	300	ns max	Full-scale step input
Throughput Rate	200	kSPS max	See Serial Interface section
POWER REQUIREMENTS			
AV_{DD}	2.7/5.25	V min/max	
V_{DRIVE}	2.7/5.25	V min/max	
I_{DD}[4]			Digital inputs = 0 V or V_{DRIVE}
During Conversion	2.7	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Normal Mode (Static)	600	µA typ	AV_{DD} = 2.7 V to 5.25 V, SCLK on or off
Normal Mode (Operational) f_{SAMPLE} = 200 kSPS	1.5	mA max	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	1.2	mA max	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Using Auto Shutdown Mode f_{SAMPLE} = 200 kSPS	900	µA typ	AV_{DD} = 4.75 V to 5.25 V, f_{SCLK} = 20 MHz
	650	µA typ	AV_{DD} = 2.7 V to 3.6 V, f_{SCLK} = 20 MHz
Auto Shutdown (Static)	0.5	µA max	SCLK on or off (20 nA typ)
Full Shutdown Mode	0.5	µA max	SCLK on or off (20 nA typ)
Power Dissipation[4]			
Normal Mode (Operational)	7.5	mW max	AV_{DD} = 5 V, f_{SCLK} = 20 MHz
	3.6	mW max	AV_{DD} = 3 V, f_{SCLK} = 20 MHz
Auto Shutdown (Static)	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V
Full Shutdown Mode	2.5	µW max	AV_{DD} = 5 V
	1.5	µW max	AV_{DD} = 3 V

[1] Temperature ranges as follows: B Version: −40°C to +85°C; W Version: −40°C to +125°C.
[2] See Terminology section.
[3] Sample tested @ 25°C to ensure compliance.
[4] See Power vs. Throughput Rate section.

TIMING SPECIFICATIONS[1]

AV_{DD} = 2.7 V to 5.25 V, $V_{DRIVE} \le AV_{DD}$, REF_{IN} = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

	Limit at T_{MIN}, T_{MAX} AD7927			
Parameter	**AV_{DD} = 3 V**	**AV_{DD} = 5 V**	**Unit**	**Description**
f_{SCLK}[2]	10	10	kHz min	
	20	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}		
t_{QUIET}	50	50	ns min	Minimum quiet time required between $\overline{CS}$ rising edge and start of next conversion
t_2	10	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	35	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4[3]	40	40	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulsewidth
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulsewidth
t_7	10	10	ns min	SCLK to DOUT valid hold time
t_8[4]	15/45	15/35	ns min/max	SCLK falling edge to DOUT high impedance
t_9	10	10	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	20	ns min	Sixteenth SCLK falling edge to $\overline{CS}$ high
t_{12}	1	1	µs max	Power-up time from full power-down/auto shutdown mode

[1] Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of AV_{DD}) and timed from a voltage level of 1.6 V, (see Figure 2). The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 0.7 × V_{DRIVE}.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means the time, quoted in the t_8 timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

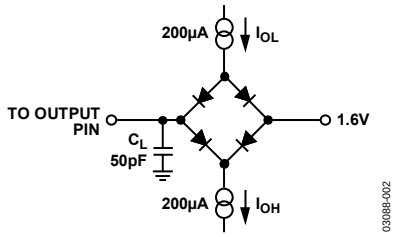

Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
V_{DRIVE} to AGND	−0.3 V to AV_{DD} + 0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to AGND	−0.3 V to +7 V
Digital Output Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
REF_{IN} to AGND	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Automotive (W Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	143°C/W (TSSOP)
θ_{JC} Thermal Impedance	45°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

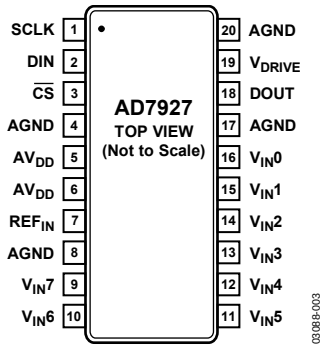

Figure 3. 20-Lead TSSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7927 conversion process.
2	DIN	Data In. Logic input. Data to be written to the AD7927 control register is provided on this input and is clocked into the register on the falling edge of SCLK (see the Control Register section).
3	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7927 and framing the serial data transfer.
4, 8, 17, 20	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7927. All analog input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
5, 6	AV_{DD}	Analog Power Supply Input. The AV_{DD} range for the AD7927 is from 2.7 V to 5.25 V. For the 0 V to 2 × REF_{IN} range, AV_{DD} should be from 4.75 V to 5.25 V.
7	REF_{IN}	Reference Input for the AD7927. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ±1% for specified performance.
16 to 9	$V_{IN}0$ to $V_{IN}7$	Analog Input 0 through Analog Input 7. Eight single-ended analog input channels that are multiplexed into the on-chip track-and-hold. The analog input channel to be converted is selected by using the address bits (ADD2 through ADD0) of the control register. ADD2 through ADD0, in conjunction with the SEQ and SHADOW bits, allow the sequencer to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or 0 V to 2 × REF_{IN}, as selected via the RANGE bit in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
18	DOUT	Data Out. Logic output. The conversion result from the AD7927 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7927 consists of two leading zeros, two address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data (MSB first). The output coding may be selected as straight binary or twos complement via the CODING bit in the control register.
19	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the AD7927 operates.

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition. Figure 9 shows a typical INL plot for the AD7927.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC. Figure 10 shows a typical DNL plot for the AD7927.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two channels.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (that is, REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in gain error between any two channels.

Zero Code Error
This applies when using the twos complement output coding option, in particular to the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the midscale transition (all 0s to all 1s) from the ideal V_{IN} voltage, that is, REF_{IN} − 1 LSB.

Zero Code Error Match
This is the difference in zero code error between any two channels.

Positive Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the last code transition (011. . .110) to (011 . . . 111) from the ideal (that is, +REF_{IN} − 1 LSB) after the zero code error has been adjusted out.

Positive Gain Error Match
This is the difference in positive gain error between any two channels.

Negative Gain Error
This applies when using the twos complement output coding option, in particular to the 2 × REF_{IN} input range with −REF_{IN} to +REF_{IN} biased about the REF_{IN} point. It is the deviation of the first code transition (100 . . . 000) to (100 . . . 001) from the ideal (that is, −REF_{IN} + 1 LSB) after the zero code error has been adjusted out.

Negative Gain Error Match
This is the difference in negative gain error between any two channels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 400 kHz sine wave signal to all seven nonselected input channels and determining how much that signal is attenuated in the selected channel with a 50 kHz signal. The figure given is the worst case across all eight channels for the AD7927.

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition, but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

Power Supply Rejection Ration (PSRR)
The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency (f) to the power of a 200 mV p-p sine wave applied to the ADC AV_{DD} supply of frequency (f_S):

$$PSRR(\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in ADC output.
Pf_S is equal to the power at Frequency f_S coupled onto the ADC AV_{DD}.

Here a 200 mV p-p sine wave is coupled onto the AV_{DD} supply. Figure 6 shows the power supply rejection ratio vs. supply ripple frequency for the AD7927 with no decoupling.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode at the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02N + 1.76)\text{dB}$$

Thus, for a 12-bit converter, this is 74 dB. Figure 5 shows the signal-to-(noise + distortion) ratio performance vs. input frequency for various supply voltages while sampling at 200 kSPS with an SCLK of 20 MHz.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7927, it is defined as:

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Figure 7 shows a graph of total harmonic distortion vs. analog input frequency for various supply voltages, and Figure 8 shows a graph of total harmonic distortion vs. analog input frequency for various source impedances (see the Analog Input section).

TYPICAL PERFORMANCE CHARACTERISTICS

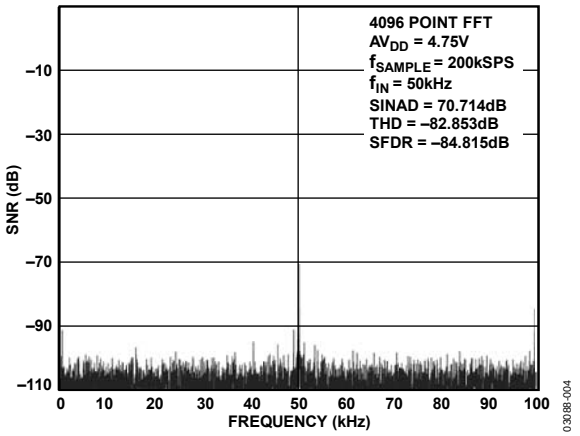

Figure 4. Dynamic Performance at 200 kSPS

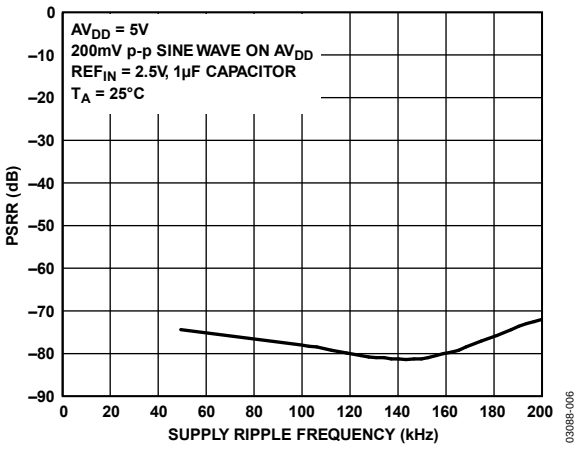

Figure 6. PSRR vs. Supply Ripple Frequency

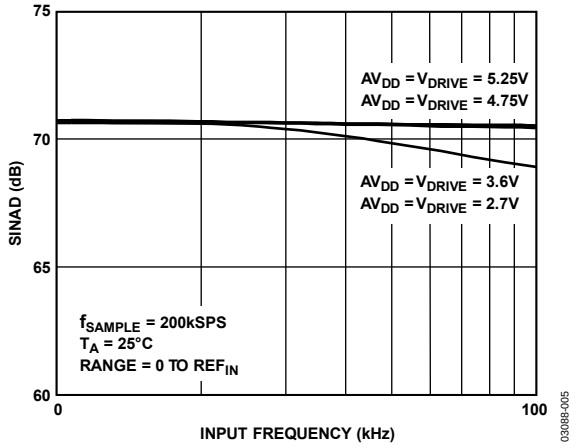

Figure 5. SINAD vs. Analog Input Frequency for Various Supply Voltages at 200 kSPS

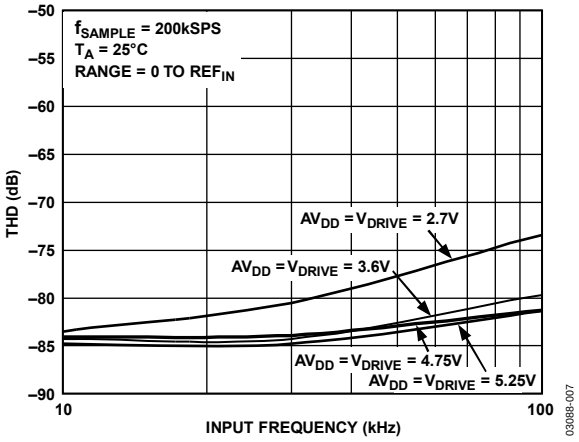

Figure 7. THD vs. Analog Input Frequency for Various Supply Voltages at 200 kSPS

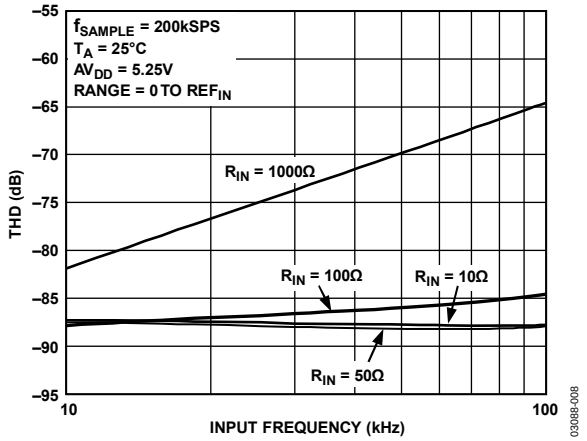

Figure 8. THD vs. Analog Input Frequency for Various Source Impedances

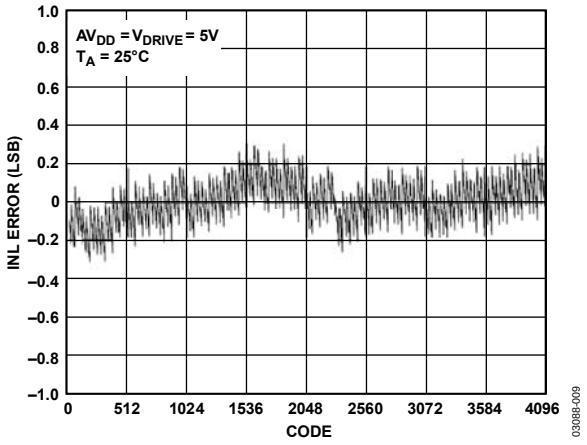

Figure 9. Typical INL

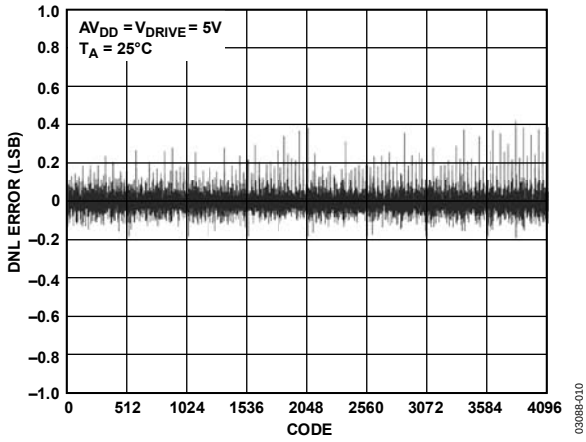

Figure 10. Typical DNL

CONTROL REGISTER

The control register on the AD7927 is a 12-bit, write-only register. Data is loaded from the DIN pin of the AD7927 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line corresponds to the AD7927 configuration for the next conversion. This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after $\overline{CS}$ falling edge) is loaded to the control register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table 5.

Table 5. Control Register Bit Functions

MSB											LSB
WRITE	SEQ	DONTC	ADD2	ADD1	ADD0	PM1	PM0	SHADOW	DONTC	RANGE	CODING

Table 6. Control Register Bit Function Description

Bit	Mnemonic	Description
11	WRITE	The value written to this bit of the control register determines whether the following 11 bits are loaded to the control register. If this bit is a 1, the following 11 bits are written to the control register; if it is a 0, then the remaining 11 bits are not loaded to the control register and it remains unchanged.
10	SEQ	The SEQ bit in the control register is used in conjunction with the SHADOW bit to control the use of the sequencer function and access the shadow register (see Table 10).
9	DONTC	Don't care.
8 to 6	ADD2 to ADD0	These three address bits are loaded at the end of the present conversion and select which analog input channel is to be converted in the next serial transfer, or they may select the final channel in a consecutive sequence as described in Table 9. The selected input channel is decoded as shown in Table 7. The address bits corresponding to the conversion result are also output on DOUT prior to the 12 bits of data (see the Serial Interface section). The next channel to be converted on is selected by the mux on the 14th SCLK falling edge.
5, 4	PM1, PM0	Power Management Bits. These two bits decode the mode of operation of the AD7927 as shown in Table 8.
3	SHADOW	The SHADOW bit in the control register is used in conjunction with the SEQ bit to control the use of the sequencer function and access the shadow register (see Table 10).
2	DONTC	Don't care.
1	RANGE	This bit selects the analog input range to be used on the AD7927. If it is set to 0, the analog input range extends from 0 V to 2 × REF_{IN}. If it is set to 1, the analog input range extends from 0 V to REF_{IN} (for the next conversion). For the 0 V to 2 × REF_{IN} range, AV_{DD} = 4.75 V to 5.25 V.
0	CODING	This bit selects the type of output coding the AD7927 uses for the conversion result. If this bit is set to 0, the output coding for the part is twos complement. If this bit is set to 1, the output coding from the part is straight binary (for the next conversion).

Table 7. Channel Selection

ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	$V_{IN}0$
0	0	1	$V_{IN}1$
0	1	0	$V_{IN}2$
0	1	1	$V_{IN}3$
1	0	0	$V_{IN}4$
1	0	1	$V_{IN}5$
1	1	0	$V_{IN}6$
1	1	1	$V_{IN}7$

Table 8. Power Mode Selection

PM1	PM0	Mode
1	1	Normal Operation. In this mode, the AD7927 remains in full power mode, regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the AD7927.
1	0	Full Shutdown. In this mode, the AD7927 is in full shutdown mode with all circuitry on the AD7927 powering down. The AD7927 retains the information in the control register while in full shutdown. The part remains in full shutdown until these bits are changed.
0	1	Auto Shutdown. In this mode, the AD7927 automatically enters full shutdown mode at the end of each conversion when the control register is updated. Wake-up time from full shutdown is 1 µs and the user should ensure that 1 µs has elapsed before attempting to perform a valid conversion on the part in this mode.
0	0	Invalid Selection. This configuration is not allowed.

SEQUENCER OPERATION

The configuration of the SEQ and SHADOW bits in the control register allows the user to select a particular mode of operation of the sequencer function. Table 9 outlines the four modes of operation of the sequencer.

Table 9. Sequence Selection

SEQ	SHADOW	Sequence Type
0	0	This configuration means that the sequence function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits, ADD0 through ADD2, in each prior write operation. This mode of operation reflects the traditional operation of a multichannel ADC, without the sequencer function being used, where each write to the AD7927 selects the next channel for conversion (see Figure 11).
0	1	This configuration selects the shadow register for programming. The following write operation loads the contents of the shadow register. This programs the sequence of channels converted on continuously with each successive valid $\overline{CS}$ falling edge (see the Shadow Register section, Table 10, and Figure 12). The channels selected need not be consecutive.
1	0	If the SEQ and SHADOW bits are set in this way, the sequence function is not interrupted upon completion of the WRITE operation. This allows other bits in the control register to be altered between conversions while in a sequence, without terminating the cycle.
1	1	This configuration is used in conjunction with the channel address bits, ADD2 to ADD0, to program continuous conversions on a consecutive sequence of channels from Channel 0 to a selected final channel as determined by the channel address bits in the control register (see Figure 13).

SHADOW REGISTER

Table 10. Shadow Register Bit Functions

MSB															LSB
$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$	$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$
----------SEQUENCE ONE----------								----------SEQUENCE TWO----------							

The shadow register on the AD7927 is a 16-bit, write-only register. Data is loaded from the DIN pin of the AD7927 on the falling edge of SCLK. The data is transferred on the DIN line at the same time that a conversion result is read from the part. This requires 16 serial clock falling edges for the data transfer. The information is clocked into the shadow register, provided that the SEQ and SHADOW bits were set to 0, 1, respectively, in the previous write to the control register. MSB denotes the first bit in the data stream. Each bit represents an analog input from Channel 0 to Channel 7. Through programming the shadow register, two sequences of channels may be selected, through which the AD7927 cycles with each consecutive conversion after the write to the shadow register. Sequence One is performed first and then Sequence Two. If the user does not wish to perform a second sequence option, then all 0s must be written to the last eight LSBs of the shadow register. To select a sequence of channels, the associated channel bit must be set for each analog input. The AD7927 continuously cycles through the selected channels in ascending order, beginning with the lowest channel, until a write operation occurs (that is, the WRITE bit is set to 1) with the SEQ and SHADOW bits configured in any way except 1, 0 (see Table 9). The bit functions are outlined in Table 10.

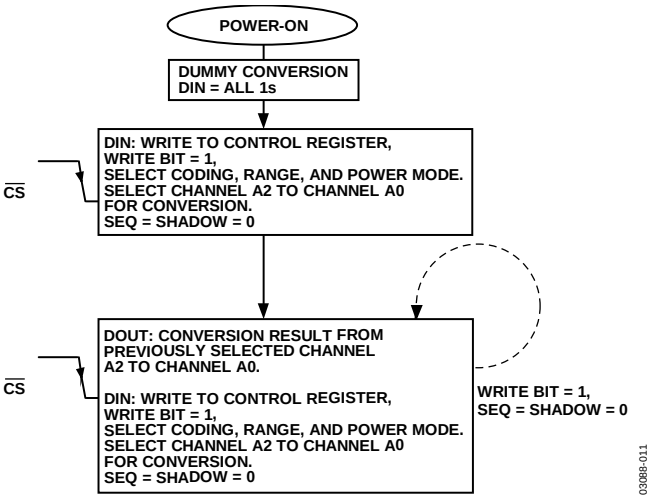

Figure 11. SEQ Bit = 0, SHADOW Bit = 0 Flowchart

Figure 11 reflects the traditional operation of a multichannel ADC, where each serial transfer selects the next channel for conversion. In this mode of operation, the sequencer function is not used.

Figure 12 shows how to program the AD7927 to continuously convert on a particular sequence of channels. To exit this mode of operation and revert back to the traditional mode of operation of a multichannel ADC (as outlined in Figure 11), ensure that the WRITE bit = 1 and the SEQ = SHADOW = 0 on the next serial transfer. Figure 13 shows how a sequence of consecutive channels can be converted on without having to program the shadow register or write to the part on each serial transfer. Again, to exit this mode of operation and revert back to the traditional mode of operation of a multichannel ADC (as outlined in Figure 11), ensure the WRITE bit = 1 and the SEQ = SHADOW = 0 on the next serial transfer.

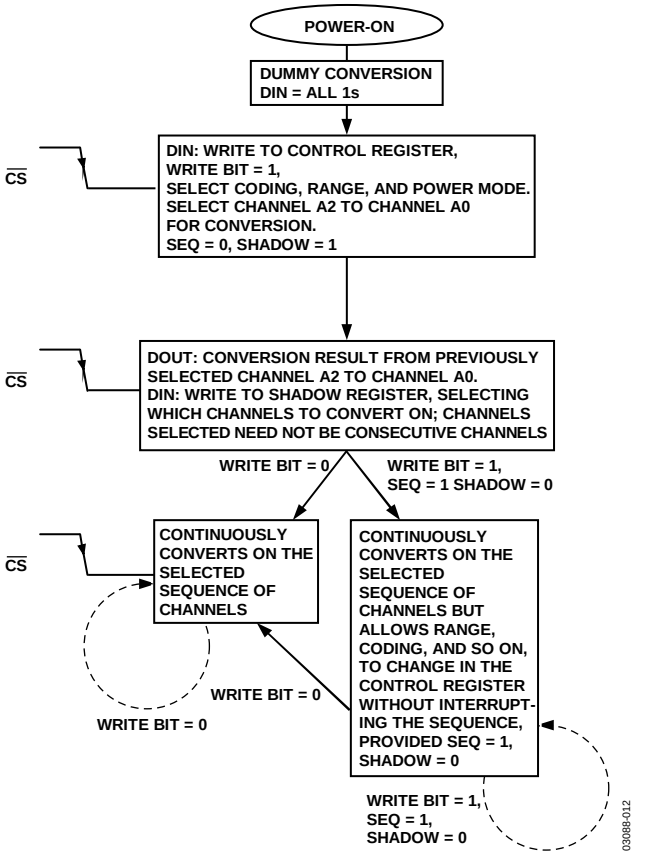

Figure 12. SEQ and SHADOW Conversion Flowchart to Continuously Convert a Sequence of Channels

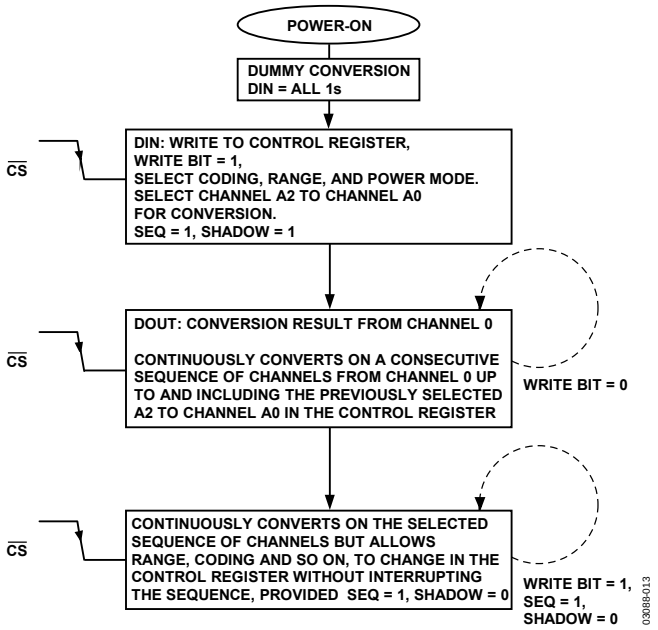

Figure 13. SEQ and SHADOW Conversion Flowchart to Convert a Sequence of Consecutive Channels

CIRCUIT INFORMATION

The AD7927 is a high speed, 8-channel, 12-bit, single-supply ADC. The part can be operated from a 2.7 V to 5.25 V supply. When operated from either a 5 V or 3 V supply, the AD7927 is capable of throughput rates of 200 kSPS. The conversion time may be as short as 800 ns when provided with a 20 MHz clock.

The AD7927 provides the user with an on-chip, track-and-hold ADC and a serial interface housed in a 20-lead TSSOP. The AD7927 has eight single-ended input channels with a channel sequencer, allowing the user to select a channel sequence through which the ADC can cycle with each consecutive $\overline{CS}$ falling edge. The serial clock input accesses data from the part, controls the transfer of data written to the ADC, and provides the clock source for the successive approximation ADC. The analog input range for the AD7927 is 0 V to REF_{IN} or 0 V to $2 \times REF_{IN}$, depending on the status of Bit 1 in the control register. For the 0 to $2 \times REF_{IN}$ range, the part must be operated from a 4.75 V to 5.25 V supply.

The AD7927 provides flexible power management options to allow the user to achieve the best power performance for a given throughput rate. These options are selected by programming the power management bits, PM1 and PM0, in the control register.

CONVERTER OPERATION

The AD7927 is a 12-bit successive approximation ADC based around a capacitive DAC. The AD7927 can convert analog input signals in the range 0 V to REF_{IN} or 0 V to $2 \times REF_{IN}$. Figure 14 and Figure 15 show simplified schematics of the ADC. The ADC is comprised of control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 14 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on the selected V_{IN} channel.

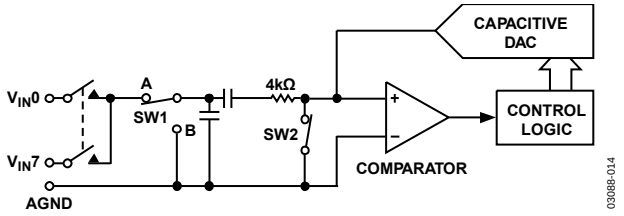

Figure 14. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 15), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 17 and Figure 18 show the ADC transfer functions.

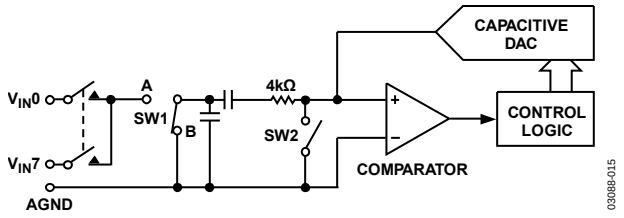

Figure 15. ADC Conversion Phase

ANALOG INPUT

Figure 16 shows an equivalent circuit of the analog input structure of the AD7927. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This causes these diodes to become forward biased and start conducting current into the substrate. 10 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. Capacitor C1, in Figure 16 is typically about 4 pF and can primarily be attributed to pin capacitance. The Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and also includes the on resistance of the input multiplexer. The total resistance is typically about 400 Ω. The capacitor, C2, is the ADC sampling capacitor and has a capacitance of 30 pF typically.

For ac applications, removing high frequency components from the analog input signal is recommended by use of an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, limit the source impedance to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases, and performance degrades (see Figure 8).

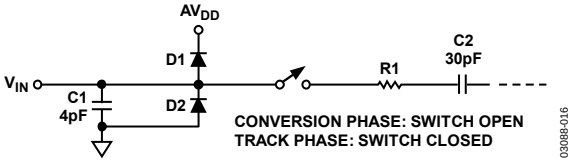

Figure 16. Equivalent Analog Input Circuit

ADC TRANSFER FUNCTION

The output coding of the AD7927 is either straight binary or twos complement, depending on the status of the LSB in the control register. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is $REF_{IN}/4096$ for the AD7927. The ideal transfer characteristic for the AD7927 when straight binary coding is selected is shown in Figure 17, and the ideal transfer characteristic for the AD7927 when twos complement coding is selected is shown in Figure 18.

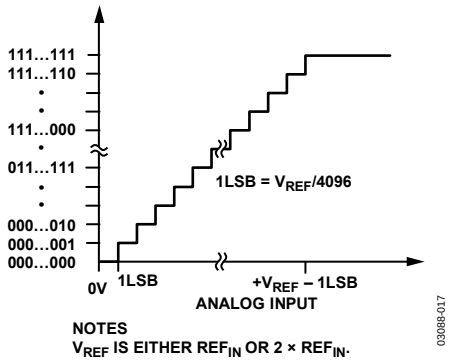

Figure 17. Straight Binary Transfer Characteristic

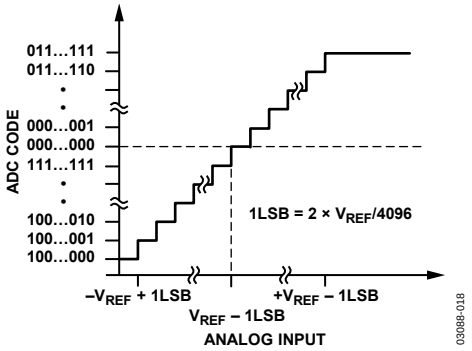

Figure 18. Twos Complement Transfer Characteristic with $REF_{IN} \pm REF_{IN}$ Input Range

HANDLING BIPOLAR INPUT SIGNALS

Figure 19 shows how useful the combination of the $2 \times REF_{IN}$ input range and the twos complement output coding scheme is for handling bipolar input signals. If the bipolar input signal is biased about REF_{IN} and twos complement output coding is selected, then REF_{IN} becomes the zero code point, $-REF_{IN}$ is negative full scale and $+REF_{IN}$ becomes positive full scale, with a dynamic range of $2 \times REF_{IN}$.

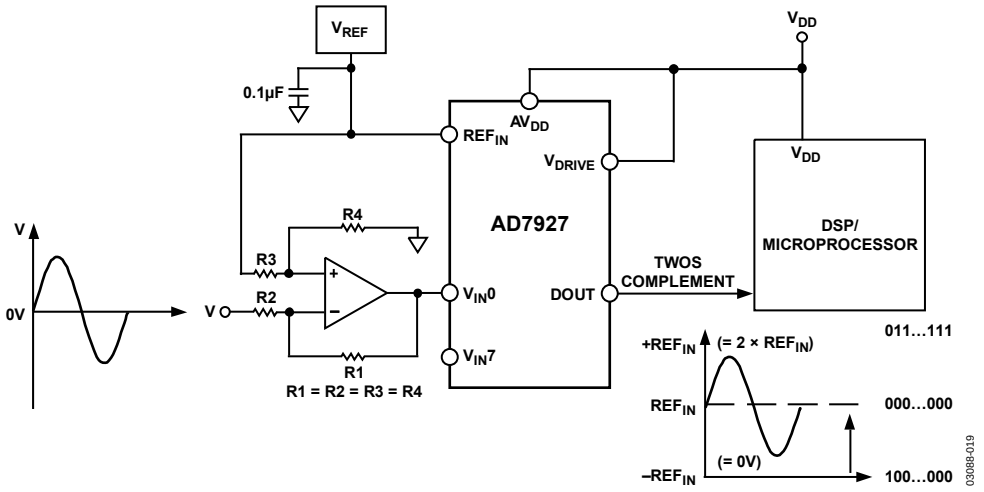

Figure 19. Handling Bipolar Signals

TYPICAL CONNECTION DIAGRAM

Figure 20 shows a typical connection diagram for the AD7927. In this setup, the AGND pin is connected to the analog ground plane of the system. In Figure 20, REF_{IN} is connected to a decoupled 2.5 V supply from a reference source, the AD780, to provide an analog input range of 0 V to 2.5 V (if the RANGE bit is 1) or 0 V to 5 V (if the RANGE bit is 0). Although the AD7927 is connected to a AV_{DD} of 5 V, the serial interface is connected to a 3 V microprocessor. The V_{DRIVE} pin of the AD7927 is connected to the same 3 V supply of the microprocessor to allow a 3 V logic interface (see the Digital Inputs section). The conversion result is output in a 16-bit word. This 16-bit data stream consists of one leading zero, three address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data. For applications where power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance (see the Modes of Operation section).

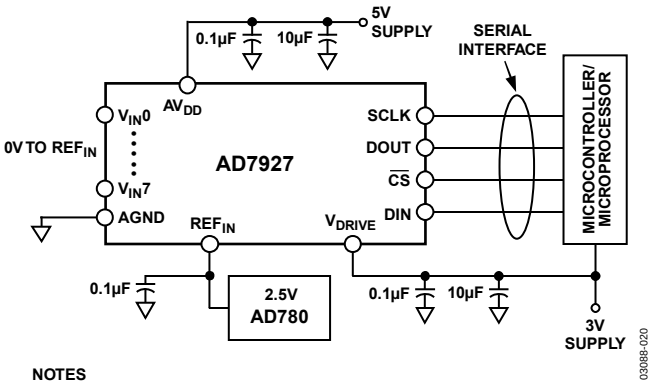

Figure 20. Typical Connection Diagram

ANALOG INPUT SELECTION

Any one of eight analog input channels may be selected for conversion by programming the multiplexer with the address bits (ADD2 though ADD0) in the control register. The channel configurations are shown in Table 7.

The AD7927 may also be configured to automatically cycle through a number of channels as selected. The sequencer feature is accessed via the SEQ and SHADOW bits in the control register (see Table 9). The AD7927 can be programmed to continuously convert on a selection of channels in ascending order. The analog input channels to be converted on are selected through programming the relevant bits in the shadow register (see Table 10). The next serial transfer then acts on the sequence programmed by executing a conversion on the lowest channel in the selection. The next serial transfer results in the conversion on the next highest channel in the sequence, and so on.

It is not necessary to write to the control register once a sequencer operation has been initiated. The WRITE bit must be set to zero or the DIN line tied low to ensure that the control register is not accidentally overwritten, or the sequence operation interrupted. If the control register is written to at any time during the sequence, the user must ensure that the SEQ and SHADOW bits are set to 1, 0, respectively to avoid interrupting the automatic conversion sequence. This pattern continues until such time as the AD7927 is written to and the SEQ and SHADOW bits are configured with any bit combination except 1, 0. On completion of the sequence, the AD7927 sequencer returns to the first selected channel in the shadow register and commence the sequence again.

Rather than selecting a particular sequence of channels, a number of consecutive channels beginning with Channel 0 may also be programmed via the control register alone without needing to write to the shadow register. This is possible if the SEQ and SHADOW bits are set to 1, 1, respectively. The channel address bits, ADD2 through ADD0, then determine the final channel in the consecutive sequence. The next conversion is on Channel 0, then Channel 1, and so on until the channel selected via the Address Bit ADD2 through Address Bit ADD0 is reached. The cycle begins again on the next serial transfer provided the WRITE bit is set to low, or if high, that the SEQ and SHADOW bits are set to 1, 0, respectively; then the ADC continues its preprogrammed automatic sequence uninterrupted.

Regardless of which channel selection method is used, the 16-bit word output from the AD7927 during each conversion always contains one leading zero, three channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result (see the Serial Interface section).

DIGITAL INPUTS

The digital inputs applied to the AD7927 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied can go to 7 V and are not restricted by the AV_{DD} + 0.3 V limit as on the analog inputs.

Another advantage of SCLK, DIN, and $\overline{CS}$ not being restricted by the AV_{DD} + 0.3 V limit is that possible power supply sequencing issues are avoided. If $\overline{CS}$, DIN, or SCLK are applied before AV_{DD}, there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to AV_{DD}.

V_{DRIVE}

The AD7927 also has the V_{DRIVE} feature. V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7927 were operated with an AV_{DD} of 5 V, the V_{DRIVE} pin could be powered from a 3 V supply. The AD7927 has a larger dynamic range with an AV_{DD} of 5 V while still being able to interface to 3 V processors. Take care to ensure V_{DRIVE} does not exceed AV_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

THE REFERENCE

An external reference source should be used to supply the 2.5 V reference to the AD7927. Errors in the reference source result in gain errors in the AD7927 transfer function and add to the specified full-scale errors of the part. A capacitor of at least 0.1 μF should be placed on the REF_{IN} pin. Suitable reference sources for the AD7927 include the AD780, REF192, and the AD1582.

If 2.5 V is applied to the REF_{IN} pin, the analog input range can be either 0 V to 2.5 V or 0 V to 5 V, depending on the setting of the RANGE bit in the control register.

MODES OF OPERATION

The AD7927 has a number of different modes of operation, which are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The mode of operation of the AD7927 is controlled by the power management bits, PM1 and PM0, in the control register, as detailed in Table 8. When power supplies are first applied to the AD7927, care should be taken to ensure that the part is placed in the required mode of operation (see the Powering Up the AD7927 section).

NORMAL MODE (PM1 = PM0 = 1)

This mode is intended for the fastest throughput rate performance because the user does not have to worry about any power-up times with the AD7927 remaining fully powered at all times. Figure 21 shows the general diagram of the operation of the AD7927 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ and the track-and-hold enters hold mode as described in the Serial Interface section. The data presented to the AD7927 on the DIN line during the first 12 clock cycles of the data transfer are loaded into the control register (provided the WRITE bit is 1). If data is to be written to the shadow register (SEQ = 0, SHADOW = 1 on the previous write), data presented on the DIN line during the first 16 SCLK cycles is loaded into the shadow register. The part remains fully powered up in normal mode at the end of the conversion as long as PM1 and PM0 are set to 1 in the write transfer during that conversion. To ensure continued operation in normal mode, PM1 and PM0 are both loaded with 1 on every data transfer. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The track-and-hold goes back into track on the 14th SCLK falling edge. $\overline{CS}$ may then idle high until the next conversion or may idle low until sometime prior to the next conversion (effectively idling $\overline{CS}$ low).

For specified performance, the throughput rate should not exceed 200 kSPS, which means there should be no less than 5 µs between consecutive falling edges of $\overline{CS}$ when converting. The actual frequency of SCLK used determines the duration of the conversion within this 5 µs cycle; however, once a conversion is complete and $\overline{CS}$ has returned high, a minimum of the quiet time, t_{QUIET}, must elapse before bringing $\overline{CS}$ low again to initiate another conversion.

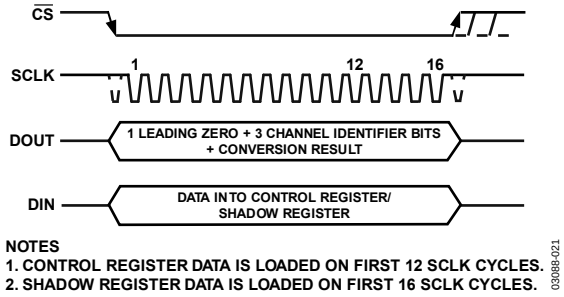

Figure 21. Normal Mode Operation

FULL SHUTDOWN (PM1 = 1, PM0 = 0)

In this mode, all internal circuitry on the AD7927 is powered down. The part retains information in the control register during full shutdown. The AD7927 remains in full shutdown until the power management bits, PM1 and PM0, in the control register are changed.

If a write to the control register occurs while the part is in full shutdown, with the power management bits changed to PM0 = $\overline{CS}$ rising edge. The track-and-hold that was in hold while the part was in full shutdown returns to track on the 14th SCLK falling edge. A full 16-SCLK transfer must occur to ensure the control register contents are updated; however, the DOUT line is not driven during this wake-up transfer.

To ensure that the part is fully powered up, $t_{POWER\ UP}$ should have elapsed before the next $\overline{CS}$ falling edge; otherwise, invalid data is read if a conversion is initiated before this time. Figure 22 shows the general diagram for this sequence.

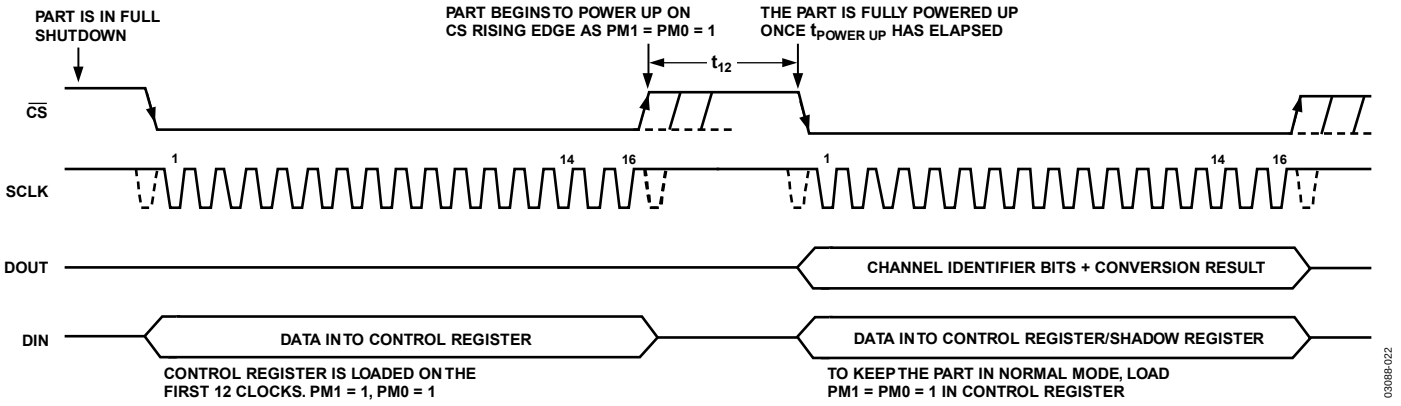

Figure 22. Full Shutdown Mode Operation

AUTO SHUTDOWN (PM1 = 0, PM0 = 1)

In this mode, the AD7927 automatically enters shutdown at the end of each conversion when the control register is updated. When the part is in shutdown, the track-and-hold is in hold mode. Figure 23 shows the general diagram of the operation of the AD7927 in this mode. In shutdown mode all internal circuitry on the AD7927 is powered down. The part retains information in the control register during shutdown. The AD7927 remains in shutdown until the next $\overline{CS}$ falling edge it receives. On this $\overline{CS}$ falling edge, the track-and-hold that was in hold while the part was in shutdown returns to track. Wake-up time from auto shutdown is 1 μs maximum, and the user should ensure that 1 μs has elapsed before attempting a valid conversion. When running the AD7927 with a 20 MHz clock, one dummy 16 SCLK transfer should be sufficient to ensure the part is fully powered up. During this dummy transfer, the contents of the control register should remain unchanged; therefore, the WRITE bit should be 0 on the DIN line.

Depending on the SCLK frequency used, this dummy transfer may affect the achievable throughput rate of the part, with every other data transfer being a valid conversion result. If, for example, the maximum SCLK frequency of 20 MHz was used, the auto shutdown mode could be used at the full throughput rate of 200 kSPS without affecting the throughput rate at all. Only a portion of the cycle time is taken up by the conversion time and the dummy transfer for wake-up.

In this mode, the power consumption of the part is greatly reduced with the part entering shutdown at the end of each conversion. When the control register is programmed to move into auto shutdown, it does so at the end of the conversion. The user can move the ADC in and out of the low power state by controlling the $\overline{CS}$ signal.

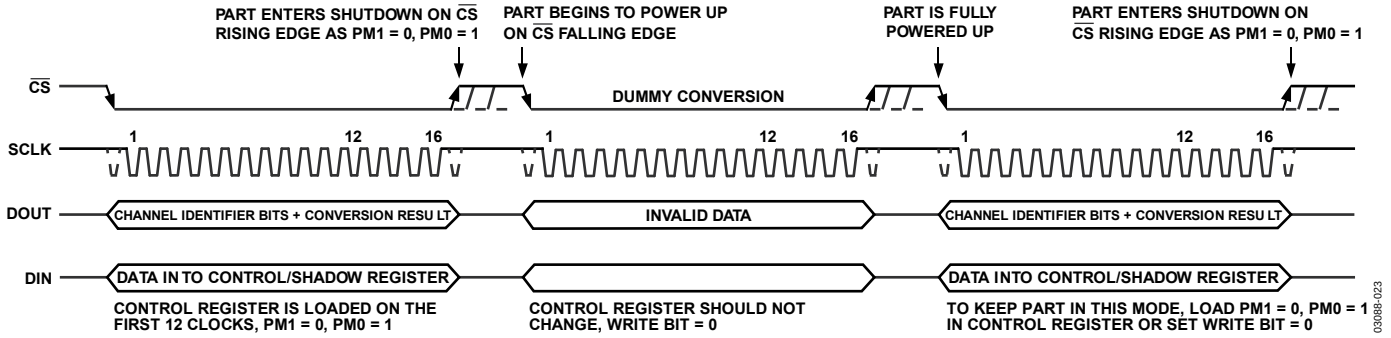

Figure 23. Auto Shutdown Mode Operation

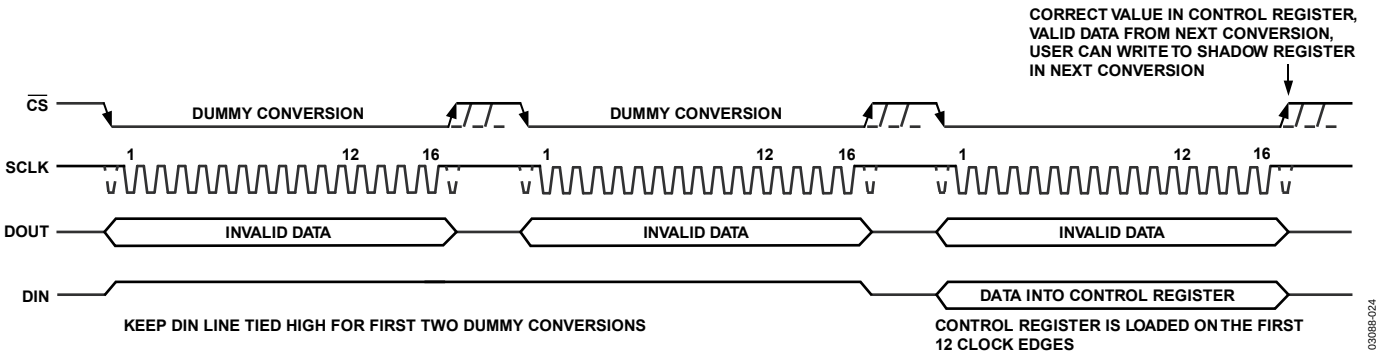

Figure 24. Three-Dummy-Conversions to Place AD7927 into the Required Operating Mode After Power Supplies Are Applied

POWERING UP THE AD7927

When supplies are first applied to the AD7927, the ADC may power up in any of the operating modes of the part. To ensure that the part is placed into the required operating mode, the user should perform a dummy cycle operation as outlined in Figure 24.

The three-dummy-conversion operation outlined in Figure 24 must be performed to place the part into the auto shutdown mode. The first two conversions of this dummy cycle operation are performed with the DIN line tied high, and for the third conversion of the dummy cycle operation, the user should write the desired control register configuration to the AD7927 to place the part into the auto shutdown mode. On the third $\overline{CS}$ rising edge after the supplies are applied, the control register contains the correct information and valid data results from the next conversion.

Therefore, to ensure the part is placed into the correct operating mode, when supplies are first applied to the AD7927, the user must first issue two serial write operations with the DIN line tied high, and on the third conversion cycle the user can then write to the control register to place to part into any of the operating modes. The user should not write to the shadow register until the fourth conversion cycle after the supplies are applied to the ADC, to guarantee the control register contains the correct data.

If the user wishes to place the part into either the normal or full shutdown mode, the second dummy cycle with DIN tied high can be omitted from the three-dummy-conversion operation outlined in Figure 24.

POWER VS. THROUGHPUT RATE

In auto shutdown mode, the average power consumption of the ADC may be reduced at any given throughput rate. The power saving depends on the SCLK frequency used, that is, conversion time. In some cases where the conversion time is quite a proportion of the cycle time, the throughput rate needs to be reduced to take advantage of the power-down modes. Assuming a 20 MHz SCLK is used, the conversion time is 800 ns, but the cycle time is 5 μs when the sampling rate is at a maximum of 200 kSPS. If the AD7927 is placed into shutdown for the remainder of the cycle time, then on average far less power is consumed in every cycle compared to leaving the device in normal mode. Furthermore, Figure 25 shows how as the throughput rate is reduced, the part remains in its shutdown longer and the average power consumption drops accordingly over time.

For example, if the AD7927 is operated in a continuous sampling mode, with a throughput rate of 200 kSPS and an SCLK of 20 MHz (AV_{DD} = 5 V), and the device is placed in auto shutdown mode, that is, if PM1 = 0 and PM0 = 1, then the power consumption is calculated as follows.

The maximum power dissipation during the conversion time is 13.5 mW (I_{DD} = 2.7 mA maximum, AV_{DD} = 5 V). If the power-up time from auto shutdown is 1 μs and the remaining conversion time is another cycle, that is, 800 ns, the AD7927 can be said to dissipate 13.5 mW for 1.8 μs during each conversion cycle. For the remainder of the conversion cycle, 3.2 μs, the part remains in shutdown. The AD7927 can be said to dissipate 2.5 μW for the remaining 3.2 μs of the conversion cycle. If the throughput rate is 200 kSPS, the cycle time is 5 μs and the average power dissipated during each cycle is (1.8/5) × (13.5 mW) + (3.2/5) × (2.5 μW) = 4.8616 mW.

Figure 25 shows the maximum power vs. throughput rate when using the auto shutdown mode with 3 V and 5 V supplies.

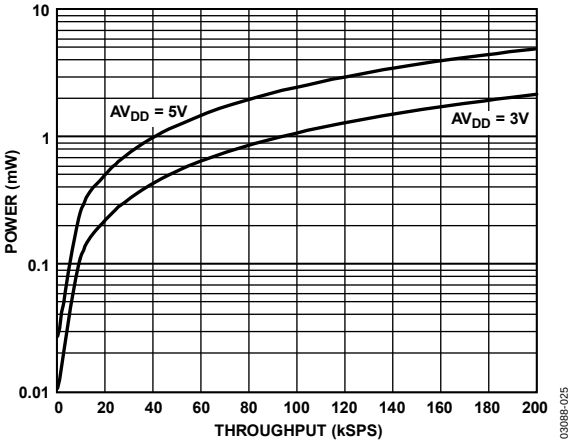

Figure 25. Power vs. Throughput Rate

SERIAL INTERFACE

Figure 26 shows the detailed timing diagram for serial interfacing to the AD7927. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7927 during each conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state; the analog input is sampled at this point. The conversion is also initiated at this point and requires 16 SCLK cycles to complete. The track-and-hold goes back into track on the 14th SCLK falling edge as shown in Figure 26 at Point B, except when the write is to the shadow register, in which case the track-and-hold does not return to track until the rising edge of $\overline{CS}$, that is, Point C in Figure 27. On the 16th SCLK falling edge the DOUT line goes back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion is terminated and the DOUT line goes back into three-state and the control register is not be updated; otherwise DOUT returns to three-state on the 16th SCLK falling edge, as shown in Figure 26. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7927. For the AD7927, the 12 bits of data are preceded by a leading zero and the three-channel address bits (ADD2 to ADD0) identifying which channel the result corresponds to. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The three remaining address bits and data bits are then clocked out by subsequent SCLK falling edges beginning with the first address bit (ADD2) thus the first falling clock edge on the serial clock has a leading zero provided and also clocks out Address Bit ADD2. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

Writing of information to the control register takes place on the first 12 falling edges of SCLK in a data transfer, assuming the MSB (that is, the WRITE bit) has been set to 1. If the control register is programmed to use the shadow register, then the writing of information to the shadow register takes place on all 16 SCLK falling edges in the next serial transfer as shown for example on the AD7927 in Figure 27. Two sequence options can be programmed in the shadow register. If the user does not want to program a second sequence, then the eight LSBs should be filled with zeros. The shadow register is updated upon the rising edge of $\overline{CS}$ and the track-and-hold begins to track the first channel selected in the sequence.

The 16-bit word read from the AD7927 always contains a leading zero and three-channel address bits that the conversion result corresponds to, followed by the 12-bit conversion result.

WRITING BETWEEN CONVERSIONS

As outlined in the Modes of Operation section, no less than 5 µs should be left between consecutive valid conversions. However, there is one case where this does not necessarily mean that at least 5 µs should always be left between $\overline{CS}$ falling edges. Consider the prior to a valid conversion. The user must write to the part to tell it to power up before it can convert successfully. Once the serial write to power up has finished, it may be desirable to perform the conversion as soon as possible and not have to wait a further 5 µs before bringing $\overline{CS}$ low for the conversion. In this case, as long as there is a minimum of 5 µs between each valid conversion, then only the quiet time between the $\overline{CS}$ rising edge at the end of the write to power up and the next $\overline{CS}$ falling edge for a valid conversion needs to be met (see Figure 28). Note that when writing to the AD7927 between these valid conversions, the DOUT line is not driven during the extra write operation, as shown in Figure 28.

It is critical that an extra write operation as outlined previously is never issued between valid conversions when the AD7927 is executing through a sequence function, as the falling edge of $\overline{CS}$ in the extra write would move the mux on to the next channel in the sequence. This means when the next valid conversion takes place, a channel result would have been missed.

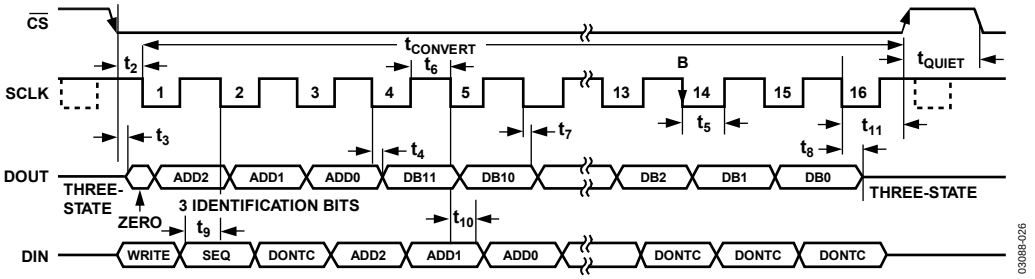

Figure 26. Serial Interface Timing Diagram

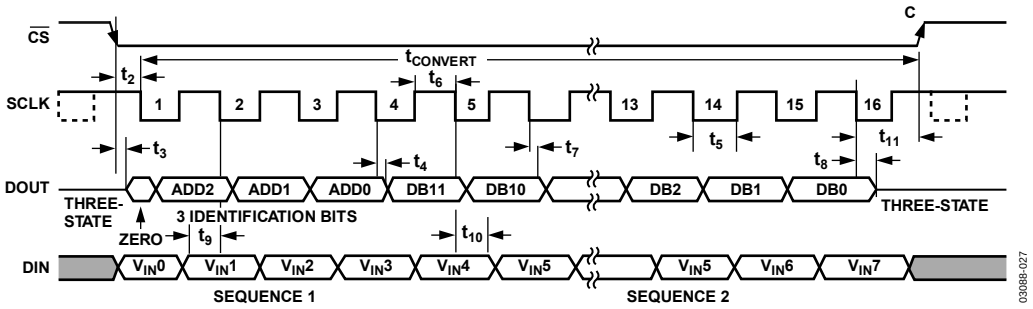

Figure 27. Writing to Shadow Register Timing Diagram

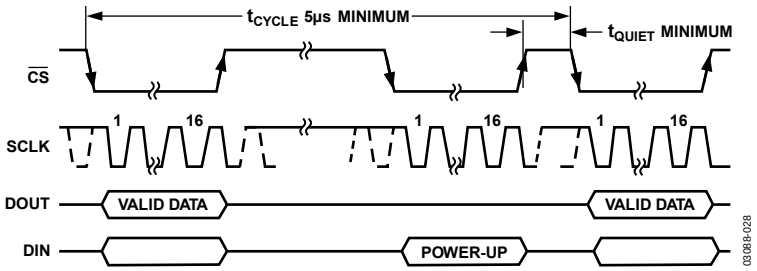

Figure 28. General Timing Diagram

MICROPROCESSOR INTERFACING

The serial interface on the AD7927 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7927 with some of the more common microcontroller and DSP serial interface protocols.

AD7927 TO TMS320C541

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7927. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7927 without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode with internal CLKX0 (TX serial clock on Serial Port 0) and FSX0 (TX frame sync from Serial Port 0). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1, and TXM = 1. The connection diagram is shown in Figure 29. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provides equidistant sampling. The V_{DRIVE} pin of the AD7927 takes the same supply voltage as that of the TMS320C541. This allows the ADC to operate at a higher voltage than the serial interface, that is, TMS320C541, if necessary.

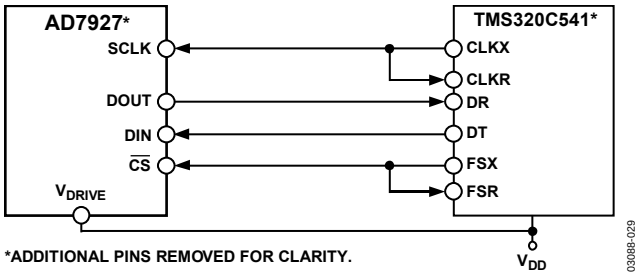

Figure 29. Interfacing to the TMS320C541

AD7927 TO ADSP-21xx

The ADSP-21xx family of DSPs is interfaced directly to the AD7927 without any glue logic required. The V_{DRIVE} pin of the AD7927 takes the same supply voltage as that of the ADSP-218x. This allows the ADC to operate at a higher voltage than the serial interface, that is, ADSP-218x, if necessary.

The SPORT0 control register should be set up as follows:

TFSW = RFSW = 1, alternate framing

INVRFS = INVTFS = 1, active low frame signal

DTYPE = 00, right justify data

SLEN = 1111, 16-bit data-words

ISCLK = 1, internal serial clock

TFSR = RFSR = 1, frame every word

IRFS = 0

ITFS = 1

The connection diagram is shown in Figure 30. The ADSP-218x has the TFS and RFS of the SPORT0 tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode and the SPORT0 control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC, and under certain conditions, equidistant sampling may not be achieved.

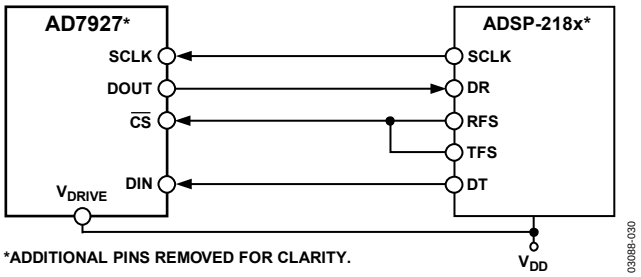

Figure 30. Interfacing to the ADSP-218x

The timer register, for instance, is loaded with a value that provides an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS or DT, (ADC control word). The TFS is used to control the RFS and therefore the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (that is, AX0 = TX0), the state of the SCLK is checked. The DSP waits until the SCLK has gone high, low, and high before transmission starts. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, then the data may be transmitted or it may wait until the next clock edge.

For example, if the ADSP-2189 had a 20 MHz crystal such that it had a master clock frequency of 40 MHz, then the master cycle time would be 25 ns. If the SCLKDIV register is loaded with the value of 3, then an SCLK of 5 MHz is obtained and eight master clock periods elapse for every one SCLK period. Depending on the throughput rate selected, if the timer registers are loaded with the value, of 803, for example, then 100.5 SCLKs occur between interrupts and subsequently between transmit instructions. This situation results in sampling that is not equidistant as the transmit instruction is occurring on a SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, then equidistant sampling is implemented by the DSP.

AD7927 TO DSP563xx

The connection diagram in Figure 31 shows how the AD7927 can be connected to the enhanced synchronous serial interface (ESSI) of the DSP563xx family of DSPs from Motorola. Each ESSI (two on board) is operated in synchronous mode (SYN bit in CRB = 1) with internally generated word length frame sync for both TX and RX (Bit FSL1 = 0 and Bit FSL0 = 0 in CRB). Normal operation of the ESSI is selected by making MOD = 0 in the CRB. Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. The FSP bit in the CRB should be set to 1 so the frame sync is negative. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx provides equidistant sampling.

In the example shown in Figure 31, the serial clock is taken from the ESSI so the SCK0 pin must be set as an output, SCKD = 1. The V_{DRIVE} pin of the AD7927 takes the same supply voltage as that of the DSP563xx. This allows the ADC to operate at a higher voltage than the serial interface, that is, DSP563xx, if necessary.

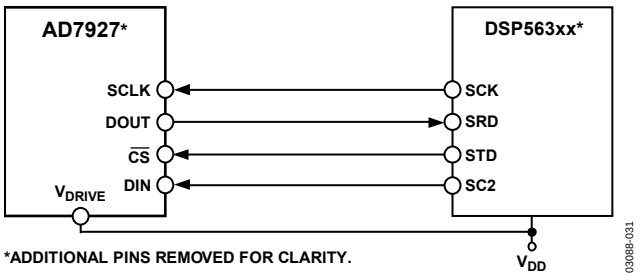

Figure 31. Interfacing to the DSP563xx

APPLICATION HINTS

GROUNDING AND LAYOUT

The AD7927 has very good immunity to noise on the power supplies as can be seen in Figure 6. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7927 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. All three AGND pins of the AD7927 should be sunk in the AGND plane. Digital and analog ground planes should be joined at only one place. If the AD7927 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7927.

Avoid running digital lines under the device as these couple noise onto the die. The analog ground plane should be allowed to run under the AD7927 to avoid noise coupling. The power supply lines to the AD7927 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, like clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

OUTLINE DIMENSIONS

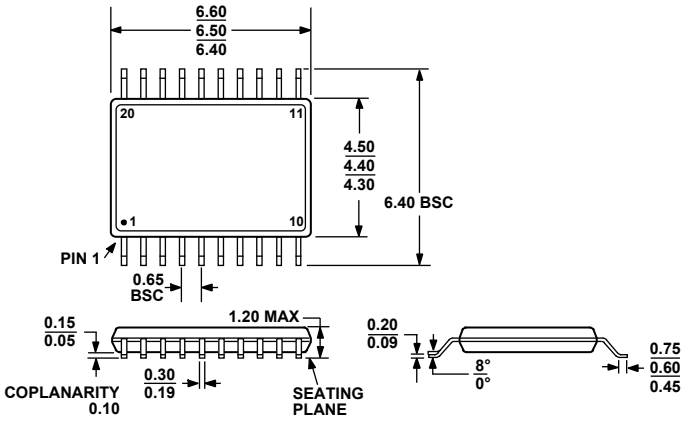

Figure 32. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Linearity Error (LSB)[3]	Package Description	Package Option
AD7927BRU	−40°C to +85°C	±1	20-Lead TSSOP	RU-20
AD7927BRU-REEL	−40°C to +85°C	±1	20-Lead TSSOP	RU-20
AD7927BRUZ	−40°C to +85°C	±1	20-Lead TSSOP	RU-20
AD7927BRUZ-REEL	−40°C to +85°C	±1	20-Lead TSSOP	RU-20
AD7927BRUZ–REEL7	−40°C to +85°C	±1	20-Lead TSSOP	RU-20
AD7927WYRUZ-REEL7	−40°C to +125°C	±1	20-Lead TSSOP	RU-20

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Linearity error refers to integral linearity error.

AUTOMOTIVE PRODUCTS

The AD7927W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

D03088-0-6/13(D)