DC to 204 kHz, Dynamic Signal Analysis, Precision 24-Bit ADC with Power Scaling

Data Sheet **AD7768-1**

FEATURES

- ADC for single-channel low power, platform DAQ designs
- Wide bandwidth
  - Sinc filter bandwidth range: DC to 204 kHz
  - Low ripple FIR bandwidth range: DC to 110.8 kHz
- Precision ac and dc performance
  - 108.5 dB dynamic range typical
  - −120 dB THD
  - ±1.1 ppm of FSR INL, ±30 µV offset error, ±30 ppm of FSR gain error
- Programmable ODR, filter type, and latency
  - ODR values up to 1024 kSPS
- Linear phase digital filter options
  - Low ripple FIR filter: ±0.005 dB maximum pass-band ripple, dc to 102.4 kHz
  - Low latency sinc5 filter
  - Low latency sinc3 filter enabling 50 Hz/60 Hz rejection
  - Programmable FIR filter option
- Programmable power consumption and bandwidth
  - Fast, highest speed
    - 52.224 kHz bandwidth, 26.4 mW (sinc5 filter)
    - 110.8 kHz bandwidth, 36.8 mW (FIR filter)
  - Median, half speed: 55.4 kHz bandwidth, 19.7 mW (FIR filter)
  - Low power, low speed: 13.9 kHz bandwidth, 6.75 mW (FIR filter)
- Power supply
  - AVDD1 − AVSS = 5.0 V typical
  - AVDD2 − AVSS = 2.0 V to 5.0 V typical
  - Analog supplies can run from split supply (true bipolar)
  - IOVDD − DGND = 1.8 V to 3.3 V typical
- Low power mode can run from single 3.0 V supply
- Pin control or SPI interface configurable
- Suite of diagnostic check mechanisms
  - Temperature, interface CRC, and memory map CRC
- Package: 28-lead, 4 mm × 5 mm, LFCSP
- Temperature range: −40°C to +125°C

APPLICATIONS

- Platform ADC to serve a superset of measurements and sensor types
  - Sound and vibration, acoustic, and material science research and development
  - Control and hardware in loop verification
  - Condition monitoring for predictive maintenance
  - Electrical test and measurement
  - Audio testing and current and voltage measurement
  - Clinical electroencephalogram (EEG), electromyogram (EMG), and electrocardiogram (ECG) vital signs monitoring
  - USB-, PXI-, and Ethernet-based modular DAQ
  - Channel to channel isolated modular DAQ designs

FUNCTIONAL BLOCK DIAGRAM

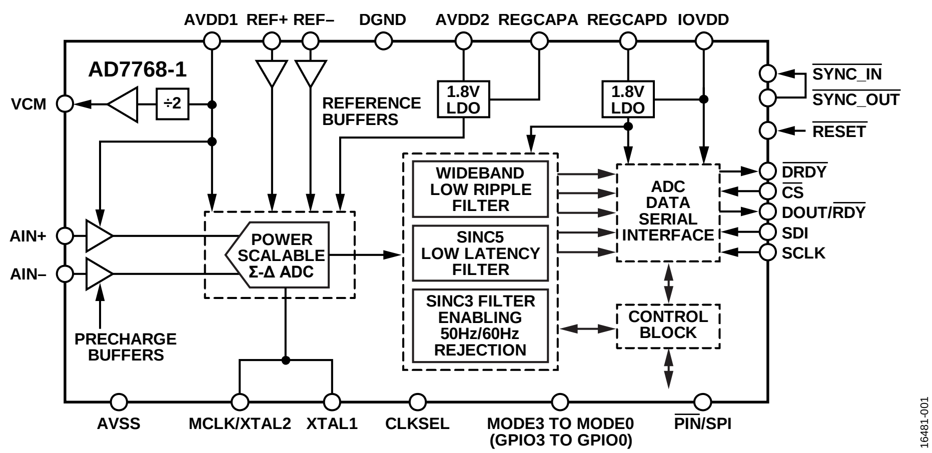

Figure 1.

Rev. A Document Feedback

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5/2018—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD7768-1 is a low power, high performance, Σ-Δ analog-to-digital converter (ADC), with a Σ-Δ modulator and digital filter for precision conversion of both ac and dc signals. The AD7768-1 is a single-channel version of the AD7768, an 8-channel, simultaneously sampling, Σ-Δ ADC. The AD7768-1 provides a single configurable and reusable data acquisition (DAQ) footprint, which establishes a new industry standard in combined ac and dc performance and enables instrumentation and industrial system designers to design across multiple measurement variants for both isolated and nonisolated applications.

The AD7768-1 achieves a 108.5 dB dynamic range when using the low ripple, finite impulse response (FIR) digital filter at 256 kSPS, giving 110.8 kHz input bandwidth, combined with ±1.1 ppm integral nonlinearity (INL), ±30 μV offset error, and ±30 ppm gain error.

A wider bandwidth, up to 500 kHz Nyquist (filter −3 dB point of 204 kHz), is available using the sinc5 filter, enabling a view of signals over an extended range.

The AD7768-1 offers the user the flexibility to configure and optimize for input bandwidth vs. output data rate (ODR) and vs. power dissipation. The flexibility of the AD7768-1 allows dynamic analysis of a changing input signal, making the device particularly useful in general-purpose DAQ systems. The selection of one of three available power modes allows the designer to achieve required noise targets while minimizing power consumption. The design of the AD7768-1 is unique in that it becomes a reusable and flexible platform for low power dc and high performance ac measurement modules.

The AD7768-1 achieves the optimum balance of dc and ac performance with excellent power efficiency. The following three operating modes allow the user to trade off the input bandwidth vs. power budgets:

- Fast mode offers both a sinc filter with up to 256 kSPS and 52.2 kHz of bandwidth, and 26.4 mW of power consumption, or a FIR filter with up to 256 kSPS, 110.8 kHz of bandwidth and 36.8 mW of power consumption.
- Median mode offers a FIR filter with up to 128 kSPS, 55.4 kHz of bandwidth and 19.7 mW of power consumption.
- Low power mode offers a FIR filter with up to 32 kSPS, 13.85 kHz of bandwidth and 6.75 mW of power consumption.

The AD7768-1 offers extensive digital filtering capabilities that meet a wide range of system requirements. The filter options allow configuration for frequency domain measurements with tight gain error over frequency, linear phase response requirements (brick wall filter), a low latency path (sinc5 or sinc3) for use in control loop applications, and measuring dc inputs with the ability to configure the sinc3 filter to reject the line frequency of either 50 Hz or 60 Hz. All filters offer programmable decimation.

A 1.024 MHz sinc5 filter path exists for users seeking an even higher ODR than is achievable using the low ripple FIR filter. This path is quantization noise limited. Therefore, it is best suited for customers requiring minimum latency for control loops or implementing custom digital filtering on an external field programmable gate array (FPGA) or digital signal processor (DSP).

The filter options include the following:

- A low ripple FIR filter with a ±0.005 dB pass-band ripple to 102.4 kHz.
- A low latency sinc5 filter with up to a 1.024 MHz data rate to maximize control loop responsiveness.
- A low latency sinc3 filter that is fully programmable, with 50 Hz/60 Hz rejection capabilities.

When using the AD7768-1, embedded analog functionality within the AD7768-1 greatly reduces the design burden over the entire application range. The precharge buffer on each analog input decreases the analog input current compared to competing products, simplifying the task of an external amplifier to drive the analog input.

A full buffer input on the reference reduces the input current, providing a high impedance input for the external reference device or in buffering any reference sense resistor scenarios used in ratiometric measurements.

The device operates with a 5.0 V AVDD1 − AVSS supply, a 2.0 V to 5.0 V AVDD2 − AVSS supply, and a 1.8 V to 3.3 V IOVDD − DGND supply.

In low power mode, the AVDD1, AVDD2, and IOVDD supplies can run from a single 3.0 V rail.

The device requires an external reference. The absolute input reference (REF_{IN}) voltage range is 1 V to AVDD1 − AVSS.

The specified operating temperature range is −40°C to +125°C. The device is housed in a 4 mm × 5 mm, 28-lead LFCSP.

Note that, throughout this data sheet, multifunction pins, such as XTAL2/MCLK, are referred to either by the entire pin name or by a single function of the pin, for example, MCLK, when only that function is relevant.

SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2.0 V to 5.5 V, IOVDD = 1.7 V to 3.6 V, DGND = 0 V, AVSS = 0 V, REF+ = 4.096 V, REF− = 0 V, MCLK = 16.384 MHz, 50:50 duty cycle, analog input precharge buffers on, reference precharge on, the filter type is a low ripple FIR filter, and $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND CODING					
ODR[1]					
	Fast sinc5	8		1024	kSPS
	Fast low ripple FIR	8		256	kSPS
	Fast sinc3	0.05		256	kSPS
	Median sinc5	4		512	kSPS
	Median low ripple FIR	4		128	kSPS
	Median sinc3	0.025		128	kSPS
	Low power sinc5	1		128	kSPS
	Low power low ripple FIR	1		32	kSPS
	Low power sinc3	0.0125		32	kSPS
Data Output Coding		24-bit twos complement data, followed by eight status bits (if enabled), followed by eight cyclic redundancy check (CRC) bits (if enabled)			
DYNAMIC PERFORMANCE					
Fast Mode	Decimation by 32, 256 kHz ODR				
Dynamic Range	Shorted inputs, sinc5 filter	110	111.5		dB
	Shorted inputs, low ripple FIR	106.5	108.5		dB
	A-weighted, 1 kHz input, −60 dBFS, decimation by 128, low ripple FIR		115		dB
Signal to Noise Ratio (SNR)	1 kHz, −0.25 dBFS, sine input				
	Sinc5 filter		110.5		dB
	Low ripple FIR	106	107.5		dB
Signal-to-Noise-and-Distortion (SINAD)	1 kHz, −0.25 dBFS, sine input	105	107.3		dB
Total Harmonic Distortion (THD)	1 kHz, −0.25 dBFS, sine input		−120	−112	dB
Spurious-Free Dynamic Range (SFDR)	1 kHz, −0.25 dBFS, sine input		125		dBc
Median Mode	Decimation by 32, 128 kHz ODR				
Dynamic Range	Shorted inputs, sinc5 filter	110	111.5		dB
	Shorted inputs, low ripple FIR	106.5	108.5		dB
SNR	1 kHz, −0.25 dBFS, sine input				
	Sinc5 filter		110.5		dB
	Low ripple FIR	106	107.5		dB
SINAD	1 kHz, −0.25 dBFS, sine input	105	107.3		dB
THD	1 kHz, −0.25 dBFS, sine input		−120	−112	dB
SFDR	1 kHz, −0.25 dBFS, sine input		125		dBc
Low Power Mode	Decimation by 32, 32 kHz ODR				
Dynamic Range	Shorted inputs, sinc5 filter	110	111.5		dB
	Shorted inputs, low ripple FIR	106.5	108.5		dB
SNR	1 kHz, −0.25 dBFS, sine input				
	Sinc filter		111		dB
	Low ripple FIR	106	107.8		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SINAD	1 kHz, −0.25 dBFS, sine input	105	107.5		dB
THD	1 kHz, −0.25 dBFS, sine input		−120	−112	dB
SFDR	1 kHz, −0.25 dBFS, sine input		125		dBc
Intermodulation Distortion (IMD)	Frequency Input A (fa) = 9.7 kHz, Frequency Input B (fb) = 10.3 kHz				
	Second order		−125		dB
	Third order		−125		dB
ACCURACY					
No Missing Codes[2]	Low ripple FIR, sinc5 decimation > 32	24			Bits
INL	Endpoint method		±1.1	±7	ppm of FSR
Offset Error	Fast mode		±30	±170	µV
	Median mode		±30	±170	µV
	Low power mode		±20	±80	µV
Offset Error Drift[2]	Fast mode		±300		nV/°C
	Median mode		±225		nV/°C
	Low power mode		±100		nV/°C
Gain Error	T_A = 25°C, reference buffer on		±30		ppm of FSR
	T_A = 25°C, reference buffer off		±30	±70	ppm of FSR
Gain Drift vs. Temperature[2]	Reference buffer off		±0.25	±0.6	ppm/°C
ANALOG INPUTS					
Differential Input Voltage	Reference voltage (V_{REF}) = REF+ − REF−	V_{REF-}		V_{REF+}	V
Absolute AINx Voltage[2]	Precharge buffers off, absolute voltage on AIN+ or AIN−	AVSS − 0.05		AVDD1 + 0.05	V
Analog Input Current	Fast mode				
Unbuffered	Differential component		±53		µA/V
	Common-mode component		±17		µA/V
Precharge Buffers On[3]			−20		µA
Input Current Drift[2]	Fast mode				
Unbuffered			±12.5		nA/V/°C
Precharge Buffer On			±3		nA/°C
EXTERNAL REFERENCE					
REF_{IN} Voltage	REF_{IN} = (REF+) − (REF−)	1		AVDD1 − AVSS	V
Absolute REFIN Voltage Limits	Reference unbuffered	AVSS − 0.05		AVDD1 + 0.05	V
	Reference precharge buffer on	AVSS		AVDD1	V
	Reference buffer on	AVSS		AVDD1	V
Average REF_{IN} Current	Reference unbuffered		±80		µA/V
	Reference precharge buffer on		±20		µA
	Reference buffer on		±300		nA
Average REF_{IN} Current Drift[2]	Reference unbuffered		±1.7		nA/V/°C
	Reference precharge buffer on		125		nA/°C
	Reference buffer on		4		nA/°C
Common-Mode Rejection	Up to 10 MHz		100		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL FILTER RESPONSE					
Low Ripple FIR Filter					
Decimation Rate	Six selectable decimation rates	32		1024	
ODR				256	kSPS
Group Delay	Latency		34/ODR		Sec
Settling Time	Complete settling		68/ODR		Sec
Pass-Band Ripple[4]				±0.005	dB
Pass Band	−0.005 dB		0.4 × ODR		Hz
	−0.1 dB pass band		0.409 × ODR		Hz
	−3 dB bandwidth		0.433 × ODR		Hz
Stop-Band Frequency	Attenuation > 105 dB		0.499 × ODR		Hz
Stop-Band Attenuation[5]			105		dB
Sinc5 Filter					
Decimation Rate	Eight selectable decimation rates	8		1024	
ODR				1024	kSPS
Group Delay	Latency		<3/ODR		Sec
Settling Time	Complete settling		<6/ODR		Sec
Pass Band	−0.1 dB bandwidth		0.0376 × ODR		Hz
	−3 dB bandwidth		0.204 × ODR		Hz
Sinc3 Filter					
Decimation Rate[4]	Decimation from decimation by 32 to decimation by 185,280 is possible in steps of 32	32		185,280	
ODR				256	kSPS
Group Delay	Latency		2/ODR		Sec
Settling Time	Complete settling to reject 50 Hz		60		ms
Pass Band	−0.1 dB bandwidth		0.0483 × ODR		Hz
	−3 dB bandwidth		0.2617 × ODR		Hz
REJECTION					
AC Power Supply Rejection Ratio (PSRR)	Input voltage (V_{IN}) = 0.1 V, dc to 16 MHz				
AVDD1	Full, median mode		100		dB
	Low power mode		85		dB
AVDD2			100		dB
IOVDD			100		dB
DC PSRR	V_{IN} = 0.1 V				
AVDD1			105		dB
AVDD2			118		dB
IOVDD			95		dB
Analog Input Common-Mode Rejection Ratio (CMRR)					
DC	V_{IN} = 0.1 V	90			dB
AC	Up to 10 kHz, see Figure 55		95		dB
Normal Mode Rejection	50 Hz ± 1 Hz, sinc3 filter, 60 Hz rejection on		80		dB
	60 Hz ±1 Hz, sinc3 filter, 60 Hz rejection on		65		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK					
MCLK					
External Clock		0.6	16.384	17	MHz
Internal Clock			16.384		MHz
Duty Cycle[2]	16.384 MHz MCLK	25:75	50:50	75:25	%
Crystal					
Frequency		8	16	17	MHz
Start-Up Time	Clock output valid		2		ms
ADC RESET					
ADC Start-Up Time After Reset	Reset rising edge to first $\overline{\text{DRDY}}$, $\overline{\text{PIN}}$ mode, decimate by 8		100		µs
Reset Low Pulse Width		0.0001		100	ms
LOGIC INPUTS					
Input Voltage					
High, V_{INH}	1.7 V ≤ IOVDD ≤ 1.9 V	0.65 × IOVDD			V
	2.2 V ≤ IOVDD ≤ 3.6 V	0.65 × IOVDD			V
Low, V_{INL}	1.7 V ≤ IOVDD ≤ 1.9 V			0.35 × IOVDD	V
	2.2 V ≤ IOVDD ≤ 3.6 V			0.7	V
Hysteresis[2]	2.2 V ≤ IOVDD ≤ 3.6 V	0.08		0.25	V
	1.7 V ≤ IOVDD ≤ 1.9 V	0.04		0.2	V
Leakage Current	Excluding $\overline{\text{RESET}}$ pin	−10	+0.05	+10	µA
	$\overline{\text{RESET}}$ pin pull-up resistor		1		kΩ
LOGIC OUTPUTS					
Output Voltage[2]					
High, V_{OH}	2.2 V ≤ IOVDD < 3.6 V, source current (I_{SOURCE}) = 500 µA, LV_BOOST off	0.8 × IOVDD			V
	1.7 V ≤ IOVDD ≤ 1.9 V, I_{SOURCE} = 200 µA, LV_BOOST on	0.8 × IOVDD			V
Low, V_{OL}	2.2 V ≤ IOVDD < 3.6 V, sink current (I_{SINK}) = 1 mA, LV_BOOST off			0.4	V
	1.7 V ≤ IOVDD ≤ 1.9 V, I_{SINK} = 400 µA, LV_BOOST on			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
VCM OUTPUT	Default setting		AVDD1 − AVSS/2		V
VCM Noise[4]	VCM = (AVDD1 − AVSS)/2, from simulation, 1 kHz bandwidth limited		10		µV rms
	VCM = 2.5 V, from simulation, 1 kHz bandwidth limited		65		µV rms
Short-Circuit Current[6]			10		mA
Load Regulation			1		mV/mA
POWER REQUIREMENTS	Power supply voltages				
AVDD1 − AVSS	All power modes	4.5	5.0	5.5	V
AVDD1 − AVSS	Low power mode only	3		5.5	V
AVDD2 − AVSS		2	2.0 to 5.0	5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND		1.7	1.8 to 3.3	3.6	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
Fast Mode					
AVDD1 Current	All buffers off, V_{CM} off		2.2	2.65	mA
	Analog input precharge on (defaults on in $\overline{PIN}$ mode)		4.1	5.1	mA
	Precharge reference buffer (per precharge buffer, defaults on in $\overline{PIN}$ mode)		1.2	1.5	mA
	Full reference buffer (per buffer)		3.2	4.15	mA
	VCM output on		0.21		mA
AVDD2 Current			4.7	5.65	mA
IOVDD Current	Sinc5 filter||low ripple FIR filter		3.35||9.2	4.4||11.5	mA
Median Mode					
AVDD1 Current	All buffers off		1.2	1.35	mA
	Analog input precharge on ($\overline{PIN}$ mode default)		2.45	2.6	mA
	Precharge reference buffer (per precharge buffer)		0.65	0.77	mA
	Full reference buffer (per buffer)		1.6	2.1	mA
AVDD2 Current			2.7	3.2	mA
IOVDD Current	Sinc5 filter||low ripple FIR filter		1.97||5	2.8||6.4	mA
Low Power Mode					
AVDD1 Current	All buffers off		0.3	0.35	mA
	Analog input precharge on ($\overline{PIN}$ mode default)		0.6	0.71	mA
	Precharge reference buffer (per precharge buffer)		0.16	0.22	mA
	Full reference buffer (per buffer)		0.4	0.56	mA
AVDD2 Current			1.15	1.37	mA
IOVDD Current	Sinc5 filter||low ripple FIR filter, 16.384 MHz MCLK, MCLK_DIV = 16		0.95||1.7	1.6||2.45	mA
Power Saving States					
Standby Mode	Serial peripheral interface (SPI) active, MCLK active, VCM off		400		µA
	SPI active, MCLK inactive, VCM off		50		µA
Power-Down Mode	Full power-down; SPI control mode only		5		µA
POWER DISSIPATION	AVDD1 = 5 V, MCLK = 16.384 MHz, external complementary metal oxide semiconductor (CMOS) MCLK				
Sinc5 Filter	AVDD2 = 2 V, IOVDD = 1.8 V				
Fast Mode	All buffers off		26.4	32.5	mW
	Analog input (A_{IN}) precharge only		35.6	44.75	mW
Median Mode	All buffers off		14.4	18.2	mW
	AIN precharge only		19.1	24.45	mW
Low Power Mode	All buffers off		5.4	7.4	mW
	AIN precharge only		6.8	9.2	mW
Low Ripple FIR Filter	AVDD2 = 2 V, IOVDD = 1.8 V				
Fast Mode	All buffers off		36.8	45.25	mW
	AIN precharge only		46.1	57.5	mW
Median Mode	All buffers off		19.7	24.7	mW
	AIN precharge only		24.4	30.95	mW
Low Power Mode	All buffers off		6.75	8.9	mW
	AIN precharge only		8.1	10.7	mW

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Standby Mode	SPI active, MCLK active, VCM off		780		µW
	SPI active, MCLK inactive, VCM off		125		µW
Power-Down Mode	Full power down, SPI control mode only		14		µW

[1] The ODR ranges refer to the programmable decimation rates available on the AD7768-1 for a fixed MCLK rate of 16.384 MHz. Varying the MCLK rate allows the user a wider variation of ODR.
[2] This specification is not production tested, but is supported by characterization data at initial product release.
[3] The typical value (−20 µA) is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common mode approaches the midpoint of the power supply rails: (AVDD1 − AVSS)/2. The analog input current scales with the MCLK frequency and the power mode (fast, median, and low power).
[4] This specification is not production tested. It is supported by a combination of design simulation and test coverage on a limited number of units.
[5] Alias rejection around frequencies related to the chop frequency may result in compound attenuation, which exceeds 105 dB. See the Antialiasing Filtering section describing front-end antialias protection for further detail.
[6] VCM can typically source 10 mA, but it is recommended to source no more than 6 mA in normal operation.

3 V OPERATION

For low power mode only. AVDD1, AVDD2, and IOVDD = 3 V, DGND = 0 V, AVSS = 0 V, REF+ = 2.5V, and REF− = 0 V, MCLK = 16.384 MHz, analog input precharge buffers on, reference precharge on, the filter type is a low ripple FIR filter, chop frequency (f_{CHOP}) = modulator frequency (f_{MOD})/32, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
ODR[1]	Low power mode				
	Low ripple FIR filter and sinc5 filter	1		32	kSPS
	Sinc3	0.0125		32	kSPS
No Missing Codes[2]	Low ripple FIR, sinc5 decimation > 32	24			Bits
DYNAMIC PERFORMANCE					
Low Power Mode	Decimation by 32, 32 kHz ODR				
Dynamic Range	Shorted inputs, sinc5 filter		106.9		dB
	Shorted inputs, low ripple FIR	100.9	104		dB
SNR	1 kHz, −0.25 dBFS, sine input				
	Low ripple FIR		102.5		dB
SINAD			102.3		dB
THD			−125	−112	dB
SFDR	1 kHz, −0.25 dBFS, sine input		120		dBc
ACCURACY					
INL	Endpoint method		±3		ppm of FSR
Offset Error	Low power mode		±40	±175	µV
Offset Error Drift[2]	Low power mode		±100		nV/°C
Gain Error	T_A = 25°C		±30		ppm/FSR
ANALOG INPUTS					
Differential Input Voltage	V_{REF} = REF+ − REF−	V_{REF-}		V_{REF+}	V
Absolute AINx Voltage	Analog input precharge buffers off, absolute voltage on AIN+ or AIN−	AVSS − 0.05		AVDD1 + 0.05	V
Analog Input Current					
Input Current Unbuffered	Differential component		±53		µA/V
	Common-mode component		±17		µA/V
Input Current[3]	Precharge buffers on, external CMOS MCLK		−20		µA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
EXTERNAL REFERENCE					
REF_{IN} Voltage	REF_{IN} = (REF+) − (REF−)	1		AVDD1 − AVSS	V
Absolute REF_{IN} Voltage Limits	Reference buffer off	AVSS − 0.05		AVDD1 + 0.05	V
	Reference buffer on	AVSS		AVDD1	V
Average REF_{IN} Current	Reference buffer off		±80		µA/V
	Reference buffer on		±20		nA
			±300		nA/V/°C
Common-Mode Rejection Ratio (CMRR)	Up to 10 MHz		100		dB

[1] The ODR ranges refer to the programmable decimation rates available on the AD7768-1 for a fixed MCLK rate of 16.384 MHz. Varying the MCLK rate allows the user a wider variation of ODR.
[2] This specification is not production tested, but is supported by characterization data at initial product release.
[3] The typical value (−20 µA) is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common mode approaches the midpoint of the power supply rails: (AVDD1 − AVSS)/2. Analog input current scales with the MCLK frequency and the power mode (fast, median, and low power).

TIMING SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2.0 V to 5.5 V, IOVDD = 2.2 V to 3.6 V, AVSS = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, and load capacitance (C_{LOAD}) = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) disabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of IOVDD and timed from a voltage level of IOVDD/2). See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested, but are supported by characterization data at initial product release.

Table 3.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	Fast mode		MCLK/2		Hz
		Median mode		MCLK/4		Hz
		Low power mode		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{DRDY}$ edge to next rising $\overline{DRDY}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz
$t_{\overline{DRDY}\_HIGH}$	$\overline{DRDY}$ high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
$t_{MCLK\_\overline{DRDY}}$	MCLK to $\overline{DRDY}$	Rising MCLK edge to $\overline{DRDY}$ rising edge	10	13	18	ns
$t_{MCLK\_\overline{RDY}}$	MCLK to $\overline{RDY}$ indicator on the DOUT/$\overline{RDY}$ pin	Rising MCLK edge to $\overline{RDY}$ falling edge	10	13	18	ns
t_{UPDATE}	ADC data update	Time prior to $\overline{DRDY}$ rising edge where the ADC conversion register updates, single conversion read		1 × t_{MCLK}		ns
$t_{\overline{START}}$	$\overline{START}$ pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_\overline{SYNC\_OUT}}$	MCLK to $\overline{SYNC\_OUT}$	Falling MCLK to falling $\overline{SYNC\_OUT}$			t_{MCLK} + 16	ns
t_{SCLK}	SCLK period		50			ns
t_1	$\overline{CS}$ falling to SCLK falling		0			ns
t_2	$\overline{CS}$ falling to data output enable				6	ns

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_3	SCLK falling edge to data output valid			10	15	ns
t_4	Data output hold time after SCLK falling edge		4			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	$\overline{\text{CS}}$ high time	4-wire interface	10			ns
t_8	SCLK high time		20			ns
t_9	SCLK low time		20			ns
t_{10}	SCLK rising edge to $\overline{\text{DRDY}}$ high	Single conversion read only; time from last SCLK rising edge to $\overline{\text{DRDY}}$ high	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to $\overline{\text{CS}}$ rising edge		6			ns
t_{12}	$\overline{\text{CS}}$ rising edge to DOUT/$\overline{\text{RDY}}$ output disable		4		7	ns
t_{13}	DOUT/$\overline{\text{RDY}}$ indicator pulse width	In continuous read mode with $\overline{\text{RDY}}$ on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	$\overline{\text{CS}}$ falling edge to SCLK rising edge		2			ns
t_{15}	$\overline{\text{SYNC\_IN}}$ setup time before MCLK rising edge		2			ns
t_{16}	$\overline{\text{SYNC\_IN}}$ pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to $\overline{\text{RDY}}$ indicator rising edge	In continuous read mode with $\overline{\text{RDY}}$ enabled on DOUT	1			ns
t_{18}	$\overline{\text{DRDY}}$ rising edge to SCLK falling edge	In continuous read mode with $\overline{\text{RDY}}$ enabled on DOUT	8			ns

1.8 V TIMING SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 1.7 V to 1.9 V, AVSS = DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, and C_{LOAD} = 20 pF, LV_BOOST bit (Bit 7, INTERFACE_FORMAT register, Register 0x14) enabled, unless otherwise noted.

These specifications were sample tested during the initial release to ensure compliance. All input signals are specified with t_R = t_F = 5 ns (10% to 90% of IOV_{DD} and timed from a voltage level of IOVDD/2. See Figure 2 to Figure 8 for the timing diagrams.

These specifications are not production tested but are supported by characterization data at initial product release.

Table 4.

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Frequency			16.384	17	MHz
t_{MCLK_HIGH}	MCLK high time		16			ns
t_{MCLK_LOW}	MCLK low time		16			ns
f_{MOD}	Modulator frequency	Fast mode		MCLK/2		Hz
		Median mode		MCLK/4		Hz
		Low power mode		MCLK/16		Hz
$t_{\overline{DRDY}}$	Conversion period	Rising $\overline{\text{DRDY}}$ edge to next rising $\overline{\text{DRDY}}$ edge, continuous conversion mode		f_{MOD}/DEC_RATE		Hz

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{DRDY_HIGH}	DRDY high time	t_{MCLK} = 1/MCLK	t_{MCLK} − 5	1 × t_{MCLK}		ns
t_{MCLK_DRDY}	MCLK to DRDY	Rising MCLK edge to DRDY rising edge	13	19	25	ns
t_{MCLK_RDY}	MCLK to RDY indicator on the DOUT/RDY pin	Rising MCLK edge to RDY falling edge	13	19	25	ns
t_{UPDATE}	ADC data update	Time prior to DRDY rising edge where the ADC conversion register updates		1 × t_{MCLK}		ns
t_{START}	START pulse width		1.5 × t_{MCLK}			ns
$t_{MCLK\_SYNC\_OUT}$	MCLK to SYNC_OUT	Falling MCLK to falling SYNC_OUT, see the Synchronization of Multiple AD7768-1 Devices section			t_{MCLK} + 31	ns
t_{SCLK}	SCLK period		50			ns
t_1	CS falling to SCLK falling		0			ns
t_2	CS falling to data output enable				11	ns
t_3	SCLK falling edge to data output valid			14	19	ns
t_4	Data output hold time after SCLK falling edge		7			ns
t_5	SDI setup time before SCLK rising edge		3			ns
t_6	SDI hold time after SCLK rising edge		8			ns
t_7	CS high time	4-wire interface	10			ns
t_8	SCLK high time		23			ns
t_9	SCLK low time		23			ns
t_{10}	SCLK rising edge to DRDY high	Time from last SCLK rising edge to DRDY high; if this is exceeded, conversion N + 1 is missed; single conversion read	1 × t_{MCLK}			ns
t_{11}	SCLK rising edge to CS rising edge		6			ns
t_{12}	CS rising edge to DOUT/RDY output disable		7.5		13	ns
t_{13}	DOUT/RDY indicator pulse width	In continuous read mode with RDY on, DOUT enabled, with SCLK idling high		1 × t_{MCLK}		ns
t_{14}	CS falling edge to SCLK rising edge		2.5			ns
t_{15}	SYNC_IN setup time before MCLK rising edge		2			ns
t_{16}	SYNC_IN pulse width		1.5 × t_{MCLK}			ns
t_{17}	SCLK rising edge to RDY indicator rising edge	In continuous read mode with RDY on, DOUT enabled	5.5			ns
t_{18}	DRDY rising edge to SCLK falling edge	In continuous read mode with RDY on, DOUT enabled	15			ns

Timing Diagrams

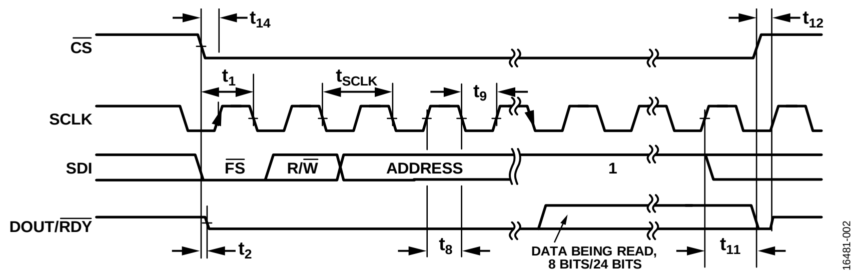

Figure 2. SPI Read Timing Diagram

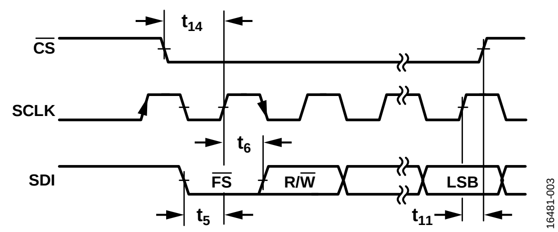

Figure 3. SPI Write Timing Diagram

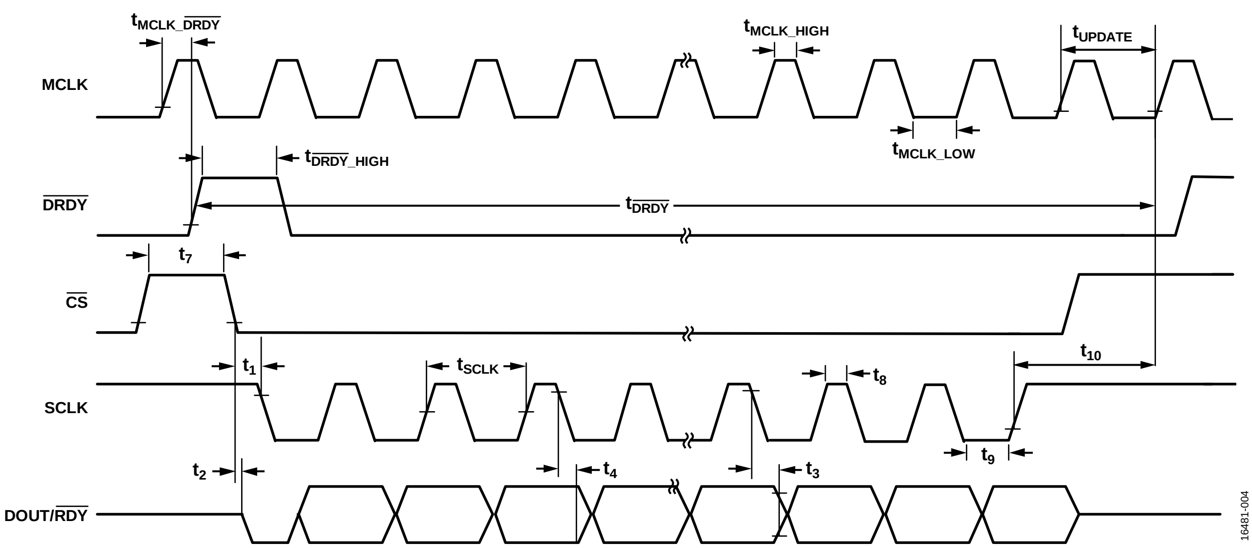

Figure 4. Reading Conversion Result in Continuous Conversion Mode (CS Toggling)

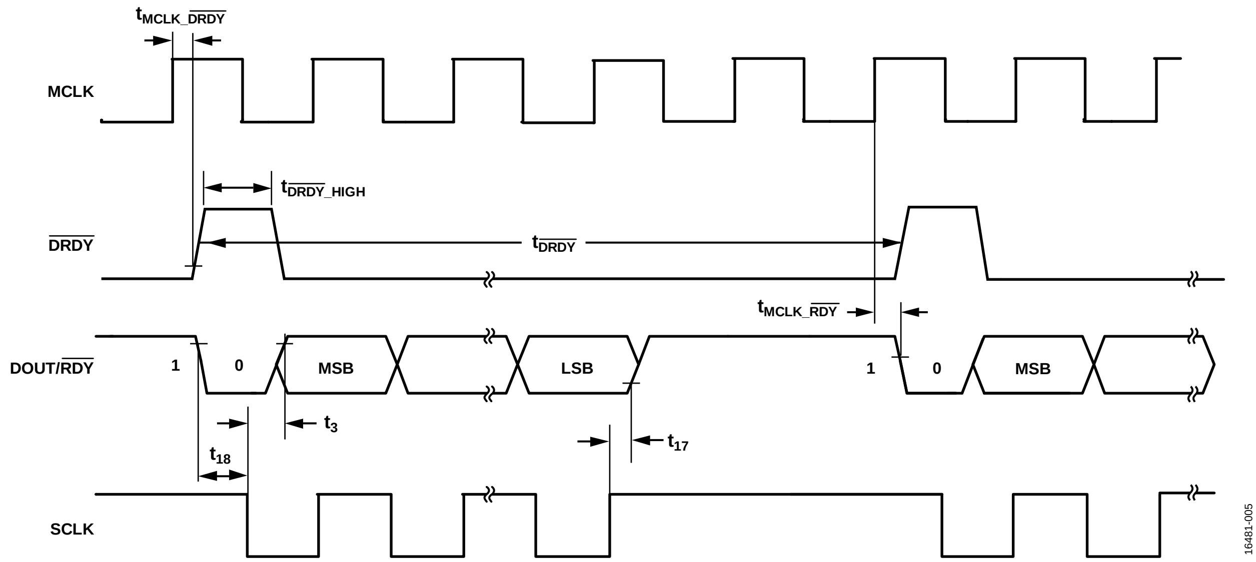

Figure 5. Reading Conversion Result in Continuous Conversion Mode, Continuous Read Mode with RDY Enabled (CS Held Low)

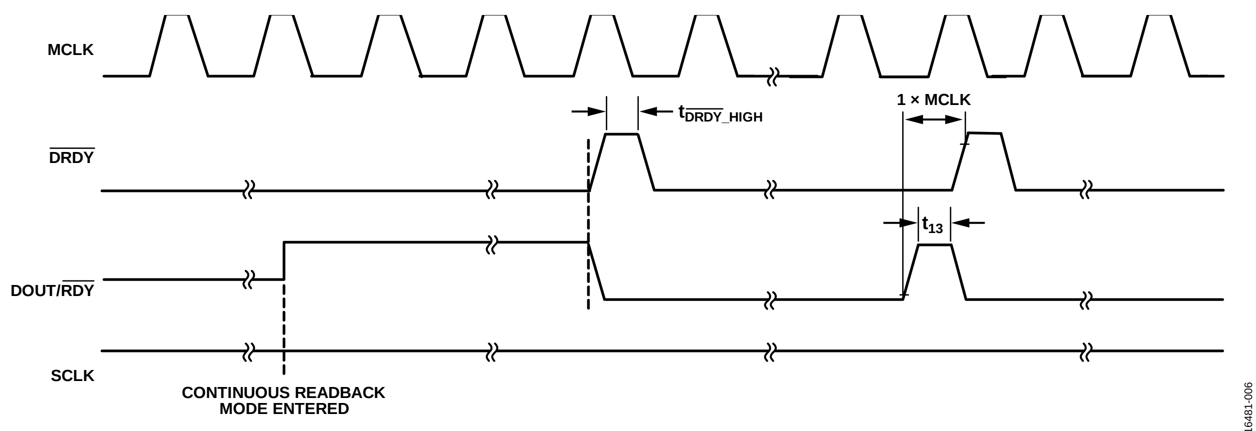

Figure 6. DOUT/RDY Behavior Without SCLK Applied

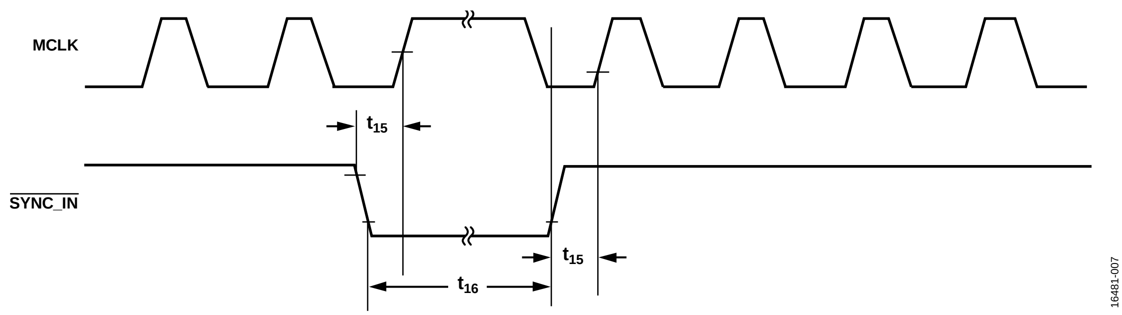

Figure 7. Synchronous SYNC_IN Pulse

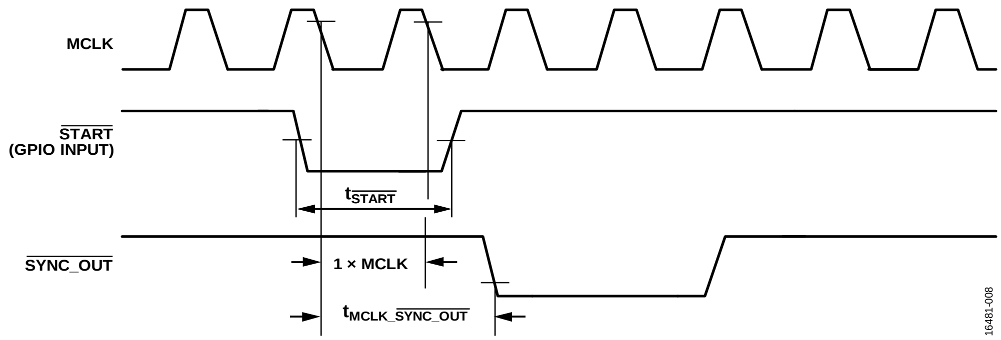

Figure 8. Asynchronous START and SYNC_OUT

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD1, AVDD2 to AVSS[1]	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD, REGCAPD to DGND (IOVDD Tied to REGCAPD for 1.8 V Operation)	−0.3 V to +2.25 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
XTAL1 to DGND	−0.3 V to +2.1 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Junction Temperature	150°C
Maximum Package Classification Temperature	260°C

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 6. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-28-12	35	0.8[3]	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.
[2] Based on a 1S0P test PCB with cold plate attached to the package top surface.
[3] Measured to exposed pad.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

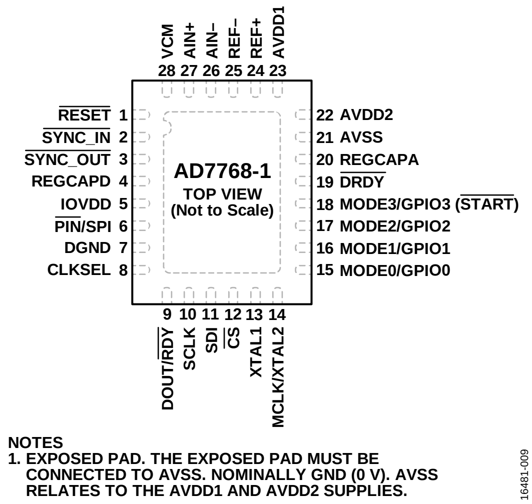

Figure 9. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	RESET	DI	Hardware Asynchronous Reset Input. After the device is powered up, it is recommended to reset the device using either the RESET pin or via a software reset. See the Reset section for further details.
2	SYNC_IN	DI	Synchronization Input. SYNC_IN receives the synchronous signal from SYNC_OUT or from the main controller. SYNC_IN enables synchronization of multiple AD7768-1 devices that require simultaneous sampling. A SYNC_IN pulse is always required when the device configuration changes in any way (for example, if the filter decimation rate changes). Apply SYNC_IN pulses directly after a DRDY pulse occurs.
3	SYNC_OUT	DO	Synchronization Output. SYNC_OUT is a digital output that is synchronous to the MCLK. To initiate this output, write a sync command over the SPI or provide a START signal via the GPIO3 pin. SYNC_OUT can then be connected to the SYNC_IN pin of its own AD7768-1 via an external trace and can then be routed to other AD7768-1 devices locally, ensuring synchronization of devices that share a common MCLK.
4	REGCAPD	AO	Digital Low Dropout (LDO) Regulator Output. Decouple this pin to DGND with a 1 µF capacitor. For IOVDD ≤ 1.8 V, use a 10 µF capacitor. Do not use the voltage output from REGCAPD in circuits external to the AD7768-1.
5	IOVDD	P	Digital Supply. The IOVDD pin sets the logic levels for all interface pins. This pin powers the digital processing via the internal digital LDO. Supply the IOVDD pin with 1.8 V to 3.3 V with respect to DGND.
6	PIN/SPI	DI	PIN Control/SPI Control. This pin sets the configuration mode of the AD7768-1 to be either pin controlled or controlled via the SPI. Logic 0: control and configuration is pin driven only. Logic 1: control and configuration is over the SPI only.
7	DGND	P	Digital Ground.
8	CLKSEL	DI	Clock Selection Pin for the AD7768-1 in PIN Control Mode. When the AD7768-1 is in PIN control mode, the logic level on CLKSEL determines which external clock source the AD7768-1 expects. The low voltage differential signaling (LVDS) clock option is only available in SPI control mode (PIN/SPI = 1). Hold the CLKSEL pin at Logic 0 or tie this pin to DGND in SPI control mode (PIN/SPI = 1). 0 = CMOS clock option. If the CMOS clock is selected, apply the clock signal to the MCLK/XTAL2 pin and connect the XTAL1 pin to DGND. 1 = crystal option. If the crystal option is selected, connect a suitable crystal across the XTAL1 and MCLK/XTAL2 pins.
9	DOUT/RDY	DO	Serial Interface Data Output and Data Ready Signal Combined. This output data pin can be configured as either a DOUT pin only, or through the SPI control mode. The pin function can also include the ready signal (RDY). The ability to program the device to provide a combined DOUT/RDY signal can reduce the number of interface lines in isolated applications.

Pin No.	Mnemonic	Type[1]	Description
10	SCLK	DI	Serial Interface Clock.
11	SDI	DI	Serial Interface Data Input.
12	$\overline{\text{CS}}$	DI	Serial Interface Chip Select Input. This pin is active low.
13	XTAL1	DI	Input 1 for Crystal or Connection to an LVDS Clock. When CLKSEL is 0, connect this pin to DGND. See the CLKSEL pin for details on the clock input configuration.
14	MCLK/XTAL2	DI	Master Clock Signal (MCLK)/External Crystal (XTAL2). XTAL2 connects to the external crystal. The AD7768-1 provides the crystal excitation. LVDS clock: second LVDS input connected to this pin. CMOS clock: operates as MCLK input. CMOS input with logic level of IOVDD/DGND.
15	MODE0/GPIO0	DI/O	Pin Control Mode ($\overline{\text{PIN}}$/SPI = 0): MODE0 pin. The MODE0 to MODE3 pins are the mode select pins for the AD7768-1. SPI Control Mode ($\overline{\text{PIN}}$/SPI = 1): GPIO0 pin. This pin operates as a general-purpose input/output pin, providing bidirectional input and output, read and write, relative to the IOVDD and DGND supply domain, which are accessed via the SPI and register map.
16	MODE1/GPIO1	DI/O	Pin Control Mode ($\overline{\text{PIN}}$/SPI = 0): MODE1 pin. The MODE0 to MODE3 pins are the mode select pins for the AD7768-1. SPI Control Mode ($\overline{\text{PIN}}$/SPI = 1): GPIO1 pin. This pin operates as a general-purpose input/output pin, providing bidirectional input and output, read and write, relative to the IOVDD and DGND supply domain, which are accessed via the SPI and register map.
17	MODE2/GPIO2	DI/O	Pin Control Mode ($\overline{\text{PIN}}$/SPI = 0): MODE2 pin. The MODE0 to MODE3 pins are the mode select pins for the AD7768-1. SPI Control Mode ($\overline{\text{PIN}}$/SPI = 1): GPIO2 pin. This pin operates as a general-purpose input/output pin, providing bidirectional input and output, read and write, relative to the IOVDD and DGND supply domain, which are accessed via the SPI and register map.
18	MODE3/GPIO3 ($\overline{\text{START}}$)	DI/O	Pin Control Mode ($\overline{\text{PIN}}$/SPI = 0): MODE3 pin. The MODE0 to MODE3 pins are the mode select pins for the AD7768-1. SPI Control Mode ($\overline{\text{PIN}}$/SPI = 1): GPIO3 pin. This pin operates as a general-purpose input/output pin, providing bidirectional input and output, read and write, relative to the IOVDD and DGND supply domain, which are accessed via the SPI and register map. Under SPI control, GPIO3 can be assigned specifically as the $\overline{\text{START}}$ input. This feature has an enable bit in the memory map (Register 0x1D, Bit 3, EN_GPIO_$\overline{\text{START}}$). Apply $\overline{\text{START}}$ pulses directly after a $\overline{\text{DRDY}}$ pulse occurs.
19	$\overline{\text{DRDY}}$	DO	Data Ready. Periodic signal output to signify conversion results are available.
20	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor. Do not use the REGCAPA pin in circuits external to the AD7768-1.
21	AVSS	P	Negative Analog Supply. Nominally ground (0 V). The AVSS pin relates to the AVDD1 and AVDD2 supplies.
22	AVDD2	P	Analog Supply Voltage, 2.0 V to 5.0 V with Respect to AVSS.
23	AVDD1	P	Analog Supply Voltage, 5.0 V ± 10% with Respect to AVSS. This supply can run at 3 V in low power mode only.
24	REF+	AI	Reference Input Positive Reference. Apply an external reference between REF+ and REF− ranging from AVDD1 to AVSS + 1 V. The device functions with a reference voltage differential in the range from 1 V to |AVDD1 − AVSS|.
25	REF−	AI	Reference Input Negative Terminal. The REF− range is from AVSS to AVDD1 − 1 V.
26	AIN−	AI	Negative Analog Input to the ADC.
27	AIN+	AI	Positive Analog Input to the ADC.
28	VCM	AO	Common-Mode Voltage Output. VCM is set to (AVDD1 − AVSS)/2 by default. Configure VCM with multiple output voltage options via an SPI write. When driving capacitive loads larger than 0.1 µF, place a 50 Ω series resistor between VCM and the capacitive load for stability purposes.
	EPAD (AVSS)	P	Exposed Pad. The exposed pad must be connected to AVSS. Nominally GND (0 V). AVSS relates to the AVDD1 and AVDD2 supplies.

[1] DI is digital input, DO is digital output, AO is analog output, P is power, DI/O is digital input or output, and AI is analog input.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, T_A = 25°C, low ripple FIR filter, decimation = ×32, MCLK= 16.384 MHz, analog input precharge buffers on, and reference precharge buffers on, unless otherwise noted.

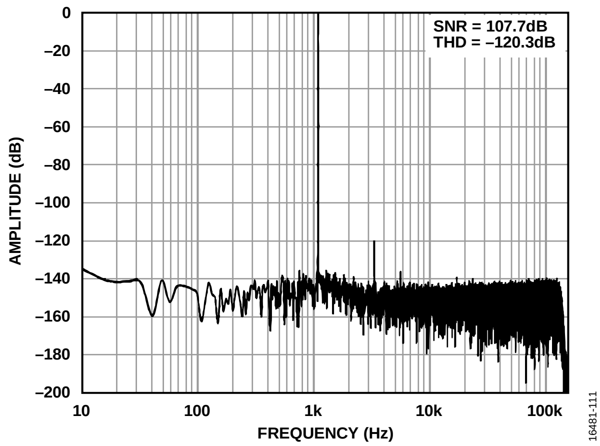

Figure 10. FFT, Fast Mode, Low Ripple FIR Filter, –0.25 dBFS

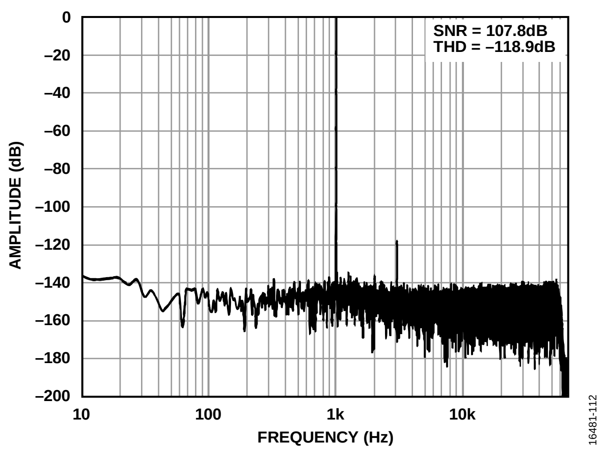

Figure 11. FFT, Median Mode, Low Ripple FIR Filter, –0.25 dBFS

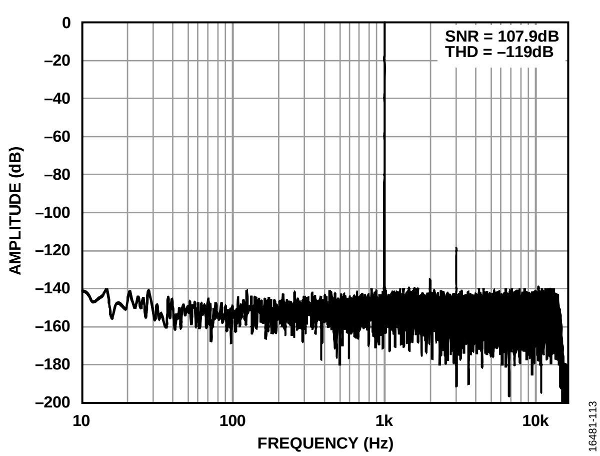

Figure 12. FFT, Low Power Mode, Low Ripple FIR Filter, –0.25 dBFS

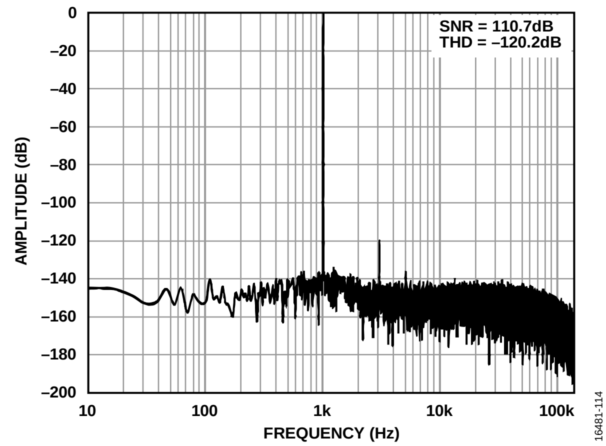

Figure 13. FFT, Fast Mode, Sinc5 Filter, –0.25 dBFS

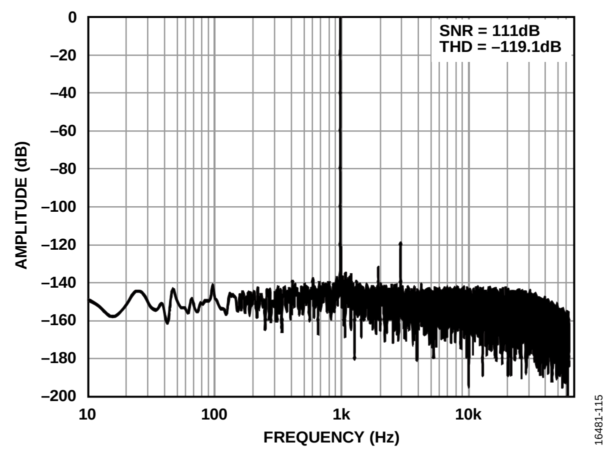

Figure 14. FFT, Median Mode, Sinc5 Filter, –0.25 dBFS

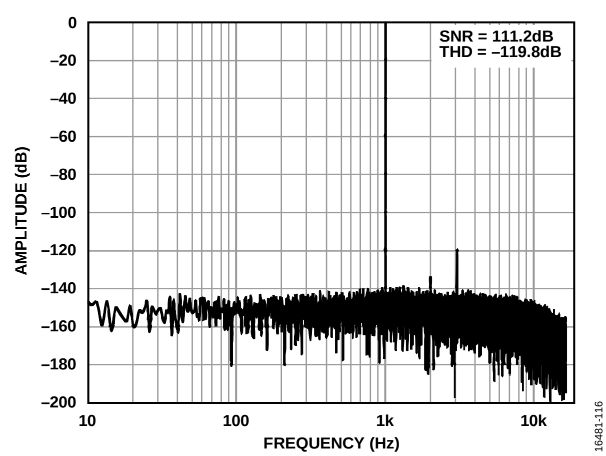

Figure 15. FFT, Low Power Mode, Sinc5 Filter, –0.25 dBFS

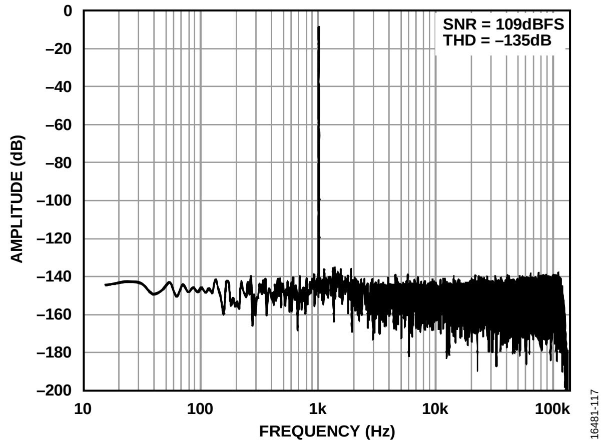

Figure 16. FFT, Fast Mode, Low Ripple FIR Filter, –10 dBFS

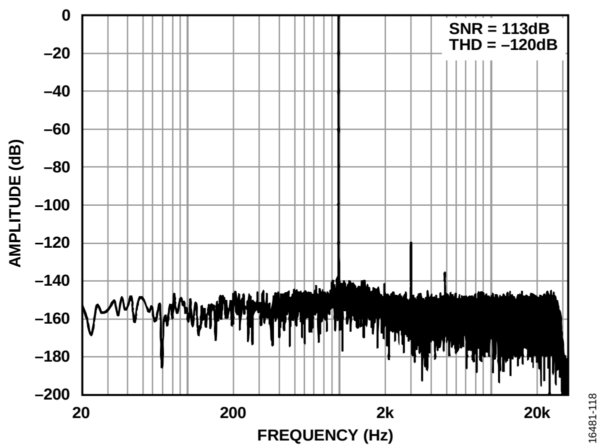

Figure 17. FFT, Fast Mode, Low Ripple FIR Filter, Decimate by 128, –0.1 dBFS

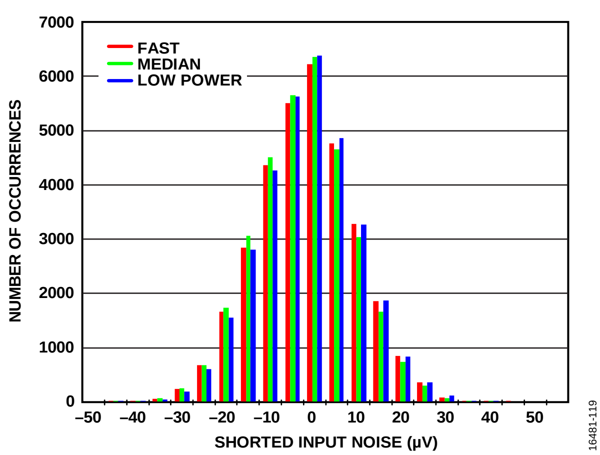

Figure 18. Shorted Input Noise, Low Ripple FIR Filter, Three Power Modes, N = 32,768

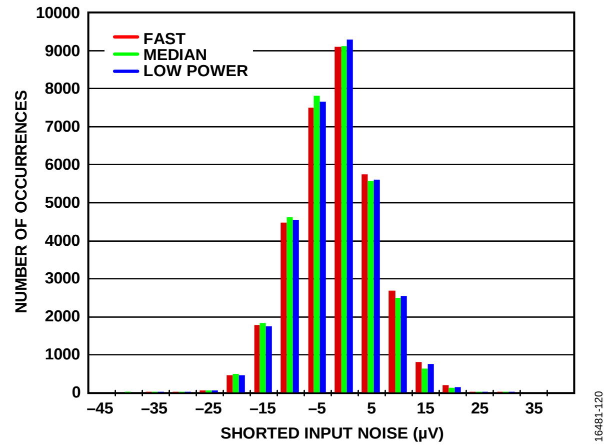

Figure 19. Shorted Input Noise, Sinc5 Filter, Three Power Modes, N = 32,768

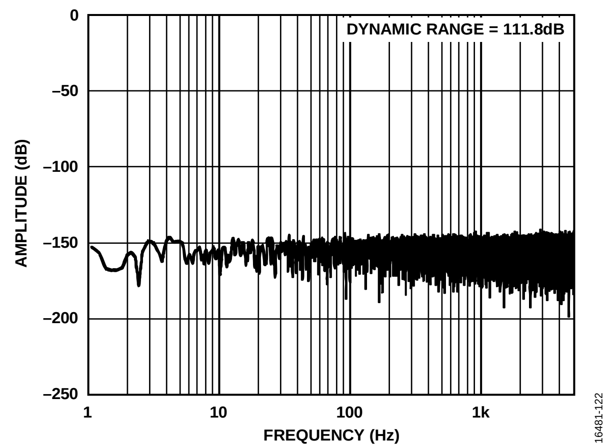

Figure 20. FFT, One Shot Mode, Sinc5 Filter, Median Power Mode, 10 kSPS ODR, Shorted Inputs

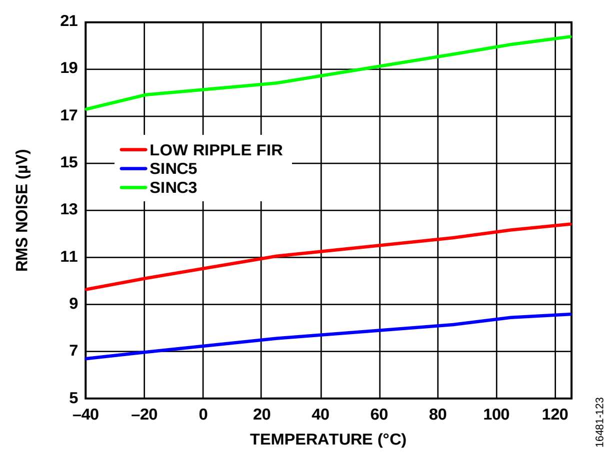

Figure 21. RMS Noise vs. Temperature, Three Filter Types, Fast Mode

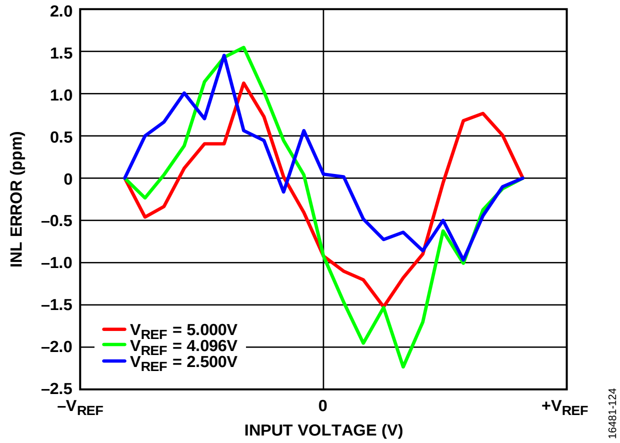

Figure 22. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Fast Mode

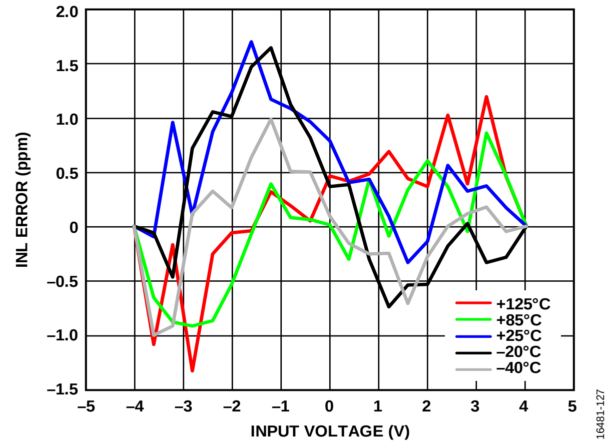

Figure 25. INL Error vs. Input Voltage for Various Temperatures, Fast Mode

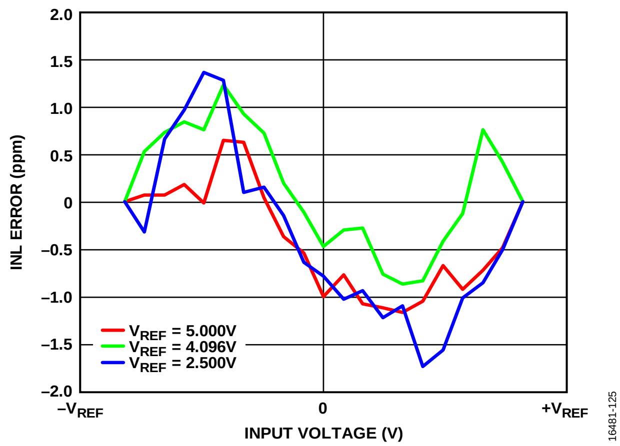

Figure 23. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Median Mode

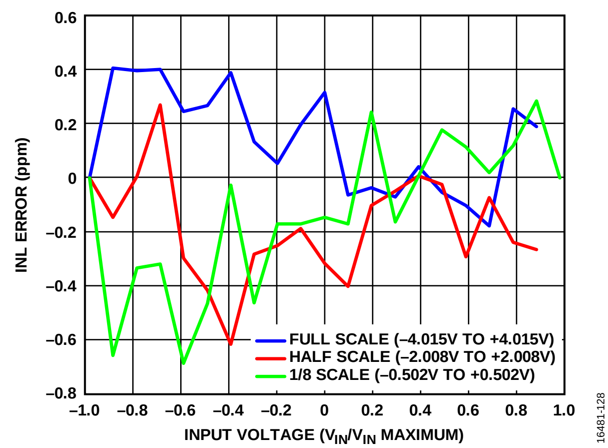

Figure 26. INL Error vs. Input Voltage, Full-Scale, Half Scale, and 1/8 Scale Inputs, 4.096 V Reference

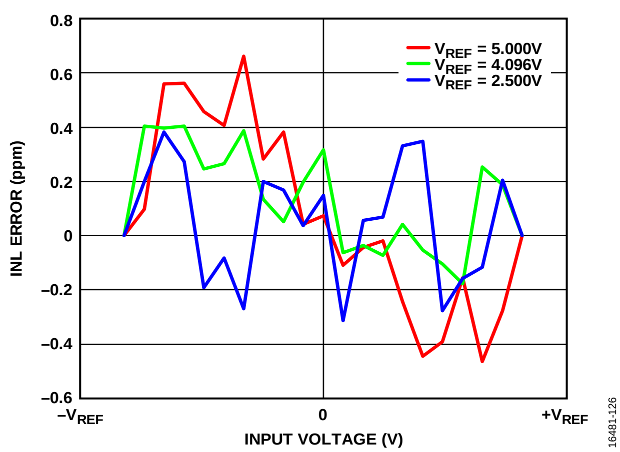

Figure 24. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Low Power Mode

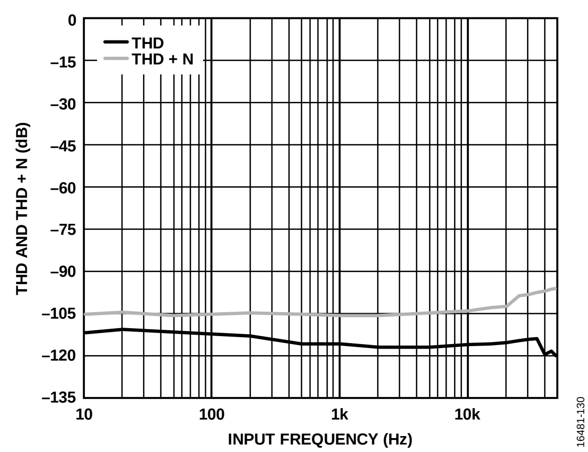

Figure 27. THD and THD + N vs. Input Frequency, Fast Mode, Low Ripple FIR Filter

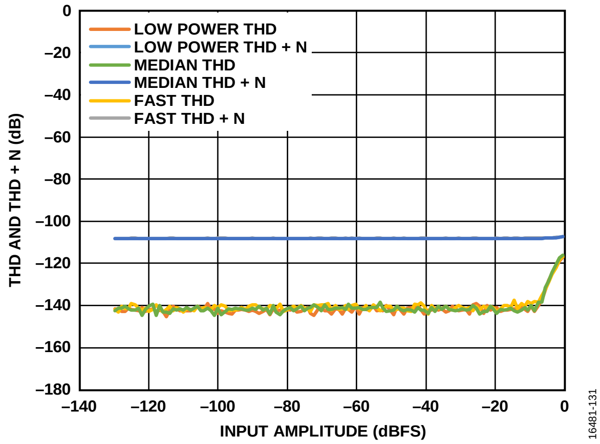

Figure 28. THD and THD + N vs. Input Amplitude, Low Ripple FIR Filter

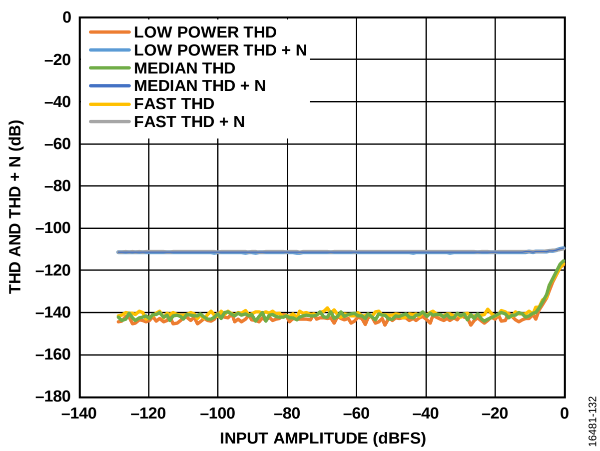

Figure 29 THD and THD + N vs. Input Amplitude, Sinc5 Filter

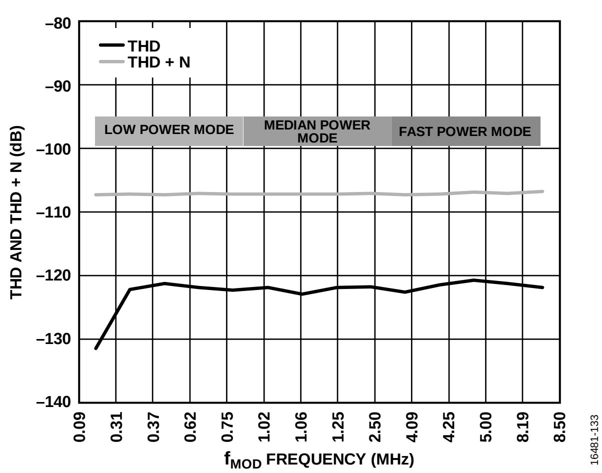

Figure 30. THD and THD + N vs. f_{MOD} Frequency, Low Ripple FIR Filter

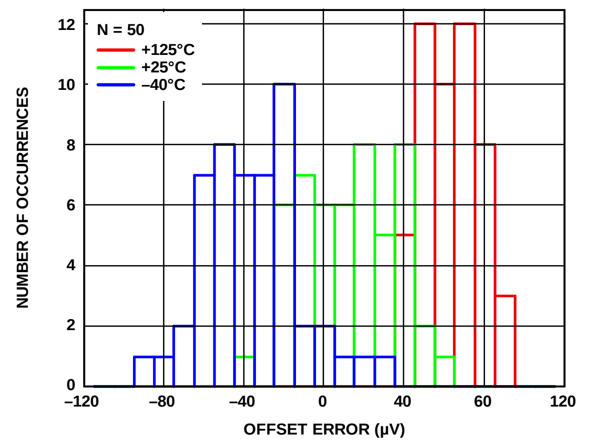

Figure 31. Offset Error Distribution, Fast Mode

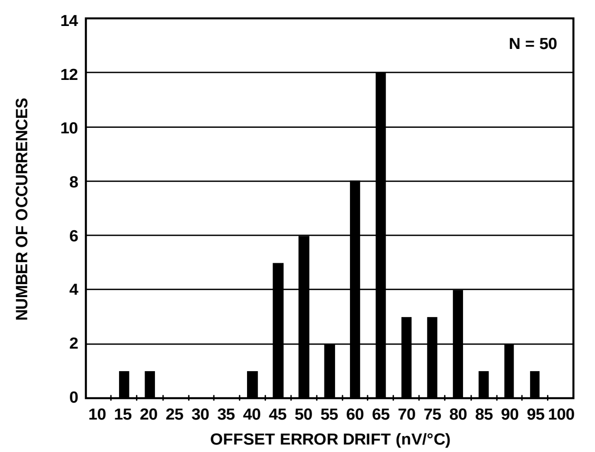

Figure 32. Offset Error Drift, Fast Mode

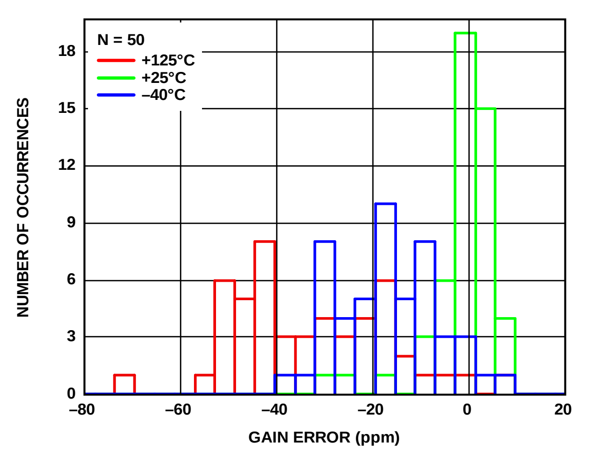

Figure 33. Gain Error Distribution, Reference Buffers Off

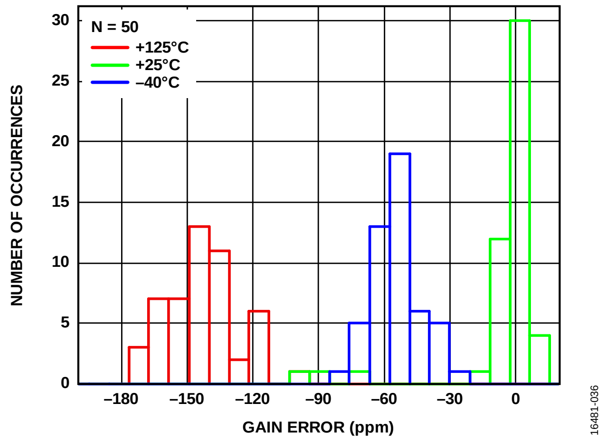

Figure 34. Gain Error Distribution, Reference Buffers On

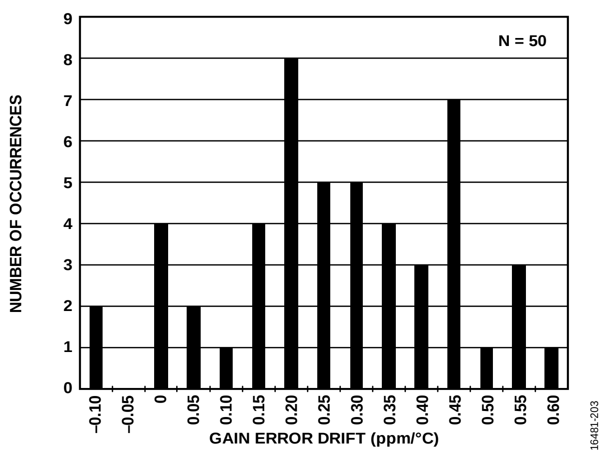

Figure 35. Gain Error Drift Reference Buffers Off

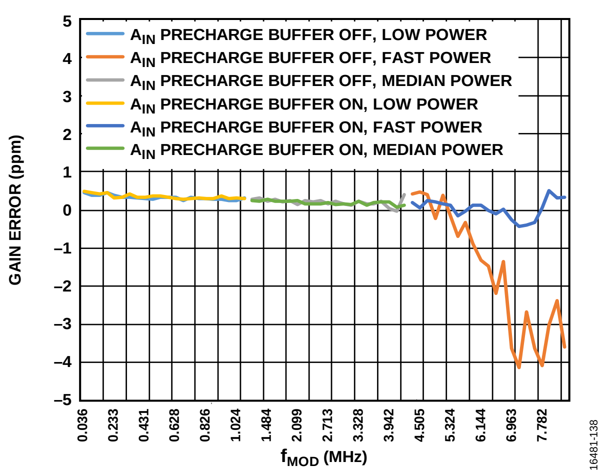

Figure 36. Gain Error vs. f_{MOD}

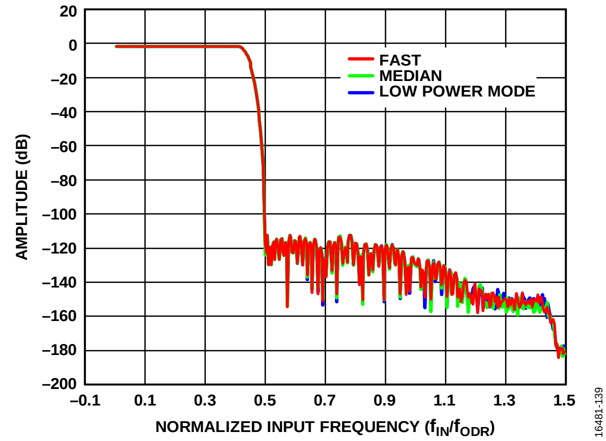

Figure 37. Low Ripple FIR Filter Profile, Amplitude vs. Normalized Input Frequency (f_{IN}/f_{ODR})

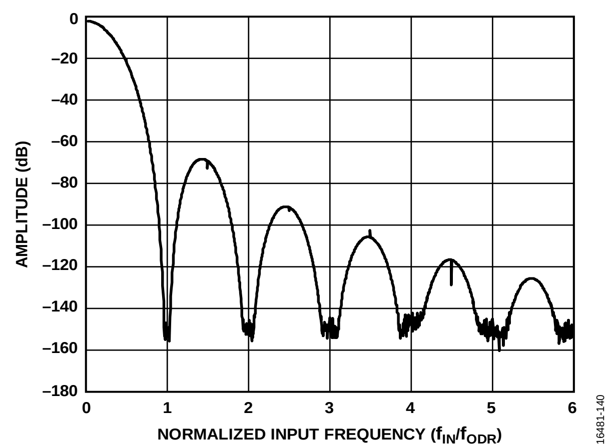

Figure 38. Sinc5 Filter Profile, Amplitude vs. Normalized Input Frequency (f_{IN}/f_{ODR})

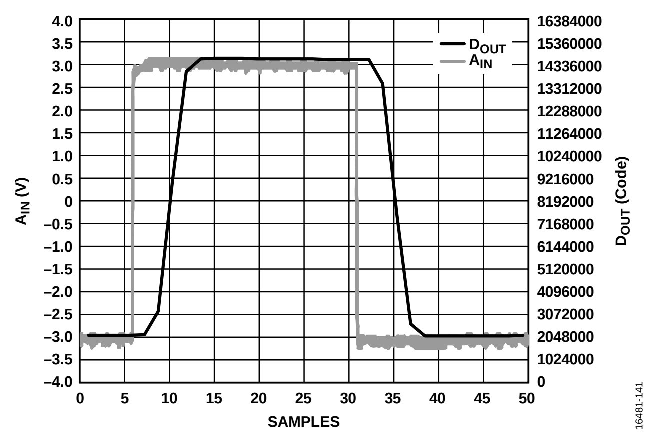

Figure 39. Step Response (A_{IN} and D_{OUT}) vs. Samples, Sinc5 Filter

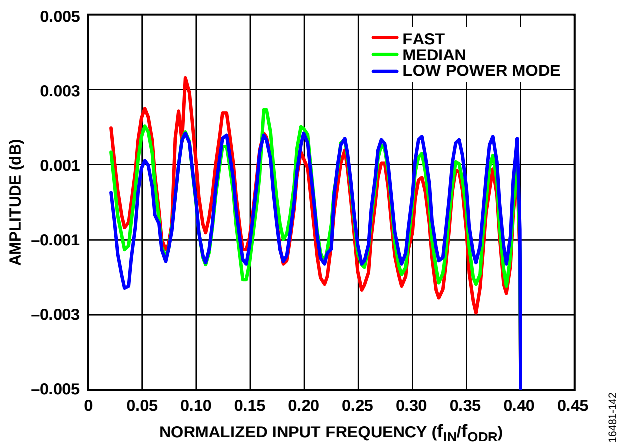

Figure 40. Low Ripple FIR Filter Ripple, Amplitude vs. Normalized Input Frequency (f_{IN}/f_{ODR})

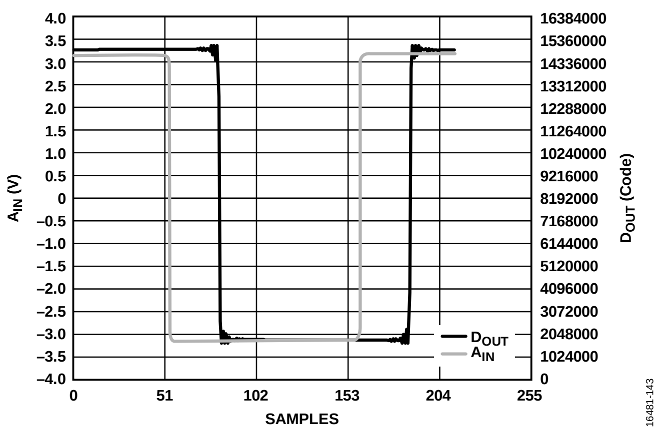

Figure 41. Step Response (A_{IN} and D_{OUT}) vs. Samples, Low Ripple Filter

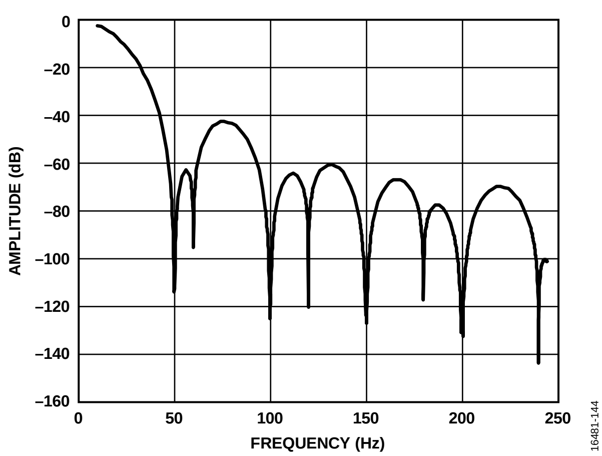

Figure 42. Sinc3 Filter Profile with 50 Hz and 60 Hz Rejection Enabled, Amplitude vs. Input Frequency, 50 Hz ODR, Decimation ×163,840

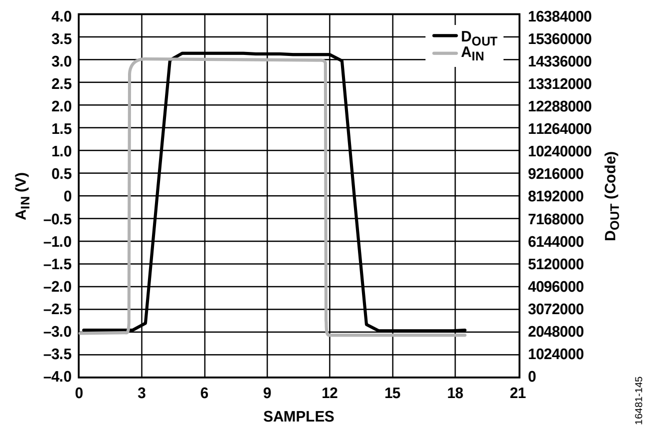

Figure 43. Step Response (A_{IN} and D_{OUT}) vs. Samples, Sinc3 Filter

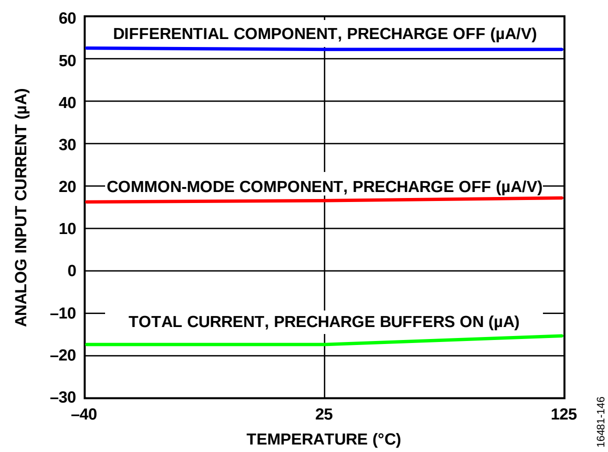

Figure 44. Analog Input Current vs. Temperature, Analog Input Precharge Buffers On/Off

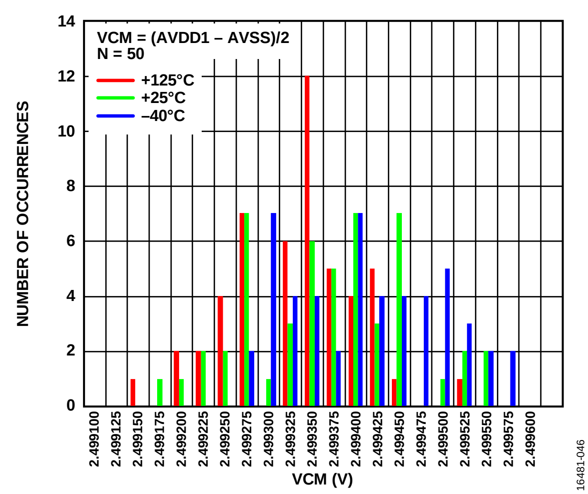

Figure 45. VCM Output Voltage Distribution, VCM = (AVDD1 – AVSS)/2

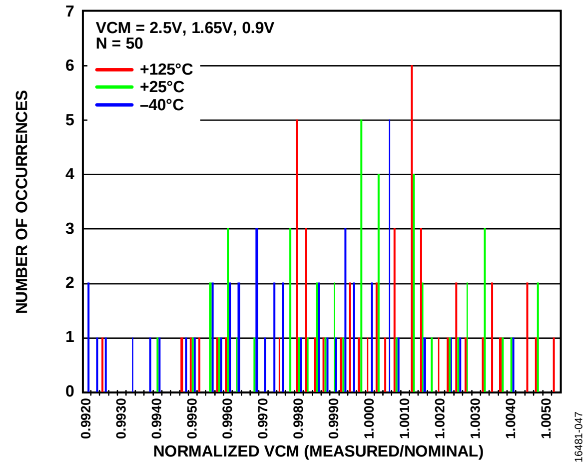

Figure 46. VCM Output Voltage Distribution, VCM = 2.5 V, 1.65 V, 0.9 V

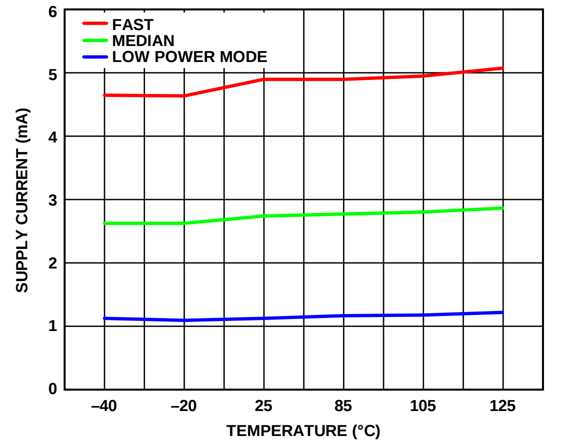

Figure 49. Supply Current vs. Temperature, AVDD2

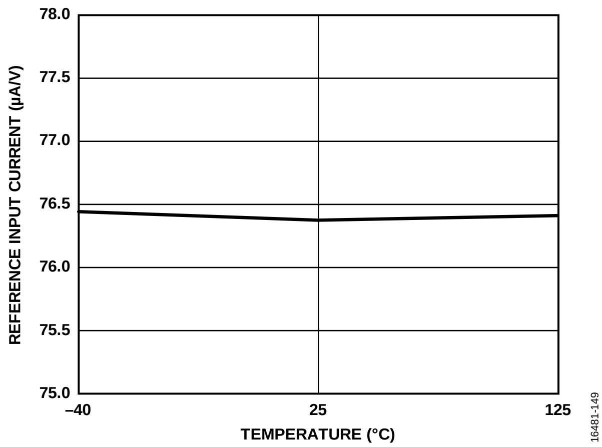

Figure 47. Reference Input Current vs. Temperature, Reference Precharge Buffers Off

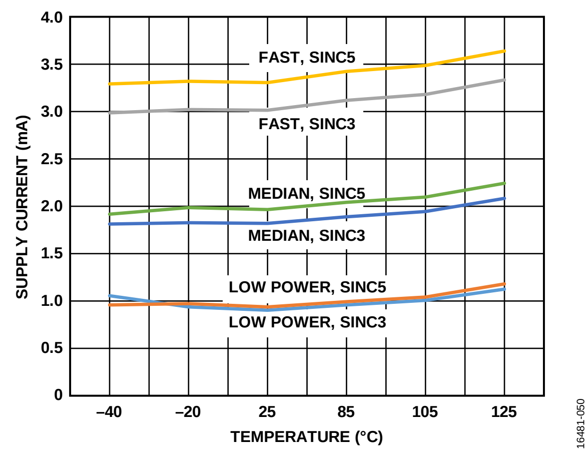

Figure 50. Supply Current vs. Temperature, IOVDD, Sinc3 and Sinc5 Filter

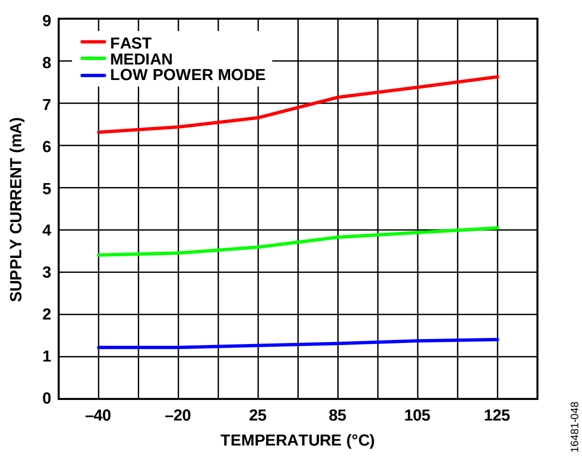

Figure 48. Supply Current vs. Temperature, AVDD1

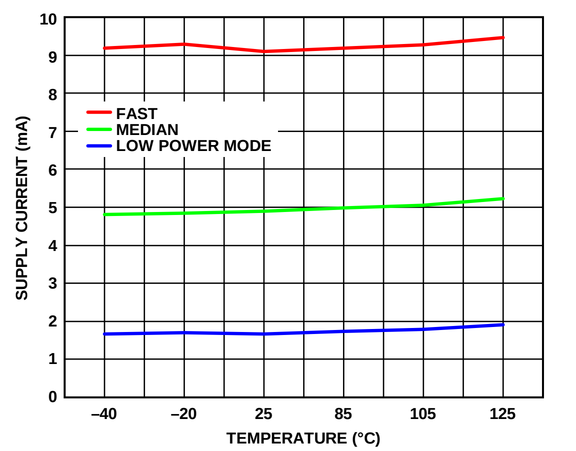

Figure 51. Supply Current vs. Temperature, IOVDD, Low Ripple FIR Filter

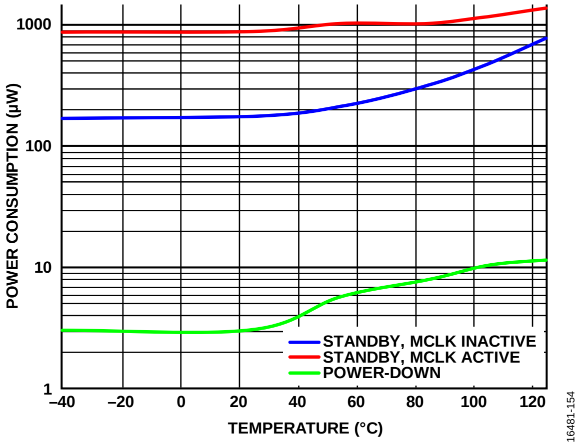

Figure 52. Power Consumption, Standby and Power-Down vs. Temperature, AVDD1, AVDD2 = 5 V, IOVDD = 1.8 V

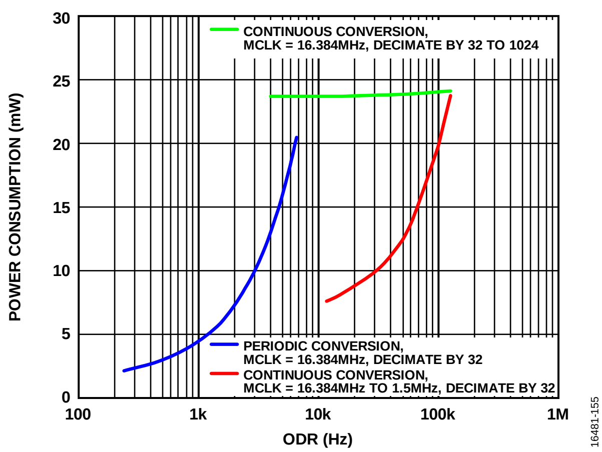

Figure 53. Power Consumption, Conversion Modes vs. ODR, Median Power Mode, Sinc5 Filter

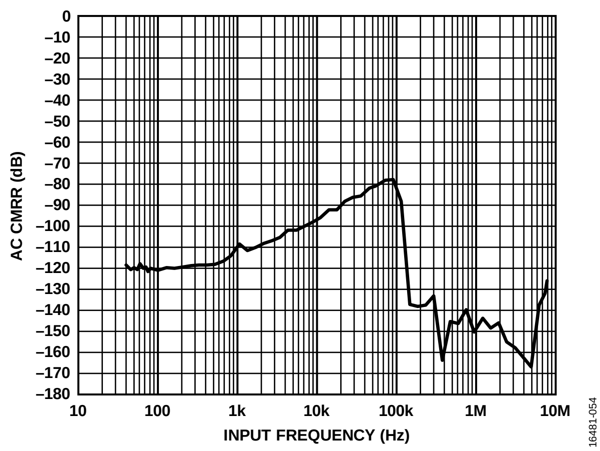

Figure 54. AC CMRR vs. Input Frequency

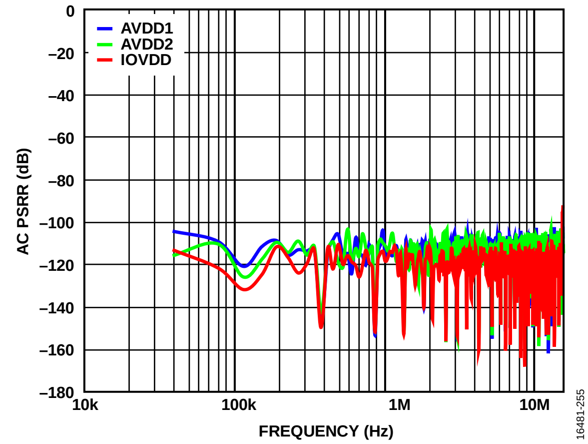

Figure 55. AC PSRR vs. Frequency, Fast Power Mode, V_{IN} = 0.1 V p-p

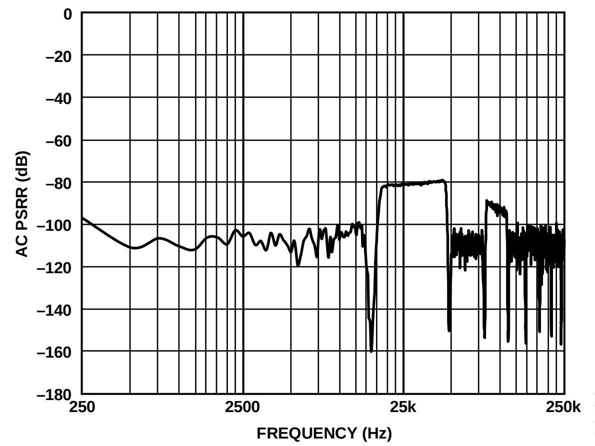

Figure 56. AVDD1 AC PSRR vs. Frequency, Low Power Mode, AVDD1 = 5 V + 0.1 V p-p

TERMINOLOGY

Common-Mode Rejection Ratio (CMRR)
CMRR is the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the common-mode voltage of AIN+ and AIN− at frequency, f_S.

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, *f*, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Integral Nonlinearity (INL) Error
INL error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured when input pins are shorted together. The value for dynamic range is expressed in decibels.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7768-1 is tested using the Canadian Collision Industry Forum (CCIF) standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Gain Error
The first transition (from 100 … 000 to 100 …001) occurs at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the ratio of the gain error change due to a temperature change of 1°C and the full-scale range (2^N). It is expressed in parts per million.

Least Significant Bit (LSB)
LSB is the smallest increment that a converter can represent. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is

$$LSB\ (\text{V}) = V_{IN}\ \text{p-p}/2^N$$

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise-and-Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels relative to the carrier (dBc), between the rms amplitude of the input signal and the peak spurious signal (excluding the first five harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Offset Error
Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Offset Error Drift
Offset error drift is the ratio of the zero error change due to a temperature change of 1°C and the full-scale code range (2^N). It is expressed in nV/°C.

THEORY OF OPERATION

The AD7768-1 is a low noise, wide bandwidth, 24-bit Σ-Δ ADC.

The AD7768-1 uses a Σ-Δ modulator with a clock running at f_{MOD}. The modulator samples the inputs at a rate of 2 × f_{MOD} to convert the analog input into an equivalent digital representation. These samples represent a quantized version of the analog input signal.

The Σ-Δ conversion technique is an oversampled architecture. This oversampled approach spreads the quantization noise over a wide frequency band (see Figure 57). To reduce the quantization noise in the signal band, the high-order modulator shapes the noise spectrum so that most of the noise energy is shifted out of the band of interest (see Figure 58). The digital filter that follows the modulator removes the large out of band quantization noise (see Figure 59).

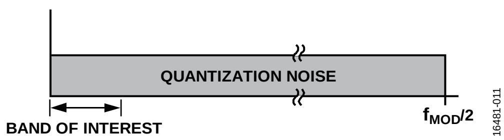

Figure 57. Σ-Δ ADC Quantization Noise (Linear Scale X-Axis)

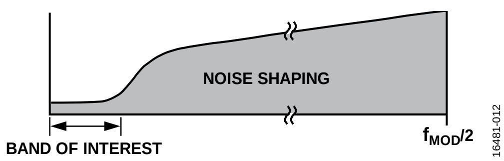

Figure 58. Σ-Δ ADC Noise Shaping (Linear Scale X-Axis)

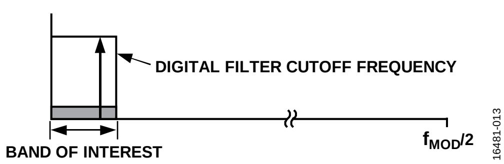

Figure 59. Σ-Δ ADC Digital Filter Cutoff Frequency (Linear Scale X-Axis)

For further information on the basic and advanced concepts of Σ-Δ ADCs, see the MT-022 Tutorial and the MT-023 Tutorial.

Digital filtering has advantages over analog filtering. First, digital filtering is insensitive to component tolerances and the variation of component parameters over time and temperature. Because digital filtering on the AD7768-1 occurs after the analog-to-digital conversion, the device can remove some of the noise injected during the conversion process. Analog filtering cannot remove noise injected during conversion. Second, the digital filter combines low pass-band ripple with a steep roll-off and high stop-band attenuation while also maintaining a linear phase response, which is difficult to achieve in an analog filter implementation.

CLOCKING, SAMPLING TREE, AND POWER SCALING

The AD7768-1 core ADC receives a master clock signal (MCLK). The MCLK signal can be sourced from one of four options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, an LVDS signal, and the internal clock. The MCLK signal received by the AD7768-1 defines the modulator clock rate (f_{MOD}) and, in turn, the sampling frequency of the modulator of 2 × f_{MOD}.

Figure 60 shows the clock tree from the MCLK input to the modulator and the digital filter. There are divider settings for MCLK. A divider in conjunction with the power mode and digital filter decimation settings are important when operating the AD7768-1.

The AD7768-1 has the ability to scale power consumption vs. the input bandwidth or noise desired. The user controls two parameters to achieve this scaling: MCLK division and power mode. When combined, these two settings determine the clock frequency of the modulator (f_{MOD}) and the bias current supplied to the modulator. The power mode (fast, median, or low power) sets the noise, speed capability, and current consumption of the modulator. The power mode is the dominant control for scaling the power consumption of the ADC.

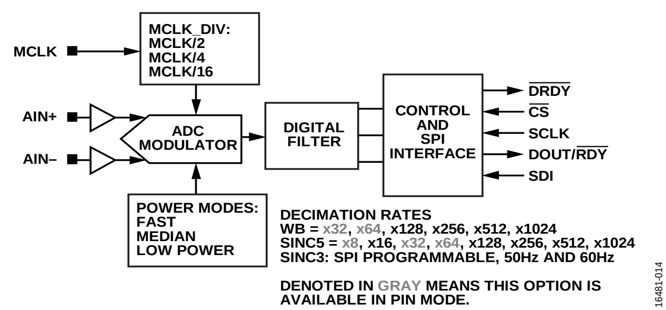

Figure 60. Sampling Structure Defined by the MCLK and MCLK_DIV Settings

Table 8. Decimation Rate Options

	Available Decimation Rates	
Filter Option	**SPI Control Mode**	**Pin Control Mode**
Low Ripple FIR	×32, ×64, ×128, ×256, ×512, ×1024	×32, ×64
Sinc5	×8, ×16, ×32, ×64, ×128, ×256, ×512, ×1024	×8, ×32, ×64
Sinc3	Programmable decimation rate	50 Hz and 60 Hz output only, based on a 16.384 MHz MCLK

To determine f_{MOD}, select one of four clock divider settings: MCLK/2, MCLK/4, MCLK/8, or MCLK/16.

Although the MCLK division and power modes are independent settings, there are restrictions in valid combinations. A valid range of modulator frequencies exists for each power mode. Table 9 describes this recommended range, which allows the device to achieve the best performance while also minimizing power consumption. The AD7768-1 specifications do not cover the performance and function beyond the maximum f_{MOD} for a given power mode.

For example, in fast mode, to maximize the ODR or input bandwidth, an MCLK rate of 16.384 MHz is required. Select an MCLK divider (MCLK_DIV) equal to 2 for a modulator frequency of 8.192 MHz.

Table 9. Recommended f_{MOD} Range for Each Power Mode

Power Mode	Recommended f_{MOD} Range (MHz)
Low Power	0.038 to 1.024
Median	1.024 to 4.096
Fast	4.096 to 8.192

Control of the settings for the power mode and the modulator frequency differ in $\overline{PIN}$ control mode vs. SPI control mode.

In SPI control mode, the user can program the power mode and MCLK_DIV independently. Independent selection of the power mode and MCLK_DIV allows full freedom in the MCLK speed selection to achieve a target modulator frequency, which can also result in a small power saving. For example, if the power mode is low power, it is more power efficient to use MCLK = 2.048 MHz with MCLK_DIV = 2 than MCLK = 16.384 MHz with MCLK_DIV = 16. Both options are valid selections and result in an f_{MOD} frequency of 1.024 MHz.

In $\overline{PIN}$ control mode, the MODEx pins determine the power mode and modulator frequency. The modulator frequency tracks the power mode, which means that f_{MOD} is fixed at MCLK/16 for low power mode, MCLK/4 for median mode, and MCLK/2 for fast mode. In $\overline{PIN}$ control mode, the MODEx pins are also used to select the filter type and decimation rate.

Power vs. Noise Performance Optimization

Depending on the bandwidth of interest for the measurement, the user can choose a strategy of either lowest current consumption or highest resolution. This choice is due to an overlap in the coverage of each power mode. There are different ways to achieve the same ODR. Using a lower MCLK frequency in tandem with a lower decimation rate allows the user to achieve the same data rate as using a higher MCLK frequency with a higher decimation.

Lower power can be achieved by using lower modulator clock frequencies. Conversely, to achieve the highest resolution, use higher modulator clock frequencies and maximize the amount of oversampling.

Example of Power vs. Noise Performance Optimization

Consider a system constraint with a maximum available MCLK of 8 MHz. The system is targeting a measurement bandwidth of approximately 25 kHz with the wideband filter, setting the ODR of the AD7768-1 to 62.5 kHz. Because of the low MCLK frequency available and the system power budget, median power mode is used. In median power mode, to achieve this 25 kHz input bandwidth, set the MCLK division and decimation ratio to balance using two configurations. This flexibility is possible only in SPI control mode.

Configuration A

To maximize the dynamic range, use the following settings:

- MCLK = 8 MHz
- Median power
- f_{MOD} = MCLK/2
- Decimation = ×64 (digital filter setting)
- ODR = 62.5 kHz

This configuration maximizes the available decimation rate (or oversampling ratio) for the bandwidth required and the MCLK rate available. The decimation averages the noise from the modulator, maximizing the dynamic range.

Configuration B

To minimize power, use the following settings:

- MCLK = 8 MHz
- Median power
- f_{MOD} = MCLK/4
- Decimation = ×32 (digital filter setting)
- ODR = 62.5 kHz

This configuration reduces the clocking speed of the modulator and the digital filter. Although the f_{MOD} frequency is within the recommended frequency range in both cases, Configuration B saves nearly 5 mW of power compared to Configuration A. The trade-off in the case of Configuration B is that the digital filter must run at a 2× lower decimation rate. This 2× reduction in decimation rate (or oversampling ratio) results in a 3 dB reduction in the dynamic range vs. Configuration A.

NOISE PERFORMANCE AND RESOLUTION

Table 10 and Table 11 show the noise performance for the low ripple FIR and sinc5 digital filters of the AD7768-1 for various ODR values and power modes. The specified noise values and dynamic ranges are typical for the bipolar input range with an external 4.096 V reference (V_{REF}). The rms noise is measured with shorted analog inputs, which are driven to (AVDD1 − AVSS)/2 using the on-board VCM buffer output.

The ratio of the rms shorted input noise to the rms full-scale input signal range calculates the dynamic range.

$$Dynamic\ Range\ (\text{dB}) = 20\log_{10}((V_{REF}/\sqrt{2})/(RMS\ Noise))$$

The LSB size for a 4.096 V reference is 488 nV and is calculated as follows:

$$LSB\ (\text{V}) = (2 \times V_{REF})/2^{24}$$

Table 10. Low Ripple FIR Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V)

ODR (kSPS)	Decimation Rate	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Fast Mode				
256	32	110.8	108.43	10.98
128	64	55.4	111.96	7.31
64	128	27.7	115.15	5.06
32	256	13.9	118.23	3.55
16	512	6.9	121.20	2.52
8	1024	3.5	124.16	1.79
Median Mode				
128	32	55.4	108.45	10.94
64	64	27.7	111.89	7.37
32	128	13.9	115.22	5.02
16	256	6.9	118.22	3.55
8	512	3.5	121.23	2.51
4	1024	1.7	124.17	1.79
Low Power Mode				
32	32	13.9	108.54	10.84
16	64	6.9	112.12	7.17
8	128	3.5	115.30	4.97
4	256	1.7	118.31	3.52
2	512	0.87	121.22	2.52
1	1024	0.43	124.33	1.76

Table 11. Sinc5 Filter Noise for Performance vs. ODR (V_{REF} = 4.096 V)

ODR (kSPS)	Decimation Rate	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Fast Mode				
1024 (16-Bit Output Only)	8	208.896	92.93	65.39
512	16	104.448	107.32	12.46
256	32	52.224	111.57	7.64
128	64	26.112	115.30	4.97
64	128	13.056	118.29	3.53
32	256	6.528	121.27	2.50
16	512	3.264	124.15	1.80
8	1024	1.632	127.16	1.27
Median Mode				
512	8	104.448	92.56	68.20
256	16	52.224	107.88	11.69
128	32	26.112	112.06	7.22
64	64	13.056	115.22	5.02
32	128	6.528	118.46	3.46
16	256	3.264	121.34	2.48
8	512	1.632	124.34	1.76
4	1024	0.816	127.20	1.26

ODR (kSPS)	Decimation Rate	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Low Power Mode				
128	8	26.112	92.41	69.39
64	16	13.056	107.82	11.77
32	32	6.528	112.15	7.15
16	64	3.264	115.37	4.93
8	128	1.632	118.35	3.50
4	256	0.816	121.27	2.50
2	512	0.408	124.24	1.78
1	1024	0.204	127.28	1.25

CORE CONVERTER

ADC Core and Signal Chain

Figure 62 shows a top level implementation of the core signal chain. The Σ-Δ modulator oversamples the analog input and passes the digital representation to the digital filter block. The data is filtered, scaled for gain and offset (depending on the user settings), and then output on the SPI interface.

The AD7768-1 can use up to a 5 V reference and converts the differential voltage between the analog inputs (AIN+ and AIN−) to a digital output. The analog inputs can be configured as either differential or pseudo differential inputs. As a pseudo differential input, either AIN+ or AIN− can be connected to a constant input voltage (such as 0 V, AVSS, or another reference voltage). The ADC converts the voltage difference between the analog input pins to a digital code on the output. Using a common-mode voltage of (AVDD1 − AVSS)/2 for the analog inputs, AIN+ and AIN−, maximizes the ADC input range. The 24-bit conversion result is in MSB first, twos complement format. Figure 61 shows the ideal transfer functions for the AD7768-1.

Use the following equation to convert from codes to volts, assuming the codes have first been converted from twos complement to straight binary:

$$Voltage = ((Code - Midscale\ Code) \times 2 \times V_{REF})/2^{24}$$

where the *Midscale Code* is 8,388,608 in straight binary, and 0x7FFFFF in Table 12 is converted to 0xFFFFFF in straight binary. Use the previous equation to calculate a voltage in the V_{REF+} to V_{REF-} range.

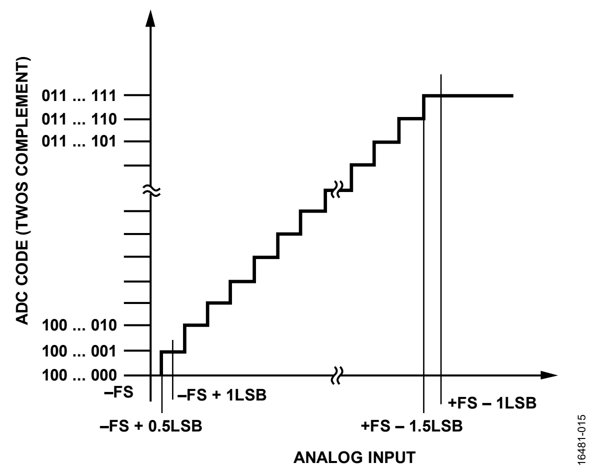

Figure 61. ADC Ideal Transfer Functions (FS is Full-Scale)

Table 12. Output Codes and Ideal Input Voltages

Description	Analog Input (AIN+ − AIN−), V_{REF} = 4.096 V	Digital Output Code, Twos Complement (Hex)
FS − 1 LSB	+4.095999512 V	0x7FFFFF
Midscale + 1 LSB	+488 nV	0x000001
Midscale	0 V	0x000000
Midscale − 1 LSB	−488 nV	0xFFFFFF
−FS + 1 LSB	−4.095999512 V	0x800001
−FS	−4.096 V	0x800000

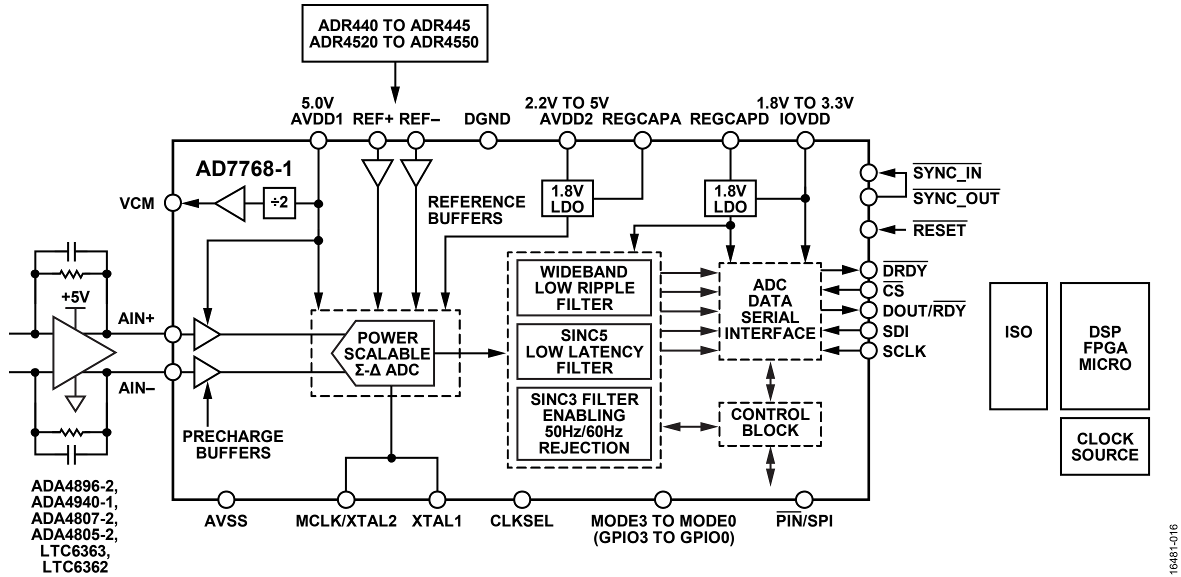

Figure 62. AD7768-1 Top Level Core Signal Chain and Control

Analog Inputs and Precharge Buffering

Figure 63 shows the analog front end of the AD7768-1. Protection diodes that protect the ADC from overvoltage and ESD events are shown on the signal path. An internal precharge amplifier that eases the driving requirement of the external buffer can drive the ADC internal sampling capacitors, shown as CS1 and CS2. The precharge amplifier charges the switched sampling capacitors for the initial part of the sampling period. The bypass switches, BPS+ and BPS–, switch out the precharge buffer. The external amplifier then drives the input capacitors for the remainder of the sampling period to fulfill the fine settling required on the input. As a result, the precharge buffer does not add noise to the conversion result, but allows lower power and lower bandwidth driver amplifiers to be used to drive the AD7768-1. The precharge buffer amplifier stage reduces the input current by a factor of 8×.

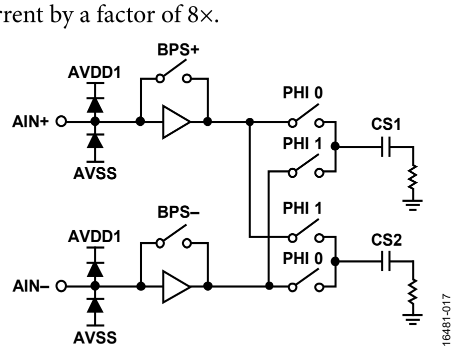

Figure 63. Analog Front End of the AD7768-1

The precharge buffers can be turned on or off using a register write. In PIN control mode, the precharge buffers are enabled by default for optimum performance.

When the precharge analog input buffers are disabled, the analog input current is sourced from the analog input source. Two components calculate the unbuffered analog input current: the differential input voltage on the analog input pair and the analog input voltage with respect to AVSS. The analog input current scales linearly with the modulator clock rate. For MCLK = 16 MHz and MCLK/2 in fast power mode, the differential input current is ~53 µA/V and the current with respect to ground is ~17 µA/V.

For example, if the precharge buffers are off, AIN+ = 5 V and AIN− = 0 V.

$$AIN+ = 5\text{ V} \times 53\text{ µA/V} + 5\text{ V} \times 17\text{ µA/V} = 350\text{ µA}$$

$$AIN- = 5\text{ V} \times 53\text{ µA/V} + 0\text{ V} \times 17\text{ µA/V} = -265\text{ µA}$$

When the precharge buffers are enabled, the absolute voltage with respect to AVSS determines the majority of the current. The worst case input current is −25 µA, measured when the analog input is close to either the AVDD1 or AVSS rails. The analog input current scales with the MCLK frequency and device power mode (see Figure 64 and Figure 65).

Full settling of the analog inputs to the ADC requires the use of an external amplifier. Pair amplifiers, such as the ADA4805-2 for low power mode, the ADA4807-2 or ADA4940-1 for median mode, and the ADA4807-2 or ADA4896-2 for fast mode, can be used with the AD7768-1. The system can operate from a single 5 V rail if the ADA4940-1 is used with a 4.096 V reference to give the amplifier sufficient headroom and footroom to achieve the best distortion performance from the amplifier. Running the AD7768-1 in median and low power modes or reducing the MCLK rate reduces the load and speed requirements of the amplifier. Therefore, lower power amplifiers can be paired with the analog inputs to achieve optimal signal chain efficiency.

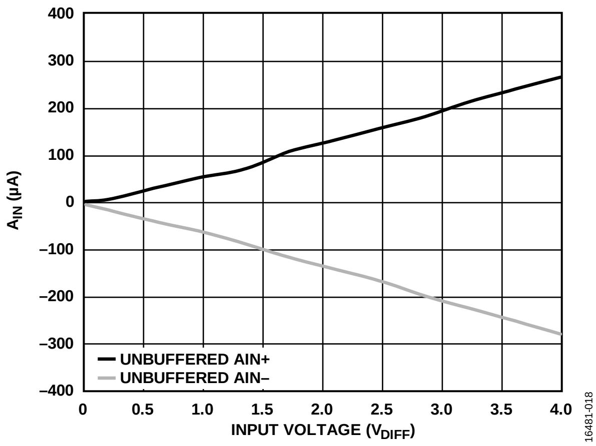

Figure 64. Analog Input Current (A_{IN}) vs. Input Voltage, Analog Input Precharge Buffer Off, VCM = 2.5 V, f_{MOD} = 8.192 MHz

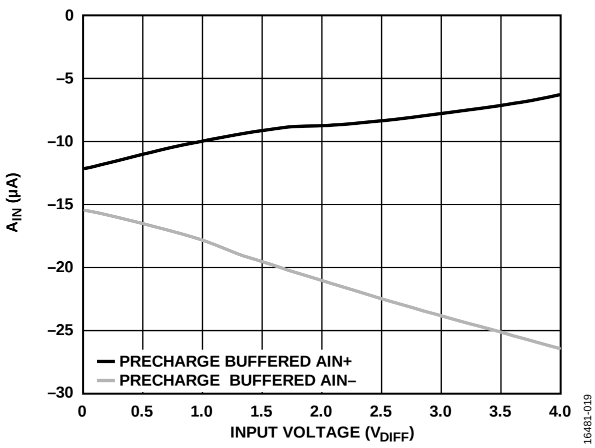

Figure 65. Analog Input Current (A_{IN}) vs. Input Voltage, Analog Input Precharge Buffer On, VCM = 2.5 V, f_{MOD} = 8.192 MHz

VCM Output

The AD7768-1 provides a buffered common-mode voltage output on the VCM pin. This buffer can bias analog input signals. By incorporating this buffer into the ADC, the AD7768-1 reduces component count and board space. In $\overline{\text{PIN}}$ control mode, the VCM potential is fixed to (AVDD1 − AVSS)/2 and is on by default.

In SPI mode, the VCM potential is configured using the ANALOG2 register (Register 0x17). The output can be enabled or disabled and set to (AVDD1 − AVSS)/2, 2.5 V, 2.05 V, 1.9 V, 1.65 V, 1.1 V, or 0.9 V referenced to AVSS. The default value is (AVDD1 − AVSS)/2.

Figure 66 is a simulation of the VCM noise for each VCM setting, plotted over a bandwidth of 100 Hz to 1 MHz. An external resistor capacitor (RC) filter is required to set the bandwidth to meet the VCM noise requirement. For example, a VCM output of 2.5 V has 180 µV rms of noise (see Figure 66). If the bandwidth is limited to 1 kHz, this noise can be reduced to approximately 65 µV rms (see Figure 66).

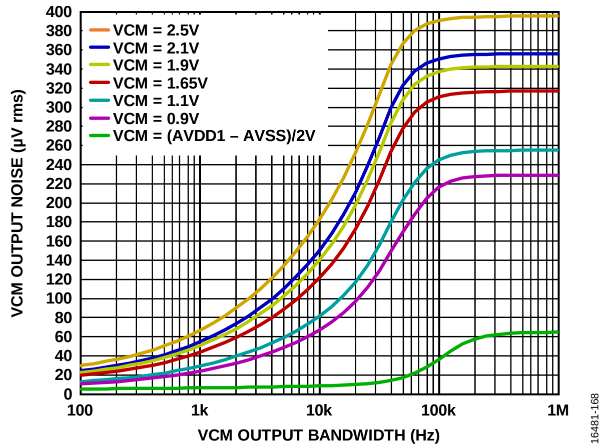

Figure 66. VCM Output Noise vs. VCM Output Bandwidth

Reference Input and Buffering

The AD7768-1 has differential reference inputs, REF+ and REF−. The absolute input reference voltage range is from 1 V to AVDD1 − AVSS.

The reference inputs can be configured for a fully buffered input on each of the REF+ and REF− pins, a precharge buffered input, or to bypass both buffers.

Use of either the full buffers or the precharge buffers reduces the burden on the external reference when driving large loads or multiple devices. The fully buffered input to the reference pins provides a high impedance input node and enables use of the AD7768-1 in ratiometric applications where the ultralow source impedance of a traditional external reference is not available.

In $\overline{\text{PIN}}$ control mode, the reference precharge buffers are on by default. In SPI mode, the user can choose fully buffered or precharge buffers.

The reference input current scales linearly with the modulator clock rate.

For MCLK = 16 MHz in fast mode, the differential input voltage is ~80 µA/V unbuffered and 20 µA/V with the precharge buffers enabled.

With the precharge buffers off, REF+ = 5 V and REF− = 0 V.

$$REF\pm = 5\text{ V} \times 80\ \mu\text{A/V} = +400\ \mu\text{A}$$

With the precharge buffers on, REF+ = 5 V, and REF− = 0 V.

$$REF\pm = \text{approximately } 20\ \mu\text{A}$$

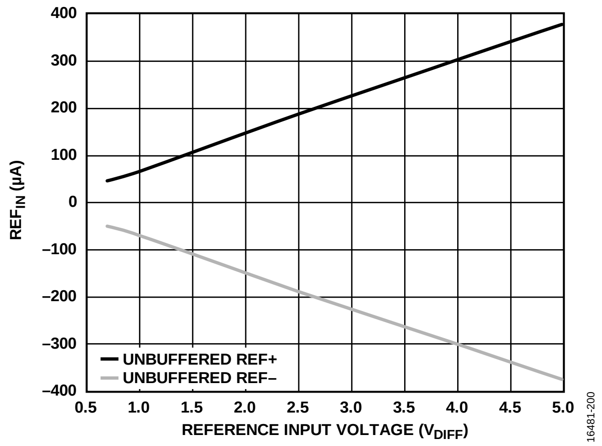

Figure 67. Reference Input Current (REF_{IN}) vs. Reference Input Voltage, Unbuffered REF+ and REF–

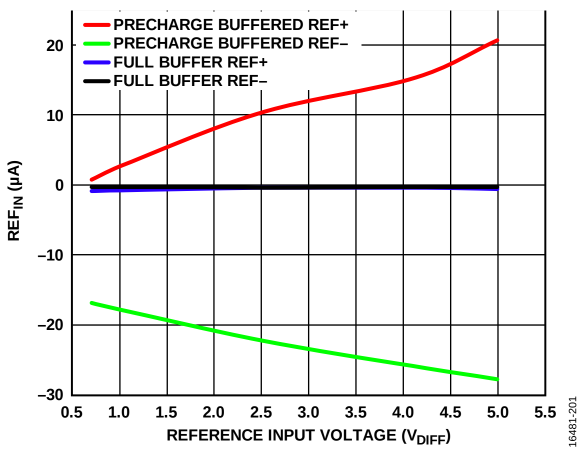

Figure 68. Reference Input Current (REF_{IN}) vs. Reference Input Voltage, Precharge Buffered REF+ and REF– and Full Buffer REF+ and REF–

For the best performance and headroom, use a 4.096 V reference, such as the ADR444 or ADR4540, that can both be supplied by a 5 V rail and shared to the AVDD1 supply.

A reference detect function is available in SPI control mode. See the Reference Detection section for details.

CLOCKING AND CLOCK SELECTION

The AD7768-1 has an internal oscillator that is used for initial power-up of the device. After the AD7768-1 completes the start-up routine, a clock handover occurs to the external MCLK. The AD7768-1 counts the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and of a frequency of at least 600 kHz. If there is a fault with the external MCLK, the handover does not occur, the AD7768-1 clock error bit is set, and the AD7768-1 continues to operate from the internal clock.

In SPI control mode, use the clock source bits in Register 0x15 to set the external MCLK source. Four clock options are available: internal oscillator, external CMOS, crystal oscillator, or LVDS. If selecting the LVDS clock option, the clock source must be selected using the CLOCK_SEL bits (Bits[7:6] in Register 0x15). If an external MCLK has already been qualified, switching back to the internal oscillator requires the external clock to remain applied for the duration of the transition.

In $\overline{\text{PIN}}$ control mode, the CLKSEL pin sets the external MCLK source. Three clock options are available in $\overline{\text{PIN}}$ control mode: an internal oscillator, an external CMOS, or a crystal oscillator. The CLKSEL pin is sampled on power-up.

Set the EN_ERR_EXT_CLK_QUAL bit (Bit 0 in Register 0x29) to turn off the clock qualification. Turning off the clock qualification allows the use of slower external MCLK rates outside the recommended MCLK frequency.

CLKSEL Pin

If CLKSEL = 0 in $\overline{\text{PIN}}$ control mode, the CMOS clock option is selected and must be applied to the MCLK pin. In this case, tie the XTAL1 pin to DGND.

If CLKSEL = 1 in $\overline{\text{PIN}}$ control mode, the crystal option is selected and must be connected between the XTAL1 and XTAL2 pins.

In SPI control mode, the CLKSEL pin does not determine the MCLK source used and CLKSEL must be tied to DGND.

Using the Internal Oscillator

In some cases, conversion using an internal clock oscillator may be preferred, such as in isolated applications where dc input voltages must be measured. Converting ac signals with the internal clock is not recommended because using the internal clock can result in degradation of SNR due to jitter.

DIGITAL FILTERING

The AD7768-1 offers three types of digital filters. The digital filters available on the AD7768-1 are

- Sinc5 low latency filter, −3 dB at 0.204 × ODR (8 rates)
- Sinc3 low latency filter, −3 dB at 0.2617 × ODR, widely programmable data rate
- Low ripple FIR filter, −3 dB at 0.43 × ODR (6 rates)

Sinc5 Filter

Most precision Σ-Δ ADCs use a sinc filter. The sinc5 filter offered in the AD7768-1 enables a low latency signal path useful for dc inputs on control loops, or for where user specific post processing is required. The sinc5 filter has a −3 dB bandwidth of 0.204 × ODR. Table 11 shows the noise performance for the sinc5 filter across power modes and decimation ratios.

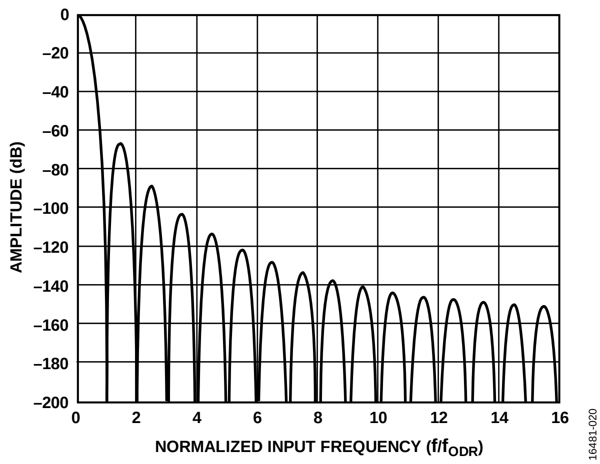

Figure 69. Sinc Filter Frequency Response

The impulse response of the filter is five times the ODR. For 250 kSPS ODR, the time to settle data fully is 20 µs. For the 1 MSPS ODR, the time to settle data fully is 5 µs.

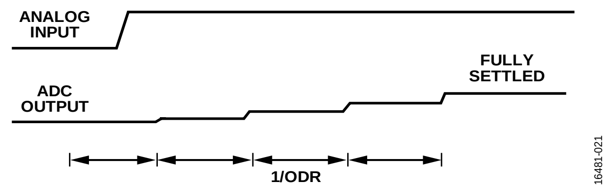

Figure 70. Sinc5 Filter Step Response

The time from a $\overline{\text{SYNC\_IN}}$ pulse to both the first $\overline{\text{DRDY}}$ and to fully settled data for various ODR values for the sinc5 filter is shown in Table 13.

Table 13. Sinc5 Filter, $\overline{\text{SYNC\_IN}}$ to Settled Data

		MCLK Periods	
MCLK Divide Setting	**Decimation Ratio**	**Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise**	**Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise**
MCLK/2	8	46	110
	16	62	190
	32	94	350
	64	162	674
	128	295	1,319
	256	561	2,609
	512	1,093	5,189
	1024	2,173	10,365
MCLK/4	8	79	207
	16	111	367
	32	175	687
	64	310	1,334
	128	576	2,624
	256	1,108	5,204
	512	2,172	10,364
	1024	4,332	20,716
MCLK/16	8	278	790
	16	406	1,430
	32	662	2,710
	64	1,194	5,290
	128	2,258	10,450
	256	4,386	20,770
	512	8,642	41,410
	1024	17,282	82,818

Sinc3 Filter

The sinc3 filter offered in the AD7768-1 enables a low latency signal path useful for dc inputs on control loops, or for eliminating unwanted known interferers at specific frequencies. The sinc3 filter path incorporates a programmable decimation rate to achieve rejection of known interferers. Decimation rates from 32 to 185,280 are achievable using the sinc3 filter. The sinc3 filter has a −3 dB bandwidth of 0.26 × ODR. Table 14 and Table 15 show the minimum rejection measured at the frequencies of interest with a 50 Hz ODR.

For example, to calculate for a 12.288 MHz MCLK to achieve an ODR of 50 Hz using the sinc3 filter, use the following equation:

$$ODR = MCLK/(MCLK\_DIV \times Decimation\ Rate)$$

Assuming the AD7768-1 is running in low power mode, MCLK_DIV = 16.

$$Decimation\ Rate = MCLK/(MCLK\_DIV \times ODR) = 1536$$

To set the decimation rate to 1536, write 47 to the sinc3 decimation rate registers (Register 0x1A and Register 0x1B) because the value in the registers is incremented by 1 and then multiplied by 32 to give the actual decimation rate.

Table 14. Sinc3 Filter 50 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	101
100 ± 2	102
150 ± 3	102
200 ± 4	102

Table 15. Sinc3 Filter 50 Hz and 60 Hz Rejection, 50 Hz ODR and Decimate by 163,840

Frequency Band (Hz)	Minimum Measured Rejection (dB)
50 ± 1	81
60 ± 1	67
100 ± 2	83
120 ± 2	72
150 ± 3	86
180 ± 3	78
200 ± 4	90
240 ± 4	87

The impulse response of the filter is three times the ODR. For 250 kSPS ODR, the time to settle data fully is 12 µs.

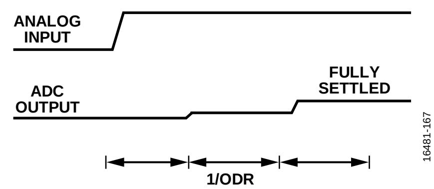

Figure 71. Sinc3 Filter Step Response

Programming for 50 Hz, 60 Hz, and 50 Hz and 60 Hz Rejection

To reject 50 Hz tones, program the ODR of the sinc3 filter to 50 Hz (see Figure 72). It is also possible to achieve simultaneous rejection of both 50 Hz and 60 Hz by setting Bit 7 in the DIGITAL_FILTER register (Register 0x19). Rejection of both 50 Hz and 60 Hz line frequencies is possible in this configuration (see Figure 42).

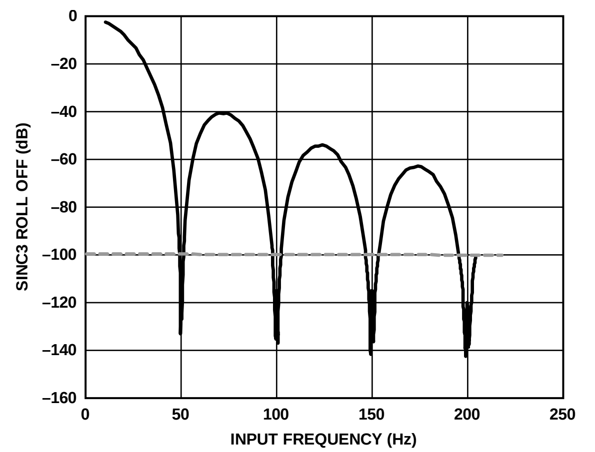

Figure 72. Sinc3 Filter Frequency Response Showing 50 Hz Rejection, 50 Hz ODR, ×163,840 Decimation

Table 16. Sinc3 Filter, $\overline{\text{SYNC\_IN}}$ to Settled Data

MCLK Divide Setting	Decimation Ratio	MCLK Periods: Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	MCLK Periods: Delay from First MCLK Rise After $\overline{\text{SYNC\_IN}}$ Rise to Earliest Settled $\overline{\text{DRDY}}$ Rise
MCLK/2	32	127	255
	64	191	447
	128	319	831
	256	575	1,599
	512	1,087	3,135
	1024	2,111	6,207
	163,840	327,743	983,103

MCLK Divide Setting	Decimation Ratio	MCLK Periods	
		Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/4	32	241	497
	64	369	881
	128	625	1,649
	256	1,137	3,185
	512	2,161	6,257
	1024	4,209	12,401
	81,920	327,793	983,153
MCLK/16	32	926	1,950
	64	1,438	3,486
	128	2,462	6,558
	256	4,510	12,702
	512	8,606	24,990
	1024	16,798	49,566
	20,480	328,094	983,454

Low Ripple FIR Filter

The FIR filter is a low ripple, input pass-band up to 0.4 × ODR. The low ripple FIR filter has almost full attenuation at 0.5 × ODR (Nyquist), maximizing antialias protection. The frequency response of the low ripple FIR filter is shown in Figure 73. The low ripple FIR filter has a pass-band ripple of ±0.005 dB, shown in Figure 74, and a stop band attenuation of 105 dB from Nyquist out to the chop frequency (f_{CHOP}). For more information on anti-aliasing and f_{CHOP} aliasing, see the Antialiasing Filtering section. The low ripple FIR filter is a 64-order digital filter. The group delay of the filter is 34/ODR. After a sync pulse, there is an additional delay from the SYNC_IN rising edge to fully settled data. The time from a SYNC_IN pulse to both the first DRDY and to fully settled data for various ODR values is shown in Table 17.

The low ripple FIR filter can be selected in one of six different decimation rates, allowing the user to choose the optimal input bandwidth and speed of the conversion vs. the desired resolution.

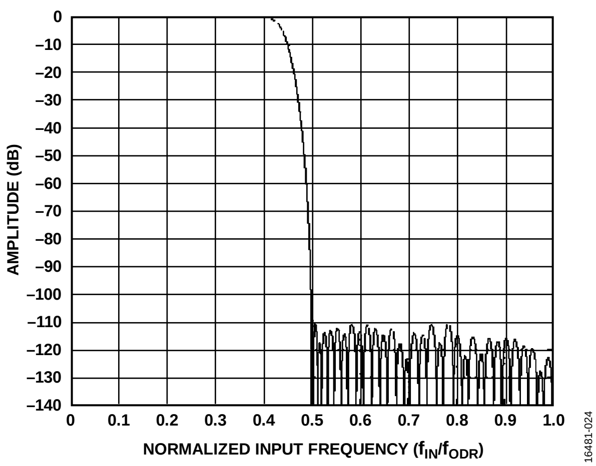

Figure 73. Low Ripple FIR Filter Frequency Response

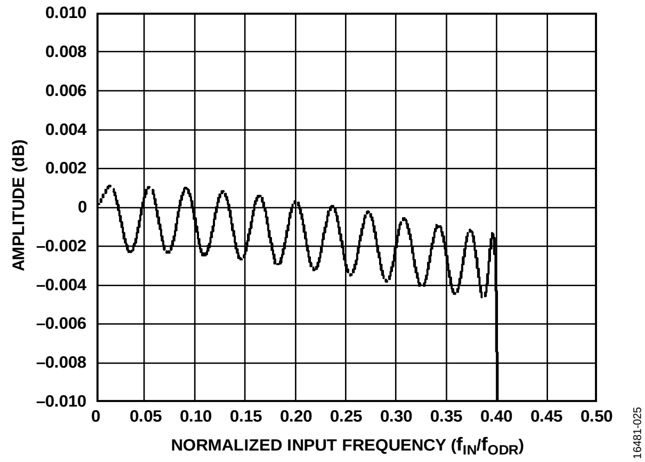

Figure 74. Low Ripple FIR Filter Pass-Band Ripple

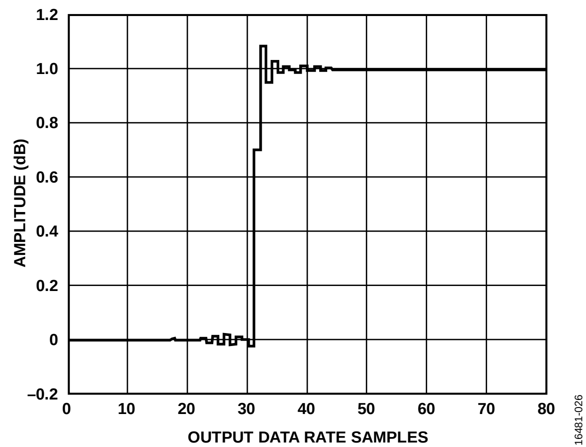

Figure 75. Low Ripple FIR Filter Step Response

Table 17. Low Ripple FIR Filter SYNC_IN to Settled Data

		MCLK Periods	
MCLK Divide Setting	**Decimation Ratio**	**Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise**	**Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled DRDY Rise**
MCLK/2	32	284	4,252
	64	413	8,349
	128	797	16,669
	256	1,565	33,309
	512	3,101	66,589
	1024	6,157	133,133
MCLK/4	32	428	8,364
	64	812	16,684
	128	1,580	33,324
	256	3,116	66,604
	512	6,188	133,164
	1024	12,300	266,252

MCLK Divide Setting	Decimation Ratio	MCLK Periods	
		Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to First $\overline{DRDY}$ Rise	Delay from First MCLK Rise After $\overline{SYNC\_IN}$ Rise to Earliest Settled $\overline{DRDY}$ Rise
MCLK/16	32	1,674	33,418
	64	3,202	66,690
	128	6,274	133,250
	256	12,418	266,370
	512	24,706	532,610
	1024	49,154	1,064,962

DECIMATION RATE CONTROL

The AD7768-1 has programmable decimation rates for the sinc and low ripple FIR digital filters. The decimation rates allow the user to band limit the measurement, which reduces the speed and input bandwidth, but increases the resolution because there is further averaging in the digital filter. Control of the decimation rate on the AD7768-1 when using the SPI control is set in the DIGITAL_FILTER register (Register 0x19) for the sinc5 and low ripple FIR filters.

The decimation rate of the sinc3 filter is controlled using the SINC3_DEC_RATE_LSB register (Register 0x1A) and the SINC3_DEC_RATE_MSB register (Register 0x1B). These registers combine to provide 13 bits of programmability. The decimation rate is set by incrementing the value in these registers by one and multiplying the value by 32. For example, setting a value of 0x5 in the SINC3_DEC_RATE_LSB register results in a decimation rate of 192 for the sinc3 filter.

In $\overline{PIN}$ control mode, the MODE0 pin controls the decimation ratio. Only decimation rates of ×32 and ×64 are available for use with the sinc5 and wideband filter options. See Table 22 for the full list of options available in $\overline{PIN}$ control mode.

ANTIALIASING FILTERING

When designing an antialiasing filter for the AD7768-1, there are three main aliasing regions to take into account. After the alias requirements of each zone are understood, the user can design an antialiasing filter to meet the needs of the specific application. The three zones for consideration are the modulator saturation point, the modulator unprotected zones, and the modulator chopping frequency.

Modulator Saturation Point

Think of the Σ-Δ modulator as a standard control loop employing negative feedback. The control loop ensures that the average processed error signal is very small over time. The control loop uses an integrator to remember preceding errors and force the mean error to zero. When the analog input slew rate is high enough, the error feedback is large, and the modulator begins to saturate due to the input. When in this state, the in band input signal converts. However, the noise floor rises significantly, affecting the parametric performance.

For the AD7768-1, the modulator input begins to saturate at $f_{MOD}/16$ for a full-scale sine wave, input signal. Figure 76 shows where the modulator is vulnerable to saturation if the input at higher frequencies is greater in amplitude than the maximum signal allowable to prevent modulator saturation. To protect against modulator saturation, a minimum of a first-order antialiasing filter is required at a −3 dB corner frequency of $f_{MOD}/16$.

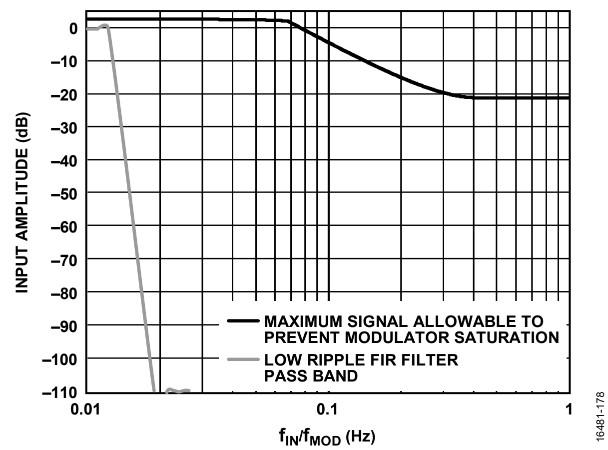

Figure 76. Modulator Saturation Area

Modulator Unprotected Zones

The AD7768-1 modulator samples on the rising and falling edge of f_{MOD} and outputs data to the digital filter at a rate of f_{MOD}. There is a zero in the frequency response profile of the modulator centered at odd multiples of f_{MOD}, which means that there is no foldback from frequencies at the f_{MOD} rate and at odd multiples of this rate. The fact that there is no foldback from frequencies at the f_{MOD} rate pushes the first unprotected zone of the AD7768-1 out to 2× f_{MOD}, which is a distinct advantage vs. traditional Σ-Δ ADCs.

However, the modulator is open to noise for even multiples of f_{MOD}. There is no attenuation at these zones. Figure 77 shows the modulator frequency response when using the low ripple FIR filter.

To protect against this additional noise, decide the level of attenuation to add to the analog signal path. A first-, second-, or third-order antialiasing filter may be required, depending on the environment of operation.

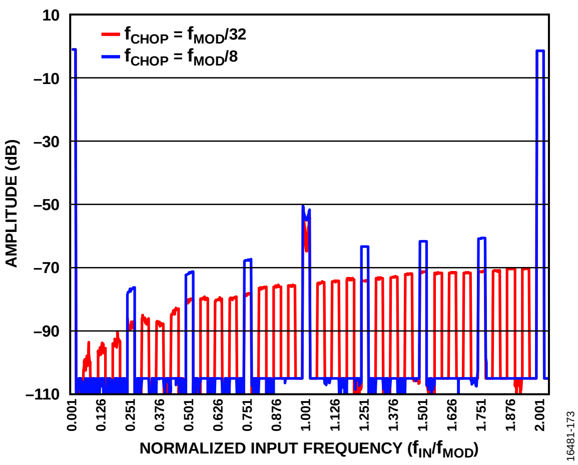

Figure 77. Rejection of Out of Band Tones

Modulator Chopping Frequency

The AD7768-1 uses a chopping technique in the modulator similar to that of a chopped amplifier to remove offset, offset drift, and 1/f noise.

The rate of chopping may result in out of band tones being aliased back to the bandwidth of interest. Figure 77 shows the rejection of out of band tones for both $f_{CHOP} = f_{MOD}/32$ (default) and $f_{CHOP} = f_{MOD}/8$. The $f_{CHOP} = f_{MOD}/8$ option is only available in SPI control mode. To protect against out of band tones aliasing back into the bandwidth of interest, the user must decide on the level of attenuation to add to the analog signal path. A first-, second-, or third-order antialiasing filter may be required, depending on the environment of operation. See the Antialiasing Filter Design Considerations section for more information.

GETTING STARTED

The AD7768-1 offers users a low power, small footprint, flexible measurement solution for ac and dc signal processing.

There are initial key decisions for the system designer to consider. At the highest level, these decisions are related to control mode, power mode, and digital filtering and decimation requirements.

Method of Configuration—$\overline{\text{PIN}}$ Control Mode or SPI Control Mode

The control mode is determined at power-up and is based on the logic level of the $\overline{\text{PIN}}$/SPI pin (tied to DGND or IOVDD). The two modes are SPI control mode and $\overline{\text{PIN}}$ control mode.

SPI control mode includes the following features:

- A superset of functions and flexibility.
- All the filters and ODR values.
- All the clock divide options to optimize the system clock frequency.
- Functional safety checking.
- Use of general-purpose input/outputs (GPIOs).
- Analog input and reference input buffer options.

$\overline{\text{PIN}}$ control mode includes the following features:

- MODEx pins that can be set to a desired fixed function. The device assumes this operation on power-up, and no further configuration is required.
- Three power modes.
- Three filter types.
- A subset of decimation rates.
- Analog input precharge buffers on by default.

SPI control offers the most flexibility, and $\overline{\text{PIN}}$ control is more suited to a fixed mode of operation, such as daisy-chaining multiple devices.

Digital Filter Type and Decimation

When selecting the digital filter type and decimate rate, consider

- The input bandwidth, filter profile requirement, or requirement for 50 Hz and/or 60 Hz rejection.
- The maximum noise target.
- The ODR requirement.

Power Mode

The selected power mode has a significant effect on the overall power consumption achievable. When selecting the power mode, consider the speed of conversion, input bandwidth, noise performance, and power consumption. In SPI control mode, select the MCLK_DIV setting for the sampling clock of the system. The power mode must be sufficient to support the modulator clock frequency settings. See Table 9 for the recommended power mode and f_{MOD} settings.

In $\overline{\text{PIN}}$ control mode, the power mode and clock divide pairings are predetermined as follow:

- Fast mode = MCLK/2
- Median mode = MCLK/4
- Low power mode = MCLK/16

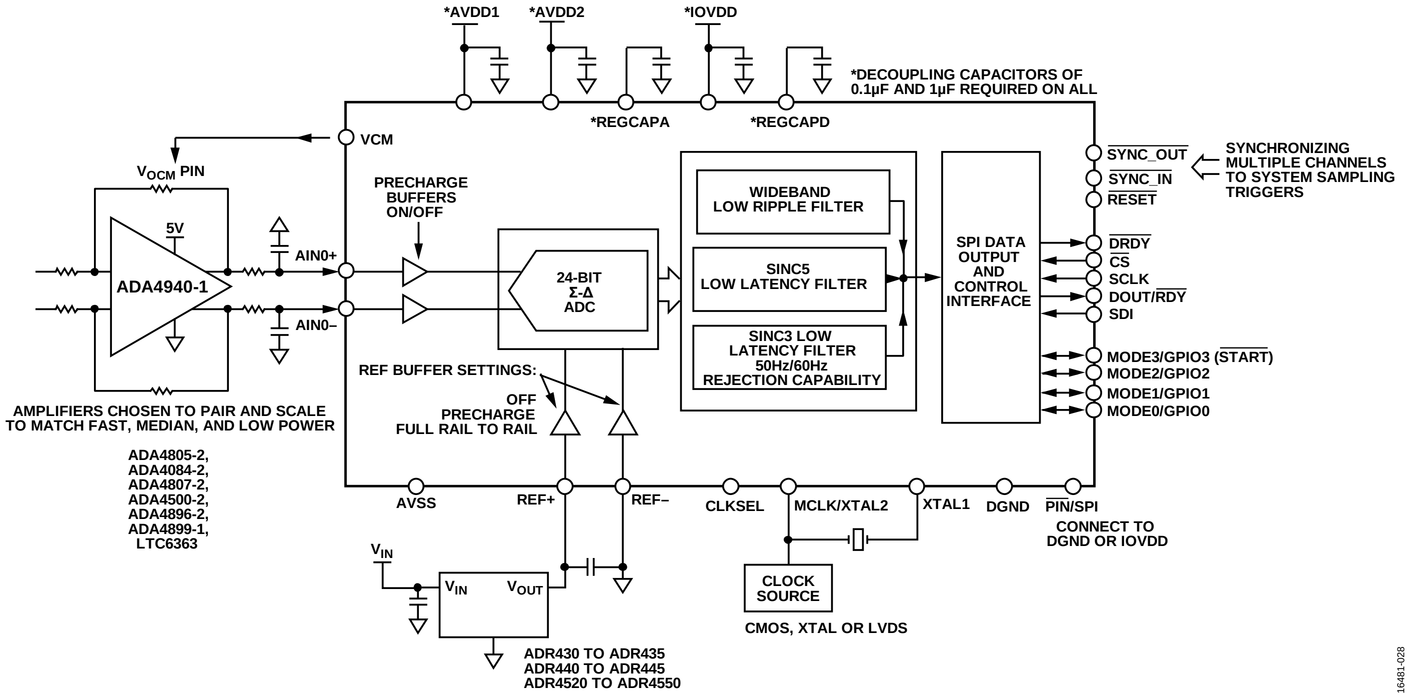

Figure 78. Typical Connection Diagram

Table 18. Operation Requirements for the AD7768-1 and the Options Available

Parameter	Description
Power Supplies	5.0 V AVDD1 supply, 2.0 V to 5.0 V AVDD2 supply, 1.8 V to 3.3 V IOVDD supply (ADP7104/ADP7118). In low power mode, the supplies can be configured for single 3 V operation as follows: AVDD1 = AVDD2 = IOVDD = 3.0 V to 3.3 V.
External Reference	2.5 V ADR4525, 4.096 V ADR4540, 5.0 V ADR4550.
External Driver Amplifier	The ADA4896-2, the ADA4940-2, the ADA4805-2, or the ADA4807-2.
External Clock	Crystal, CMOS, or LVDS clock for the ADC modulator sampling.
Microcontroller, FPGA, or DSP	Input/output voltage of 1.8 V to 3.3 V.

Table 19. Speed, Dynamic Range, THD, and Power Overview, Decimate by 32[1]

				Power Dissipation (mW)	
Power Mode	**ODR**	**Dynamic Range (dB)**	**THD (dB)**	**Low Ripple FIR Filter**	**Sinc Filter**
Fast	256 kSPS	108.5 (low ripple FIR filter)	−120	36.8	26.4
Median	128 kSPS	108.5 (low ripple FIR filter)	−120	19.7	14.4
Low Power	32 kSPS	108.5 (low ripple FIR filter)	−120	6.75	5.4

[1] Analog input precharge buffer on, reference precharge buffers on, and VCM disabled. Typical values are AVDD1 = 5.0 V, AVDD2 = 2.0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, MCLK = 16.384 MHz, and T_A = 25°C.

POWER SUPPLIES

The AD7768-1 has three independent power supply pins (AVDD1, AVDD2, and IOVDD). These pins are powered within the following ranges:

- AVDD1 = 5.0 V ± 10%, 2.5 V ± 10%, when AVSS = −2.5 V, and 3.3 V ± 10% (in low power mode only)
- AVDD2 = 2.0 V to 5.0 V
- IOVDD (with a regulator) = 1.8 V to 3.3 V

AVDD1 and AVDD2 are referred to AVSS, and IOVDD is referred to DGND.

The AVDD1 supply powers the analog front end, reference input, and common-mode output circuitry. AVDD1 is referenced to AVSS.

The AD7768-1 can be used with a ±2.5 V split supply configuration to enable converting a true bipolar input. When using split supplies, refer to the Absolute Maximum Ratings section, which describes the voltage allowed between the AVSS and IOVDD supplies. There is a limit on the tolerance in the voltage difference between IOVDD and AVSS.

The AVDD2 supply connects to an internal 1.8 V analog LDO regulator. This regulator powers the ADC core and enhances the PSRR. AVDD2 is referenced to AVSS. AVDD2 − AVSS can range from 5.5 V (maximum) to 2.0 V (minimum). For bipolar inputs, AVDD2 must remain within 5.5 V of the AVSS potential.

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and IOVDD − DGND can vary from 3.6 V (maximum) to 1.7 V (minimum).

Single-Supply Mode

The AD7768-1 can operate from a single 3.0 V supply rail in low power mode. This feature eliminates the inefficiency of generating multiply supply rails or applications where only a 3.0 V rail is available. The single-supply operation is limited to 3.3 V ± 10% and is available only when operating in low power mode.

The recommended compatible components for single-supply operation are the ADP7104-3.3 precision LDO, the ADR443 precision 3.0 V reference, and the ADA4807-2 or ADA4084-2 low power rail-to-rail input and output precision amplifiers.

Recommended Power Supply Configuration

Figure 79 shows the ADP2384/LT3470A stepping down the supply voltage efficiently while the ADP7118/LT3009 LDO provides a low noise voltage input. The ADP7118 or the LT3009 provide positive supply rails for optimal converter performance, creating either a single 5 V or 3.3 V or a dual AVDD1/IOVDD supply, depending on the required supply configuration. Alternatively, the ADP7118 or the LT3009 can operate from input voltages up to 20 V if the design is space constrained.

The LT3009 is an ideal component for a single channel design due to its small form factor.

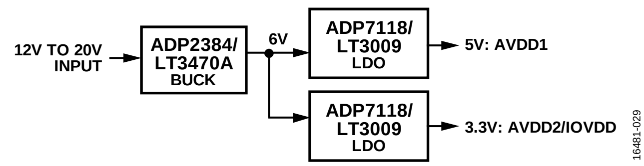

Figure 79. Power Supply Configuration

An alternative solution, which can save even more space in the system, is the LT6658. The LT6658 is a dual output, precision voltage reference that can also supply high current. The LT6658 can power both the analog supplies (AVDD1 and AVDD2) and be the reference input. The reference buffering options on the AD7768-1 can be used with this, if required. Figure 80 shows the LT6658 used in a system where AVDD1 is powered from Output 1 and the reference voltage for the AD7768-1 is taken from Output 2.

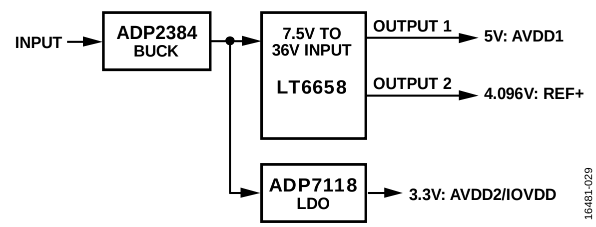

Figure 80. LT6658 Used as Both an AVDD1 Supply and Reference

DEVICE CONFIGURATION METHOD

The AD7768-1 has two options for controlling device functionality. On power-up, the mode is determined by the state of the PIN/SPI pin. The two modes of configuration are

- SPI: over a 3- or 4-wire SPI interface (complete configurability)
- PIN: pin strapped digital logic inputs (a subset of complete configurability)

On power-up, the user must apply a soft or hard reset to the device when using either control mode. A SYNC_IN pulse is also recommended after the reset or after any change to the device configuration. Choose between controlling and configuring over the SPI or via pin connections only.

The first design decision is setting the ADC in either the SPI or PIN mode of configuration. In either mode, the digital host reads the ADC data over the SPI port lines.

PIN Configuration

An overview of the PIN control mode features is as follows:

- No SPI write access to the device.
- Pins control all functions.
- ADC results read back over the SPI pins.

- ADC result includes an 8-bit status header output after each conversion result.
- SDI pin can be used to create a daisy chain of multiple devices operating in PIN mode.

SPI Control

An overview of the SPI control mode features is as follows:

- Standard SPI Mode 3 interface for register access, where the ADC always behaves as an SPI slave.
- Indication of a new conversion via the DRDY pin output. A second method allows the user to merge the ready signal within the DOUT output stream, which allows a reduction in the number of lines across an isolation barrier.
- Reading back conversions can be performed by writing 8 bits to address the ADC register and reading back the result from the register.
- Continuous readback mode, which is enabled via an SPI write. There is no need to supply the 8 bits to address the ADC_DATA register (Register 0x2C). Data readback occurs on the application of SCLK. The DRDY pin indicates that a conversion result is complete and can be used to trigger a readback of the conversion result.
- In continuous read back mode, there is the option to append either the 8-bit status header or an 8-bit CRC check, or both.

PIN CONTROL MODE OVERVIEW

PIN control mode eliminates the need for SPI communication to set the required mode of operation. For situations where the user requires a single, known configuration, reduce routing signals to the digital host. PIN control mode is useful in digitally isolated applications where minimal configuration is needed. PIN control mode offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In PIN control mode, the analog input precharge buffers and reference input precharge buffers are enabled by default for best performance.

An automatic sync pulse drives out on the SYNC_OUT pin in PIN control mode when the device is either initially powered up or after a reset. A SYNC_OUT pulse also occurs when a GPIOx pin toggles, meaning after a change to the PIN control mode settings of the device, the synchronization is automatically performed. For this synchronization to work, tie SYNC_OUT to SYNC_IN, eliminating the need to provide a synchronous SYNC_IN pulse. The SYNC_OUT of one device can also be tied to the SYNC_IN of many devices when the synchronization of multiple devices is required. If synchronization of multiple devices is required, all devices must share a common MCLK.

Power Mode

In PIN control mode, the device automatically scales the power mode of the ADC and divides the applied MCLK to a specified setting for that mode. Table 20 shows the modulator division for each power mode.

Table 20. Modulator Rate for PIN Control Mode

Power Mode	Modulator Rate, f_{MOD}
Fast	MCLK/2
Median	MCLK/4
Low Power	MCLK/16

In SPI control mode, separate register bits control the power mode of the ADC and MCLK division independently. Take care to follow the recommended settings in Table 9 if setting the power mode and modulator rate independently.

Data Output Format

PIN control mode has a set output format for conversion data. The rising DRDY edge indicates that a new conversion is ready. The next 24 serial clock falling edges clock out the 24-bit ADC result. The following eight serial clocks output the status bits of the AD7768-1. The ADC data is output MSB first in twos complement format. If further SCLK falling edges are applied to the ADC after clocking out the status bits, the logic level applied to SDI is clocked out, similar to a daisy-chain scenario. In Figure 81, an extra serial clock edge (33rd falling edge) is shown. If an extra serial clock edge occurs, the logic level of the SDI pin clocks out.

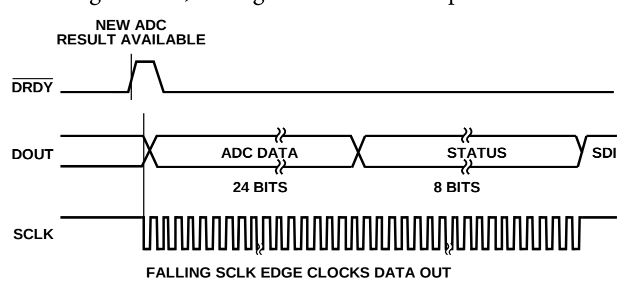

Figure 81. PIN Mode Data Output Format (This Figure Does Not Show the CS Signal)

Table 21. Differences in Control and Interface Pin Functions in PIN Control Mode and SPI Control Mode

	Pin Function	
Mnemonic	PIN Control Mode	SPI Control Mode
MODE0/GPIO0	MODE0 configuration pin	GPIO0 pin
MODE1/GPIO1	MODE1 configuration pin	GPIO1 pin
MODE2/GPIO2	MODE2 configuration pin	GPIO2 pin

Mnemonic	Pin Function	
	PIN Control Mode	SPI Control Mode
MODE3/GPIO3	MODE3 configuration pin	GPIO3 pin
CS	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the AD7768-1 via a register read/write and readback of the ADC conversion results
SCLK	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the AD7768-1 via a register read/write and readback of the ADC conversion results
SDI	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the AD7768-1 via a register read/write and readback of the ADC conversion results
DOUT/RDY	SPI pin for readback of ADC conversion results	SPI interface for full configuration of the AD7768-1 via a register read/write and readback of the ADC conversion results

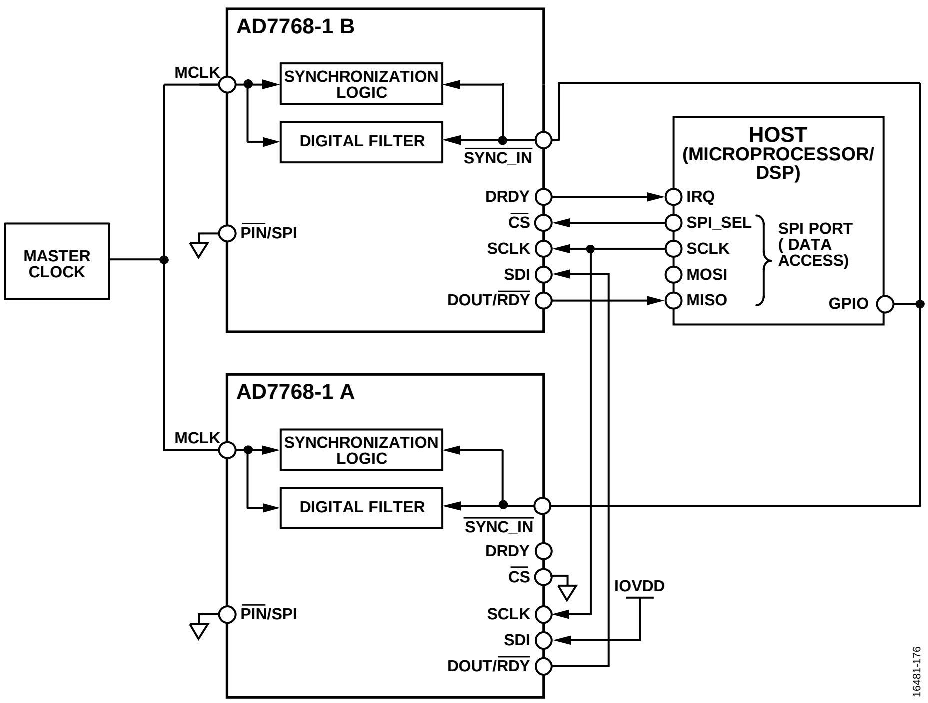

Figure 82. Daisy-Chaining Multiple AD7768-1 Devices

Diagnostics and Status Bits

PIN control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

The status header reports the internal CRC errors, memory map flipped bits, and the undetected external clock, indicating a reset is required. The status header also reports filter settled and filter saturated signals. Users can determine when to ignore data by monitoring these error flags.

If a significant error shows in the status bits, a reset of the ADC using RESET pin is recommended because, like in PIN mode, there is no way to interrogate further for specific errors.

Daisy-Chaining—PIN Control Mode Only

Daisy-chaining devices allows multiple devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7768-1 devices. Daisy-chaining devices is only possible in PIN control mode.

When configured for daisy-chaining, only one AD7768-1 device has its data interface in direct connection with the digital host. For the AD7768-1, cascading the DOUT/RDY pin of the upstream AD7768-1 device to the SDI pin of the next downstream AD7768-1 device in the chain implements this daisy-chaining. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the serial clock frequency used and the time available to clock through multiple 32-bit conversion outputs (24-bit conversion + 8-bit status) before the next conversion is complete.

The daisy-chaining feature is useful to reduce component count and to wire connections to the controller.

Figure 82 shows an example of daisy-chaining multiple AD7768-1 devices.

The daisy-chain scheme depends on all devices receiving the same MCLK and SCLK, being synchronized, and being configured with the same decimation rate. The chip select signal (CS) gates each conversion chain of data, its rising edge resetting the SPI to a known state after each conversion ripples through. The AD7768-1 device that is furthest from the controller must have its SDI pin tied to IOVDD, logic high.

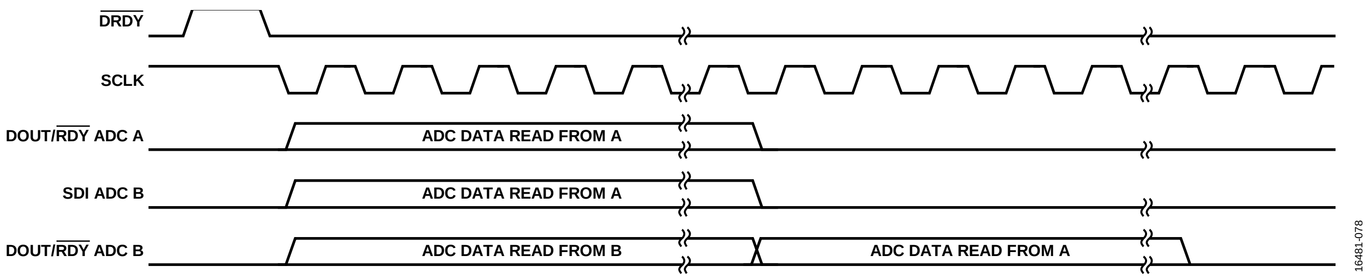

Figure 83. Data Output Format When Devices Daisy-Chained (PIN Control Mode Only)

Table 22. PIN Control Settings for MODEx Pins

MODEx Pin Settings					AD7768-1 Configuration			MCLK = 16.384 MHz
MODEx (Hex)	MODE3/ GPIO3	MODE2/ GPIO2	MODE1/ GPIO1	MODE0/ GPIO0	Power Mode	Filter	Decimation	ODR
0	0	0	0	0	Fast (MCLK/2)	Low ripple FIR	×32	256 kHz
1	0	0	0	1	Fast (MCLK/2)	Low ripple FIR	×64	128 kHz
2	0	0	1	0	Fast (MCLK/2)	Sinc5	×32	256 kHz
3	0	0	1	1	Fast (MCLK/2)	Sinc5	×64	128 kHz
4	0	1	0	0	Median (MCLK/4)	Low ripple FIR	×32	128 kHz
5	0	1	0	1	Median (MCLK/4)	Low ripple FIR	×64	64 kHz
6	0	1	1	0	Median (MCLK/4)	Sinc5	×32	128 kHz
7	0	1	1	1	Median (MCLK/4)	Sinc5	×64	64 kHz
8	1	0	0	0	Low power (MCLK/16)	Low ripple FIR	×32	32 kHz
9	1	0	0	1	Low power (MCLK/16)	Low ripple FIR	×64	16 kHz
A	1	0	1	0	Low power (MCLK/16)	Sinc5	×32	32 kHz
B	1	0	1	1	Low power (MCLK/16)	Sinc5	×64	16 kHz
C	1	1	0	0	Fast (MCLK/2)	Sinc5	×8	1 MHz
D	1	1	0	1	Fast (MCLK/2)	Sinc3 50 Hz and 60 Hz rejection[1]	×163,840	50 Hz
E	1	1	1	0	Low power (MCLK/16)	Sinc3 50 Hz and 60 Hz rejection[1]	×20,480	50 Hz
F	1	1	1	1	Standby			

[1] Sinc3 filter, rejection of 50 Hz and 60 Hz. Rejection of 50 Hz and 60 Hz is possible only if the MCLK applied in PIN control mode is equal to 16.384 MHz. The decimation rate is tuned internally for these pin mode settings so that the sinc filter notches fall at 50 Hz and 60 Hz.

SPI CONTROL OVERVIEW

SPI control offers a superset of flexibility and diagnostics to the user, and the categories described in Table 23 define the major controls, conversion modes, and diagnostic monitoring abilities enabled in SPI control mode.

Table 23. SPI Control Capabilities

SPI Control	Capabilities	Meaning for the User
Power Mode	Fast, medium, low power, standby, power down	The ability to scale power and save power with full control.
MCLK Division	MCLK/2 to MCLK/16	The ability to customize clock frequency relating to the bandwidth of interest.
MCLK Source	CMOS, crystal, LVDS, and internal clock	Allows the user a distributed or local clock capability.
Digital Filter Style	Sinc5, low ripple FIR, sinc3 (programmable)	The ability to customize the latency and frequency response to the measurement target of the user and its bandwidth.
Interface Format	Bit length	The ability to change between a 24-bit and a 16-bit conversion length in continuous read mode.
	Status bits	The ability to view output device status bits with the ADC conversion results.
	CRC	The ability to implement error checking when transmitting data.
	Data streaming	The ability to stream conversion data, eliminating interface write overhead.
Analog Buffers	Analog input precharge	Eases requirements on the ADC driver amplifier. Allows use of a lower power or lower bandwidth driver amplifier.
	Reference input precharge	Reduces reference input current, making it easier to filter the reference.
	Reference input full buffer	This full high impedance buffer enables filtering of reference source and enables high impedance sources, that is, reference resistors.
Conversion Modes	Single conversion	The ability to return to standby after one conversion.
	One shot	The ability to perform a conversion similar to a timed successive approximation register (SAR) conversion, in which the AD7768-1 converts on a timed pulse.
	Continuous conversion	Normal operation keeps the modulator continually converting, offering the fastest response to a change on the input.
	Duty-cycled conversion	The ability to save more power for point conversions. Times the rate of conversion and sets the time for the ADC to remain in standby after the conversion completes.
	Calibration	The ability to run a calibration of the system and to save gain calibration or offset calibration results to the system settings of the user by reading back from the gain/offset registers.
Conversion Targets	Analog inputs	The ability to measure the input signal applied at the analog input pins.
	Temperature sensor	The ability to measure local temperatures with an on-chip temperature sensor. Used for relative temperature measurement.
	Diagnostic sources	The ability to measure reference inputs and internal voltages for periodic functional safety checking.
GPIO Control	Up to four GPIOx pins	The ability to control other local hardware (such as gain stages),to power down other blocks in the signal chain, or read local status signals over the SPI interface of the AD7768-1.
System Offset and Gain Correction	System calibration routines	The ability to correct offset and/or gain by writing to registers when the environment changes (that is, the temperature increases). Requires characterization of system errors to feed these registers.
Diagnostics	Internal checks and flags	Users can have the highest confidence in the conversion results.

SPI CONTROL MODE

MCLK Source and MCLK Division

MCLK division bits control the divided ratio between the MCLK applied at the input to the AD7768-1 and the clock used by the ADC modulator. Select the division ratio best for configuration of the clocks.

The following options are available as the MCLK input source in SPI mode:

- LVDS
- External crystal
- CMOS input MCLK

Pulling CLOCK_SEL low configures the AD7768-1 for a CMOS clock. Pulling CLOCK_SEL high enables the use of an external crystal.

Pulling CLOCK_SEL high and setting Bits[7:6] of Register 0x15 enables the application of the LVDS clock to the MCLK pin. LVDS clocking is exclusive to SPI mode and requires the register selection for operation.

Power-Down Mode

Power-down mode has the lowest possible current consumption. All blocks on the ADC are turned off. A specific code is required to wake the ADC up. All register contents are lost when entering power-down mode. Disconnect all inputs to the ADC when entering power-down mode. See the power and clock control register (POWER_CLOCK), Register 0x15, for further details.

Standby Mode

Analog clocking and power functions are powered down. The digital LDO and register settings are retained when in standby mode. This mode is best used in scenarios where the ADC is not in use, briefly, and the user wants to save power.

SPI Synchronization

The AD7768-1 can be synchronized over the SPI. The final SCLK rising edge of the command is the instance of synchronization. This command initiates the SYNC_OUT pin to pulse active low and then back active high again. SYNC_OUT is a signal synchronized internally to the MCLK of the ADC. By connecting the output of SYNC_OUT to the SYNC_IN input, the user can synchronize that individual ADC. Routing SYNC_OUT to other AD7768-1 devices also ensures the devices are synchronized, as long as the devices share a common MCLK source.

It is recommended to perform synchronization functions directly after the DRDY pulse. If the AD7768-1 SYNC_IN pulse occurs too close to the upcoming DRDY pulse edge, the upcoming DRDY pulse may still be output because the SYNC_IN pulse has not yet propagated through the device.

When using the SYNC_OUT function with an IOVDD voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit to a one (Register 0x1D, Bit 6).

Offset Calibration

In SPI control mode, the AD7768-1 offers the ability to calibrate offset and gain. The user can alter the gain and offset of the AD7768-1 and its subsystem. These options are available in SPI control mode only.

The offset correction registers provide 24-bit, signed, twos complement registers for channel offset adjustment. If the channel gain setting is at the ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset calibration occurs before gain calibration, the LSB ratio of −4/3 changes linearly with gain adjustment via the gain correction registers.

Further register information and calibration instructions are available within the offset registers.

Gain Calibration

In SPI control mode, the user can alter the gain and offset of the AD7768-1 and its subsystem. These options are available in SPI control mode only.

The ADC has an associated gain coefficient that is stored for each ADC after factory programming. Nominally, this gain is approximately the 0x555555 value (for an ADC channel). The user can overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard coded, programmed factory setting.

$$Data = \left[\frac{3 \times V_{IN}}{V_{REF}} \times 2^{21} - (Offset)\right] \times \frac{Gain}{4} \times \frac{4{,}194{,}300}{2^{42}}$$

Further register information and calibration instructions are available within the gain registers.

Reset over SPI Control Interface

The user can issue a reset command to the AD7768-1 by writing to the SPI_RESET bits in the SYNC_RESET register. Two successive writes to these bits are required to initiate the device reset.

Resume from Shutdown

Shutdown mode features the lowest possible current consumption with all blocks on the device turned off, including the standard SPI interface. Therefore, to wake the ADC up from this mode, either a hardware reset on the RESET pin, or a specific code on the SPI SDI input, is required. The specific sequence required on SDI consists of a 1 followed by 63 zeros, clocked in by SCLK while CS is low, which allows the system to wake up the AD7768-1 from shutdown without using the RESET pin. This reset function is useful in isolated applications where the number of pins brought across the isolation barrier must be minimized.

GPIO and START Functions

When operating in SPI mode, the AD7768-1 has additional GPIO functionality. This fully configurable mode allows the device to operate four GPIOs. These pins can be configured as read or write in any order.

GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO. Then, this information can be read from the SPI interface of the AD7768-1.

The GPIOx pins can be set as inputs or outputs on a per pin basis, and there is an option to configure outputs as open-drain.

In SPI control mode, one of the GPIOx pins can be assigned the function of the START input. The START function allows a signal asynchronous to MCLK to be used to generate the SYNC_OUT signal to reset the digital filter path of the AD7768-1. The START pin function can be enabled on GPIO3.

SPI Mode Diagnostic Features

The AD7768-1 includes diagnostic coverage across the internal blocks. The diagnostics in the following list allow the user to monitor the ADC and to increase confidence in the fidelity of the data acquired:

- Reference detection
- Clock qualification
- CRC on SPI transaction
- Flags for detection of an illegal register write
- CRC checks
- POR monitor
- MCLK counter

In addition, these diagnostics are useful in situations where instruments require remote checking of power supplies and references during initialization stages.

The diagnostics are selectable by the user via enable registers. The flags for power-on reset (POR) and the clock qualification are on by default. The flags are readable via registers, but also ripple through to the top level status bits that can be output with each ADC conversion, if desired.

Reference Detection

Write 1 to Bit 3 of the ADC_DIAG_ENABLE register (Register 0x29) to enable the reference detection block in SPI control mode. When enabled, the error flags in the ADC_DIAG_STATUS register (Register 0x2F). Any error flags then propagate through to the MASTER_STATUS register (Register 0x2D). The reference error flags when the reference applied on the REF+ pin is below 1/3 of (AVDD1 − AVSS).

Clock Qualification

The clock qualification check attempts to detect when a valid MCLK is detected. When the MCLK applied is greater than 600 kHz, the clock qualification passes. The error flags in both the ADC_DIAG_STATUS register (Register 0x2F) and the MASTER_STATUS register (Register 0x2D). If the clock detected is below the 600 kHz frequency threshold, or if an external MCLK is not detected, the clock qualification error bit is set to 1. To disable the clock qualification check, write 0 to Bit 0 of the ADC_DIAG_ENABLE register (Register 0x29).

CRC on SPI Transaction

See the CRC Check on Serial Interface section for more details.

Flags for Detection of Illegal Register Write

See the SPI Control Interface Error Handling section for more details.

CRC Checks

Enable CRC checks in the DIG_DIAG_ENABLE register (Register 0x2A) to check the state of the memory map of the AD7768-1 and the internal random access memory (RAM) and fuse settings. If any of these errors flag on the device, perform a reset to return the device to a valid state.

POR Monitor

The POR monitor flag appears in both the MASTER_STATUS register and the status bits when output. The POR flag indicates that a reset or a temporary supply brown out occurred.

MCLK Counter

The MCLK_COUNTER register (Register 0x31) updates every 64 MCLKs. The MCLK counter register verifies that the AD7768-1 is still receiving a valid MCLK. Read the MCLK counter register according to the specific MCLK to SCLK ratio to ensure that a valid read occurs. The SCLK applied to read the MCLK_COUNTER register must not be less than 2.1 × MCLK or greater than 4.6 × MCLK. For example, if MCLK = 2 MHz, the SCLK applied cannot be in the 4.2 MHz to 9.2 MHz range. If the MCLK to SCLK ratio is not adhered to, the read may corrupt because the MCLK may update during the read of the register, causing an error.

Product Identification (ID) Number

The AD7768-1 contains ID registers that allow software interrogation of the silicon. The class of the product (precision ADC), product ID, device revision, and grade of device can all be read from the registry over the SPI. The vendor ID for Analog Devices, Inc., is also included in the registry for readback. These registers, in addition to a scratch pad that allows free reads from and writes to a specific register address, are methods of verifying the correct operation of the serial control interface.

Table 24. Product Identification Registers

Register (Hex)	Name	Bit Fields	
0x03	Chip type	Reserved	Class
0x04	Product ID [7:0]	PRODUCT_ID[7:0]	
0x05	Product ID [15:8]	PRODUCT_ID[15:8]	
0x06	Grade and revision	Grade	DEVICE_REVISION
0x0A	Scratch pad	Value	
0x0C	Vendor ID	VID[7:0]	
0x0D		VID[15:8]	

DIGITAL INTERFACE

The AD7768-1 has a 4-wire SPI interface. The interface operates in SPI Mode 3. In SPI Mode 3, SCLK idles high, the first data is clocked out on the first falling or drive edge of SCLK, and data is clocked in on the rising or sample edge. Figure 85 shows SPI Mode 3 operation where the falling edge of SCLK is driving out the data and the rising edge of SCLK is when the data is sampled.

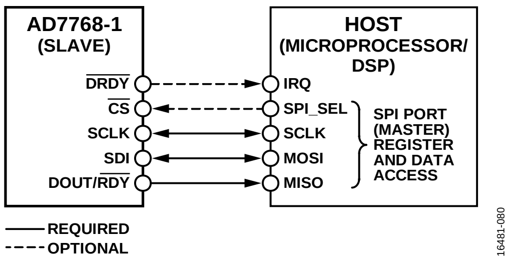

Figure 84. Basic Serial Port Connection Diagram

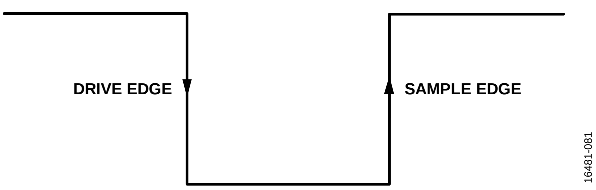

Figure 85. SPI Mode 3

SPI Reading and Writing

To use SPI control mode, set the PIN/SPI pin high. The SPI control operates as a 4-wire interface allowing read and write access. In systems where CS can be tied low, such as those requiring isolation, the AD7768-1 can operate in a 3-wire configuration. Figure 84 shows a typical connection between the AD7768-1 and the digital host. The corresponding 3-wire interface involves tying the CS pin low and using SCLK, SDI, and DOUT/RDY.

The format of the SPI read or write is shown in Figure 86. The MSB is the first bit in both read and write operations. An active low frame start signal (FS) begins the transaction, followed by the R/W bit that determines if the transaction being carried out is to a read (1) or a write (0). The next six bits are used for the address, and the eight bits of data to be written follow. All registers in the AD7768-1 are 8 bits in width, except for the ADC_DATA register (Register 0x2C), which is 24 bits in width. In the case where CS is tied low, the last SCLK rising edge completes the SPI transaction and resets the interface. When reading back data with CS held low, it is recommended that SDI idle high to prevent an accidental reset of the device where SCLK is free running (see the Reset section).

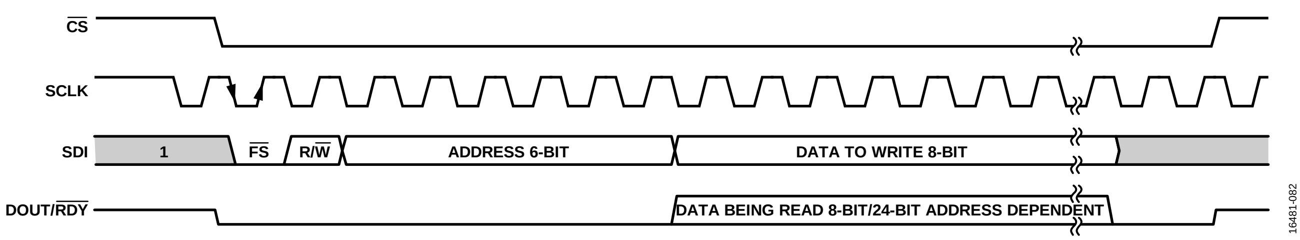

Figure 86. SPI Basic Read/Write Frame

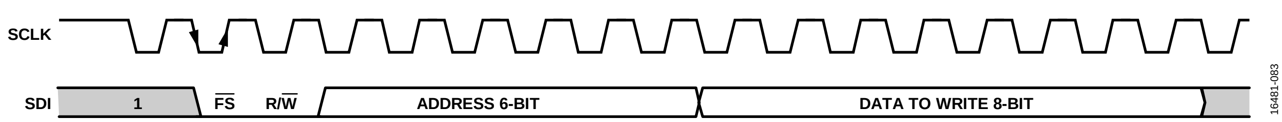

Figure 87. 3-Wire SPI Write Frame (CS = 0)

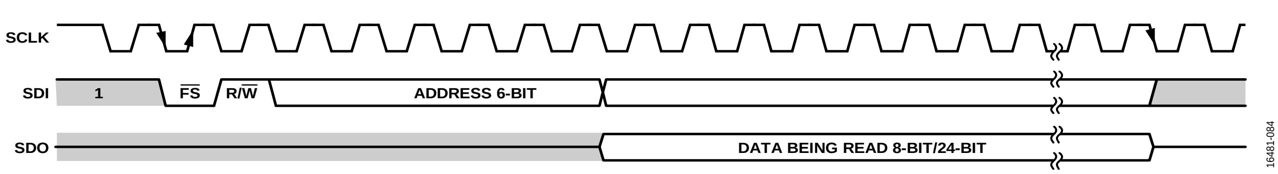

Figure 88. 3-Wire SPI Read Frame (CS = 0)

SPI Control Interface Error Handling

The AD7768-1 SPI control interface detects if an illegal command is received. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the AD7768-1, error bits are set in the SPI_DIAG_STATUS register (Register 0x2E).

Five sources of SPI error can be detected. These detectable error sources must be enabled in the SPI_DIAG_ENABLE register (Register 0x28). Only the EN_ERR_SPI_IGNORE (Bit 4) error is enabled on startup.

The five detectable sources of SPI error are as follows:

- SPI CRC error. This error occurs when the received CRC/XOR does not match the calculated CRC/XOR.
- SPI read error. This error occurs when an incorrect read address is detected (for example, when the user attempts to access a register that does not exist).
- SPI write error. This error occurs when a write to an incorrect address is detected (for example, when the user attempts to write to a register that does not exist).
- SPI clock count error. When the SPI transaction is controlled by $\overline{CS}$, this error flags when the SPI clock count during the frame is not equal to 8, 16, 24, 32, or 40. This error can be detected in both continuous read mode and normal SPI mode.
- SPI ignore error. This error flags when an SPI transaction is attempted before initial power-up completes.

All SPI errors are sticky, meaning they can only be cleared if the user writes a 1 to the corresponding error location.

CRC Check on Serial Interface

The AD7768-1 can deliver up to 40 bits with each conversion result, consisting of 24 bits of data and eight status bits, with the option to add eight further CRC/XOR check bits in SPI mode only.

The status bits default per the description in the Status Header section. The CRC functionality is available only when operating in SPI control mode. When the CRC functionality is in use, the CRC message is calculated internally by the AD7768-1. The CRC is then appended to the conversion data and the optional status bits.

The AD7768-1 uses a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

To generate the checksum, shift the data by eight bits to create a number ending in eight Logic 1s.

The polynomial is aligned such that the MSB is adjacent to the leftmost Logic 1 of the data. Apply an exclusive OR (XOR) function to the data to produce a new, shorter number. The polynomial is again aligned such that the MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, which is the 8-bit checksum.

If enabled, the SPI writes always use CRC, regardless of whether the XOR option is selected in the INTERFACE_FORMAT register (Register 0x14). The initial CRC checksum for SPI transactions is 0x00, unless reading back data in continuous read mode, in which case the initial CRC is 0x03.

If using the XOR option in continuous read mode, the initial value is set to 0x6C. The XOR option is only available for SPI reads.

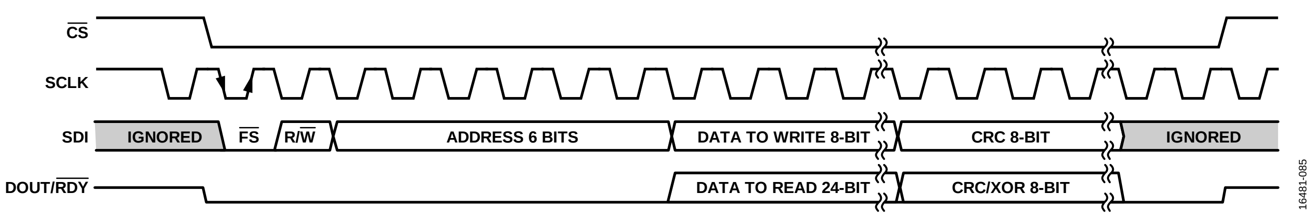

Figure 89. Data Output Format When Using CRC

Conversion Read Modes

The digital interface of the AD7768-1 is a 4-wire SPI implementation operating in Mode 3 SPI. An 8-bit write instruction is needed to access the memory map address space. All registers are eight bits wide, with the exception of the ADC data register. The AD7768-1 operates in a continuously converting mode by default. The user must decide whether to read the data. Two read modes are available to access the ADC conversion results: single-conversion read mode and continuous read mode

Single-read mode is a basic SPI read cycle where the user must write an 8-bit instruction to read the ADC data register. The status register must be read separately, if needed

Write a 1 to the LSB of the INTERFACE_FORMAT register to enter continuous read mode. Subsequent data reads do not require an initial 8-bit write to query the ADC_DATA register. Simply provide the required number of SCLKs for continuous readback of the data. Figure 90 shows an SPI read in continuous read mode.

Key considerations for users on the interface are as follows:

- Conversion data is available for readback after the rising edge of $\overline{\text{DRDY}}$. In continuous read mode, the $\overline{\text{RDY}}$ function can be enabled, and the $\overline{\text{DRDY}}$ function can be ignored. Data is available for readback on the falling edge of $\overline{\text{RDY}}$.
- The ADC conversion data register is updated internally 1 MCLK period prior to the rising $\overline{\text{DRDY}}$ edge.
- MCLK has a maximum frequency of 16.384 MHz.
- SCLK has a maximum frequency of 20 MHz.
- The $\overline{\text{DRDY}}$ high time is $1 \times t_{MCLK}$
- In fast power mode, decimate by 32, the $\overline{\text{DRDY}}$ period is ~4 µs, the fastest conversion can have a $\overline{\text{DRDY}}$ period of 1 µs.
- The $\overline{\text{CS}}$ rising edge resets the serial data interface. If $\overline{\text{CS}}$ is tied low, the final rising SCLK edge of the SPI transaction resets the serial interface. The point at which the interface is reset corresponds to 16 × SCLKs for a normal read operation and up to 40 SCLKs when reading back ADC conversion data, plus the status and CRC headers.

Single-Conversion Read Mode

When using single-conversion read mode, the ADC_DATA register can be accessed in the same way as a normal SPI read transaction. The ADC_DATA register (Register 0x2C), is 24 bits wide. Therefore, 32 SCLKs are required to read a conversion result.

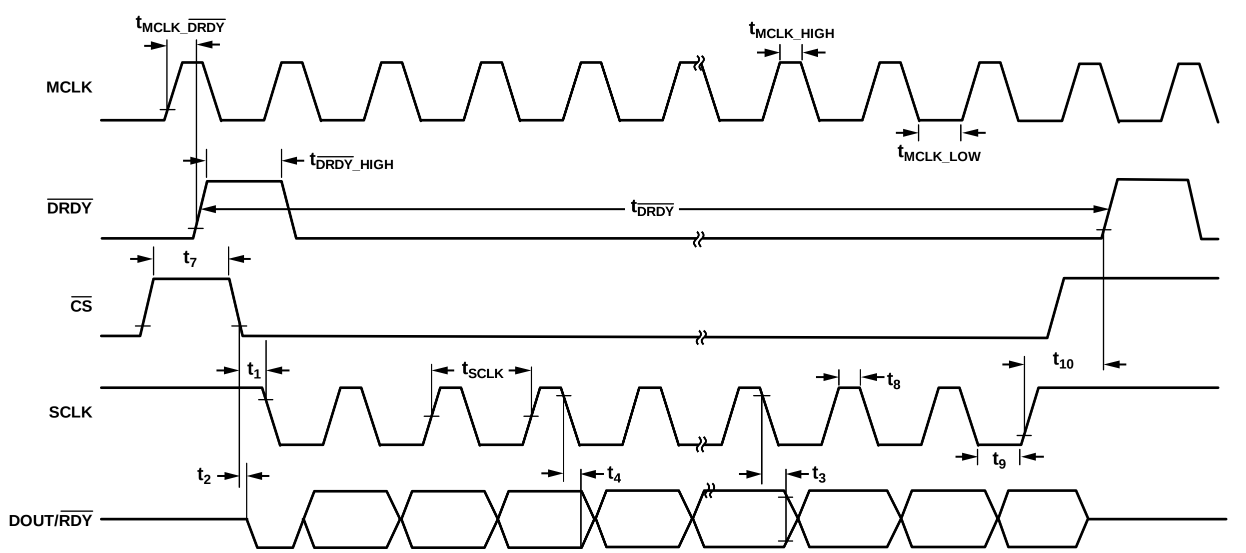

Figure 90. Serial Interface Timing Diagram, Example Reflects Reading an ADC Conversion in Continuous Read Mode

Continuous Read Mode

To eliminate the overhead of needing to write a command to read the ADC data register each time, the user can place the ADC in continuous read mode so that the ADC register can be read directly after the data ready signal is pulsed. In continuous read mode, data is output on the falling edge of the first SCLK received. Therefore, only 24 SCLKs are required to read a conversion. In this continuous read mode, it is also possible to append one or both of the status or CRC headers (eight bits each) to the conversion result. If both the status and CRC headers are enabled, the data format is ADC data + status bits + CRC.

When the $\overline{\text{RDY}}$ function is not used, the ADC conversion result can be read multiple times in the $\overline{\text{DRDY}}$ period, as is shown in Figure 91. When the $\overline{\text{RDY}}$ function is enabled, the DOUT/$\overline{\text{RDY}}$ pin goes high after reading the AD7768-1 conversion result and, therefore, the data cannot be read more than once (see Figure 92).

Continuous readback is the readback mode used in $\overline{\text{PIN}}$ control mode. However, in this mode, the data output format is fixed. There is no option for $\overline{\text{RDY}}$ on the DOUT pin. See the Pin Control Mode Overview section for more details.

When using continuous read mode with the LV_BOOST bit enabled (Bit 7 in the INTERFACE_FORMAT register, Register 0x14), it is necessary to re-enable LV_BOOST each time continuous read mode is exited.

Exiting Continuous Read Mode

To exit continuous read mode, write a key of 0x6C on the SDI, which allows access to the register map one more time and allows further configuration of the device. To comply with a normal SPI write, use the $\overline{\text{CS}}$ signal to reset the SPI interface after this key is entered. If $\overline{\text{CS}}$ cannot be controlled and is permanently held low, 16 SCLKs are needed to complete the transaction so that the SPI interface remains synchronized. For example, when $\overline{\text{CS}}$ is permanently tied low, write 0x006C to exit continuous read mode when using the 3-wire version of the interface. The exit command must be written between $\overline{\text{DRDY}}$ pulses to ensure that the device exits correctly.

A software reset can also be written in this mode in the same way as the exit command, but by writing 0xAD instead of 0x6C.

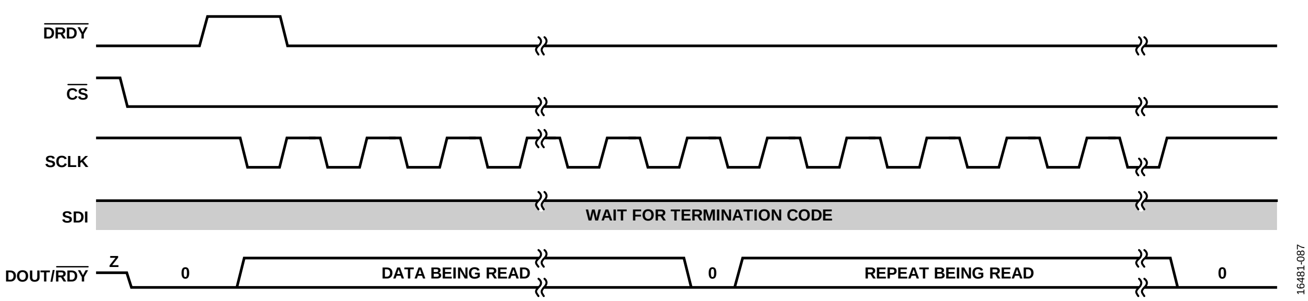

Figure 91. Continuous ADC Read Data Format with $\overline{\text{RDY}}$ Function Disabled

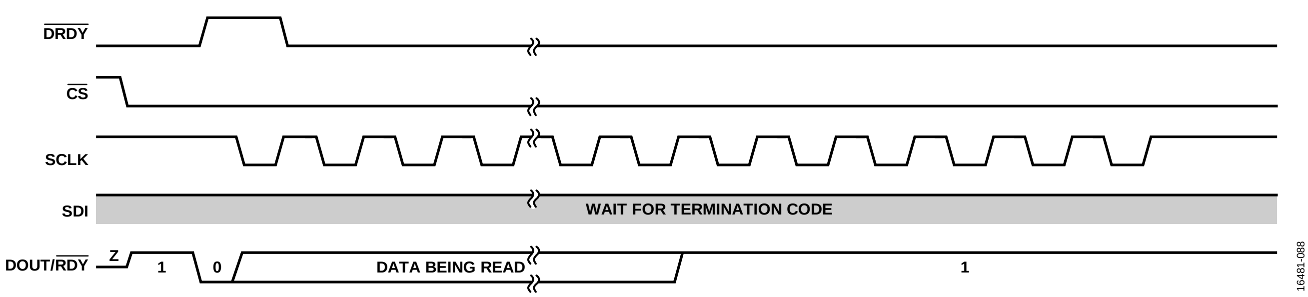

Figure 92. Continuous ADC Read Data Format with $\overline{\text{RDY}}$ Function Enabled on the DOUT/$\overline{\text{RDY}}$ Pin

DATA CONVERSION MODES

The four data conversion modes available in SPI control mode are as follows:

- Continuous conversion
- One shot conversion
- Single conversion
- Duty cycled conversion

The default conversion mode is continuous conversion. A SYNC_IN pulse must be provided to the AD7768-1 after any change to the configuration of the device, including changing filter settings and data conversion modes.

Continuous Conversion Mode

In continuous conversion mode, the ADC continuously converts and a new ADC result is ready at an interval determined by the ODR, which is the default conversion operation in SPI control mode. This is the only data conversion mode in which the wide-band filter is available. Two methods of data readback are available to the user in SPI control mode and are described in the Conversion Read Modes section.

One Shot Conversion Mode

Figure 93 shows the device operating in one shot conversion mode. In this mode, conversions occur on request by the master device, for example, the DSP or FPGA. The SYNC_IN pin receives the command initiating the data output.

In one shot conversion mode, the ADC runs continuously. However, the SYNC_IN pin rising controls the point in time from which data is output.

To receive data, the master device must pulse the SYNC_IN pin, which resets the filter and forces DRDY low. DRDY subsequently goes high to indicate to the master device that the device has valid settled data available.

When the master asserts SYNC_IN and the AD7768-1 receives the rising edge of this signal, the digital filter is reset, the full settling time of the filter elapses before the data is settled, and the output is available. The duration of the settling time depends on the filter path and decimation rate. One shot conversion mode is only available for use with the sinc5 or sinc3 filters because these filters feature a minimal settling time. Continuous conversion mode is not available as an option for use with the low ripple FIR filter.

When settled data is available, the DRDY signal pulses. The time from the SYNC_IN signal until the ADC path settled data ($t_{SETTLED}$) is shown in Figure 93. After settled data is available, DRDY is asserted high, and the user can read the conversion result. The device then waits for another SYNC_IN signal before outputting more data.

The settling time is calculated relative to the settling time of the filter used, with some added latency for starting the one shot conversion. This settling time limits the overall throughput achievable in one shot conversion mode.

Because the ADC is sampling continuously, one shot conversion mode affects the sampling theory of the AD7768-1. Periodically sending a SYNC_IN pulse to the device is a form of subsampling of the ADC output. The bandwidth around this subsampling rate can now alias down to the baseband. Consider keeping the SYNC_IN pulse synchronous with the master clock to ensure coherent sampling and to reduce the effects of jitter on the frequency response, which otherwise heavily distort the output.

Any SPI configuration of the AD7768-1 required is performed in continuous conversion mode before switching back to one shot conversion mode.

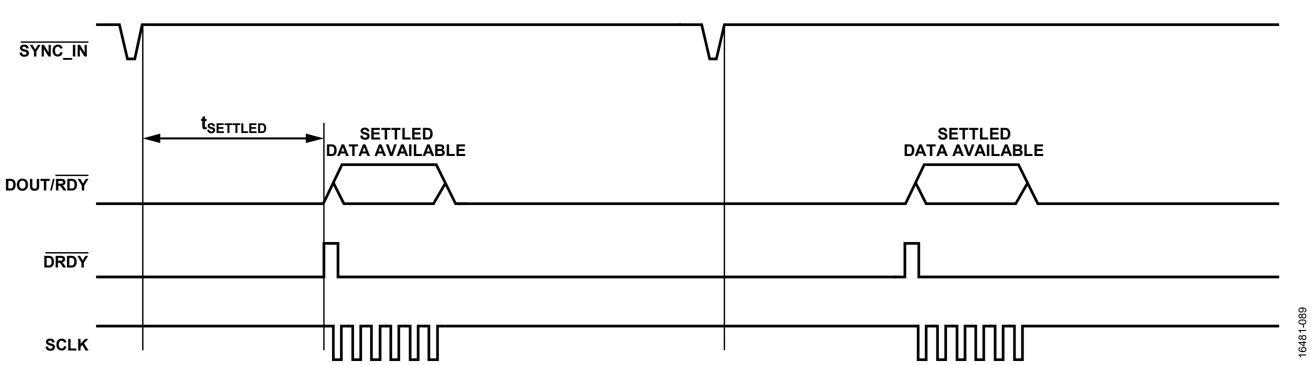

Figure 93. One Shot Conversion Mode, SYNC_IN Pin Driven with an External Source

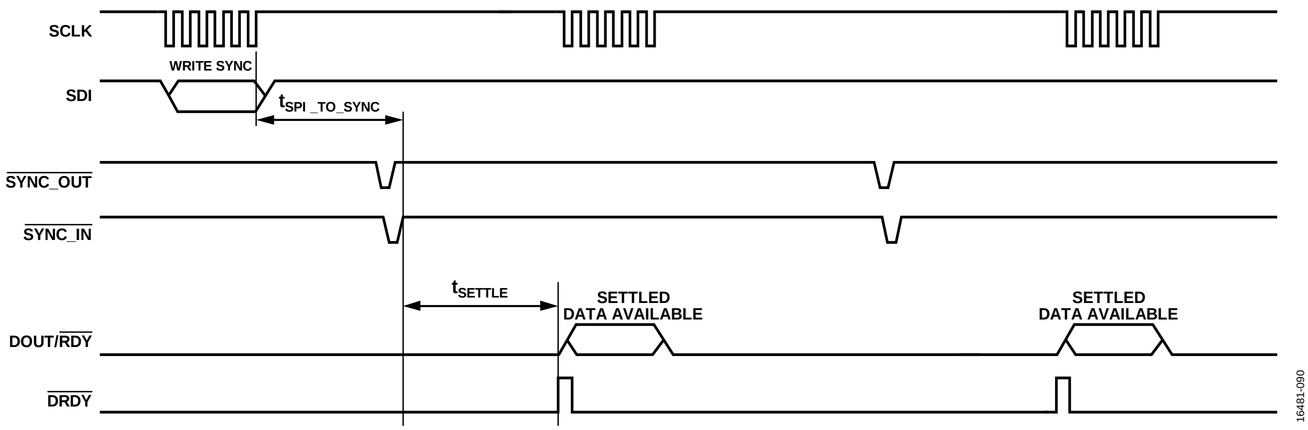

Figure 94. One Shot Conversion Mode, SYNC_IN Pulse Initiated by a Register Write

Single-Conversion Mode

In single-conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. Only use single-conversion mode when operating in low power and median power modes. The user must send a command to initiate the read and subsequently read back the ADC conversion result. Use a toggle of the SYNC_IN pin to exit the device from standby and to start a new conversion.

Any SPI configuration of the AD7768-1 required must be performed in continuous conversion mode before then switching back to single-conversion mode.

Duty Cycled Conversion Mode

In duty cycled conversion mode, the ADC wakes up from standby, performs a conversion, and then returns to standby. The user can set the period between each conversion, and the ADC automatically performs the single conversion before returning to standby, repeating the single conversion performed by the ADC at a period specified by the user. Only use duty cycled conversion mode when operating in low power and median power modes. Duty cycled conversion mode allows a method to reduce the power consumption for dc point conversions, and to eliminate any overhead in timing and initiating the conversion.

Use a toggle of the SYNC_IN pin to begin the duty cycled conversion mode sequence. DRDY toggles once when a settled result is reached. Then, the device enters standby one more time. The DUTY_CYCLE_RATIO register controls the determined idle time.

Any SPI configuration of the AD7768-1 required must be performed in continuous conversion mode before switching back to duty cycled conversion mode.

SYNCHRONIZATION OF MULTIPLE AD7768-1 DEVICES

An important consideration when using multiple AD7768-1 devices in a system is synchronization. The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal. A SYNC_IN pulse must be provided to the AD7768-1 both after power-up and after any change to the configuration of the device. This pulse serves to flush out the digital filters and ensures that the device is in a known configuration, as well as synchronizing multiple devices in a system.

The AD7768-1 offer three options to ease system synchronization. Choosing between the options depends on the system. However, the most basic consideration is whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

If a signal that is synchronous to the base MCLK signal cannot be provided, use one of the following methods:

- Configure the GPIOx pin of one of the AD7768-1 devices in the system to be a START input. Apply a START pulse to the configured GPIOx pin. Route the SYNC_OUT pin output to the SYNC_IN input of that same device and all other devices that are to be synchronized.
- The AD7768-1 samples the asynchronous START pulse and generates a SYNC_OUT pulse related to the base MCLK signal for local distribution.
- Use synchronization over SPI (only available in SPI control mode). Write a synchronization command to one predetermined ADC device. Connect the SYNC_OUT pin of this device to its own SYNC_IN pin and to the SYNC_IN pin of any other device locally. Similar to the START pin method, the SPI synchronization is received by one device and, subsequently, the SYNC_OUT signal is routed to local devices to allow synchronization.

If a SYNC_IN signal synchronous to the base MCLK can be provided, apply the SYNC_IN synchronous signal to the SYNC_IN pin from a star point and connect directly to the pin of each AD7768-1 device. The SYNC_IN signal is sampled on the rising MCLK edge and, therefore, setup and hold times are associated with the SYNC_IN input relative to the AD7768-1 MCLK rising edge (see Figure 7).

In this case, SYNC_OUT is redundant and can remain open-circuit or tied to IOVDD. GPIOx can be used for a different purpose because it is not required for the START function. Synchronization in channel to channel isolated systems is shown in Figure 95. Synchronization can be carried out through an SPI transaction for the setup shown in Figure 95. If a precise SYNC_IN pulse is required, additional isolation channels may be required.

It is recommended to perform synchronization functions directly after the DRDY pulse. If the AD7768-1 SYNC_IN pulse occurs too close to the upcoming DRDY pulse edge, the upcoming DRDY pulse may still be output because the SYNC_IN pulse has not yet propagated through the device.

When using the SYNC_OUT function with an IOVDD voltage of 1.8 V, it is recommended to set the SYNC_OUT_POS_EDGE bit (Register 0x1D, Bit 6) to 1.

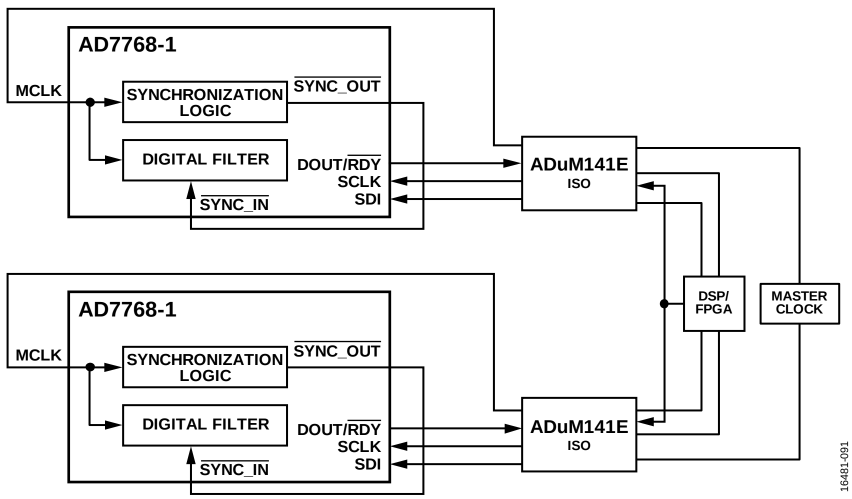

Figure 95. Synchronization in Channel to Channel Isolated Systems

ADDITIONAL FUNCTIONALITY OF THE AD7768-1

Reset

After powering up the device, it is recommended to perform a full reset. There are multiple options available on the AD7768-1 to perform a reset, including

- Using the dedicated $\overline{\text{RESET}}$ pin. See the Pin Configuration and Function Descriptions section.
- When in continuous read mode, the AD7768-1 monitors for the exit command or a reset command of 0xAD. See the Exiting Continuous Read Mode section for more details.
- A software reset can be performed by two consecutive writes to the SYNC_RESET register (Register 0x1D).
- When $\overline{\text{CS}}$ is held low, it is possible to provide a reset by clocking in a 1 followed by 63 zeros on SDI, which is the SPI resume command reset function used to exit power-down mode.

The time taken from $\overline{\text{RESET}}$ to an SPI write must be at least 200 µs.

Status Header

In SPI control mode, the status header can be output after the conversion result when operating the AD7768-1 in continuous read back mode. The status header mirrors the MASTER_STATUS register (Register 0x2D).

In $\overline{\text{PIN}}$ control mode, the status header is output by default after the conversion result. The status header contains the following bits and functions:

- The MASTER_ERROR bit is an OR of all other errors present and can be monitored to provide a quick indication of a problem having occurred.
- The ADC_ERROR bit sets to 1 if any error is present in the ADC_DIAG_STATUS register (Register 0x2F). It is an OR of the error bits in the ADC_DIAG_STATUS register.
- The DIG_ERROR bit sets to 1 if any error is present in the DIG_DIAG_STATUS register (Register 0x30). It is an OR of the error bits in the DIG_DIAG_STATUS register.
- The ADC_ERR_EXT_CLK_QUAL bit sets if a valid clock is not detected (see the Clock Qualification section).
- The ADC_FILT_SATURATED bit sets to 1 if the digital filter is clipped on either positive or negative full scale. The clipping can be caused by the analog input exceeding the analog input range, or by a large step input to the device that causes a large overshoot in the digital filter. In addition, the filter may saturate if the ADC gain registers are incorrectly set. The combination of a full-scale signal and a large gain saturates the digital filter.
- The ADC_FILT_NOT_SETTLED bit is set to 1 if the output of the digital filter is not settled. The digital filters are cleared following a RESET pulse, or after a SYNC_IN command is received. Table 13, Table 16, and Table 17 list the time for SYNC_IN to settled data for each filter type. When using the low ripple FIR filter, the filter not settled bit takes longer to update and propagate through the device than to read the status header. The filter not settled bit appears set when in fact the data output is settled. The worst case update delay is 128 MCLK cycles for the low ripple, wideband filter, decimate by 1024 setting. In this case, if the readback is delayed by 128 MCLK cycles, the filter not settled bit has time to update, and the time to settled data is equal to the data shown in Table 13, Table 16, and Table 17.
- The SPI_ERROR bit sets to 1 if any error is present in the SPI_DIAG_STATUS register (Register 0x2E). The bit is an OR of the error bits in the SPI_DIAG_STATUS register.
- The POR_FLAG bit detects if a reset or a temporary supply brown out occurred. In $\overline{\text{PIN}}$ control mode, instead of being the POR flag, this bit is always set to 1 and then detects if that the interface is operating correctly.

Diagnostics

Internal diagnostics are available on the AD7768-1 that allow the user to check both the functionality of the ADC and the environment in which the ADC is operating. The internal diagnostics are enabled in the conversion register (Register 0x18). To use the diagnostics, the device must be configured to low power mode, MCLK_DIV = MCLK/16, and the analog input precharge buffers must be enabled. The diagnostics available are as follows:

- The temperature sensor is an on-chip temperature sensor that determines the approximate temperature. Temperature changes measured give approximately a 0.6 mV/°C change in the dc converted voltage. For example, at ambient temperature, the conversion result is approximately 180 mV. A 50°C increase in temperature reads back as approximately 210 mV, signaling, for example, a potential fault or the need to calibrate the system.
- The analog input short disconnects the AIN+ and AIN− pins from the external input and creates an internal short across the analog input pins that can detect a fault.
- The voltage converted is V_{REF+} for positive full scale, if selected.
- The voltage converted is V_{REF-} for negative full scale, if selected.

APPLICATIONS INFORMATION

ANALOG INPUT RECOMMENDATIONS

The design of the AD7768-1 analog input circuitry has a significant effect on the overall performance of the system. The AD7768-1 incorporates precharge buffers on the analog inputs to aid the driver amplifier. Enabling the analog input precharge buffers allows a lower power amplifier to be used to drive the AD7768-1. See the Analog Inputs and Precharge Buffering section for more details.

Recommended Driver Amplifiers

Depending on the required input bandwidth to the ADC, or the power consumption considerations of the overall system, there are a range of amplifiers suitable to be paired with the AD7768-1 for a particular power mode.

Table 25 describes the recommended driver amplifiers for the AD7768-1 based on the power mode selected. Each power mode selected ultimately corresponds to a modulator frequency and a maximum ODR. The driver amplifiers are selected for their suitability to settle the analog inputs for a particular power mode. The settings for both Table 25 and Table 26 are MCLK frequency = 16.384 MHz, input = 1 kHz, an applied tone of −0.5 dBFS, and a low ripple FIR filter is selected.

Table 26 shows the benefits of the analog input precharge buffers. In this case, the ADA4807-2 is the ADC driver chosen to drive the AD7768-1 in fast power mode. Enabling the precharge buffers gives more than a 20 dB improvement in THD, allowing the amplifier to become a valid choice of the driver at the fastest data rate. See Application Note AN-1384 for how to pair a range of suitable driver amplifiers with the AD7768-1.

Table 25. Amplifier Pairing Options for Various Power Modes for the Low Ripple FIR Filter

AD7768-1 Power Mode	Amplifier	Analog Input Precharge Buffer	SNR (dB)	THD (dB)
Fast	ADA4945-1	On	106.0	−120.7
	ADA4896-2	On	106	−119.9
Median	ADA4807-2	Off	105.7	−121.3
	ADA4805-2	Off	106.2	−119.8
	ADA4945-1	Off	106.7	−117.7
Low Power	ADA4805-2	Off	105.8	−120.5
	LTC6363	Off	105.6	−120

Table 26. Benefits of the Analog Input Precharge Buffers

AD7768-1 Power Mode	Amplifier	Analog Input Precharge Buffer	SNR (dB)	THD (dB)
Fast	ADA4807-2	Off	105.1	−104
	ADA4807-2	On	104.9	−124.5

ANTIALIASING FILTER DESIGN CONSIDERATIONS

When designing the antialiasing filter for the AD7768-1, the modulator aliasing zones due to the modulator chopping (see the Antialiasing Filtering section) must be considered. If the environment in which the AD7768-1 operates is subject to large out of band tones at the input, the order of the antialiasing filter is critical. Figure 96 shows the roll-off for the input antialiasing filter from a simple second-order implementation to a more complex fourth-order roll-off. It is assumed in Figure 96 that the filter corner frequency is set at ¾ × ODR for the decimate by 32 setting. Setting the corner frequency at ¾ × ODR means that the flat pass band of the low ripple FIR filter can be maintained while also maximizing rejection at f_{MOD} and 2 × f_{MOD}. To prevent out of band tones appearing in band, at least a third-order antialiasing filter is needed to fully reject tones at 2 × f_{MOD}.

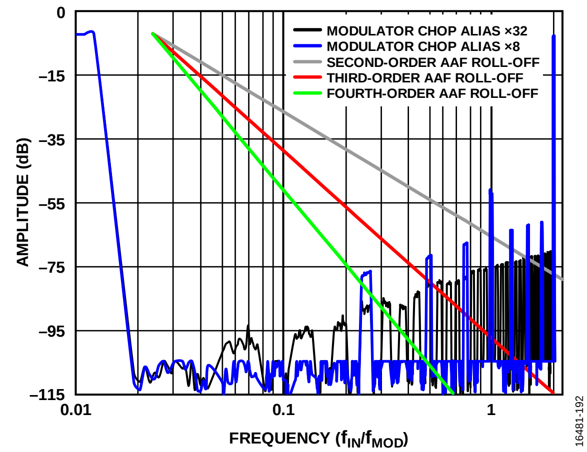

Figure 96. Combined Digital and Analog Filter Response for Various Orders of the Analog Antialiasing Filter

One method of designing a third-order antialiasing filter is to use a multiple feedback architecture, as shown in Figure 97. Only one active component, the ADA4940-1 in the case of Figure 97, is needed to achieve a third-order roll-off response. The input to the ADA4940-1 is typically an instrumentation amplifier, such as the AD8421, for precision dc applications. This circuit can be tuned for a particular input range, noise, or power requirement, as necessary.

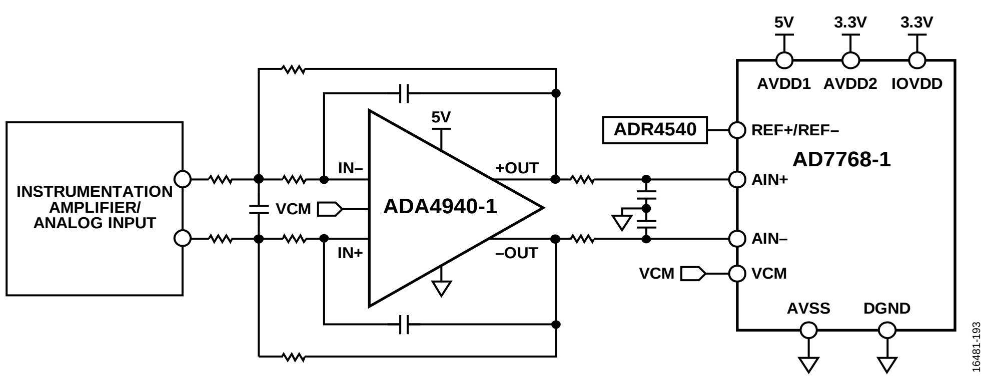

Figure 97. Implementation of a Multiple Feedback, Low-Pass Filter

RECOMMENDED INTERFACE

The AD7768-1 interface is flexible to allow the many modes of operation and for data output formats to work across different DSPs and microcontroller units (MCUs). To achieve maximum performance, the recommended interface configuration for reading conversion results is shown in Figure 98. This recommended implementation uses a synchronous SCLK to MCLK relationship.

Configure the interface as follows to achieve the recommended operation:

1. Tie the CS signal low during the conversion readback.
2. Enter continuous readback mode to avoid needing to provide the address bits for the ADC_DATA register. Continuous readback mode is the default readback mode in PIN mode.
3. 32 bits of data are clocked out, consisting of the 24-bit conversion result plus eight bits that can be selected to be either the status or CRC bits. In PIN mode, this is always the conversion result plus the eight status bits.
4. Provide an SCLK that is a divided down version of MCLK. For example, SCLK = MCLK/2 in a case where decimate by 32 is selected.
5. Clocking 32 bits ensures that the data readback operation fills the entire DRDY period when SCLK = MCLK/2. SCLK runs continuously. The readback spans the full DRDY period, thus spreading the dynamic current needed on IOVDD across the full ODR period.
6. The DRDY signal can synchronize the data being read into the host controller.

Figure 98 shows how the recommended interface operates. The data read back spans the entire length of the DRDY period and the LSB remains until DRDY goes high for the next conversion.

Initializing the Recommended Interface

To configure the recommended interface, take the following steps:

1. Configure the device settings, such as power mode, decimation ratio, filter type, and so on.
2. Enter continuous readback mode.
3. Issue a synchronization pulse to apply the changes to the digital domain and to reset the digital filter. Issue the pulse immediately after DRDY goes high.

Recommended Interface for Reading Data

The recommended interface for reading data is as follows:

1. Synchronize the host controller with the DRDY or RDY pulse. See Figure 6 for details on the RDY behavior before data is clocked out.
2. Generate SCLK based on the DRDY or RDY timing. SCLK is high when the DRDY signal goes high and transitions on the MCLK falling edges (see Figure 98) to ensure that the LSB can be read correctly as the DOUT/RDY output is reset on the DRDY rising edge. However, SCLK rising occurs before this transition.
3. The MSB is clocked out on the next falling edge of SCLK.
4. In PIN control mode, the LSB of the conversion output is the last bit of the status output. In PIN control mode, this bit is always 1 and, therefore, does not need to be read.

Resynchronization of the Recommended Interface

Because the full ODR period is for clocking data, the RDY signal no longer flags after each LSB outputs. This signal only flags if the AD7768-1 is in continuous readback mode, or if the AD7768-1 does not count 32 SCLKs within 1 × t_{MCLK} before DRDY, as is shown in Figure 98.

The RDY function is only available in continuous readback mode. In normal readback, where the ADC_DATA register must be addressed each time, the DOUT line is reset 1 × t_{MCLK} before DRDY, as per t_{10} in the Timing Specifications section. If DRDY is used, the device operates as normal, and conversion readback is timed from the DRDY pulse. In the case where RDY detects the beginning of each sample, and where the data readback loses synchronization, the SCLK timing can be recovered by one of the following two methods:

- Using CS to reset the interface and to observe the RDY transition.
- Stopping SCLK toggling until the RDY transition is detected one more time.

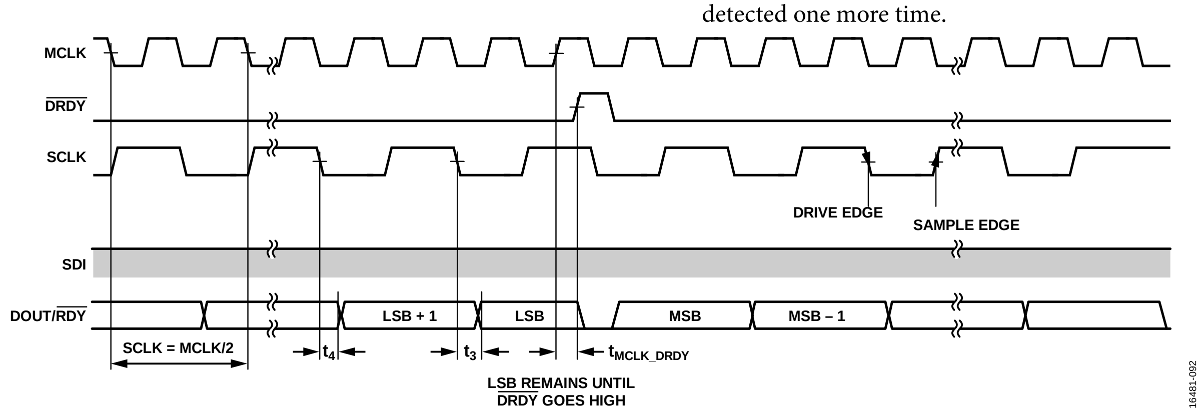

Figure 98. Recommended Interface for Reading Conversions, SPI Control, Continuous Readback Mode

PROGRAMMABLE DIGITAL FILTER

If there are additional filter requirements outside of the digital filters offered by default on the AD7768-1, there is the added option of designing and uploading a custom digital filter to memory. This upload overwrites the default low ripple FIR filter coefficients to be replaced by a set of user defined coefficients.

The AD7768-1 filter path has three separate stages:

- Initial sinc filter
- Sinc compensation filter
- Low ripple FIR filter

The user cannot change the first two stages. The only programmable stage is the third stage, where the default low ripple FIR filter coefficients can be replaced by a set of user-defined coefficients.

The data rate into the third stage is double the final ODR due to a fixed decimation by two that occurs after the final stage of filtering. Therefore, the programmable FIR stage receives data at a rate that is decimated from f_{MOD} by rates of 16, 32, 64, 128, 256, and 512.

After the final decimation by 2, the overall decimation values are given and are in the range of decimate by 32 to decimate by 1024. The data rates into the final FIR stage are listed in Table 27. Table 27 describes the data rate into the final filter stage for each power mode, assuming the correct MCLK_DIV setting is selected for the corresponding power mode. For example, when median power mode is selected, MCLK_DIV must be MCLK/4.

Filter Coefficients

The AD7768-1 low ripple FIR filter uses a set of 112 coefficients. By writing the appropriate key to the AD7768-1, these coefficients can be overwritten. Then, the customized filter coefficients can upload and lock into memory. If the AD7768-1 is reset, these coefficients must be rewritten.

The coefficients uploaded are subject to the following required conditions:

- The number of coefficients in a full set is 112, which is made up of 56 coefficients that are mirrored to make the total coefficients sum 112. Therefore, only 56 coefficients are written to during any one filter upload.
- Coefficients written must be in integer form. The format used is twos complement.
- The coefficient data register to be written is 24 bits wide, which is the only 24-bit register write used on the AD7768-1. Only 23 bits are used for the coefficients. The remaining MSB is a control bit, detailed in the Register 0x33.
- Filter coefficients are scaled such that the 56 coefficients must sum to 2^{22}. The total (112) coefficients, therefore, sum to 2^{23}.

For example, if the filter coefficient to be written to is −0.0123, this value is scaled to $-0.0123 \times 2^{22} = -51{,}590$. In twos complement format, this value is represented by 0x7F367A.

Each filter coefficient is written by first selecting the coefficient address. Then, a separate write of the data occurs, which is repeated for all 56 coefficients from Address 0 to Address 55.

Because the FIR size cannot be changed, the filter group delay remains fixed at 34/ODR when using the programmable filter option. If a shorter number of coefficients are required, padding the end coefficients with zeros can achieved this requirement. The group delay of the uploaded filter must always be equal to the group delay of the default AD7768-1 FIR filter that equals approximately 34/ODR.

Each time either the coefficient address register or the coefficient data register (COEFF_CONTROL or COEFF_DATA) are accessed, the user must wait a period before performing another read or write. The following equation determines the wait time:

$$t_{WAIT} = 512/MCLK$$

This wait time allows time for the register contents to update. Then, the coefficients are written to memory.

Table 27. Data Rates into the Final FIR Input Stage

	Input to Third Stage, Programmable FIR (MCLK = 16.384 MHz)								
Power Mode	**512 kHz**	**256 kHz**	**128 kHz**	**64 kHz**	**32 kHz**	**16 kHz**	**8 kHz**	**4 kHz**	**2 kHz**
Fast	Yes	Yes	Yes	Yes	Yes	Yes		Not applicable	Not applicable
Median	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes	Not applicable	Not applicable
Low Power	Not applicable	Not applicable	Not applicable	Yes	Yes	Yes	Yes	Yes	Yes

Upload Sequence

To program a user defined set of filter coefficients, perform the following sequence:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. The following key must be written to access the filter upload. First, write 0xAC to the ACCESS_KEY register (Register 0x34). Second, write 0x45 to the ACCESS_KEY register. Bit 0 (the key bit) of the ACCESS_KEY register can be read back to check if the key is entered correctly.
3. Write 0xC0 to the COEFF_CONTROL register (Register 0x32). Wait for t_{WAIT} sec to perform the following actions:
   a. Set the coefficient address to Address 0.
   b. Enable the access to memory (COEFFACCESSEN = 1).
   c. Allow a write to the coefficient memory (COEFFWRITEEN = 1).
4. The address of the first coefficient is selected. Write the required coefficient to the COEFF_DATA register (Register 0x33), and then wait for t_{WAIT} sec. Always wait t_{WAIT} sec between writes to Register 0x32 and Register 0x33.
5. Repeat Step 4 and Step 5 for each of the 56 coefficients. For example, write 0xC1 to COEFF_CONTROL to select coefficient Address 1. After waiting t_{WAIT} sec, enter the coefficient data. Increment the data until Coefficient 55 is reached. (Coefficient 55 is a write of 0xF7 to COEFF_CONTROL.)
6. Disable writing to the coefficients by first writing 0x80 to COEFF_CONTROL. Then, wait t_{WAIT} sec. Then, write 0x00 to COEFF_CONTROL to disable coefficient access.
7. Set USERCOEFFEN = 1 by writing 0x800 to COEFF_DATA to allow the user to toggle the synchronization pulse and to begin reading data.
8. Exit the filter upload by writing 0x55 to the ACCESS_KEY register (Register 0x34).
9. Send a synchronization pulse to the AD7768-1. One way of sending this pulse is by writing to the SYNC_RESET register (Register 0x1D). The filter upload is now complete.

The RAM CRC error check fails when the digital filter uploads. To disable this check, use the DIG_DIAG_ENABLE register (Register 0x2A).

See the Register Details for further details on the register bits.

Example Filter Upload

The following sequence programs a sinc1 filter. The coefficients in Address 0 to Address 23 = 0. The coefficients from Address 24 to Address 55 = 131,072 ($2^{22}/32$). When MCLK = 16.384 MHz and ODR = 256 kHz, the filter notch appears at 8 kHz and multiples of 8 kHz. This filter provides low noise and is recognizable by the distinctive filter profile shown in Figure 99.

To program the filter, take the following steps:

1. Write 0x4 to the filter bits in the DIGITAL_FILTER register (Register 0x19, Bits[6:4]).
2. Enter the key by writing to the ACCESS_KEY register (Register 0x34).
3. Write 0xC0 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, and COEFFWRITEEN = 1). Wait t_{WAIT} sec.
4. Write 0x000000 to COEFF_DATA (Register 0x33). Wait t_{WAIT} sec.
5. Write 0xC1 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec. In this case, the coefficient in Address 0 is equal to Address 1 and, therefore, the value in COEFF_DATA does not change.
6. Write 0xC2 to the COEFF_CONTROL register (COEFFADDR = 2). Wait t_{WAIT} sec.
7. Increment the address of the COEFF_CONTROL register (COEFFADDR = 23) until the write of 0xD7. Continue to wait t_{WAIT} sec.
8. Write 0xD8 to COEFF_CONTROL (COEFFADDR = 24).
9. Write 0x010000 to COEFF_DATA. Wait t_{WAIT} sec.
10. Write 0xD9 to COEFF_CONTROL (COEFFADDR = 25). Wait t_{WAIT} sec.
11. Write 0xDA to COEFF_CONTROL (COEFFADDR = 26) Wait t_{WAIT} sec.
12. Increment the address of the COEFF_CONTROL register (COEFFADDR = 55) until the write 0xF7. Wait t_{WAIT} sec.
13. Disable write and access by first writing 0x80 to the COEFF_CONTROL register. Wait t_{WAIT} sec. Then, write 0x00 to the COEFF_CONTROL register.
14. Set USERCOEFFEN = 1 to allow the user to toggle synchronization without reloading the default coefficients. (Write 0x800000 to COEFF_DATA.)
15. Exit the write by writing 0x55 to the ACCESS_KEY register.
16. Toggle synchronization.
17. Gather data. The resulting filter profile is shown in Figure 99.

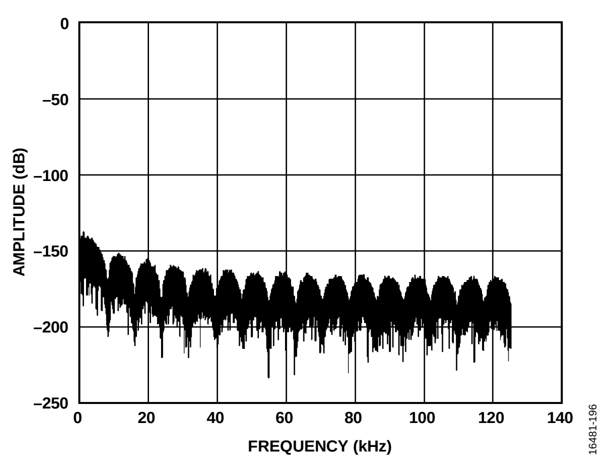

Figure 99. Example Filter Profile Upload

Filter Upload Verification

To check that the filter coefficients are uploaded correctly, it is possible to read back the values written to the COEFF_DATA register. This read can be performed after an upload by taking the following steps:

1. Enter the key by writing to the ACCESS_KEY register (Register 0x34). First, write 0xAC to the ACCESS_KEY register, and then write 0x45 to the ACCESS_KEY register.
2. Write 0x80 to the COEFF_CONTROL register, Register 0x32, (COEFFADDR = 0, COEFFACCESSEN = 1, COEFFWRITEEN = 0). Wait t_{WAIT} sec.
3. Read back the contents of the 24-bit COEFF_DATA register (Register 0x33). Check that the coefficient matches the uploaded value.
4. Write 0x81 to the COEFF_CONTROL register (COEFFADDR = 1). Wait t_{WAIT} sec.
5. Read the 24-bit COEFF_DATA register for Address 1. Increment and continue to read back the data. Continue to wait t_{WAIT} sec between updates to the COEFF_CONTROL register.
6. Disable the coefficient access by writing 0x00 to the COEFF_CONTROL register.
7. Exit the readback process by writing 0x55 to the ACCESS_KEY register.

ELECTROMAGNETIC COMPATIBILITY (EMC) TESTING

The AD7768-1 is suitable for a wide variety of applications, including applications requiring isolated channels in an industrial environment, or in condition-based monitoring solutions.

To ensure robust operation in harsh environments, the AD7768-1 was tested at an IC level for various EMC standards. The EMC testing was carried out to IEC standards and includes radiated immunity (IEC 62132-2), radio frequency radiated emissions (IEC 61967-2) and Electrical Fast Transients (EFT, IEC 62215-3). The decoupling capacitors required for correct operation of the device are in place for any EMC testing carried out.

Radiated Immunity

Radiated immunity testing was carried out as per IEC 62132-2. The test characterizes the immunity to electromagnetic interference (EMI) from radio frequencies during the normal operation of the device. The test frequency is from 150 kHz to 1 GHz, and the results seen in Table 28 were collected with both amplitude modulated (AM) and continuous wave (CW) interference applied. The AD7768-1 achieves Class A performance for both AM and CW radiated immunity to the maximum tested rating of 100 V/m.

Table 28. Radiated Immunity Test Results as per IEC 62132-2 Standard

Test Type	Test Level (V/m)	Class
AM	100	A
CW	100	A

Radiated Emissions

Radiated emissions testing was carried out as per IEC 61967-2. The test characterizes the electromagnetic frequencies generated during normal operation of the device. The test frequency was from 150 kHz to 1 GHz. The results shown in Table 29 were collected with an externally applied MCLK equal to 16.384 MHz applied to the device. The highest amplitudes radiated from the devices measured occurred at multiples of the MCLK frequency.

Table 29. Maximum Radiated Emissions Measured as per the IEC 61967-2 Standard, MCLK = 16.384 MHz, Low Ripple FIR Filter, Fast Power Mode

Frequency (MHz)	Amplitude (dB µV)
65.52	22.37
32.76	22.15
49.14	20.22

Electrical Fast Transients (EFTs)

EFT testing was carried out as per the IEC 62215-3 standard. EFT testing involves coupling multiple fast transient pulses to the pins of the device under test (DUT). The input is a transient pulse train applied at both the 5 kHz and 100 kHz input frequencies, according to IEC 61000-4-4. The results of the EFT testing are shown in Table 30, with the AD7768-1 achieving Class A performance up to ±1 kV.

Table 30. EFT Testing Results

AD7768-1 Pin	Test Level (V)	Performance Class
AVDD1	±1000	A
AVDD2	±1000	A
IOVDD	±1000	A

AD7768-1 SUBSYSTEM LAYOUT

The layout for the AD7768-1 and the surrounding subsystem is approximately shown in Figure 100. Analog inputs, reference inputs, and analog supplies are applied to the top left corner.

The IOVDD supply, digital interface, and clocking are all applied to the bottom right corner.

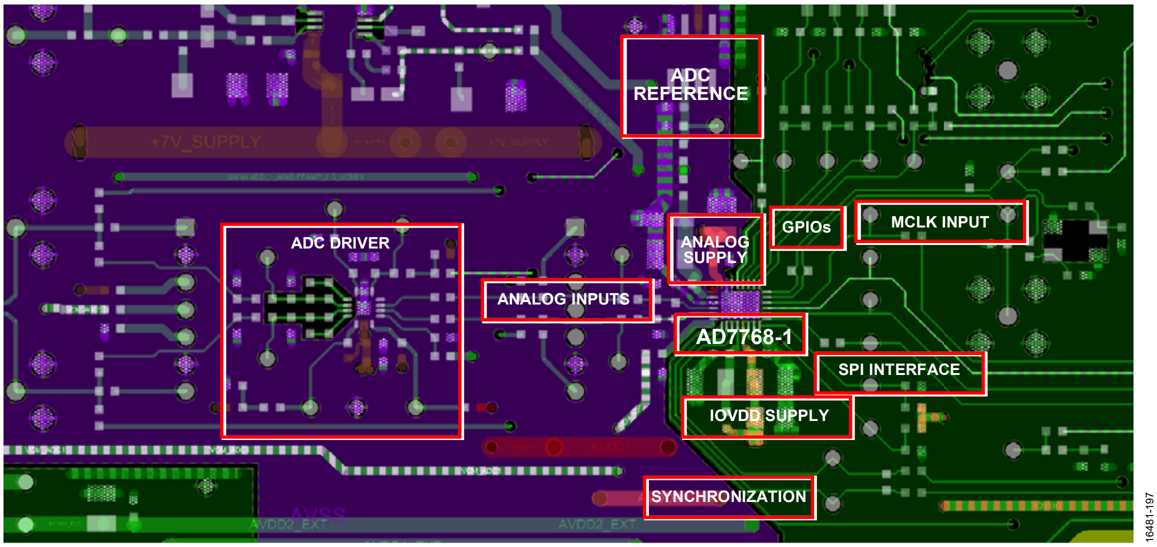

Figure 100. Subsystem Layout

REGISTER SUMMARY

Table 31. Register Summary

Reg (Hex)	Bit Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
03	CHIP_TYPE	[7:0]	Reserved				Class				0x07	R
04	PRODUCT_ ID_L	[7:0]	PRODUCT_ID[7:0]								0x01	R
05	PRODUCT_ ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
06	CHIP_GRADE	[7:0]	Grade				DEVICE_REVISION				0x00	R
0A	SCRATCH_ PAD	[7:0]	Value								0x00	R/W
0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
14	INTERFACE_ FORMAT	[7:0]	LV_BOOST	EN_SPI_CRC	CRC_ TYPE	STATUS_ EN	CONVLEN	EN_RDY_ DOUT	Reserved	EN_CONT_ READ	0x00	R/W
15	POWER_ CLOCK	[7:0]	CLOCK_SEL		MCLK_DIV		POWER_ DOWN	MOD_ OUTPUT	PWRMODE		0x00	R/W
16	Analog	[7:0]	REF_BUF_POS		REF_BUF_NEG		Reserved		AIN_ BUFF_ POS_OFF	AIN_ BUFF_ NEG_OFF	0x00	R/W
17	ANALOG2	[7:0]	CHOP_ FREQUENCY	Reserved				VCM			0x00	R/W
18	Conversion	[7:0]	DIAG_MUX_SELECT				CONV_ DIAG_ SELECT	CONV_MODE			0x00	R/W
19	DIGITAL_ FILTER	[7:0]	EN_60HZ_REJ	Filter			Reserved	DEC_RATE			0x00	R/W
1A	SINC3_DEC_ RATE_MSB	[7:0]	Reserved			SINC3_DEC[12:8]					0x00	R/W
1B	SINC3_DEC_ RATE_LSB	[7:0]	SINC3_DEC[7:0]								0x00	R/W
1C	DUTY_ CYCLE_RATIO	[7:0]	IDLE_TIME								0x00	R/W
1D	SYNC_RESET	[7:0]	SPI_START	SYNC_OUT_ POS_EDGE	Reserved		EN_GPIO_ START	Reserved	SPI_RESET		0x80	R/W
1E	GPIO_ CONTROL	[7:0]	UGPIO_EN	GPIO2_OPEN_ DRAIN_EN	GPIO1_ OPEN_ DRAIN_EN	GPIO0_ OPEN_ DRAIN_EN	GPIO3_ OP_EN	GPIO2_ OP_EN	GPIO1_ OP_EN	GPIO0_ OP_EN	0x00	R/W
1F	GPIO_WRITE	[7:0]	Reserved				GPIO_ WRITE_3	GPIO_ WRITE_2	GPIO_ WRITE_1	GPIO_ WRITE_0	0x00	R/W
20	GPIO_READ	[7:0]	Reserved				GPIO_ READ_3	GPIO_ READ_2	GPIO_ READ_1	GPIO_ READ_0	0x00	R
21	OFFSET_HI	[7:0]	Offset[23:16]								0x00	R/W
22	OFFSET_MID	[7:0]	Offset[15:8]								0x00	R/W
23	OFFSET_LO	[7:0]	Offset[7:0]								0x00	R/W
24	GAIN_HI	[7:0]	Gain[23:16]								0x00	R/W
25	GAIN_MID	[7:0]	Gain[15:8]								0x00	R/W
26	GAIN_LO	[7:0]	Gain[7:0]								0x00	R/W
28	SPI_DIAG_ ENABLE	[7:0]	Reserved			EN_ERR_ SPI_ IGNORE	EN_ERR_ SPI_CLK_ CNT	EN_ERR_ SPI_RD	EN_ERR_ SPI_WR	Reserved	0x10	R/W
29	ADC_DIAG_ ENABLE	[7:0]	Reserved		EN_ERR_ DLDO_ PSM	EN_ERR_ ALDO_ PSM	EN_ERR_ REF_DET	EN_ERR_ FILTER_ SATURATED	EN_ERR_ FILTER_ NOT_ SETTLED	EN_ERR_ EXT_CLK_ QUAL	0x07	R/W
2A	DIG_DIAG_ ENABLE	[7:0]	Reserved			EN_ERR_ MEMMAP_ CRC	EN_ERR_ RAM_CRC	EN_ERR_ FUSE_CRC	Reserved	EN_FREQ_ COUNT	0x0D	R/W
2C	ADC_DATA	[23:16]	ADC_READ_DATA[23:16]								0x000 000	R
		[15:8]	ADC_READ_DATA[15:8]									
		[7:0]	ADC_READ_DATA[7:0]									

Reg (Hex)	Bit Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
2D	MASTER_STATUS	[7:0]	MASTER_ERROR	ADC_ERROR	DIG_ERROR	ADC_ERR_EXT_CLK_QUAL	ADC_FILT_SATURATED	ADC_FILT_NOT_SETTLED	SPI_ERROR	POR_FLAG	0x00	R
2E	SPI_DIAG_STATUS	[7:0]	Reserved			ERR_SPI_IGNORE	ERR_SPI_CLK_CNT	ERR_SPI_RD	ERR_SPI_WR	ERR_SPI_CRC	0x00	R/W
2F	ADC_DIAG_STATUS	[7:0]	Reserved		ADC_ERR_DLDO_PSM	ADC_ERR_ALDO_PSM	ERR_REF_DET	ADC_FILT_SATURATED	ADC_FILT_NOT_SETTLED	ADC_ERR_EXT_CLK_QUAL	0x00	R
30	DIG_DIAG_STATUS	[7:0]	Reserved			ERR_MEMMAP_CRC	ERR_RAM_CRC	ERR_FUSE_CRC	Reserved		0x00	R
31	MCLK_COUNTER	[7:0]	MCLK_COUNTER								0x00	R
32	COEFF_CONTROL	[7:0]	COEFFACCESSEN	COEFFWRITEEN	COEFFADDR						0x00	R/W
33	COEFF_DATA	[23:16]	USERCOEFFEN	COEFFDATA[22:16]							0x000000	R/W
		[15:8]	COEFFDATA[15:8]									
		[7:0]	COEFFDATA[7:0]									
34	ACCESS_KEY	[7:0]	Reserved							Key	0x00	R

REGISTER DETAILS

COMPONENT TYPE REGISTER

Register: 0x03, Reset: 0x07, Name: CHIP_TYPE

Table 32. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	Reserved	Reserved.	0x0	R
[3:0]	Class	Chip type. 111: analog to digital converter.	0x7	R

UNIQUE PRODUCT ID REGISTERS

Register: 0x04, Reset: 0x01, Name: PRODUCT_ID_L

Table 33. Bit Descriptions for PRODUCT_ID_L

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID [7:0]	0x1	R

Register: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

Table 34. Bit Descriptions for PRODUCT_ID_H

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID [15:8]	0x0	R

DEVICE GRADE AND REVISION REGISTER

Register: 0x06, Reset: 0x00, Name: CHIP_GRADE

Table 35. Bit Descriptions for CHIP_GRADE

Bit(s)	Bit Name	Description	Reset	Access
[7:4]	Grade	Device grade	0x0	R
[3:0]	DEVICE_REVISION	Device revision ID	0x0	R

USER SCRATCHPAD REGISTER

Register: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

Table 36. Bit Descriptions for SCRATCH_PAD

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Value	Scratch pad; read and/or write area communication	0x0	R/W

DEVICE VENDOR ID REGISTERS

Register: 0x0C, Reset: 0x56, Name: VENDOR_L

Table 37. Bit Descriptions for VENDOR_L

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Vendor ID [7:0]. Analog Devices vendor ID.	0x56	R

Register: 0x0D, Reset: 0x04, Name: VENDOR_H

Table 38. Bit Descriptions for VENDOR_H

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Vendor ID [15:8]. Analog Devices vendor ID.	0x4	R

INTERFACE FORMAT CONTROL REGISTER

Register: 0x14, Reset: 0x00, Name: INTERFACE_FORMAT

Table 39. Bit Descriptions for INTERFACE_FORMAT

Bit(s)	Bit Name	Description	Reset	Access
7	LV_BOOST	Boosts drive strength of SPI output for use with IOVDD levels of 1.8 V, or when a high capacitive load is present on the DOUT/RDY pin. The default state is LV_BOOST enabled when in PIN control mode. 0: disables LV_BOOST. 1: enables LV_BOOST. This bit must be re-enabled following an exit from continuous read mode, if applicable.	0x0	R/W
6	EN_SPI_CRC	Activates CRC on all SPI transactions. 0: disable CRC function on all SPI transfers. 1: enable CRC function on all SPI transfers.	0x0	R/W
5	CRC_TYPE	Selects CRC method as XOR or 8-bit polynomial. 1: XOR instead of CRC (applied to read transactions only). 0: CRC bits are based on CRC-8 polynomial. CRC check of interface transfers uses 8-bit CRC polynomial.	0x0	R/W
4	STATUS_EN	Enables status bits output. In SPI control mode, the status bits can be output after the ADC conversion result by setting the bits in this bit field. In PIN control mode, the status bits are output after the ADC conversion result by default. 0: disable output of status bits with ADC conversion result in continuous read mode. 1: output status bits with ADC conversion result in continuous read mode.	0x0	R/W
3	CONVLEN	Conversion result output length. 0: full, 24-bit. 1: output only 16 MSB of the ADC result.	0x0	R/W
2	EN_RDY_DOUT	Enables the RDY signal on the DOUT/RDY pin. Enables the RDY indicator on the DOUT/RDY pin in continuous read mode. Setting this bit causes DOUT/RDY to signal the availability of ADC conversion data. 0: disables RDY function on SDO in continuous read mode. 1: enables RDY function on SDO in continuous read mode.	0x0	R/W
1	Reserved	Reserved.	0x0	R
0	EN_CONT_READ	Continuous read enable bit. 0: disables continuous read mode. 1: enables continuous read mode.	0x0	R/W

POWER AND CLOCK CONTROL REGISTER

Register: 0x15, Reset: 0x00, Name: POWER_CLOCK

Table 40. Bit Descriptions for POWER_CLOCK

Bit(s)	Bit Name	Description	Reset	Access
[7:6]	CLOCK_SEL	Options for setting the clock used by the device. 0: CMOS clock on MCLK/XTAL2. 1: crystal oscillator. 10: LVDS input enable. 11: internal coarse RC clock (diagnostics).	0x0	R/W

Bit(s)	Bit Name	Description	Reset	Access
[5:4]	MCLK_DIV	Sets the division of the MCLK to create the ADC modulator frequency (f_{MOD}). 0: modulator CLK is equal to master clock divided by 16. 1: modulator CLK is equal to master clock divided by 8. 10: modulator CLK is equal to master clock divided by 4. 11: modulator CLK is equal to master clock divided by 2.	0x0	R/W
3	POWER_DOWN	Places device into a power-down state. All blocks including the SPI are powered down. The standard SPI is not active in this state. Power-down is the lowest power consumption mode. To enter power-down mode, write 0x08 to this register. If the user attempts to set Bit 3 while also setting other bits in this register, the SPI write command is ignored, the device does not enter power-down, and the other bits are not set. Power-down mode can be exited in three ways: by a reset using the AD7768-1 $\overline{\text{RESET}}$ pin, by issuing the SPI resume command over SDI and SCLK, or by using the power cycle of the device. 0: device powered on. 1: device powered down.	0x0	R/W
2	MOD_OUTPUT	Selects modulator output mode. Selecting modulator mode forces the power mode to low power mode and ignores any user changes to the power mode bits (PWRMODE, Bits[1:0]) in this register. 0: disables raw modulator output. 1: enables raw modulator output.	0x0	R/W
[1:0]	PWRMODE	Sets the power consumption mode of the ADC core. This setting, in conjunction with MCLK_DIV, creates the conditions for power scaling the ADC vs. input bandwidth/throughput. 0: low power mode. 10: median power mode. 11: fast power mode.	0x0	R/W

ANALOG BUFFER CONTROL REGISTER

Register: 0x16, Reset: 0x00, Name: Analog

Used to turn on or off front end buffering.

Table 41. Bit Descriptions for Analog

Bit(s)	Bit Name	Description	Reset	Access
[7:6]	REF_BUF_POS	Buffering options for the reference positive input. 0: precharge reference buffer on. 1: unbuffered reference input. 10: full reference buffer on.	0x0	R/W
[5:4]	REF_BUF_NEG	Buffering options for the reference negative input. 0: precharge Reference buffer on. 1: unbuffered input. 10: full Reference buffer on.	0x0	R/W
[3:2]	Reserved	Reserved.	0x0	R
1	AIN_BUFF_POS_OFF	AIN+ precharge buffer disabled. Setting this bit disables the precharge buffer on the positive analog input. 0: AIN+ precharge buffer enabled. 1: AIN+ precharge buffer disabled.	0x0	R/W
0	AIN_BUFF_NEG_OFF	AIN– precharge buffer disabled. Setting this bit disables the precharge buffer on the negative analog input. 0: AIN– precharge buffer enabled. 1: AIN– precharge buffer disabled.	0x0	R/W

VCM CONTROL REGISTER

Register: 0x17, Reset: 0x00, Name: ANALOG2

Table 42. Bit Descriptions for ANALOG2

Bit(s)	Bit Name	Description	Reset	Access
7	CHOP_FREQUENCY	Selects the chop frequency for use within the modulator. 0: sets the chopping frequency of the modulator. This is the default chop setting of $f_{MOD}/32$. Setting the chop rate to $f_{MOD}/32$ gives the best offset and offset drift performance. 1: sets the chopping frequency of the modulator. This sets the chop rate to $f_{MOD}/8$. Setting the chop rate to $f_{MOD}/8$ allows the user to push the first chop alias further from the pass band. See Figure 77.	0x0	R/W
[6:3]	Reserved	Reserved.	0x0	R
[2:0]	VCM	Sets output from the VCM pin. The VCM output voltage can be used as a common-mode voltage within the amplifier preconditioning circuits external to the AD7768-1. 000: VCM output set to (AVDD1 − AVSS)/2. 001: VCM output set to 2.5 V. 010: VCM output set to 2.05 V. 011: VCM output set to 1.9 V. 100: VCM output set to 1.65 V. 101: VCM output set to 1.1 V. 110: VCM output set to 0.9 V. 111: VCM output off.	0x0	R/W

CONVERSION SOURCE SELECT AND MODE CONTROL REGISTER

Register: 0x18, Reset: 0x00, Name: Conversion

Table 43. Bit Descriptions for Conversion

Bit(s)	Bit Name	Description	Reset	Access
[7:4]	DIAG_MUX_SELECT	Selects which signal to route through the diagnostic mux. Perform diagnostic checks in low power mode only. 0: temperature sensor. 1000: AIN± short (zero check). 1001: positive full scale. 1010: negative full scale.	0x0	R/W
3	CONV_DIAG_SELECT	Selects the input for conversion as AIN± or the diagnostic mux. 0: set the input for conversion from AIN±. 1: set the input for conversion from the diagnostic mux.	0x0	R/W

Bit(s)	Bit Name	Description	Reset	Access
[2:0]	CONV_MODE	Sets the conversion mode of the ADC. 000: continuous conversion mode. The modulator is converting continuously. Continuous DRDY pulse for every filter conversion. 001: continuous one shot mode. One shot is the method of using the SYNC_IN time to start a conversion. It is similar to a conversion start signal when using one shot mode. The ADC modulator is continuously running while waiting on a SYNC_IN rising edge. On release of a pulse (low to high transition) to the SYNC_IN pin, a new conversion begins, converting and integrating over the settling time of the filter selected. DRDY toggles when the conversion completes, indicating it is available for readback over the SPI. 010: single-conversion standby mode. In single-conversion standby mode, the ADC runs one conversion with the selected filter, sampling and integrating over the full settling time of the filter before providing a single conversion result. After the conversion is complete, the ADC goes into standby. Initiating another single conversion from standby means that there is a start-up time to come out of standby before the ADC begins converting to produce the single conversion. This mode is recommended for use in low power mode. 011: periodic conversion standby mode. Low power periodic conversion is a method of setting the single conversion to run in a timed loop. A separate register sets the ratio for the time spent in standby vs. converting. The ADC automatically comes out of standby periodically, performs a single conversion, and then returns to standby again without the need for the user to initiate the single conversion over the SPI. 100: standby. Sets the device to standby mode. 101: sets the device to standby mode. 110: sets the device to standby mode. 111: sets the device to standby mode.	0x0	R/W

DIGITAL FILTER AND DECIMATION CONTROL REGISTER

Register: 0x19, Reset: 0x00, Name: DIGITAL_FILTER

Table 44. Bit Descriptions for DIGITAL_FILTER

Bit(s)	Bit Name	Description	Reset	Access
7	EN_60HZ_REJ	For use with the sinc3 filter only. First, program the sinc3 filter to output at 50 Hz. Subsequently selecting the EN_60HZ_REJ bit allows one zero of the sinc3 filter to fall at 60 Hz. This bit only enables rejection of both 50 Hz and 60 Hz if it is set in combination with programming the sinc3 filter for the 50 Hz ODR. 0: sinc3 filter optimized for single-frequency rejection, 50 Hz or 60 Hz. 1: filter operation is modified to allow both 50 Hz and 60 Hz rejection.	0x0	R/W
[6:4]	Filter	Selects the style of filter for use. 000: sinc5 filter. Decimate ×32 to ×1024. Use the DEC_RATE bits to select one of the six available decimation rates from ×32 to ×1024. 001: sinc5 filter. Decimate ×8 only. Enables a maximum data rate of 1 MHz. This path allows viewing of wider bandwidth; however, it is quantization noise limited so that output data is reduced to 16 bits. 010: sinc5 filter. Decimate ×16 only. Enables a maximum data rate of 512 kHz. This path allows viewing of wider bandwidths. 011: sinc3 filter. Decimation rate is selected via 13 bits in sinc 3 decimation rate register. The sinc3 filter can be tuned to reject 50 Hz or 60 Hz, and with the EN_60HZ_REJ bit can allow rejection of both 50 Hz and 60 Hz. Decimation rate is selected via SINC3_DEC bits in sinc3 decimation rate MSB and LSB registers. The sinc3 filter can be tuned to reject 50 Hz or 60 Hz and with the EN_60HZ_REJ bit set can allow rejection of both 50 Hz and 60 Hz when used with a 16.384 MHz MCLK.	0x0	R/W

Bit(s)	Bit Name	Description	Reset	Access
		100: low ripple FIR filter. FIR filter with low ripple pass band and sharp transition band. Use DEC_RATE bits to select one of six available decimation rates from ×32 to ×1024. 101: not used. 110: not used. 111: not used.		
3	Reserved	Reserved.	0x0	R
[2:0]	DEC_RATE	Selects the decimation rate for the sinc5 filter and the brick wall, low-pass FIR filter. 0: decimate ×32. 1: decimate ×64. 10: decimate ×128. 11: decimate ×256. 100: decimate ×512. 101: decimate ×1024. 110: decimate ×1024. 111: decimate ×1024.	0x0	R/W

SINC3 DECIMATION RATE (MSB REGISTER)

Register: 0x1A, Reset: 0x00, Name: SINC3_DEC_RATE_MSB

Table 45. Bit Descriptions for SINC3_DEC_RATE_MSB

Bit(s)	Bit Name	Description	Reset	Access
[7:5]	Reserved	Reserved.	0x0	R
[4:0]	SINC3_DEC[12:8]	Determines the decimation rate used with the sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give the actual DEC_RATE.	0x0	R/W

SINC3 DECIMATION RATE (LSB REGISTER)

Register: 0x1B, Reset: 0x00, Name: SINC3_DEC_RATE_LSB

Table 46. Bit Descriptions for SINC3_DEC_RATE_LSB

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	SINC3_DEC[7:0]	Determines the decimation rate of used with the sinc3 filter. Value entered is incremented by 1 and multiplied by 32 to give the actual DEC_RATE.	0x0	R/W

PERIODIC CONVERSION RATE CONTROL REGISTER

Register: 0x1C, Reset: 0x00, Name: DUTY_CYCLE_RATIO

DUTY_CYCLE_RATIO sets the time used in periodic conversion mode. Only use periodic conversion mode in median mode or low power mode.

Table 47. Bit Descriptions for DUTY_CYCLE_RATIO

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	IDLE_TIME	Sets idle time for periodic conversion when in standby. A 1 in this registers corresponds to time for one output from filter selected. The value in this register is incremented by one and doubled.	0x0	R/W

SYNCHRONIZATION MODES AND RESET TRIGGERING REGISTER

Register: 0x1D, Reset: 0x80, Name: SYNC_RESET

Table 48. Bit Descriptions for SYNC_RESET

Bit(s)	Bit Name	Description	Reset	Access
7	SPI_START	Trigger START signal. Allows user to initiate a SYNC_OUT pulse over the SPI. Setting this bit low drives a low pulse through SYNC_OUT that can be used as a SYNC_IN signal to the same device and other AD7768-1 devices where synchronized sampling is required. This bit clears itself after use.	0x1	R/W
6	SYNC_OUT_POS_EDGE	SYNC_OUT drive edge select. Setting this bit causes SYNC_OUT to be driven low by the positive edge of MCLK. Device default is that SYNC_OUT is driven low on the negative edge of MCLK.	0x0	R/W
[5:4]	Reserved	Reserved.	0x0	R
3	EN_GPIO_START	Enable START function on the GPIO input. Allows the user to use one of the GPIOx pins as a START input pin. When enabled, a low pulse on the START input generates a low pulse through SYNC_OUT that can be used as a SYNC_IN signal to the same device and other AD7768-1 devices where synchronized sampling is required. When enabled GPIO3 becomes the START input. While the START function is enabled, the GPIOx pins cannot be used for general-purpose input/output reading and writing. The remaining GPIOs are set to outputs. 0: disabled 1: enabled	0x0	R/W
2	Reserved	Reserved.	0x0	R
[1:0]	SPI_RESET	Enables device reset over SPI. Two writes to these bits are required to initiate the reset. The user must first set the bits to 11, and then set the bits to 10. When this sequence is detected on these two bits, the reset occurs. It is not dependent on other bits in this register being set or cleared.	0x0	R/W

GPIO PORT CONTROL REGISTER

Register: 0x1E, Reset: 0x00, Name: GPIO_CONTROL

Table 49. Bit Descriptions for GPIO_CONTROL

Bit(s)	Bit Name	Description	Reset	Access
7	UGPIO_EN	Universal enabling of GPIOx pins. This bit must be set high to allow the user to change the GPIO settings.	0x0	R/W
6	GPIO2_OPEN_DRAIN_EN	Change GPIO2 output from strong driver to open drain.	0x0	R/W
5	GPIO1_OPEN_DRAIN_EN	Change GPIO1 output from strong driver to open drain.	0x0	R/W
4	GPIO0_OPEN_DRAIN_EN	Change GPIO0 output from strong driver to open drain.	0x0	R/W
3	GPIO3_OP_EN	Output Enable for GPIO pin. 0 = input, 1 = output.	0x0	R/W
2	GPIO2_OP_EN	Output Enable for GPIO pin. 0 = input, 1 = output.	0x0	R/W
1	GPIO1_OP_EN	Output Enable for GPIO pin. 0 = input, 1 = output.	0x0	R/W
0	GPIO0_OP_EN	Output Enable for GPIO pin. 0 = input, 1 = output.	0x0	R/W

GPIO OUTPUT CONTROL REGISTER

Register: 0x1F, Reset: 0x00, Name: GPIO_WRITE

Table 50. Bit Descriptions for GPIO_WRITE

Bit(s)	Bit Name	Description	Reset	Access
[7:4]	Reserved	Reserved	0x0	R
3	GPIO_WRITE_3	Write to this bit to set GPIO3 high.	0x0	R/W
2	GPIO_WRITE_2	Write to this bit to set GPIO2 high.	0x0	R/W
1	GPIO_WRITE_1	Write to this bit to set GPIO1 high.	0x0	R/W
0	GPIO_WRITE_0	Write to this bit to set GPIO0 high.	0x0	R/W

GPIO INPUT READ REGISTER

Register: 0x20, Reset: 0x00, Name: GPIO_READ

Table 51. Bit Descriptions for GPIO_READ

Bit(s)	Bit Name	Description	Reset	Access
[7:4]	Reserved	Reserved	0x0	R
3	GPIO_READ_3	Read the value from GPIO3.	0x0	R
2	GPIO_READ_2	Read the value from GPIO2.	0x0	R
1	GPIO_READ_1	Read the value from GPIO1.	0x0	R
0	GPIO_READ_0	Read the value from GPIO0.	0x0	R

OFFSET CALIBRATION MSB REGISTER

Register: 0x21, Reset: 0x00, Name: OFFSET_HI

Table 52. Bit Descriptions for OFFSET_HI

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Offset[23:16]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction; therefore, the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION MID REGISTER

Register: 0x22, Reset: 0x00, Name: OFFSET_MID

Table 53. Bit Descriptions for OFFSET_MID

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Offset[15:8]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction; therefore, the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

OFFSET CALIBRATION LSB REGISTER

Register: 0x23, Reset: 0x00, Name: OFFSET_LO

Table 54. Bit Descriptions for OFFSET_LO

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Offset[7:0]	User offset calibration coefficient. The offset correction registers provide 24-bit, signed, twos-complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction; therefore, the ratio above changes linearly with any gain adjustment applied via the gain calibration registers.	0x0	R/W

GAIN CALIBRATION MSB REGISTER

Register: 0x24, Reset: 0x00, Name: GAIN_HI

Table 55. Bit Descriptions for GAIN_HI

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Gain[23:16]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION MID REGISTER

Register: 0x25, Reset: 0x00, Name: GAIN_MID

Table 56. Bit Descriptions for GAIN_MID

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Gain[15:8]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

GAIN CALIBRATION LSB REGISTER

Register: 0x26, Reset: 0x00, Name: GAIN_LO

Table 57. Bit Descriptions for GAIN_LO

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	Gain[7:0]	User gain calibration coefficient. The ADC has an associated factory programmed gain calibration coefficient. The coefficient is stored in the ADC during factory programming and the nominal value is around 0x555555. The user can read back the factory programmed value and may overwrite the gain register setting to apply their own calibration coefficient. The user offset calibration coefficient correction is applied to the digital filter output data before the gain calibration correction.	0x0	R/W

SPI INTERFACE DIAGNOSTIC CONTROL REGISTER

Register: 0x28, Reset: 0x10, Name: SPI_DIAG_ENABLE

Table 58. Bit Descriptions for SPI_DIAG_ENABLE

Bit(s)	Bit Name	Description	Reset	Access
[7:5]	Reserved	Reserved	0x0	R
4	EN_ERR_SPI_IGNORE	SPI ignore error enabled	0x1	R/W
3	EN_ERR_SPI_CLK_CNT	SPI clock count error enabled. The SPI clock count error is only valid for SPI transactions that use $\overline{CS}$.	0x0	R/W
2	EN_ERR_SPI_RD	SPI read error enabled	0x0	R/W
1	EN_ERR_SPI_WR	SPI write error enabled	0x0	R/W
0	Reserved	Reserved	0x0	R

ADC DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x29, Reset: 0x07, Name: ADC_DIAG_ENABLE

Table 59. Bit Descriptions for ADC_DIAG_ENABLE

Bit(s)	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
5	EN_ERR_DLDO_PSM	DLDO PSM error enabled	0x0	R/W
4	EN_ERR_ALDO_PSM	ALDO PSM error enabled	0x0	R/W
3	EN_ERR_REF_DET	Reference detect enable	0x0	R/W
2	EN_ERR_FILTER_SATURATED	Filter saturated error enabled	0x1	R/W
1	EN_ERR_FILTER_NOT_SETTLED	Filter not settled error enabled	0x1	R/W
0	EN_ERR_EXT_CLK_QUAL	Enable qualification check on external clock	0x1	R/W

DIGITAL DIAGNOSTIC FEATURE CONTROL REGISTER

Register: 0x2A, Reset: 0x0D, Name: DIG_DIAG_ENABLE

Table 60. Bit Descriptions for DIG_DIAG_ENABLE

Bit(s)	Bit Name	Description	Reset	Access
[7:5]	Reserved	Reserved	0x0	R
4	EN_ERR_MEMMAP_CRC	Memory map CRC error enabled	0x0	R/W
3	EN_ERR_RAM_CRC	RAM CRC error enabled	0x1	R/W
2	EN_ERR_FUSE_CRC	Fuse CRC error enabled	0x1	R/W
1	Reserved	Reserved	0x0	R/W
0	EN_FREQ_COUNT	Enable MCLK counter	0x1	R/W

CONVERSION RESULT REGISTER

Address: 0x2C, Reset: 0x000000, Name: ADC_DATA

Table 61. Bit Descriptions for ADC_DATA

Bit(s)	Bit Name	Description	Reset	Access
[23:16]	ADC_READ_DATA[23:16]	ADC read data	0x0	R
[15:8]	ADC_READ_DATA[15:8]	ADC read data	0x0	R
[7:0]	ADC_READ_DATA[7:0]	ADC read data	0x0	R

DEVICE ERROR FLAGS MASTER REGISTER

Register: 0x2D, Reset: 0x00, Name: MASTER_STATUS

See the Status Header section for additional information.

Table 62. Bit Descriptions for MASTER_STATUS

Bit	Bit Name	Description	Reset	Access
7	MASTER_ERROR	Master error	0x0	R
6	ADC_ERROR	Any ADC error (OR)	0x0	R
5	DIG_ERROR	Any digital error (OR)	0x0	R
4	ADC_ERR_EXT_CLK_QUAL	No clock error; applied to master status register only	0x0	R
3	ADC_FILT_SATURATED	Filter saturated	0x0	R
2	ADC_FILT_NOT_SETTLED	Filter not settled	0x0	R
1	SPI_ERROR	Any SPI error (OR)	0x0	R
0	POR_FLAG	POR flag	0x0	R

SPI INTERFACE ERROR REGISTER

Register: 0x2E, Reset: 0x00, Name: SPI_DIAG_STATUS

Table 63. Bit Descriptions for SPI_DIAG_STATUS

Bit(s)	Bit Name	Description	Reset	Access
[7:5]	Reserved	Reserved.	0x0	R
4	ERR_SPI_IGNORE	SPI ignore error	0x0	R/W1C
3	ERR_SPI_CLK_CNT	SPI clock count error	0x0	R
2	ERR_SPI_RD	SPI read error	0x0	R/W1C
1	ERR_SPI_WR	SPI write error	0x0	R/W1C
0	ERR_SPI_CRC	SPI CRC error	0x0	R/W1C

ADC DIAGNOSTICS OUTPUT REGISTER

Register: 0x2F, Reset: 0x00, Name: ADC_DIAG_STATUS

Table 64. Bit Descriptions for ADC_DIAG_STATUS

Bit(s)	Bit Name	Description	Reset	Access
[7:6]	Reserved	Reserved	0x0	R
5	ADC_ERR_DLDO_PSM	Digital low dropout (DLDO) power supply monitor (PSM) error	0x0	R
4	ADC_ERR_ALDO_PSM	Analog low dropout (ALDO) PSM error	0x0	R
3	ERR_REF_DET	Reference detection error	0x0	R
2	ADC_FILT_SATURATED	Filter saturated	0x0	R
1	ADC_FILT_NOT_SETTLED	Filter not settled	0x0	R
0	ADC_ERR_EXT_CLK_QUAL	No clock error; applied to master status register only	0x0	R

DIGITAL DIAGNOSTICS OUTPUT REGISTER

Register: 0x30, Reset: 0x00, Name: DIG_DIAG_STATUS

Table 65. Bit Descriptions for DIG_DIAG_STATUS

Bit(s)	Bit Name	Description	Reset	Access
[7:5]	Reserved	Reserved	0x0	R
4	ERR_MEMMAP_CRC	Memory map CRC error	0x0	R
3	ERR_RAM_CRC	RAM CRC error	0x0	R
2	ERR_FUSE_CRC	Fuse CRC error	0x0	R
[1:0]	Reserved	Reserved	0x0	R

MCLK DIAGNOSTIC OUTPUT REGISTER

Register: 0x31, Reset: 0x00, Name: MCLK_COUNTER

Table 66. Bit Descriptions for MCLK_COUNTER

Bit(s)	Bit Name	Description	Reset	Access
[7:0]	MCLK_COUNTER	MCLK counter. This register increments after every 64 MCLKs.	0x0	R

COEFFICIENT CONTROL REGISTER

Register: 0x32, Reset: 0x00, Name: COEFF_CONTROL

Table 67. Bit Descriptions for COEFF_CONTROL

Bit(s)	Bit Name	Description	Reset	Access
7	COEFFACCESSEN	Setting this bit to a 1 allows access to the coefficient memory.	0x0	R/W
6	COEFFWRITEEN	Enables write to the coefficient memory. Write a 1 to enable.	0x0	R/W
[5:0]	COEFFADDR	Address to be accessed for the coefficient memory. The address ranges from 0 to 55 for 56 coefficients that form one symmetrical half of the 112 coefficients.	0x00	R/W

COEFFICIENT DATA REGISTER

Register: 0x33, Reset: 0x00, Name: COEFF_DATA

Table 68. Bit Descriptions for COEFF_DATA

Bit(s)	Bit Name	Description	Reset	Access
23	USERCOEFFEN	Setting this bit to a 1 prevents the coefficients from ROM over writing the user defined coefficients after a sync toggle. A sync pulse is required after every change to the AD7768-1 digital filter configuration, including a customized filter upload.	0x0	R/W
[22:0]	COEFFDATA	Filter coefficients written to memory are written to these bits. These bits are 23 bits wide.	0x000000	R/W

ACCESS KEY REGISTER

Register: 0x34, Reset: 0x00, Name: ACCESS_KEY

Table 69. Bit Descriptions for ACCESS_KEY

Bit(s)	Bit Name	Description	Reset	Access
[7:1]	Reserved	Reserved.		
0	Key	A specific key must be written to the ACCESS_KEY register prior to any filter upload. If written correctly, the key bit reads back as 1.	0x0	R/W

OUTLINE DIMENSIONS

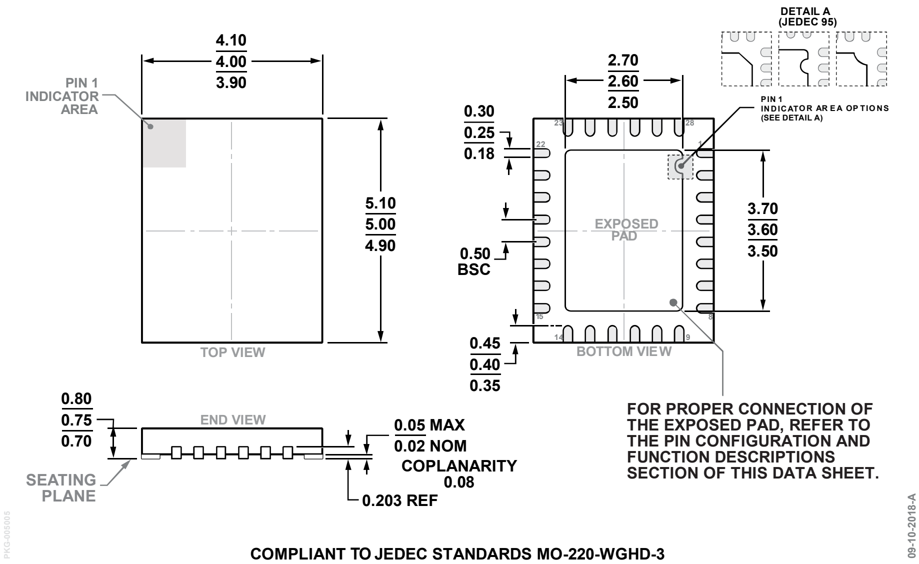

Figure 101. 28-Lead Lead Frame Chip-Scale Package [LFCSP]
4 mm × 5 mm Body and 0.75 mm Package Height
(CP-28-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7768-1BCPZ	−40°C to +125°C	28-Lead Lead Frame Chip-Scale Package [LFCSP]	CP-28-12
AD7768-1BCPZ-RL	−40°C to +125°C	28-Lead Lead Frame Chip-Scale Package [LFCSP]	CP-28-12
AD7768-1BCPZ-RL7	−40°C to +125°C	28-Lead Lead Frame Chip-Scale Package [LFCSP]	CP-28-12
EV-AD7768-1FMCZ		Evaluation Board	
EVAL-SDP-CH1Z		Controller Board	

[1] Z = RoHS Compliant Part.