Precision, High Speed, BiFET Quad Op Amp

AD713

FEATURES

AC performance
- **1 µs settling to 0.01% for 10 V step**
- **20 V/µs slew rate**
- **0.0003% total harmonic distortion (THD)**
- **4 MHz unity gain bandwidth**

DC performance
- **1.5 mV maximum offset voltage**
- **8 µV/°C typical drift**
- **150 V/mV minimum open-loop gain**
- **2 µV p-p typical noise, 0.1 Hz to 10 Hz**
- **True 14-bit accuracy**
- **Single version: AD711, dual version: AD712**
- **Available in 16-lead SOIC, 14-lead PDIP and CERDIP**

APPLICATIONS

Active filters
Quad output buffers for 12- and 14-bit DACs
Input buffers for precision ADCs
Photo diode preamplifier applications

GENERAL DESCRIPTION

The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die. The single-pole response of the AD713 provides fast settling: l µs to 0.01%. This feature, combined with its high dc precision, makes the AD713 suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713 low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications. The AD713 is internally compensated for stable operation at unity gain. The AD713J is rated over the commercial temperature range of 0°C to 70°C. The AD713A is rated over the industrial temperature of −40°C to +85°C.

The AD713 is offered in 16-lead SOIC, 14-lead PDIP, and 14-lead CERDIP packages.

CONNECTION DIAGRAMS

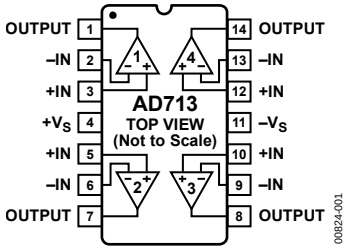


Figure 1. 14-Lead PDIP (N) and CERDIP (Q) Packages

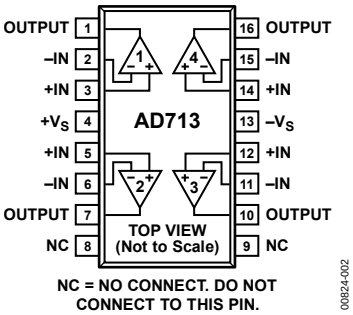


Figure 2. 16-Lead SOIC_W (RW) Package

PRODUCT HIGHLIGHTS

1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074, TL084, LT1058, LF347, and OPA404.
2. Slew rate is 100% tested for a guaranteed minimum of 16 V/µs (J and A grades).
3. The combination of Analog Devices, Inc., advanced processing technology, laser wafer drift trimming, and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

Rev. F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

AD713* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-106: A Collection of Amp Applications
- AN-214: Ground Rules for High Speed Circuits
- AN-349: Keys to Longer Life for CMOS
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- AD713: Military Data Sheet
- AD713: Precision, High Speed, BiFET Quad Op Amp
- AD713: Quad Precision, Low Cost, High Speed, BiFET Op Amp Data Sheet

TOOLS AND SIMULATIONS

- Analog Filter Wizard
- Analog Photodiode Wizard
- AD713 SPICE Macro-Model

DESIGN RESOURCES

- AD713 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD713 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

7/11—Rev. E to Rev. F

Changes to Figure 2 ... 1

6/11—Rev. D to Rev. E

Changed 8 µV/°C Maximum Drift to 8 µV/°C Typical Drift in Features Section ... 1

5/11—Rev. C to Rev. D

Updated Format ... Universal
Changes to Features Section, General Description Section, and Product Highlights Section ... 1
Deleted S, K, B, and T Grades Throughout ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 5
Added Typical Performance Characteristics Summary ... 6
Change to Figure 7 ... 7
Changes to Figure 15, Figure 17, and Figure 18 ... 8
Deleted Figure 9 and Figure 10; Renumbered Sequentially ... 9
Changes to Figure 23 Caption and Figure 24 Caption ... 10
Added Test Circuits Section ... 11
Moved Figures 26, Figure 27, and Figure 28 ... 11
Changes to Figure 29 ... 12
Changes to DAC Buffers (I-to-V Converters) Section ... 13
Changes to Figure 37 and Table 5 ... 14
Changed C1 to C_L ... 14
Changes to Figure 43 and Figure 44 ... 15
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 19

10/01—Rev. B to Rev. C

Edits to Features ... 1
Edits to Product Description ... 1
Edits to Ordering Guide ... 3
Edits to Metallization Photograph ... 3

SPECIFICATIONS

V_S = ±15 V at T_A = 25°C, unless otherwise noted.

Table 1.

		AD713J/AD713A			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Unit**
INPUT OFFSET VOLTAGE[1]					
Initial Offset			0.3	1.5	mV
Offset	T_{MIN} to T_{MAX}		0.5	2	mV
vs. Temp			5		µV/°C
vs. Supply		78	95		dB
	T_{MIN} to T_{MAX}	76	95		dB
Long-Term Stability			15		µV/Month
INPUT BIAS CURRENT[2]	V_{CM} = 0 V		40	150	pA
	V_{CM} = 0 V at T_{MAX}			3.4/9.6	nA
	V_{CM} = ±10 V		55	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		10	75	pA
	V_{CM} = 0 V at T_{MAX}			1.7/4.8	pA
MATCHING CHARACTERISTICS					
Input Offset Voltage			0.5	1.8	mV
	T_{MIN} to T_{MAX}		0.7	2.3	mV
Input Offset Voltage Drift			8		µV/°C
Input Bias Current			10	100	pA
Crosstalk	f = 1 kHz			−130	dB
	f = 100 kHz			−95	dB
FREQUENCY RESPONSE					
Small Signal Bandwidth	G = −1	3.0	4.0		MHz
Full Power Response	V_O = 20 V p-p		200		kHz
Slew Rate	G = −1	16	20		V/µs
Settling Time to 0.01%			1.0	1.2	µs
Total Harmonic Distortion	f = 1 kHz; $R_L \geq 2$ kΩ; V_O = 3 V rms		0.0003		%
INPUT IMPEDANCE					
Differential[3]			3×10^{12}||5.5		Ω||pF
Common Mode[4]			3×10^{12}||5.5		Ω||pF
INPUT VOLTAGE RANGE					
Differential			±20		V
Common-Mode Voltage			+14.5/−11.5		V
	T_{MIN} to T_{MAX}	−11		+13	V
Common Mode	V_{CM} = ±10 V	78	88		dB
Rejection Ratio	T_{MIN} to T_{MAX}	76	84		dB
	V_{CM} = ±11 V	72	84		dB
	T_{MIN} to T_{MAX}	70	80		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		2		µV p-p
	f = 10 Hz		45		nV/√Hz
	f = 100 Hz		22		nV/√Hz
	f = 1 kHz		18		nV/√Hz
	f = 10 kHz		16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V; $R_L \geq 2$ kΩ	150	400		V/mV
	T_{MIN} to T_{MAX}	100			V/mV

Parameter	Test Conditions/Comments	AD713J/AD713A Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Voltage	$R_L \geq 2\ k\Omega$	+13/−12.5	+13.9/−13.3		V
	T_{MIN} to T_{MAX}	±12	+13.8/−13.1		V
Current	Short circuit		25		mA
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±4.5		±18	V
Quiescent Current			10.0	13.5	mA
TRANSISTOR COUNT	Number of transistors		120		

[1] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = 25°C.
[2] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = 25°C. For higher temperatures, the current doubles every 10°C.
[3] Defined as the voltage between inputs, such that neither exceeds ±10 V from ground.
[4] Typically exceeding −14.1 V negative common-mode voltage on either input results in an output phase reversal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage[1]	±18 V
Output Short-Circuit Duration	
(For One Amplifier)	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD713J	0°C to 70°C
AD713A	−40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C

[1] For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead PDIP (N-14)	100	30	°C/W
14-Lead CERDIP (Q-14)	110	30	°C/W
16-Lead SOIC_W (RW-16)	100	30	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15 V at T_A = 25°C, unless otherwise noted.

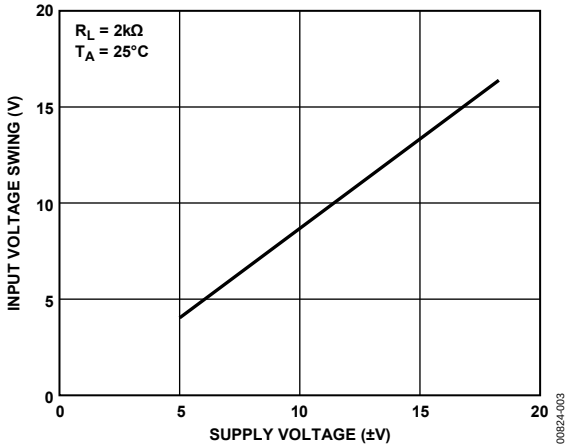


Figure 3. Input Voltage Swing vs. Supply Voltage

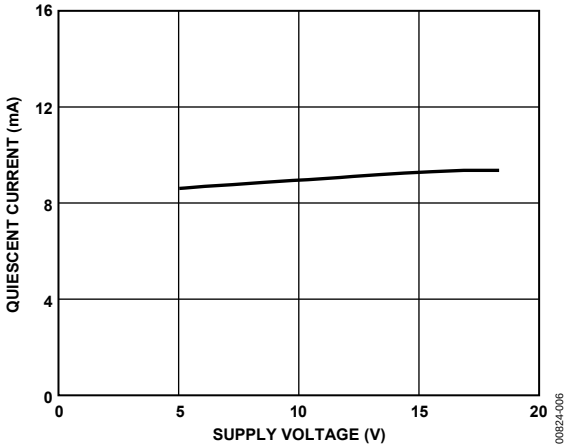


Figure 6. Quiescent Current vs. Supply Voltage

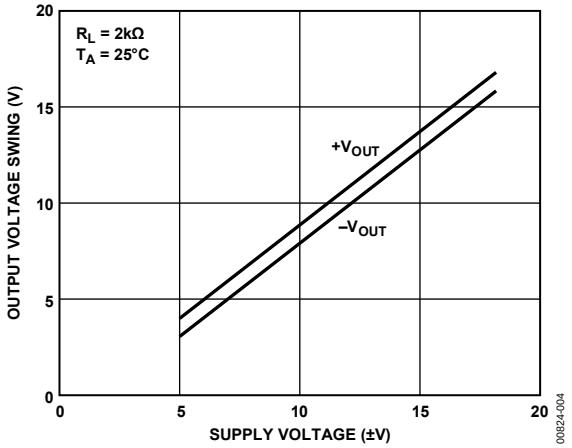


Figure 4. Output Voltage Swing vs. Supply Voltage

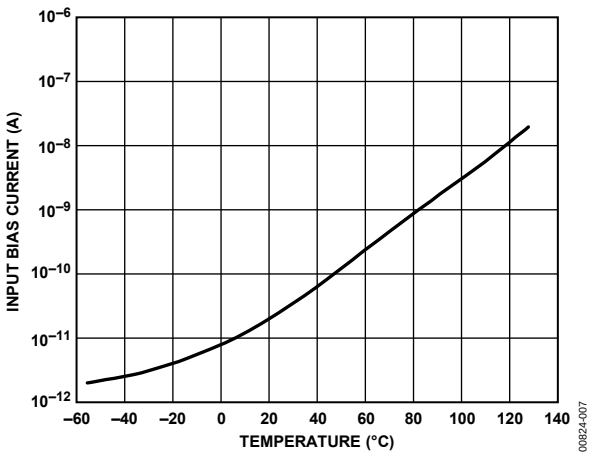


Figure 7. Input Bias Current vs. Temperature

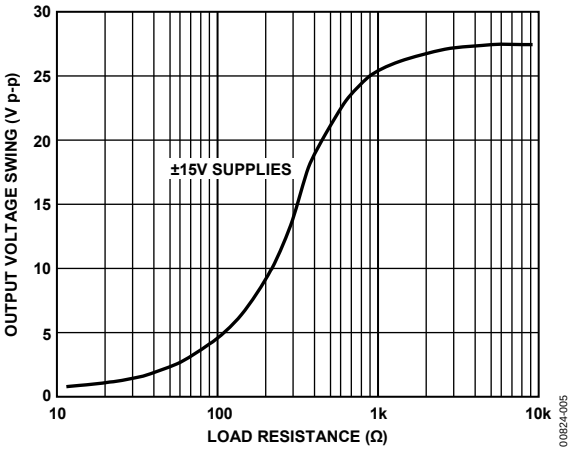


Figure 5. Output Voltage Swing vs. Load Resistance

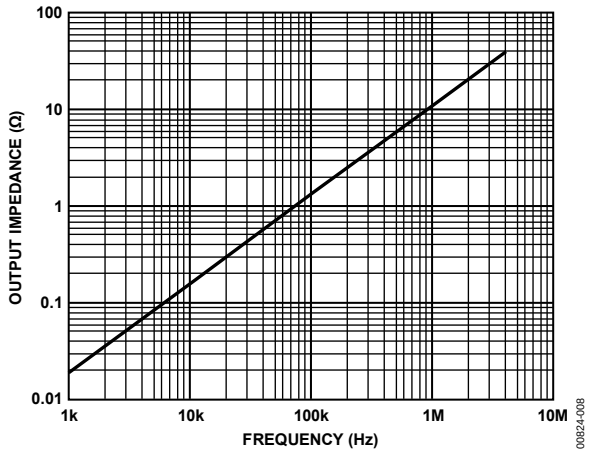


Figure 8. Output Impedance vs. Frequency, G = 1

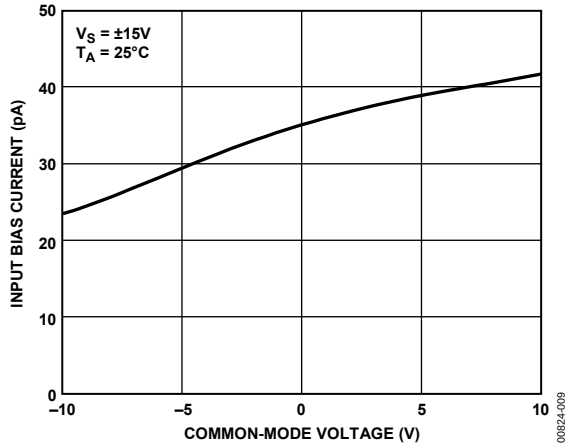


Figure 9. Input Bias Current vs. Common Mode Voltage

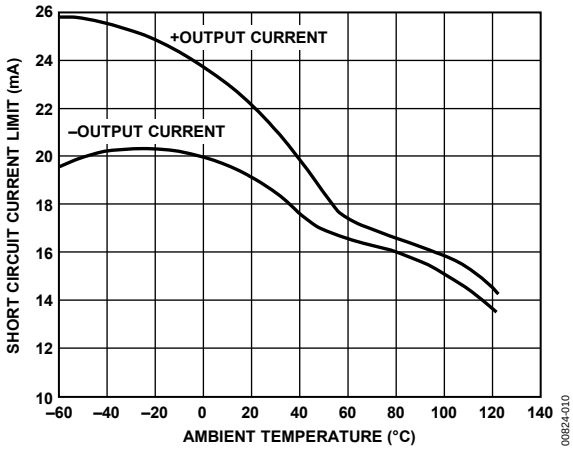


Figure 10. Short-Circuit Current Limit vs. Temperature

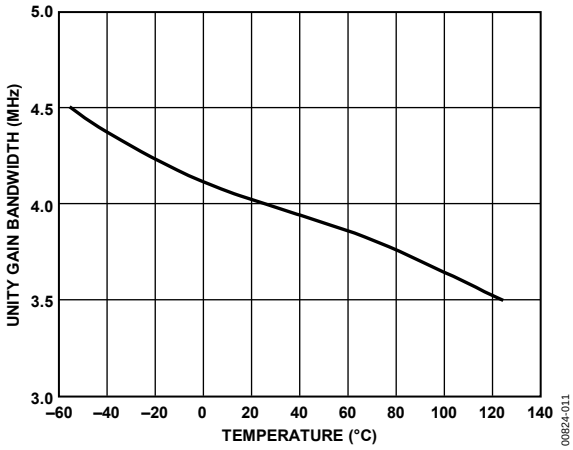


Figure 11. Gain Bandwidth vs. Temperature

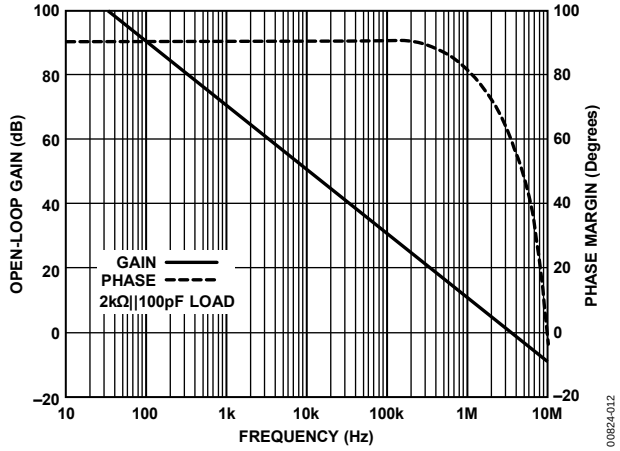


Figure 12. Open-Loop Gain and Phase Margin vs. Frequency

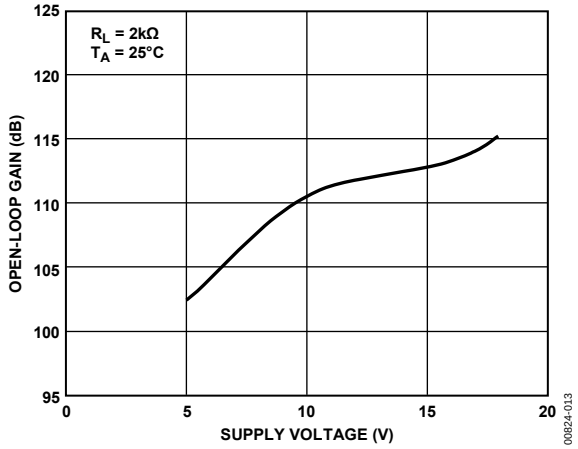


Figure 13. Open-Loop Gain vs. Supply Voltage

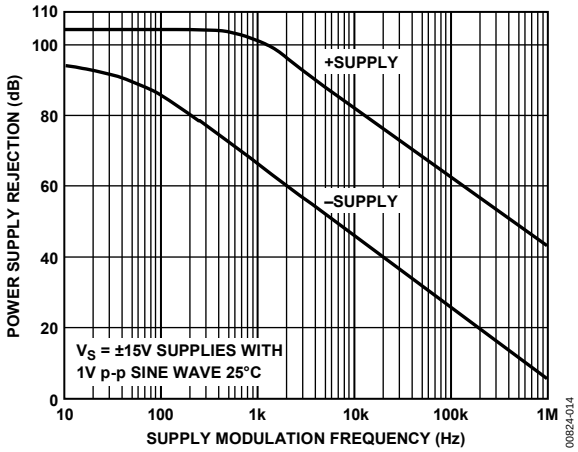


Figure 14. Power Supply Rejection vs. Frequency

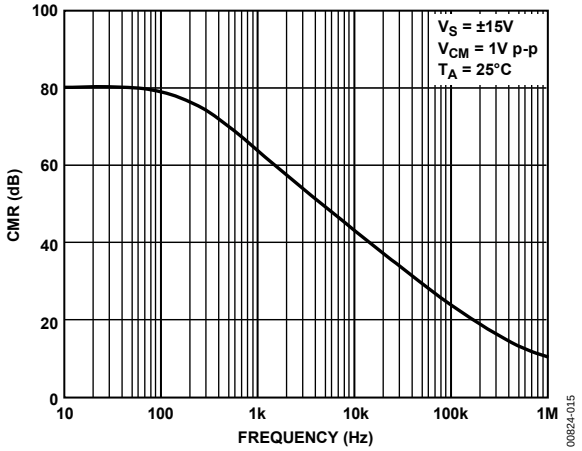


Figure 15. Common-Mode Rejection vs. Frequency

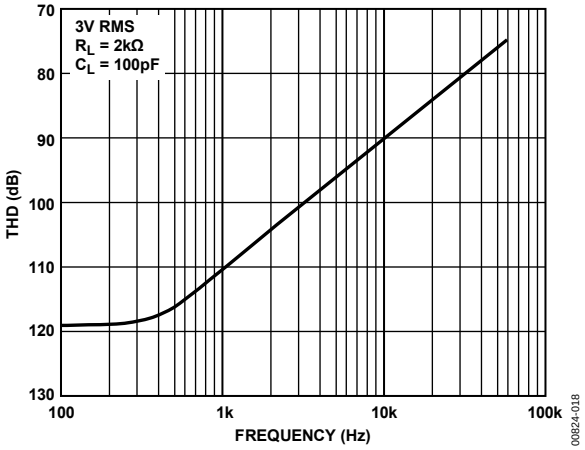


Figure 18. Total Harmonic Distortion vs. Frequency

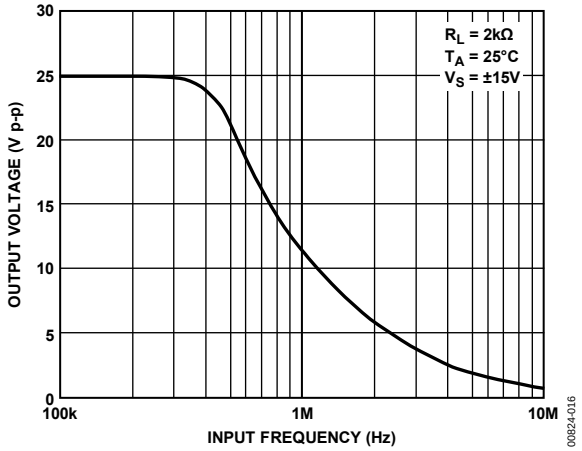


Figure 16. Large Signal Frequency Response

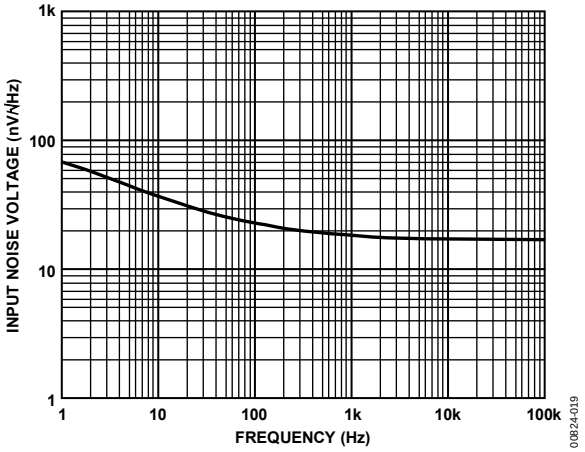


Figure 19. Input Noise Voltage Spectral Density

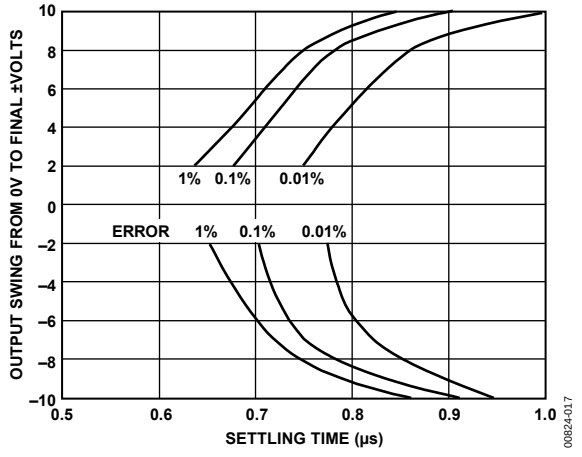


Figure 17. Output Swing and Error vs. Settling Time

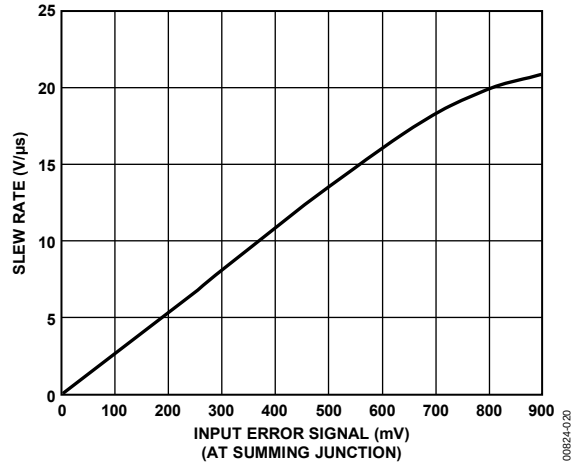


Figure 20. Slew Rate vs. Input Error Signal

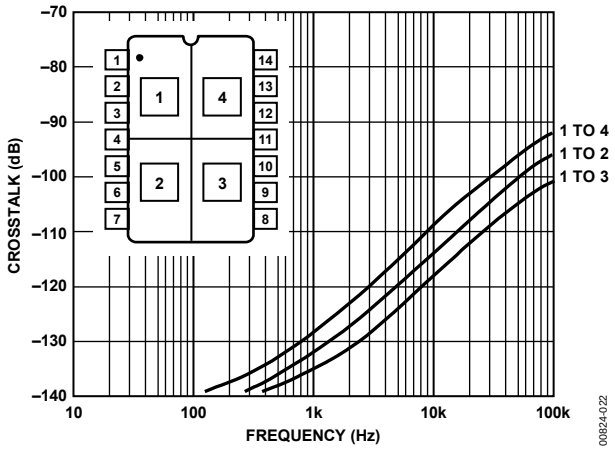


Figure 21. Crosstalk vs. Frequency (see Figure 26 for Test Circuit)

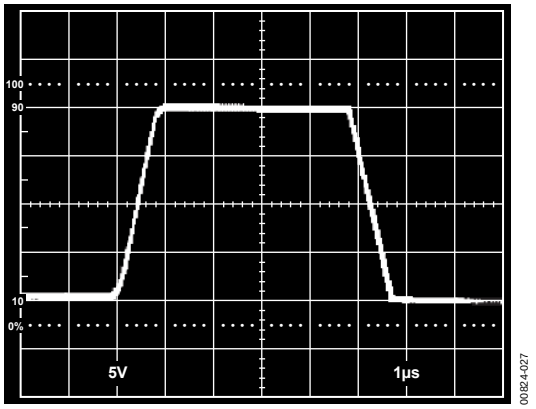


Figure 24. Unity Gain Inverter Pulse Response—Small Signal (see Figure 28)

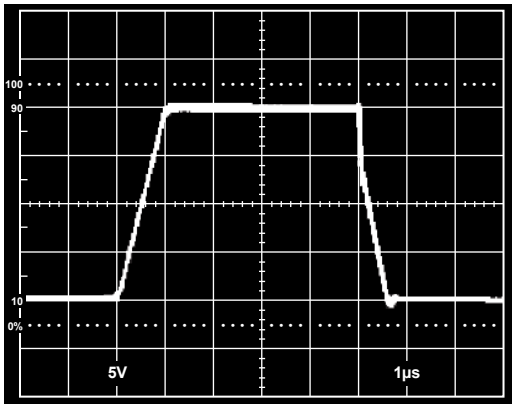


Figure 22. Unity Gain Follower Pulse Response—Large Signal (see Figure 27 for Test Circuit)

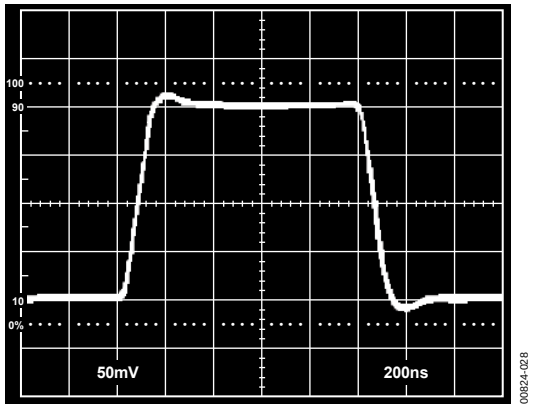


Figure 25. Unity Gain Inverter Pulse Response—Small Signal (see Figure 28)

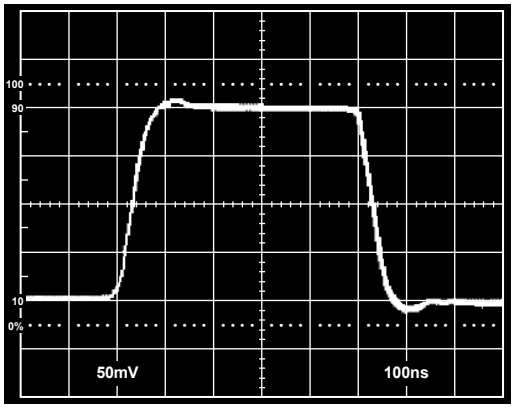


Figure 23. Unity Gain Follower Pulse Response—Small Signal (see Figure 27)

TEST CIRCUITS

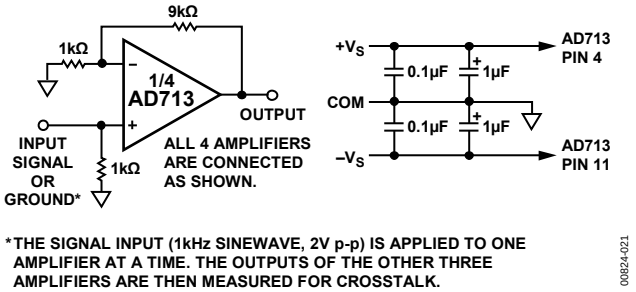


Figure 26. Crosstalk Test Circuit for Figure 21

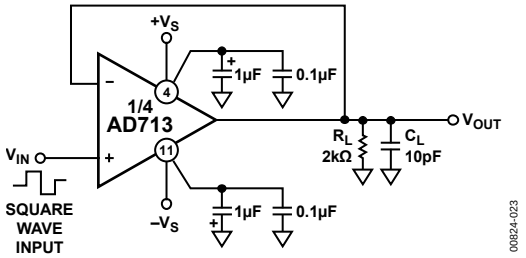


Figure 27. Unity Gain Follower Circuit for Figure 22 and Figure 23

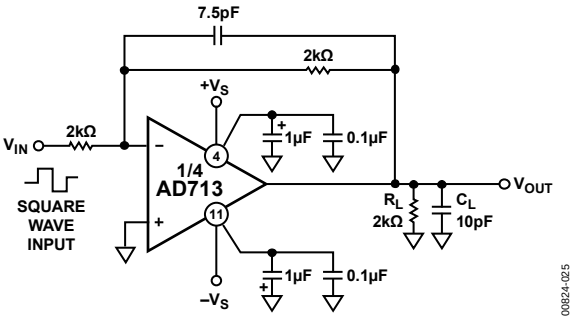


Figure 28. Unity Gain Inverter Circuit for Figure 24 and Figure 25

THEORY OF OPERATION

MEASURING AD713 SETTLING TIME

Figure 30 and Figure 31 show the dynamic response of the AD713 while operating in the settling time test circuit of Figure 29. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD713 under test, is clamped, amplified by Op Amp A2, and then clamped again.

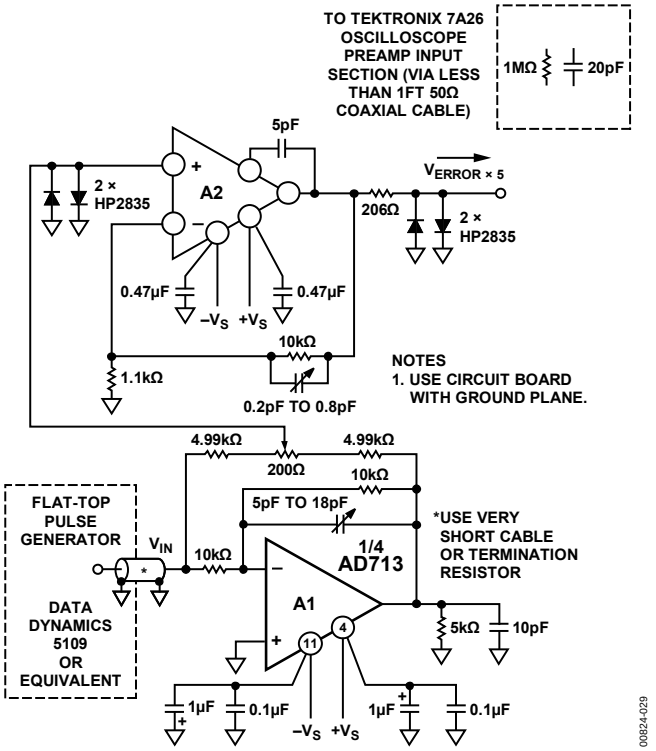


Figure 29. Settling Time Test Circuit

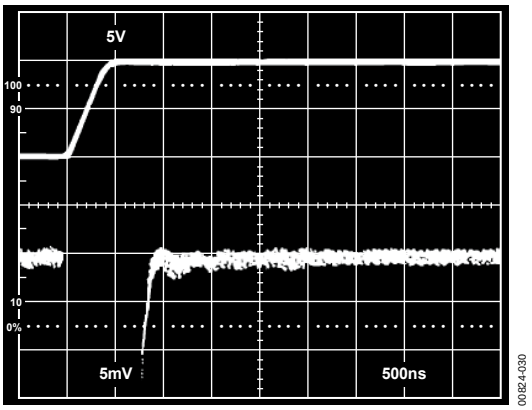


Figure 30. Settling Characteristics 0 V to 10 V Step, Upper Trace: Output of AD713 Under Test (5 V/div), Lower Trace: Amplified Error Voltage (0.01%/div)

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp Type 7A26 was carefully chosen because it recovers from the approximately 0.4 V overload quickly enough to allow accurate measurement of the AD713 1 µs settling time. Amplifier A2 is a very high speed FET input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD713 under test (providing an overall gain of 5).

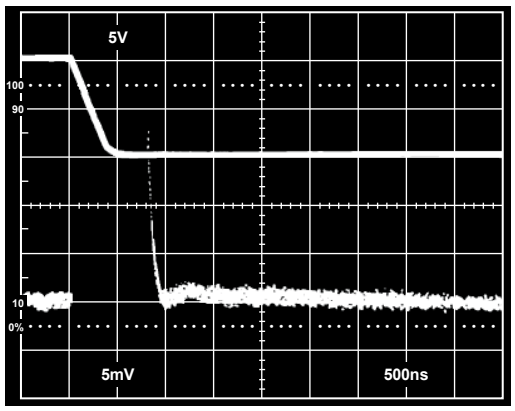


Figure 31. Settling Characteristics to –10 V Step, Upper Trace: Output of AD713 Under Test (5 V/div), Lower Trace: Amplified Error Voltage (0.01%/div)

POWER SUPPLY BYPASSING

The power supply connections to the AD713 must maintain a low impedance to ground over a bandwidth of 4 MHz or more. This is especially important when driving a significant resistive or capacitive load because all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. As shown in Figure 32, a 0.1 µF ceramic and a 1 µF electrolytic capacitor placed as close as possible to the amplifier (with short lead lengths to power supply common) assures adequate high frequency bypassing in most applications. A minimum bypass capacitance of 0.1 µF should be used for any application.

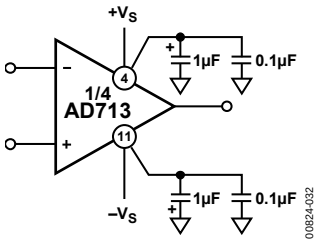


Figure 32. Recommended Power Supply Bypassing

A HIGH SPEED INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 33 can provide a range of gains from unity up to 1000 and higher using only a single AD713. The circuit bandwidth is 1.2 MHz at a gain of 1 and 250 kHz at a gain of 10; settling time for the entire circuit is less than 5 µs to within 0.01% for a 10 V step, (G = 10). Other uses for Amplifier A4 include an active data guard and an active sense input.

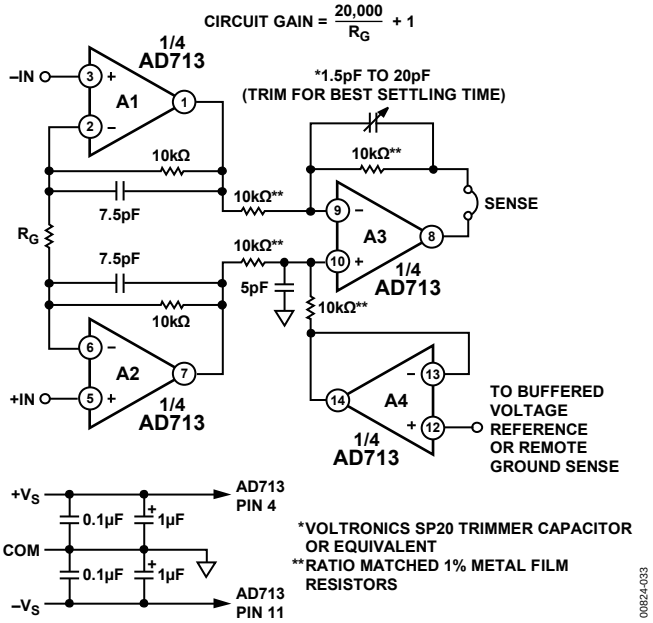


Figure 33. High Speed Instrumentation Amplifier Circuit

Table 4 provides a performance summary for this circuit. Figure 34 shows the pulse response of this circuit for a gain of 10.

Table 4. Performance Summary for the High Speed Instrumentation Amplifier Circuit

Gain	R_G	Bandwidth	Settling Time (0.01%)
1	NC[1]	1.2 MHz	2 µs
2	20 kΩ	1.0 MHz	2 µs
10	4.04 kΩ	0.25 MHz	2 µs

[1] NC = no connect.

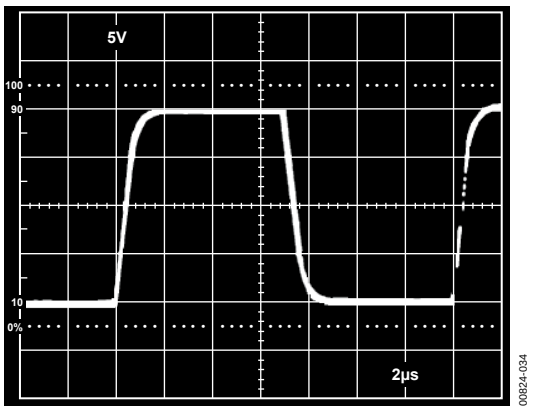


Figure 34. Pulse Response of High Speed Instrumentation Amplifier, Gain = 10

A HIGH SPEED 4-OP-AMP CASCADED AMPLIFIER CIRCUIT

Figure 35 shows how the four amplifiers of the AD713 can be connected in cascade to form a high gain, high bandwidth amplifier. This gain of 100 amplifier has a −3 dB bandwidth greater than 600 kHz.

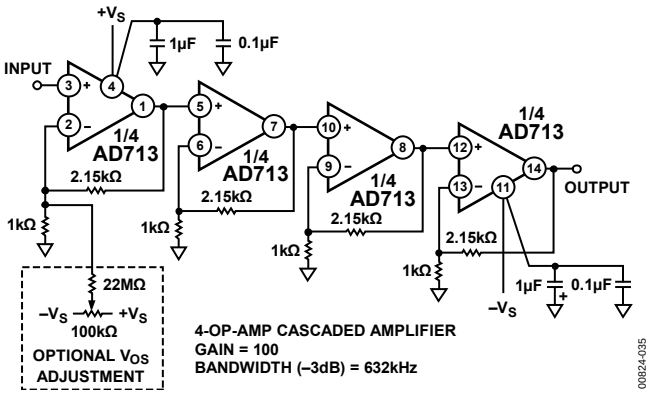


Figure 35. High Speed 4-Op-Amp Cascaded Amplifier Circuit

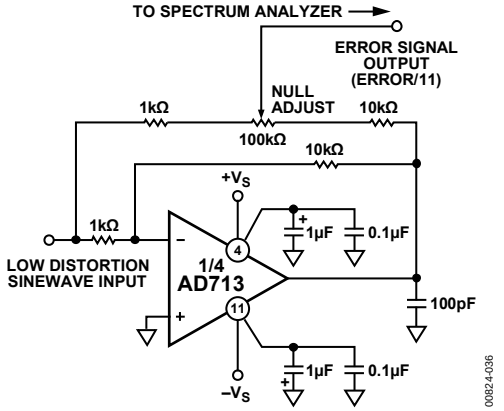


Figure 36. THD Test Circuit

HIGH SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

The wide input dynamic range of JFET amplifiers makes them ideal for use in both waveform reconstruction and digital audio DAC applications. The AD713, in conjunction with a 16-bit DAC, can achieve 0.0016% THD without requiring the use of a deglitcher in digital audio applications.

Driving the Analog Input of an Analog-to-Digital Converter

An op amp driving the analog input of an analog-to-digital converter (ADC), such as that shown in Figure 37, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may vary by several hundred millivolts, resulting in high frequency modulation of the analog-to-digital input current. The output impedance of a feedback amplifier is made artificially low by its

loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value.

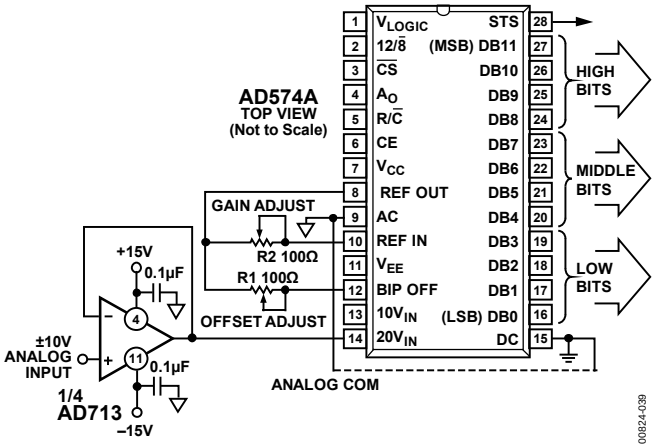


Figure 37. AD713 as an ADC Buffer

Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω, due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the analog-to-digital conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier output returns to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidths, yielding slow recovery from output transients. The AD713 is ideally suited as a driver for ADCs because it offers both a wide bandwidth and a high open-loop gain.

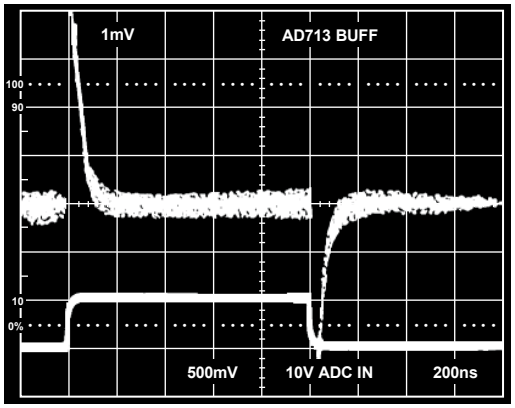


Figure 38. Buffer Recovery Time Source Current = 2 mA

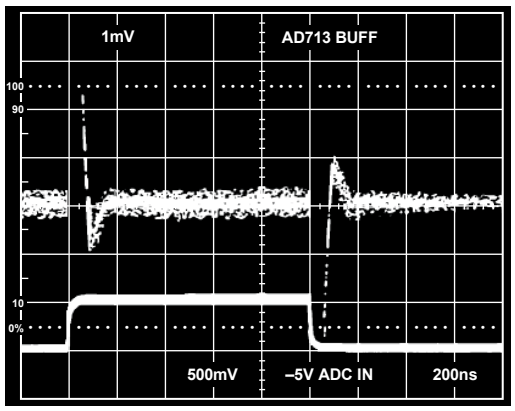


Figure 39. Buffer Recovery Time Sink Current = 1 mA

Driving A Large Capacitive Load

The circuit of Figure 40 uses a 100 Ω isolation resistor that enables the amplifier to drive capacitive loads exceeding 1500 pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low-pass filter formed by the 100 Ω series resistor and the load capacitance, C_L. Figure 41 shows a typical transient response for this connection.

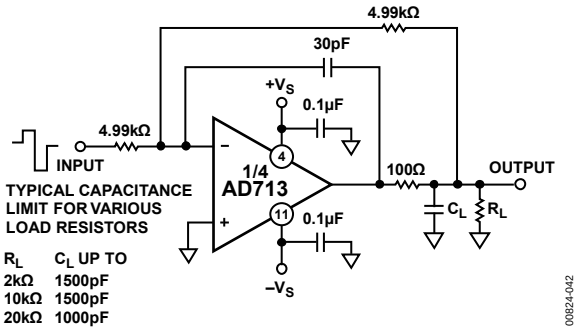


Figure 40. Circuit for Driving a Large Capacitance Load

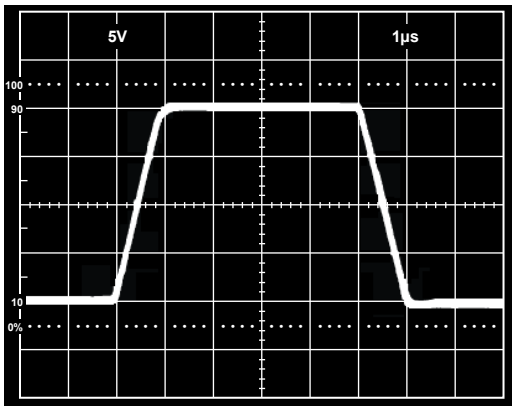


Figure 41. Transient Response, R_L = 2 kΩ, C_L = 500 pF

CMOS DAC APPLICATIONS

The AD713 is an excellent output amplifier for CMOS DACs. It can be used to perform both two- and four-quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and infinity for codes containing all 0s.

For example, the output resistance of the AD7545 modulates between 11 kΩ and 33 kΩ. Therefore, with the DAC's internal feedback resistance of 11 kΩ, the noise gain varies from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC amplifier performance. The AD713, with its guaranteed 1.5 mV input offset voltage, minimizes this effect, achieving 12-bit performance.

Figure 42 and Figure 43 show the AD713 and a 12-bit CMOS DAC, the AD7545, configured for either a unipolar binary (two-quadrant multiplication) or bipolar (four-quadrant multiplication) operation. Capacitor C1 provides phase compensation, which reduces overshoot and ringing.

Table 5. Recommended Trim Resistor Values vs. Grades for AD7545 for V_D = 5 V

Trim Resistor	JN/AQ	KN/BQ	LN/CQ	GLN/GCQ
R1	500 Ω	200 Ω	100 Ω	20 Ω
R2	150 Ω	68 Ω	33 Ω	6.8 Ω

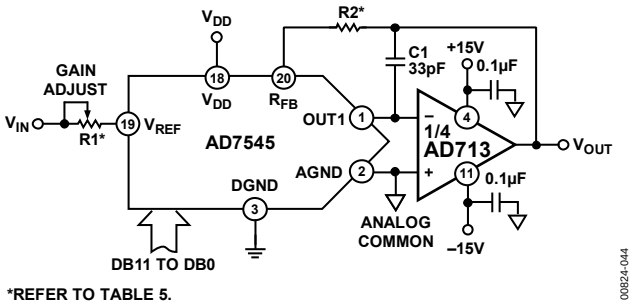


Figure 42. Unipolar Binary Operation

FILTER APPLICATIONS

A Programmable State Variable Filter

For the state variable or universal filter configuration of Figure 44 to function properly, DAC A1 and DAC B1 must control the gain and Q of the filter characteristic, and DAC A2 and DAC B2 must accurately track for the simple expression of f_C to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp gain bandwidth limitations.

This filter provides low-pass, high-pass, and band-pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required. The programmable range for component values shown is f_C = 0 kHz to 15 kHz and Q = 0.3 to 4.5.

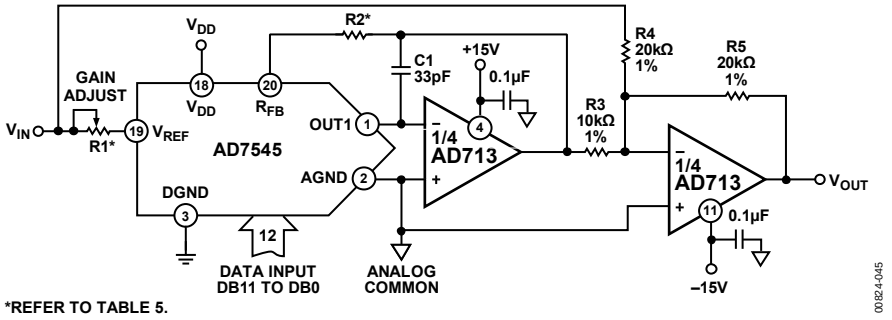


Figure 43. Bipolar Operation

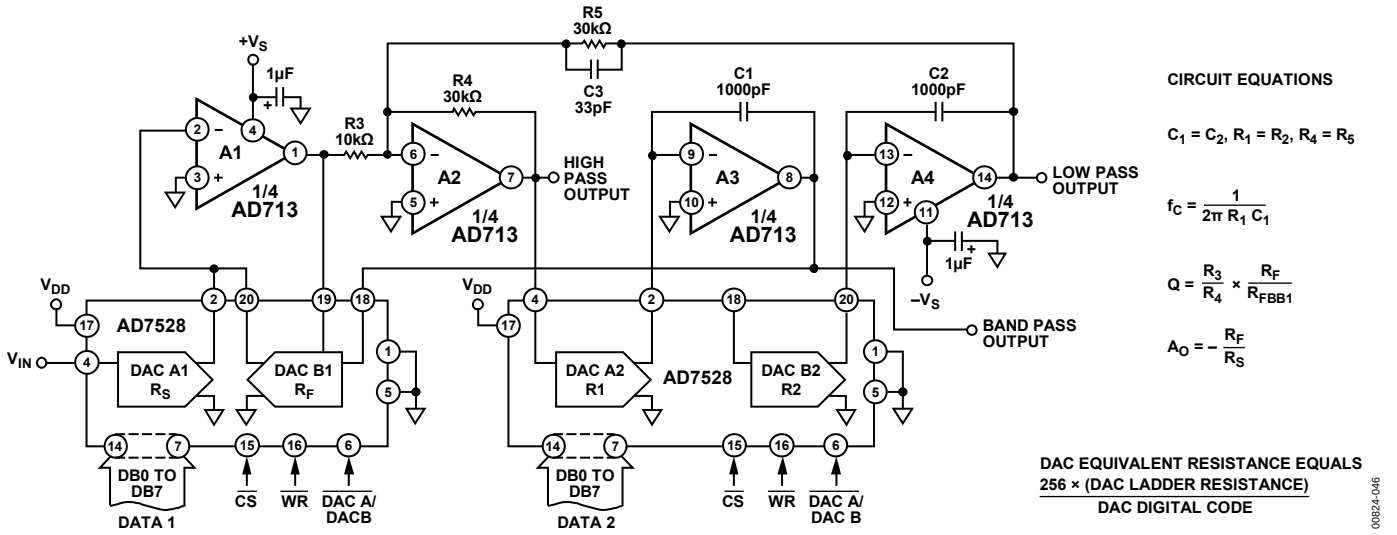


Figure 44. A Programmable State Variable Filter Circuit

GIC AND FDNR FILTER APPLICATIONS

The closely matched and uniform ac characteristics of the AD713 make it ideal for use in generalized impedance converter (GIC)/gyrator and frequency dependent negative resistor (FDNR) filter applications. Figure 47 and Figure 48 show the AD713 used in two typical active filters. The first shows a single AD713 simulating two coupled inductors configured as a one-third octave band-pass filter. A single section of this filter meets ANSI Class II specifications and handles a 7.07 V rms signal with <0.002% THD (20 Hz to 20 kHz).

Figure 48 shows a seven-pole antialiasing filter for a 2× oversampling (88.2 kHz) digital audio application. This filter has <0.05 dB pass-band ripple and 19.8 µs ± 0.3 µs delay, at dc to 20 kHz, and handles a 5 V rms signal (V_S = ±15 V) with no overload at any internal nodes.

The filter of Figure 47 can be scaled for any center frequency by using the following formula:

$$f_C = \frac{1.11}{2\pi RC}$$

where all resistors and capacitors scale equally. Resistors R3 to R8 should not be greater than 2 kΩ in value to prevent parasitic oscillations caused by the amplifier's input capacitance.

If this is not practical, add small lead capacitances (10 pF to 20 pF) across R5 and R6. Figure 45 and Figure 46 show the output amplitude vs. frequency of these filters.

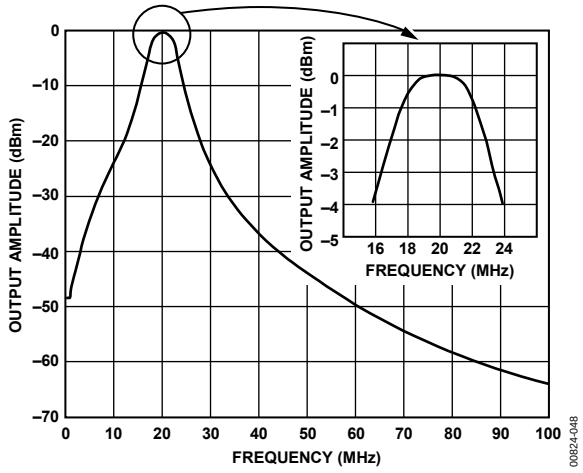


Figure 45. Output Amplitude vs. Frequency of 1/3 Octave Filter

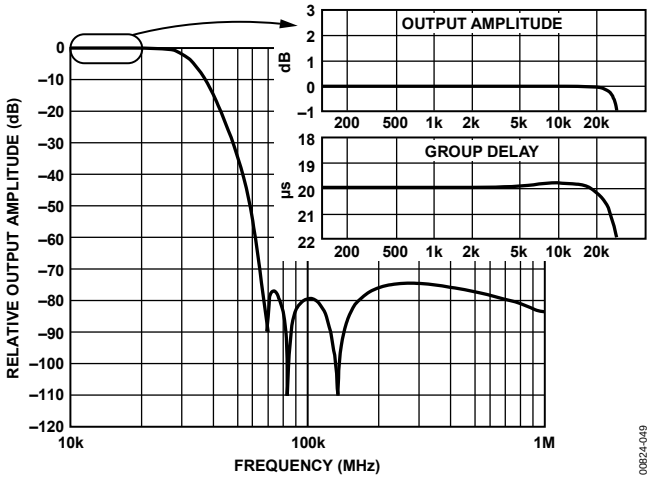


Figure 46. Relative Output Amplitude vs. Frequency of Antialiasing Filter

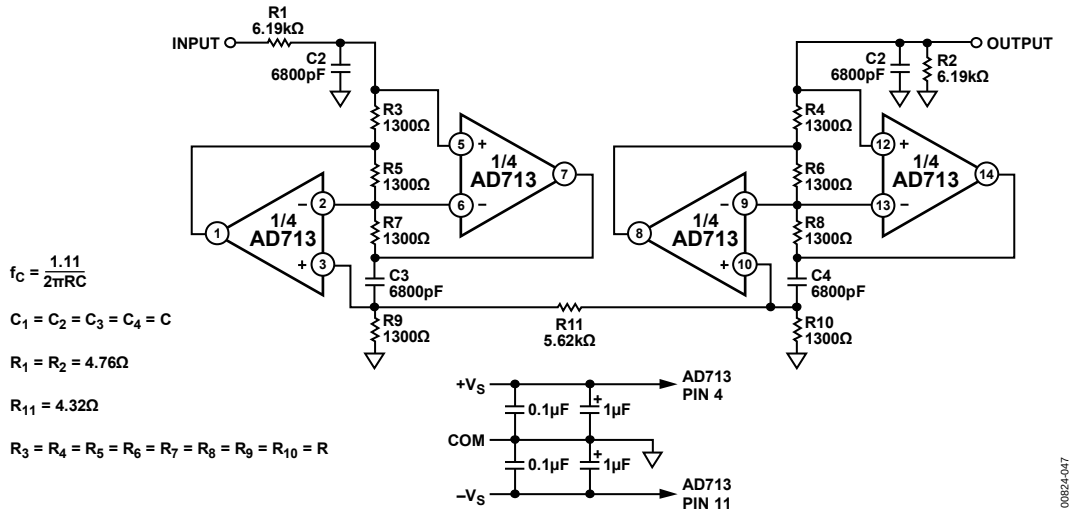


Figure 47. A 1/3 Octave Filter Circuit

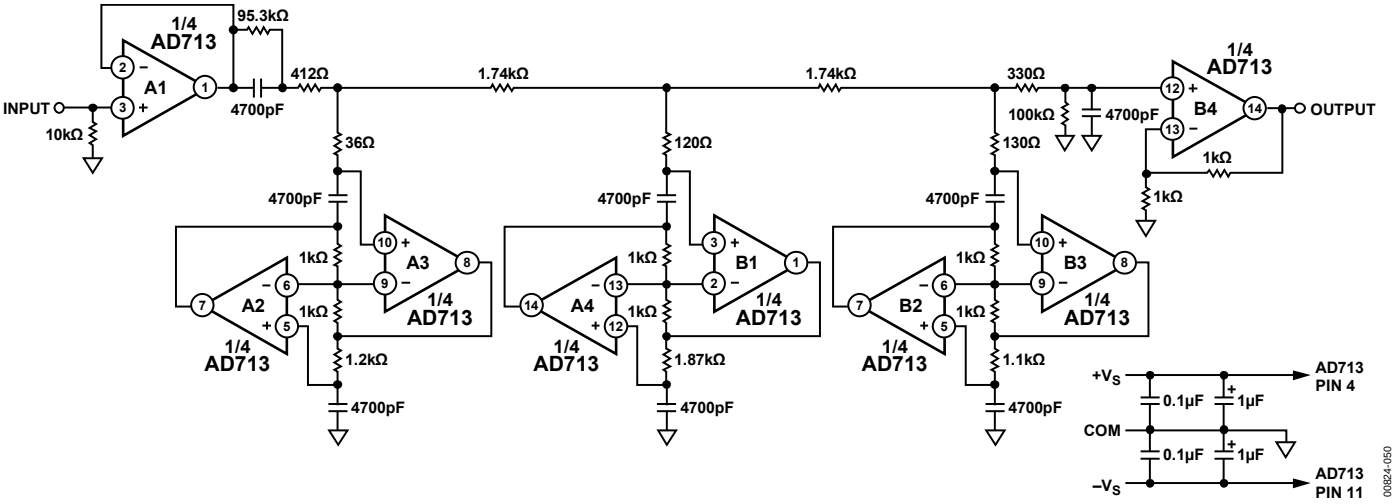
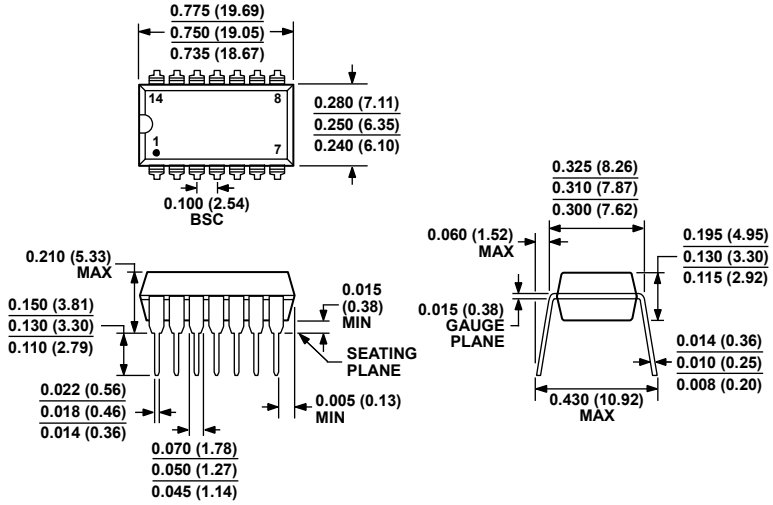


Figure 48. An Antialiasing Filter

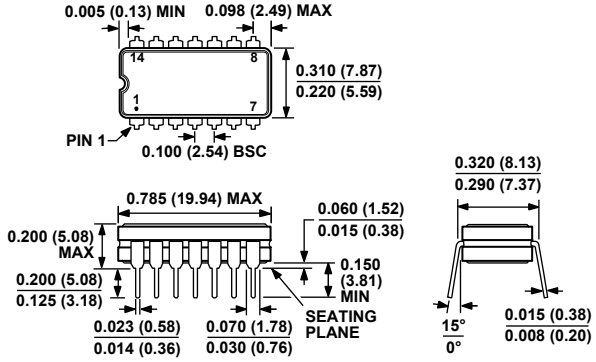
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 49. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-14)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Dimensions shown in inches and (millimeters)

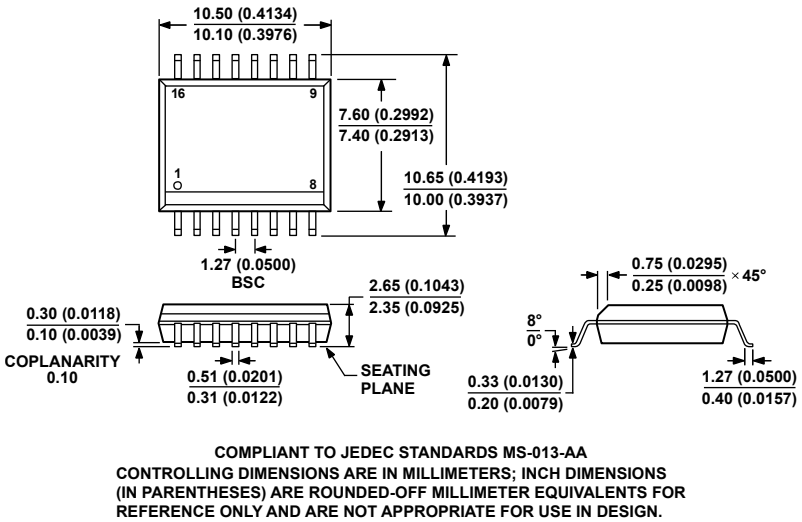


Figure 51. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD713AQ	−40°C to +85°C	14-Lead CERDIP	Q-14
AD713JNZ	0°C to 70°C	14-Lead PDIP	N-14
AD713JR-16	0°C to 70°C	16-Lead SOIC_W	RW-16
AD713JR-16-REEL	0°C to 70°C	16-Lead SOIC_W	RW-16
AD713JR-16-REEL7	0°C to 70°C	16-Lead SOIC_W	RW-16
AD713JRZ-16	0°C to 70°C	16-Lead SOIC_W	RW-16
AD713JRZ-16-REEL	0°C to 70°C	16-Lead SOIC_W	RW-16
AD713JRZ-16-REEL7	0°C to 70°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D00824-0-7/11(F)