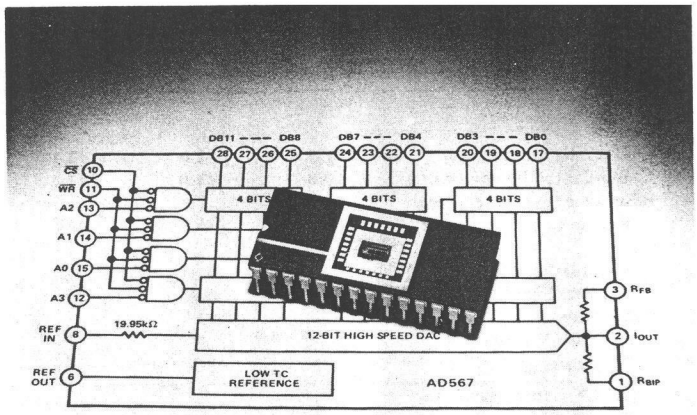
Microprocessor-Compatible 12-Bit D/A Converter

AD567



FEATURES

- Single Chip Construction
- Double-Buffered Latch for 8-Bit μP-Compatibility
- Fast Settling Time: 500ns max to ±1/2LSB
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K)
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs
- Low Cost

PRODUCT DESCRIPTION

The AD567 is a complete high speed 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD567 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD567 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K grade) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD567 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD567 is available in three performance grades. The AD567J and K are specified for use over the 0 to +70°C temperature range and are available in either a 28-pin hermetically-sealed, ceramic DIP or a 28-pin molded plastic DIP (N package). The AD567S grade is specified for the −55°C to +125°C range and is available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The AD567 is a complete current output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for an A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current switch design* provides high dc accuracy and an optimally-damped settling characteristic. Output current settling time is 500 nanoseconds maximum to ±1/2LSB.
6. The single-chip construction makes the AD567 inherently more reliable than multichip hybrid designs. The AD567S grade with guaranteed linearity and monotonicity over the −55°C to +125°C range is especially recommended for high reliability needs in harsh environments. The unit is available processed to MIL-STD-883, Level B.

***Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.**

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SPECIFICATIONS (T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = -12V or -15V, unless otherwise specified)

MODEL	AD567J MIN	AD567J TYP	AD567J MAX	AD567K MIN	AD567K TYP	AD567K MAX	UNITS
DATA INPUTS[1] (Pins 10-15 and 17-28)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-17	-25		-17	-25	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 1, 2, 3)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)	0.1	1.0		0.1	1.0		mA
POWER DISSIPATION		300	495		300	495	mW
PRICE (100+)		AD567JN	$12.95		AD567KN	$17.95	
		AD567JD	$14.95		AD567KD	$22.95	

NOTES

[1] The digital input specifications are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc ±10%.

Specifications subject to change without notice.

MODEL	AD567SD/AD567SD/883B MIN	TYP	MAX	UNITS
DATA INPUTS[1] (Pins 10–15 and 17–28)				
TTL or 5 Volt CMOS				
Input Voltage				
Bit ON Logic "1"	+2.0		+5.5	V
Bit OFF Logic "0"			+0.7	V
Logic Current (each bit)				
Bit ON Logic "1"		+120	+300	μA
Bit OFF Logic "0"		+35	+100	μA
RESOLUTION			12	Bits
OUTPUT				
Current				
Unipolar (all bits on)	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	Ω
Offset				
Unipolar		0.01	0.05	% of F.S.
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15	% of F.S.
Capacitance		25		pF
Compliance Voltage				
T_{min} to T_{max}	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2	LSB
		(0.006)	(0.012)	% of F.S.
T_{min} to T_{max}		±1/2	±3/4	LSB
		(0.012)	(0.018)	% of F.S.
DIFFERENTIAL NONLINEARITY				
+25°C		±1/2	±3/4	LSB
T_{min} to T_{max}		MONOTONICITY GUARANTEED		
TEMPERATURE COEFFICIENTS				
With Internal Reference				
Unipolar Zero		1	2	ppm/°C
Bipolar Zero		5	10	ppm/°C
Gain (Full Scale)		15	30	ppm/°C
Differential Nonlinearity		2		ppm/°C
TEMPERATURE RANGE				
Operating	-55		+125	°C
Storage	-65		+150	°C
POWER REQUIREMENTS				
V_{CC}, +11.4 to +16.5V dc		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-17	-25	mA
POWER SUPPLY GAIN SENSITIVITY[2]				
V_{CC} = +11.4 to +16.5V dc		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT				
RANGES (see Figures 1, 2, 3)		0 to +5		V
		-2.5 to +2.5		V
		0 to +10		V
		-5 to +5		V
		-10 to +10		V
EXTERNAL ADJUSTMENTS				
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15	% of F.S.
Gain Adjustment Range (Figure 2)	±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			% of F.S.
REFERENCE INPUT				
Input Impedance	15k	20k	25k	Ω
REFERENCE OUTPUT				
Voltage	9.90	10.00	10.10	V
Current (available for external loads)	0.1	1.0		mA
POWER DISSIPATION		300	495	mW
PRICE (100+)		AD567SD	$59.00	
		AD567SD/883B	$68.00	

Specifications subject to change without notice.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DW}	Data Valid to End of $\overline{WR}$	50	—	—	ns
t_{CW}	$\overline{CS}$ Valid to End of $\overline{WR}$	100	—	—	
t_{AW}	Address Valid to End of $\overline{WR}$	100	—	—	ns
t_{WP}	Write Pulse Width	100	—	—	ns
t_{DH}	Data Hold Time	0	—	—	ns
t_{SETT}	Output Current Settling Time	—	400	500	ns

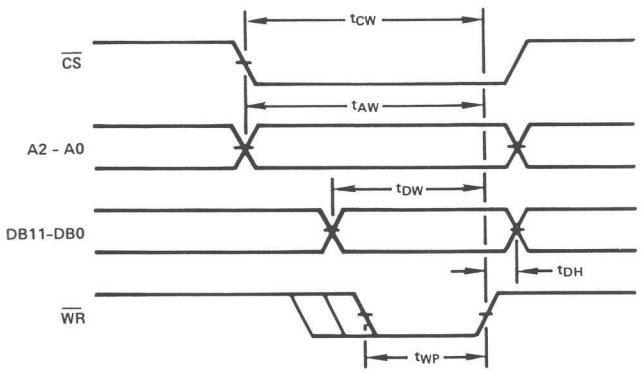
ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . .0V to +18V
V_{EE} to Power Ground . . . . . .0V to −18V
Voltage on DAC Output (Pin 2) . . . . . .−3V to +12V
Digital Inputs (Pins 10–15, 17–28)
to Power Ground. . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out. . . . . .Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

TIMING DIAGRAMS

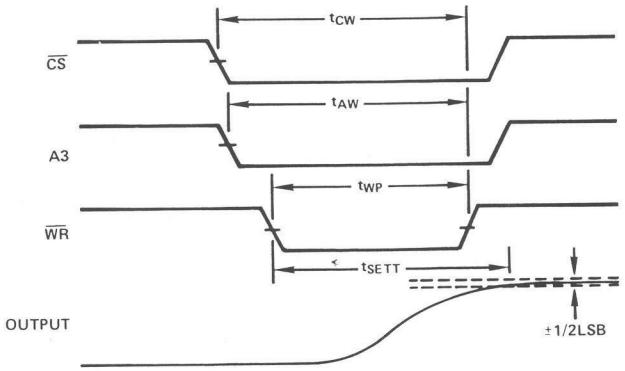
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)



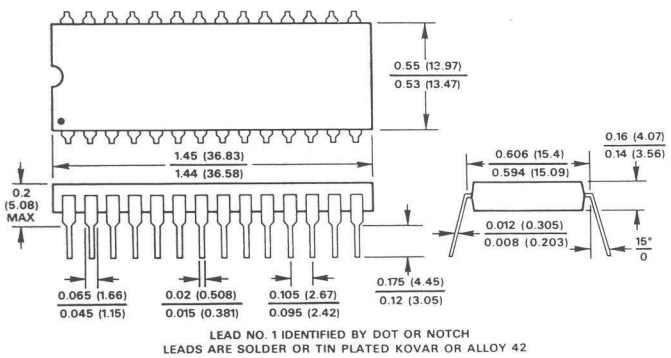
WRITE CYCLE #2

(Load Second Rank from First Rank; A_2, A_1, A_0 = 1)

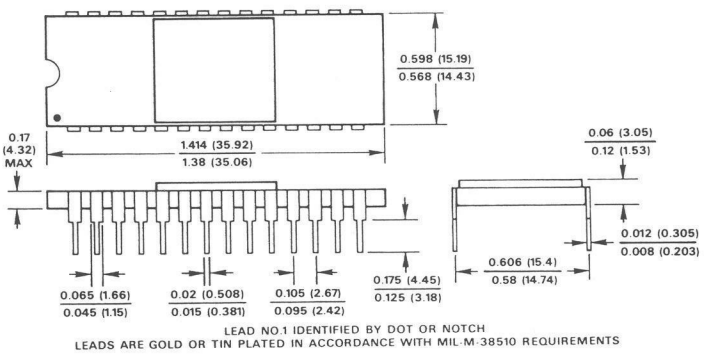


OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



28-Pin Plastic DIP (N Package)

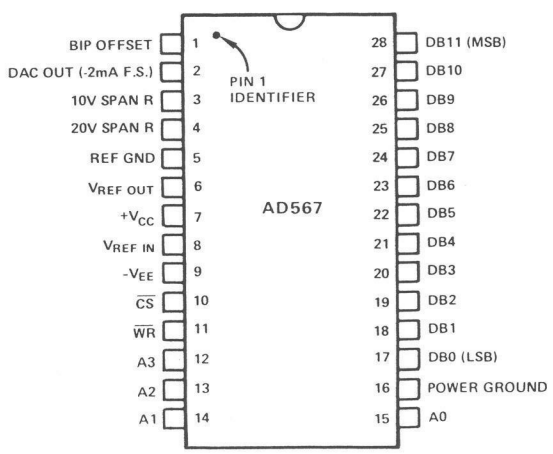


28-Pin Ceramic DIP (D Package)

AD567 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	GAIN T.C. MAX
AD567JN	Plastic	Com	±1/2LSB	50ppm/°C
AD567KN	Plastic	Com	±1/4LSB	20ppm/°C
AD567JD	Ceramic	Com	±1/2LSB	50ppm/°C
AD567KD	Ceramic	Com	±1/4LSB	20ppm/°C
AD567SD	Ceramic	Mil	±1/2LSB	30ppm/°C
AD567SD/883B	Ceramic	Mil	±1/2LSB	30ppm/°C

PIN CONNECTIONS
TOP VIEW



THE AD567 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

RELATIVE ACCURACY: Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD567 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K version and 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of input. All versions of the AD567 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD567K has a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1.0ppm/°C) of error. The resulting error could then be as much as 0.01% + 0.006% (initial error, 1/4LSB) = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD567 are 100% tested for monotonicity over the full operating temperature range.

ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L; AD517L; AD741L; AD301AL; AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD544 is recommended for buffered voltage-output applications which require fast settling time to ±1/2LSB. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

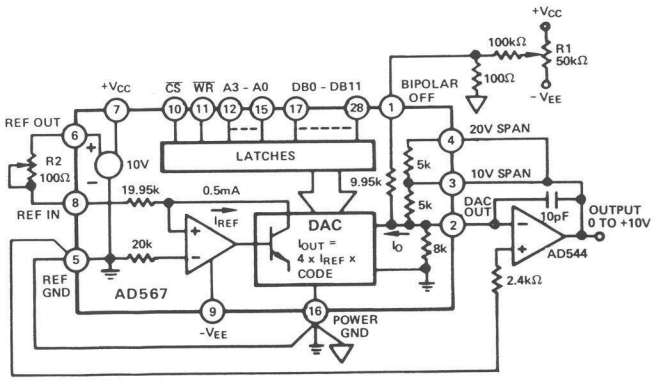


Figure 1. 0 to +10V Unipolar Voltage Output

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 1, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 1 should be connected to pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 3 to the op amp output.

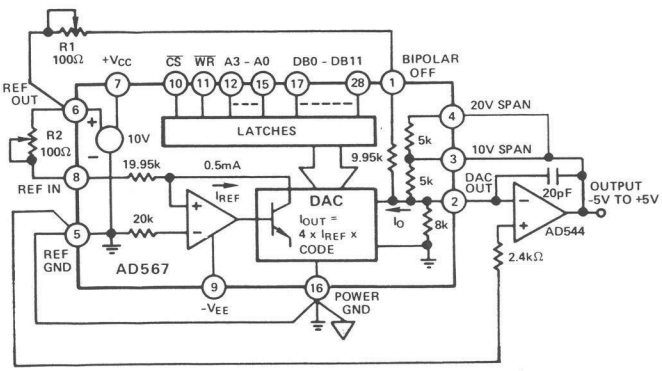


Figure 2. ±5V Bipolar Voltage Output

FIGURE 2. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3 OTHER VOLTAGE RANGES

The AD567 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 4. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 4 to pin 2 and connecting pin 3 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 4 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

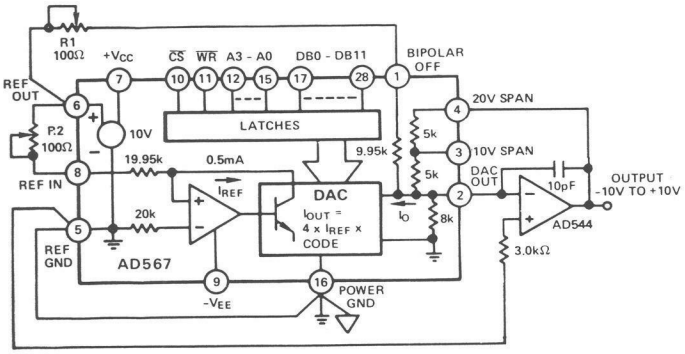


Figure 3. ±10V Voltage Output

The internal resistor values shown in Figures 1, 2, and 3 are nominal values only, as is the output current. These values are subject to an absolute tolerance of approximately ±20%. Furthermore, the resistors in the AD567 exhibit a temperature coefficient of approximately −50ppm/°C. While these absolute tolerances may appear excessively wide, the ratios of the resistor values and tracking TC are extremely well-controlled. In applications where the internal feedback resistor determines the output voltage range it is the ratios which determine the accuracy. However, in applications where the desired full scale range requires use of an external resistor, sufficient trim range must be provided to compensate for the tolerance of the internal resistance.

INTERNAL/EXTERNAL REFERENCE USE

The AD567 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD567 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The AD567 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD567 reference output should be buffered with an external op amp if it is required to supply additional output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

OUTPUT VOLTAGE COMPLIANCE

The AD567 has a typical output compliance range from −1.5 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 4.

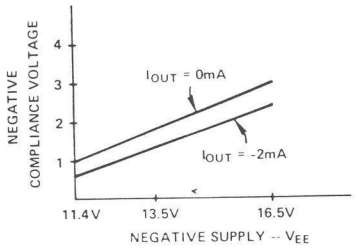


Figure 4. Typical Negative Compliance Range vs. Negative Supply

GROUNDING RULES

The AD567 brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD567; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

It is also important to properly apply decoupling capacitors on the power supplies for the AD567 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of both the AD567 and the amplifier directly to the reference ground pin of the AD567. Any load driven by the output amplifier should also be referred to the reference ground pin.

Output Range	Connect Pin 3 to:	Connect Pin 4 to:	Connect Pin 1 to:
0 to +5V	Amplifier Output	Pin 2	Pin 5
0 to +10V	Amplifier Output	Amplifier Output	Pin 5
−2.5V to +2.5V	Amplifier Output	Pin 2	Pin 6 (through 50Ω)
−5V to +5V	Amplifier Output	Amplifier Output	Pin 6 (through 50Ω)
−10V to +10V	—	Amplifier Output	Pin 6 (through 50Ω)

Table 1. Connections for Various Output Ranges

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD567 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD567 logic section.

The latches are controlled by the address inputs, A0–A3, and the $\overline{CS}$ and $\overline{WR}$ inputs. All control inputs are active low, consistent with general practice in microprocessor systems. The $\overline{CS}$ and $\overline{WR}$ inputs must both be low for any operation to occur. The four address lines each enable one of the four latches, as indicated in Table 2 below.

All latches in the AD567 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

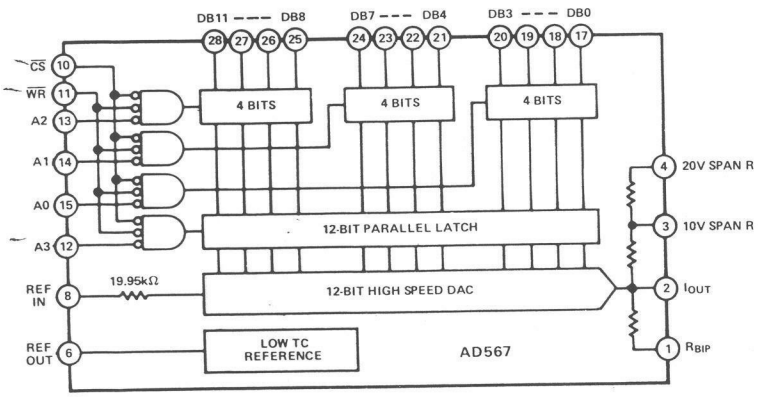


Figure 5. AD567 Block Diagram

$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No Operation
X	1	X	X	X	X	No Operation
0	0	1	1	1	0	Enable 4 LSBs of First Rank
0	0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table 2. AD567 Truth Table

MICROPROCESSOR BUS INTERFACING

The AD567 interface logic is configured with enough flexibility to allow relatively simple interface to the various microprocessor bus structures. The required control signals, $\overline{CS}$ and $\overline{WR}$, are easily derived in most systems. Usually a base address is decoded, and this active-low signal is used for $\overline{CS}$ (Chip Select). Either I/O Write or Memory Write can be used for $\overline{WR}$, depending on the system design. The relative timing of these signals is not important and they are interchangeable.

The address lines determine which of the latches are being enabled. It is permissible to enable two or more latches simultaneously, as in the examples of 8-, 12-, and 16-bit interfaces.

The double-buffered latch permits data to be loaded into the first rank latches of several AD567s and subsequently strobed into the second rank registers of all the DACs. All analog outputs will then update simultaneously.

4-BIT PROCESSOR INTERFACE

Many industrial control applications use four-bit microprocessors but require 12-bit accurate analog control voltages. The AD567 is well suited to these applications, due to its flexible control structure.

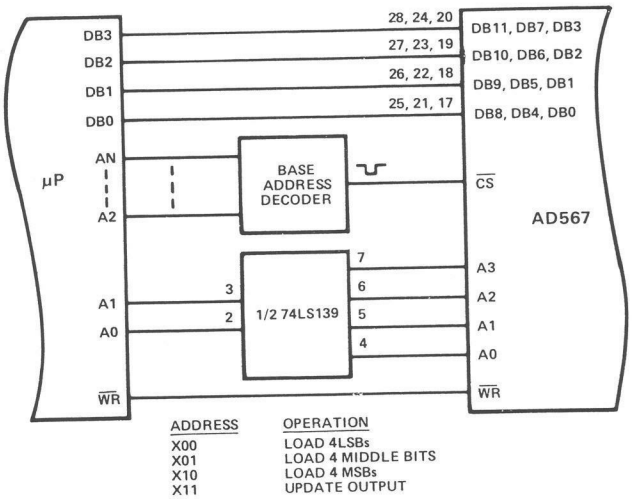


Figure 6. Addressing for 4-Bit Microprocessor Interface

Each AD567 occupies four locations in a 4-bit microprocessor system. A single 74LS139 2-to-4 decoder is used to provide sequential addresses for the four AD567 registers. $\overline{CS}$ is derived from an address decoder driven from the high order address bits. The system $\overline{WR}$ is used for the $\overline{WR}$ input of the AD567.

8-BIT MICROPROCESSOR INTERFACE

The AD567 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

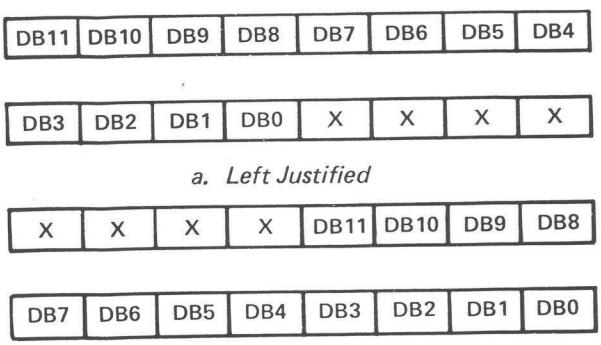


Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD567 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD567 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

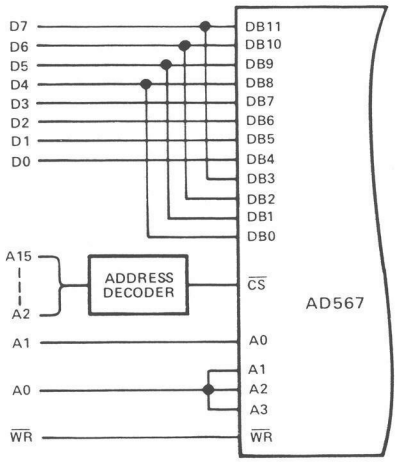


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD567 still occupies two adjacent locations in the processor's memory map.

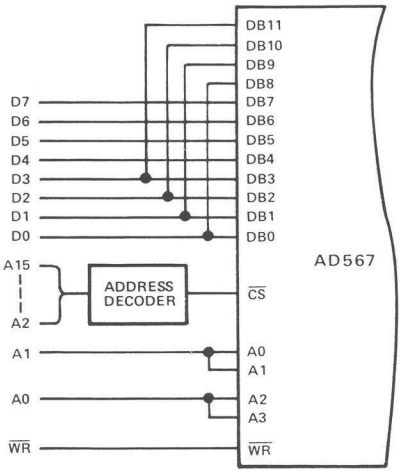
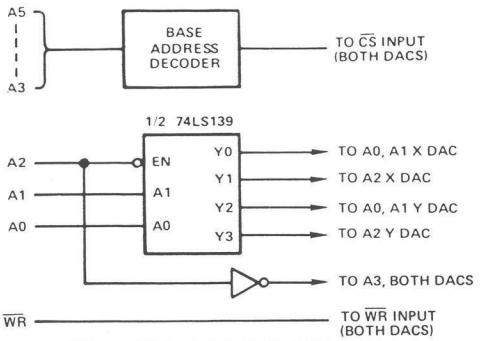


Figure 9. Right-Justified 8-Bit Bus Interface

USING MULTIPLE AD567 DACS IN 8-BIT SYSTEMS

Many applications use multiple digital-to-analog converters driven from the same data bus. For example, automatic test equipment systems often require all analog outputs to be produced simultaneously. Vector-scan graphic systems require that the X and Y coordinates of the stroke endpoints be updated simultaneously. The AD567 can be used with a very simple address decoder to perform this function, as shown in Figure 10. The 74LS139 two-line to four-line decoder and one inverter provide a set of distinct address pulses which assign the registers of the two DACs to a block of consecutive memory locations. In this circuit, write operations to addresses X000 and X001 load the first rank registers of one DAC in a right-justified data format. Addresses X010 and X011 load the first tank of another DAC, also in a right-justified format. A write to any address from X100 to X111 will load the second rank registers of both DACs simultaneously from their respective first rank registers.



A2	A1	A0	OPERATION
0	0	0	LOAD 8LSB – X DAC
0	0	1	LOAD 4MSB – X DAC
0	1	0	LOAD 8LSB – Y DAC
0	1	1	LOAD 4MSB – Y DAC
1	X	X	UPDATE BOTH DACS

Figure 10. Addressing for Two DACs (Right-Justified) on 8-Bit Bus

USING THE AD567 WITH 12- AND 16-BIT BUSES

The AD567 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied to low, and the latch is enabled by $\overline{CS}$ and $\overline{WR}$ going low. The AD567 thus occupies a single memory location.

This configuration renders the second rank register transparent, using the first rank of registers as the data latch. The $\overline{CS}$ input can be driven from an active-low decoded address, and $\overline{WR}$ can be the system $\overline{WR}$ signal. It should be noted that any data bus activity during the period when $\overline{CS}$ and $\overline{WR}$ are both active will cause activity at the AD567 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

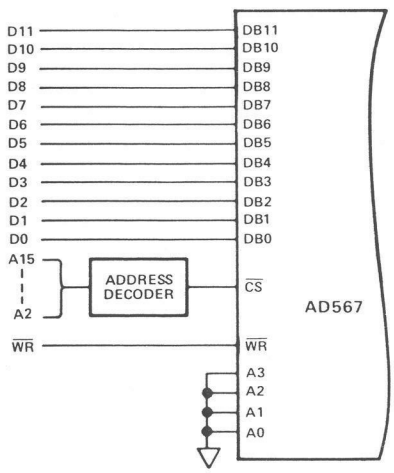


Figure 11. Connections for 12- and 16-Bit Bus Interface

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 12. The input line can be modeled as a 30kΩ resistance connected to a -0.7V rail, in parallel with a 5pF capacitance to ground.

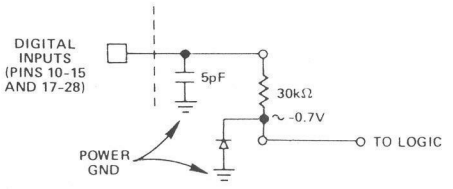


Figure 12. Equivalent Digital Input Circuit

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