ANALOG DEVICES

5 V, 12-Bit *nano*DAC, Serial Interface in MSOP and LFCSP Packages

AD5626

FEATURES

8-lead MSOP and 8-lead LFCSP packages
Complete voltage output with internal reference
1 mV/bit with 4.095 V full scale
5 V single-supply operation
No external components required
3-wire serial interface, 20 MHz data loading rate
Low power: 2.5 mW

APPLICATIONS

Portable instrumentation
Digitally controlled calibration
Servo controls
Process control equipment
PC peripherals

GENERAL DESCRIPTION

The AD5626, a member of the *nano*DAC® family, is a complete serial input, 12-bit, voltage output digital-to-analog converter (DAC) designed to operate from a single 5 V supply. It contains the DAC, input shift register and latches, reference, and a rail-to-rail output amplifier. The AD5626 monolithic DAC offers the user low cost and ease of use in 5 V only systems.

Coding for the AD5626 is natural binary with the MSB loaded first. The output op amp can swing to either rail and is set to a range of 0 V to 4.095 V for a one-millivolt-per-bit resolution. It is capable of sinking and sourcing 5 mA. An on-chip reference is laser trimmed to provide an accurate full-scale output voltage of 4.095 V.

This part features a serial interface that is high speed, three-wire, DSP compatible with data in (SDIN), clock (SCLK), and load strobe ($\overline{\text{LDAC}}$). There is also a chip-select pin for connecting multiple DACs.

The $\overline{\text{CLR}}$ input sets the output to zero scale at power on or upon user demand.

The AD5626 is specified over the extended industrial temperature range (–40°C to +85°C). The AD5626 is available in MSOP and LFCSP surface-mount packages.

FUNCTIONAL BLOCK DIAGRAM

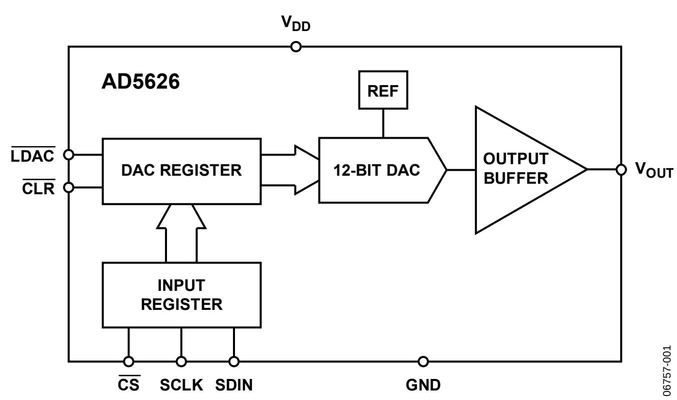


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

12/07—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_{DD} = 5.0 V ± 5%, −40°C ≤ T_A ≤ +85°C, B grade device, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution	N		12			Bits
Relative Accuracy	INL		−1	±1/4	+1	LSB
Differential Nonlinearity	DNL	No missing codes	−1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 0x000		1/2	3	LSB
Full-Scale Voltage	V_{FS}	Data = 0xFFF[1]	4.063	4.095	4.111	V
Full-Scale Tempco[2, 3]	TCV_{FS}			32		ppm/°C
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 0x800	±5	±7		mA
Load Regulation at Midscale	L_{REG}	R_L = 402 Ω to ∞, data = 0x800		1	3	LSB
Capacitive Load	C_L	No oscillation[2]		500		pF
LOGIC INPUTS						
Logic Input						
Low Voltage	V_{IL}				0.8	V
High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}				10	pF
AC CHARACTERISTICS[2]						
Voltage Output Settling Time	t_S	To ±1 LSB of final value[3]		16		µs
DAC Glitch				15		nV-s
Digital Feedthrough				15		nV-s
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, no load		1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, no load		0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, no load		7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, no load		2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

[1] Includes internal voltage reference error.
[2] These parameters are guaranteed by design and not subject to production testing.
[3] The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

TIMING CHARACTERISTICS

@ V_{DD} = 5.0 V ± 5%, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_{CH}	30	ns min	Clock width high
t_{CL}	30	ns min	Clock width low
t_{LDW}	20	ns min	Load pulse width
t_{DS}	15	ns min	Data setup
t_{DH}	15	ns min	Data hold
t_{CLRW}	30	ns min	Clear pulse width
t_{LD1}	15	ns min	Load setup
t_{LD2}	10	ns min	Load hold
t_{CSS}	30	ns min	Select
t_{CSH}	20	ns min	Deselect

[1] These parameters are guaranteed by design and not subject to production testing.
[2] All input control signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

Timing Diagram

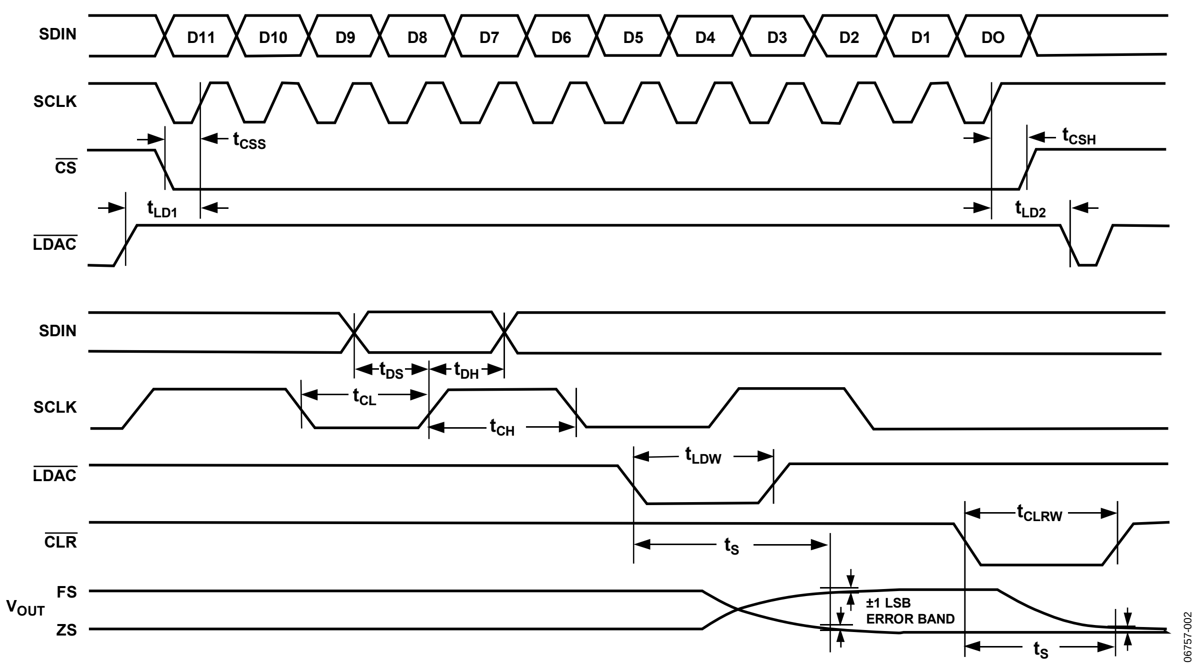


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +10 V
Logic Inputs to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND	50 mA
Package Power Dissipation	$(T_J \max - T_A)/\theta_{JA}$
Thermal Resistance (θ_{JA})	
8-Lead MSOP	220°C/W
8-Lead LFCSP	62°C/W
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

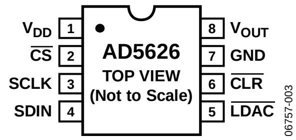


Figure 3. 8-Lead MSOP Pin Configuration

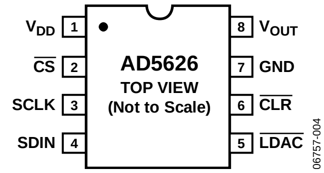


Figure 4. 8-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Supply. Nominal value 5 V ± 5%.
2	$\overline{\text{CS}}$	Chip Select. Active low input.
3	SCLK	Clock Input. Clock input for the internal serial input shift register.
4	SDIN	Serial Data Input. Data on this pin is clocked into the internal serial register on positive clock edges of the SCLK pin. The most significant bit (MSB) is loaded first.
5	$\overline{\text{LDAC}}$	Serial Register Data Write to DAC Register. Active low input that writes the serial register data into the DAC register. Asynchronous input.
6	$\overline{\text{CLR}}$	Clear DAC Register. Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale. Asynchronous input.
7	GND	Ground. Analog ground for the DAC. This also serves as the digital logic ground reference voltage.
8	V_{OUT}	Voltage Output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature, and power supply variations.

Table 5. Control Logic Truth Table[1]

$\overline{\text{CS}}$[2,3]	CLK[2]	$\overline{\text{CLR}}$	$\overline{\text{LD}}$[4]	Serial Shift Register Function	DAC Register Function
H	X	H	H	No effect	Latched
L	L	H	H	No effect	Latched
L	H	H	H	No effect	Latched
L	↑+	H	H	Shift-register-data advanced one bit	Latched
↑+	L	H	H	Shift-register-data advanced one bit	Latched
H	X	H	↓−	No effect	Updated with current shift register contents
H	X	H	L	No effect	Transparent
H	X	L	X	No effect	Loaded with all zeros
H	X	↑+	H	No effect	Latched all zeros

[1] ↑+ indicates a positive logic transition; ↓– indicates a negative logic transition; X = don't care.
[2] $\overline{\text{CS}}$ and CLK are interchangeable.
[3] Returning $\overline{\text{CS}}$ high avoids an additional false clock of serial data input.
[4] Do not clock in serial data while $\overline{\text{LD}}$ is low.

TYPICAL PERFORMANCE CHARACTERISTICS

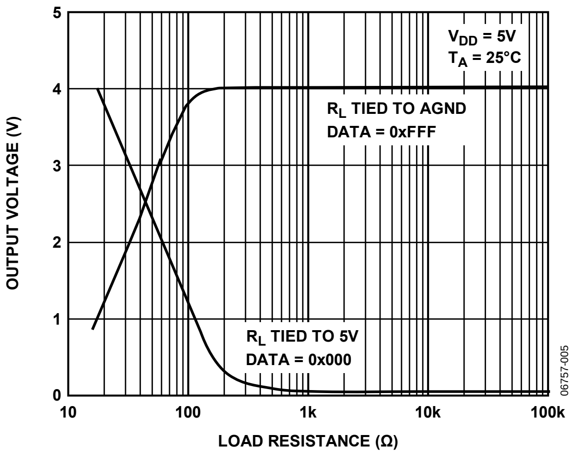


Figure 5. Output Voltage vs. Load

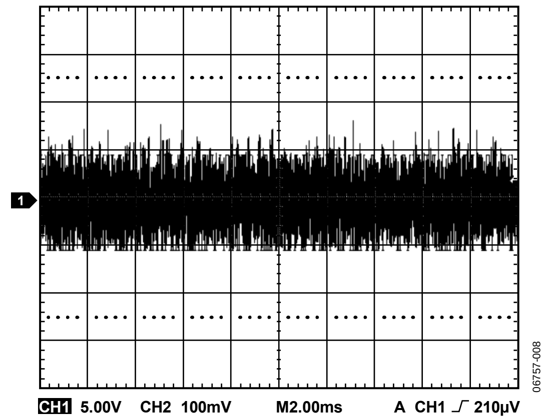


Figure 8. Broadband Noise

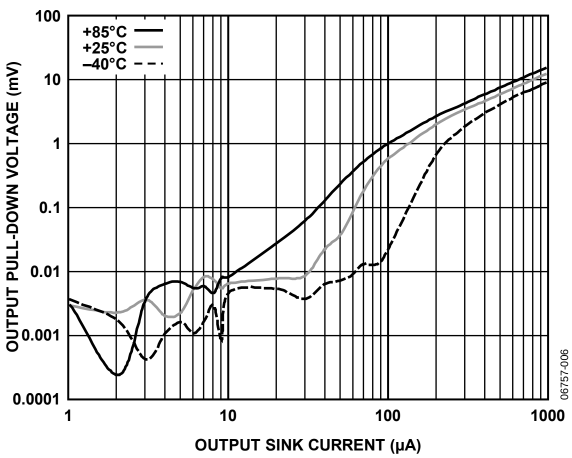


Figure 6. Output Pull-Down Voltage vs. Output Sink Current Capability

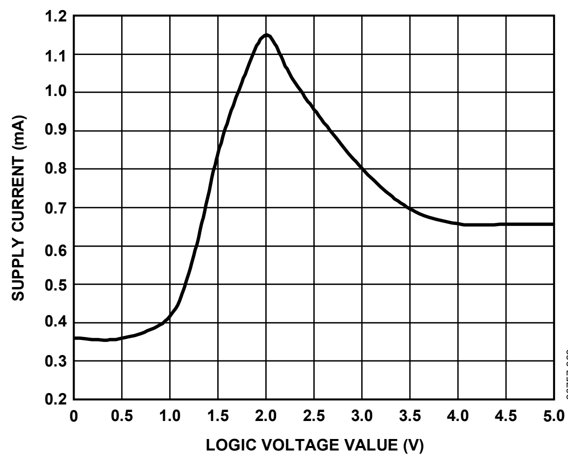


Figure 9. Supply Current vs. Logic Input Voltage

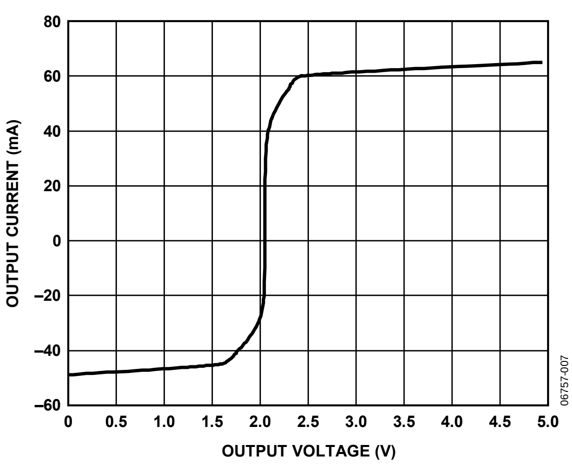


Figure 7. Short-Circuit Current

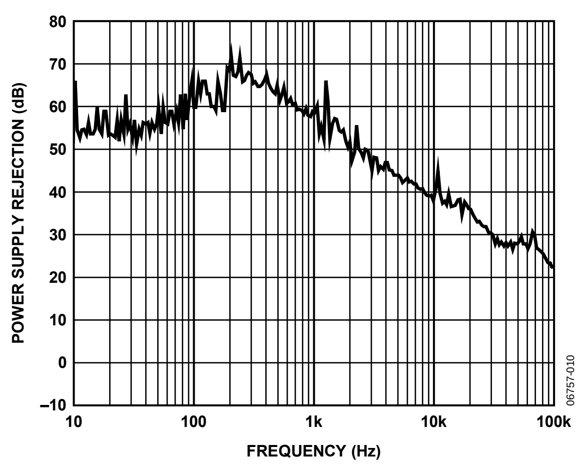


Figure 10. Power Supply Rejection vs. Frequency

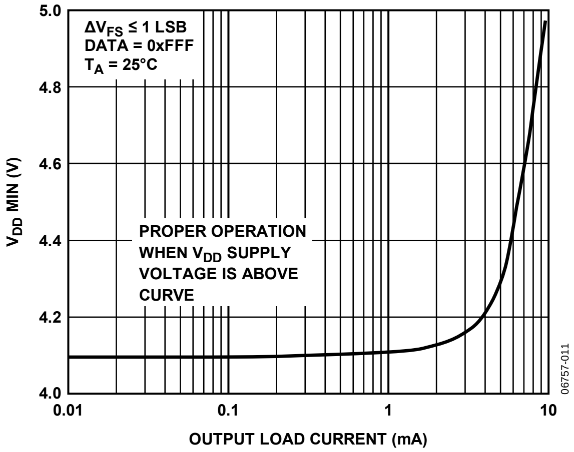


Figure 11. Minimum Supply Voltage vs. Load

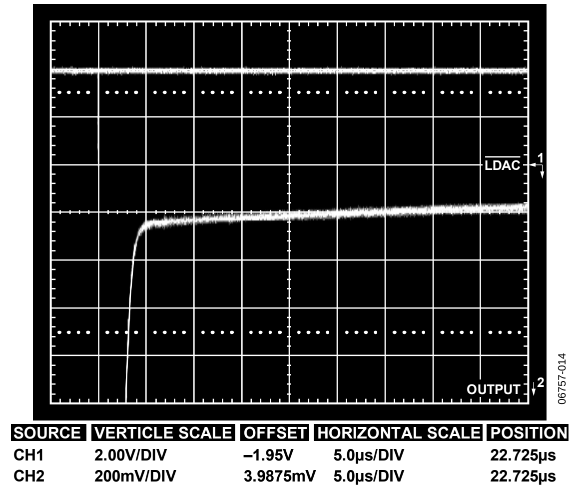


Figure 14. Rise Time Detail

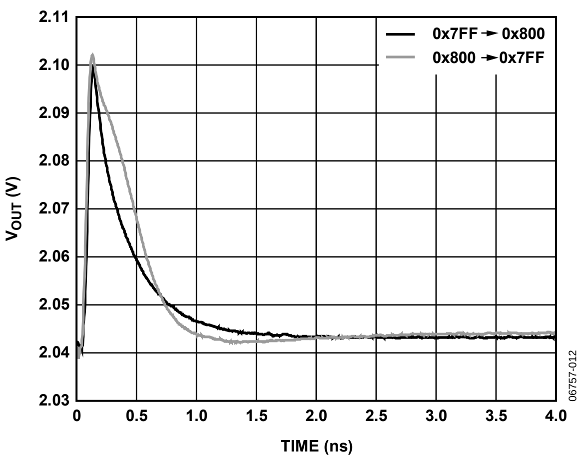


Figure 12. Midscale DAC Glitch Performance

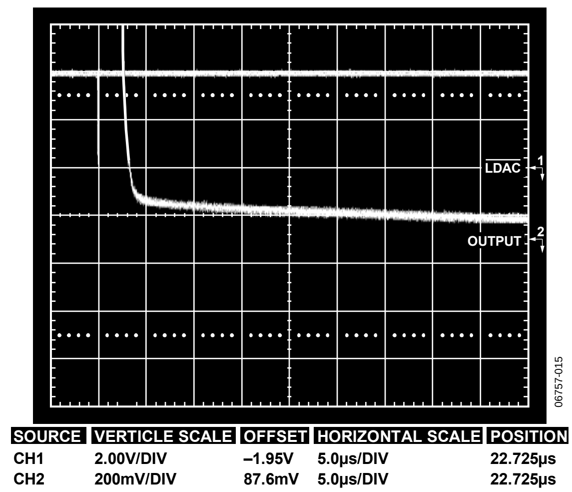


Figure 15. Fall Time Detail

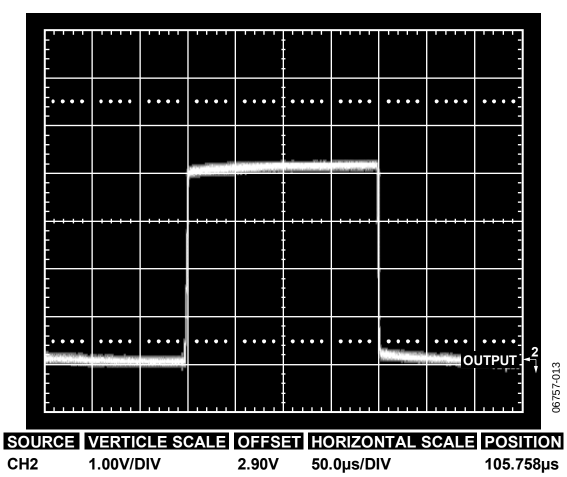


Figure 13. Large Signal Settling Time

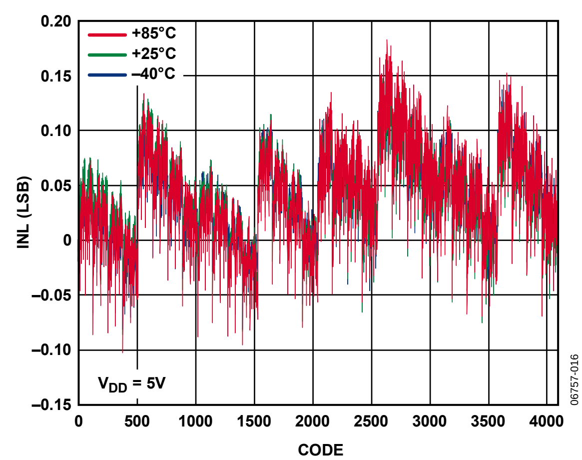


Figure 16. Integral Linearity Error vs. Digital Code

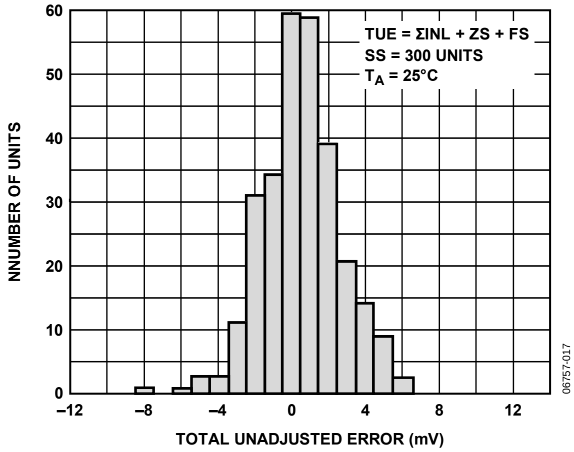


Figure 17. Total Unadjusted Error Histogram

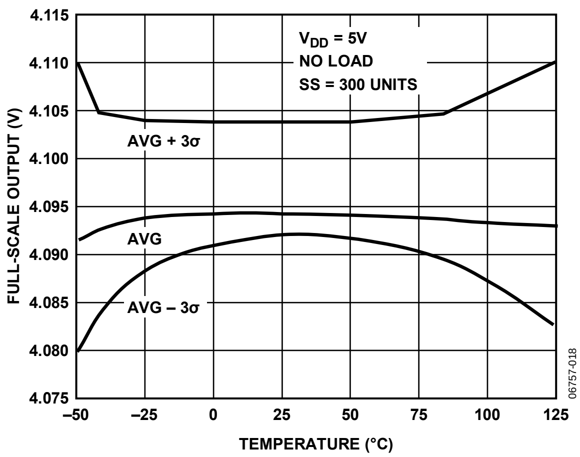


Figure 18. Full-Scale Output Voltage vs. Temperature

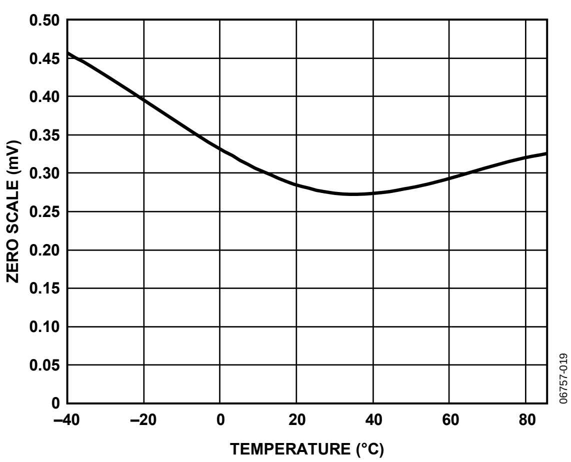


Figure 19. Zero-Scale Voltage vs. Temperature

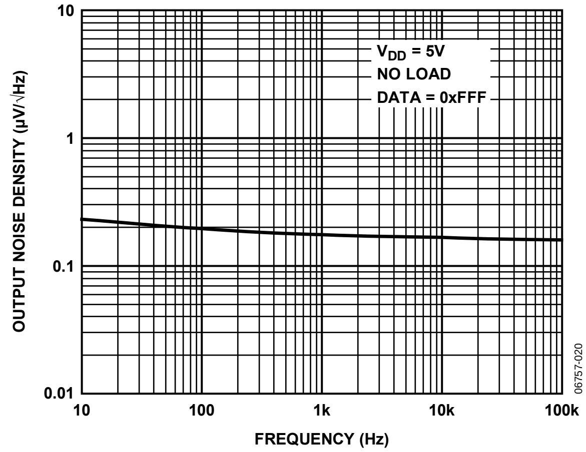


Figure 20. Output Voltage Noise vs. Frequency

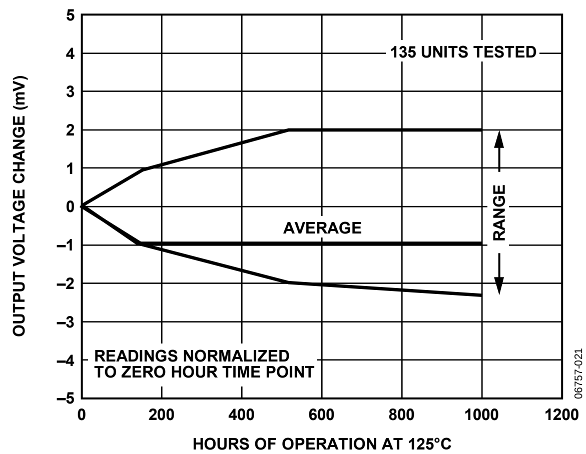


Figure 21. Long-Term Drift Accelerated by Burn-In

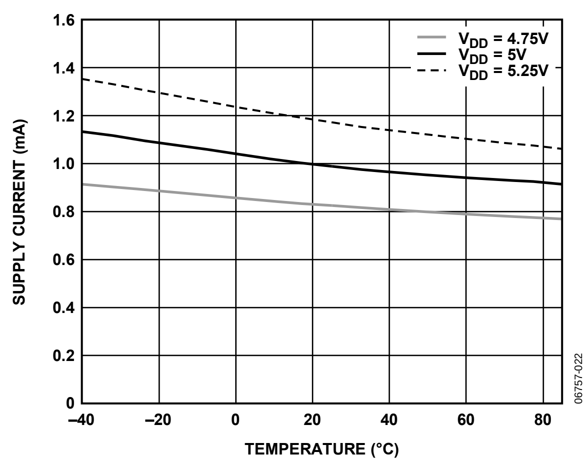


Figure 22. Supply Current vs. Temperature

THEORY OF OPERATION

The AD5626 is a complete, ready-to-use, 12-bit digital-to-analog converter (DAC). It contains a voltage-switched, 12-bit, laser-trimmed DAC, a curvature-corrected band gap reference, a rail-to-rail output op amp, a DAC register, and a serial data input register. The serial data interface consists of an SCLK, serial data in (SDIN), and a load strobe ($\overline{\text{LDAC}}$). This basic 3-wire interface offers maximum flexibility for interface to the widest variety of serial data input loading requirements. In addition, a $\overline{\text{CS}}$ select is provided for multiple packaging loading and a power-on-reset $\overline{\text{CLR}}$ pin to simplify start or periodic resets.

DAC SECTION

The DAC is a 12-bit voltage mode device with an output that swings from the GND potential to the 2.5 V internal band gap voltage. It uses a laser trimmed, rail-to-rail ladder which is switched by N-channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output internally connects to the rail-to-rail output op amp.

AMPLIFIER SECTION

A low power consumption, precision amplifier buffers the DAC output. This amplifier contains a differential PNP pair input stage that provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages.

The rail-to-rail amplifier is configured with a gain of 1.6384 (= 4.095 V/2.5 V) to set the 4.095 V full-scale output (1 mV/LSB). See Figure 23 for an equivalent circuit schematic of the analog section.

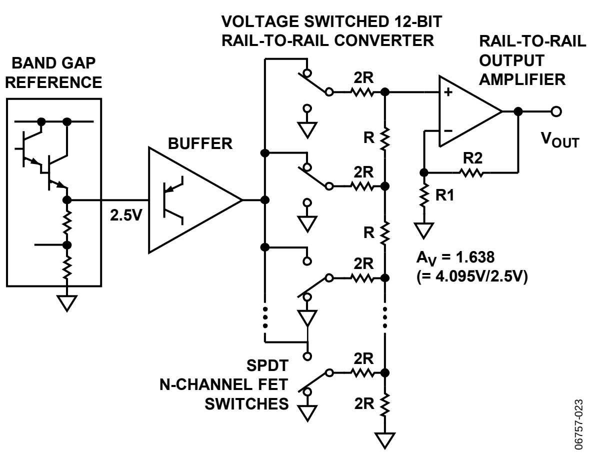


Figure 23. Equivalent AD5626 Schematic of Analog Section

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals vs. positive slewing signals. See the oscilloscope photos in the Typical Performance Characteristics section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier is designed to provide precision performance when operating near either power supply.

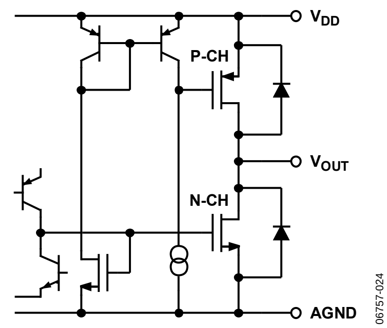


Figure 24. Equivalent Analog Output Circuit

Figure 24 shows an equivalent output schematic of the rail-to-rail amplifier with its N-channel pull-down FETs that pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can supply GND terminated loads, especially at the low supply tolerance values of 4.75 V. Figure 5 and Figure 6 provide information on output swing performance near ground and full-scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

POWER SUPPLY

The very low power consumption of the AD5626 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power consumption sensitive applications, it is important to note that the internal power consumption of the AD5626 is strongly dependent on the actual logic input voltage levels present on the SDIN, $\overline{\text{CS}}$, $\overline{\text{LDAC}}$, and $\overline{\text{CLR}}$ pins. Because these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving Logic V_{OH} and Logic V_{OL} voltage levels. The graph in Figure 9 shows the effect on total AD5626 supply current as a function of the actual value of input logic voltage. Consequently, use of CMOS logic vs. TTL minimizes power dissipation in the static state. A V_{IL} = 0 V on the SDIN, $\overline{\text{CS}}$, and $\overline{\text{CLR}}$ pins provides the lowest standby power dissipation of 2.5 mW (500 µA × 5 V).

As with any analog system, it is recommended that the AD5626 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection vs. frequency performance. This should be taken into account when using higher frequency, switched mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the AD5626 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from 4.75 V to 5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD5626 is possible down to 4.3 V. The minimum operating supply voltage vs. load current plot, shown in Figure 11, provides information for operation below V_{DD} = 4.75 V.

TIMING AND CONTROL

The AD5626 has a separate serial input register from the 12-bit DAC register that allows preloading of a new data value into the serial register without disturbing the present DAC output voltage. After the new value is fully loaded in the serial input register, it can be asynchronously transferred to the DAC register by strobing the $\overline{\text{LDAC}}$ pin. The DAC register uses a level sensitive $\overline{\text{LDAC}}$ strobe that should be returned high before any new data is loaded into the serial input register. At any time, the contents of the DAC register can be reset to zero by strobing the $\overline{\text{CLR}}$ pin that causes the DAC output voltage to go to zero volts. Figure 2 details all of the timing requirements together with Table 5, the control logic truth table.

APPLICATIONS INFORMATION

POWER SUPPLIES, BYPASSING, AND GROUNDING

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD5626 has been designed for 5 V applications, it is ideal for those applications under microprocessor or microcomputer control. In these applications, digital noise is prevalent; therefore, special care must be taken to ensure that its inherent precision is maintained by exercising particularly good engineering judgment when addressing the power supply, grounding, and bypassing issues using the AD5626.

Use a well-filtered and regulated power supply for the AD5626. The device has been completely characterized for a 5 V supply with a tolerance of ±5%. Because a 5 V logic supply is almost universally available, it is not recommended to connect the DAC directly to an unfiltered logic supply without careful filtering. Tapping a logic circuit supply for the DAC supply is unwise because fast logic with nanosecond transition edges induce high current pulses. The high transient current pulses can generate glitches hundreds of millivolts in amplitude due to wiring resistances and inductances. This high frequency noise corrupts the analog circuits internal to the DAC and causes errors.

Even though their spike noise is lower in amplitude, directly tapping the output of a 5 V system supply can cause errors because these supplies are of the switching regulator type that can and do generate a great deal of high frequency noise. Therefore, power the DAC and any associated analog circuitry directly from the system power supply outputs using appropriate filtering.

Figure 25 illustrates how a clean, analog-grade supply can be generated from a 5 V logic supply using a differential LC filter with separate power supply and return lines. With the values shown, this filter can easily handle 100 mA of load current without saturating the ferrite cores. Higher current capacity can be achieved with larger ferrite cores. For lowest noise, all electrolytic capacitors should be of the low equivalent series resistance (ESR) type.

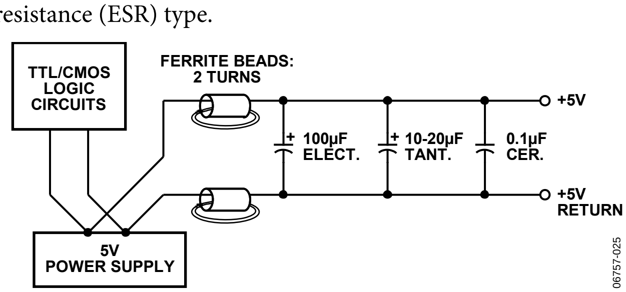


Figure 25. Properly Filtering a 5 V Logic Supply Yields a High Quality Analog Supply

To fit the AD5626 in an 8-lead package, only one ground connection to the device is accommodated. The ground connection of the DAC serves as the return path for supply currents as well as the reference point for the digital input thresholds. The ground connection also serves as the supply rail for the internal voltage reference and the output amplifier. Therefore, to minimize errors, connect the ground connection of the AD5626 to a high quality analog ground, such as the one previously described. Generous bypassing of the DACs supply effectively reduces supply line induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor is recommended. Connect the decoupling capacitors between the DAC supply pin (Pin 1) and the analog ground (Pin 7).

Figure 26 shows how the ground and bypass connections should be made to the AD5626.

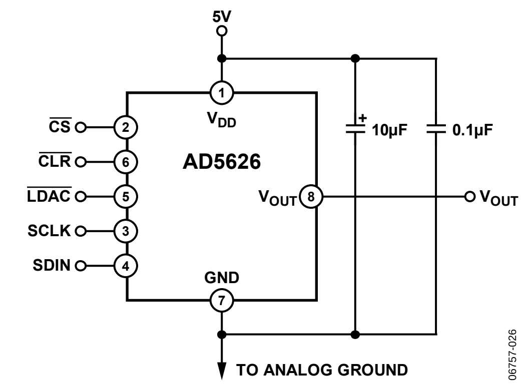


Figure 26. Recommended Grounding and Bypassing Scheme for the AD5626

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD5626. As shown in Figure 27, the AD5626 is designed to drive loads as low as 2 kΩ in parallel with 500 pF. The code table for this operation is provided in Table 6.

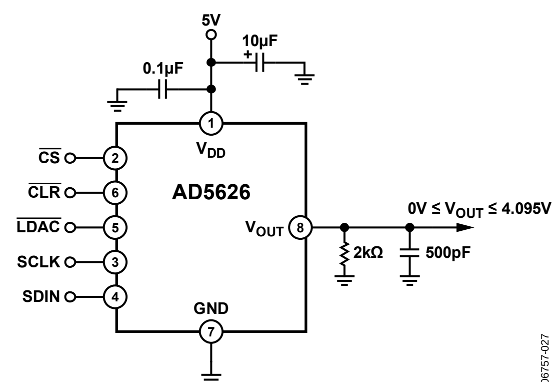


Figure 27. Unipolar Output Operation

Table 6. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	4.095
801	2049	2.049
800	2048	2.048
7FF	2047	2.047
000	0	0

OPERATING THE AD5626 ON 12 V OR 15 V SUPPLIES ONLY

Although the AD5626 has been specified to operate on a single, 5 V supply, a single 5 V supply may not be available in many applications. Because the AD5626 consumes no more than 2.5 mA maximum, an integrated voltage reference, such as the ADR02, can be used as the 5 V supply for the AD5626. See Figure 28 for the circuit configuration. Notice that the output voltage of the reference requires no trimming because of the excellent load regulation and tight initial output voltage tolerance of the ADR02. Although the maximum supply current of the AD5626 is 2.5 mA, local bypassing of the ADR02 output with at least 0.1 μF at the DAC voltage supply pin is recommended to prevent the internal digital circuits of the DAC from affecting the internal voltage reference of the DAC.

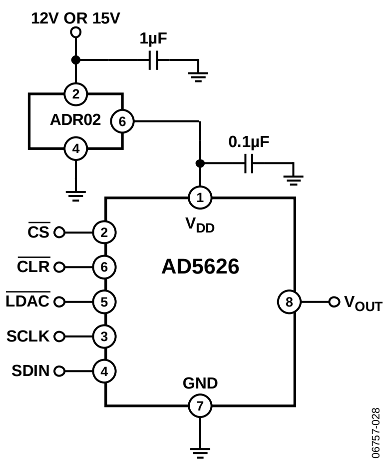


Figure 28. Operating the AD5626 on 12 V or 15 V Supplies Using an ADR02 Voltage Reference

MEASURING OFFSET ERROR

One of the most commonly specified endpoint errors associated with real world nonideal DACs is offset error. In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 V.

There are some DACs where offset errors are present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single-supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the AD5626, for example, the zero-scale error is specified to be ±3 LSBs. Because zero scale coincides with zero volt, it is not possible to measure negative offset error.

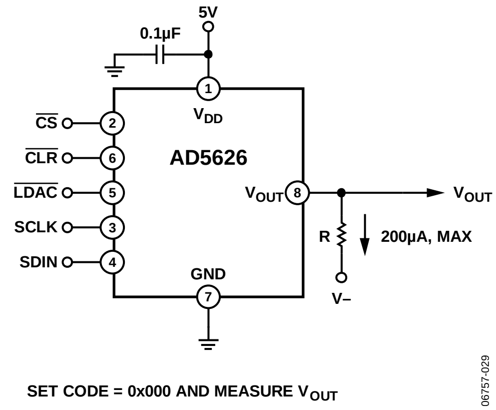


Figure 29. Measuring Zero-Scale or Offset Error

By adding a pull-down resistor from the output of the AD5626 to a negative supply as shown in Figure 29, offset errors can be read at zero code. This configuration forces the output P-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 μA, maximum.

BIPOLAR OUTPUT OPERATION

Although the AD5626 has been designed for single-supply operation, bipolar operation is achievable using the circuit illustrated in Figure 30. The circuit uses a single-supply, rail-to-rail OP295 op amp and the REF03 to generate the −2.5 V reference required to level shift the DAC output voltage.

Note that the −2.5 V reference is generated without the use of precision resistors. The circuit configuration provides an output voltage in the range of $-5\ V \le V_{OUT} \le +5\ V$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table 7 lists the relationship between the digital codes and output voltage. The transfer function of the circuit is given by

$$V_O = -1\ \text{mV} \times \textit{Digital Code} \times \frac{R4}{R1} + 2.5 \times \frac{R4}{R2}$$

and, for the circuit values shown, becomes

$$V_O = -2.44\ \text{mV} \times \textit{Digital Code} + 5\ \text{V}$$

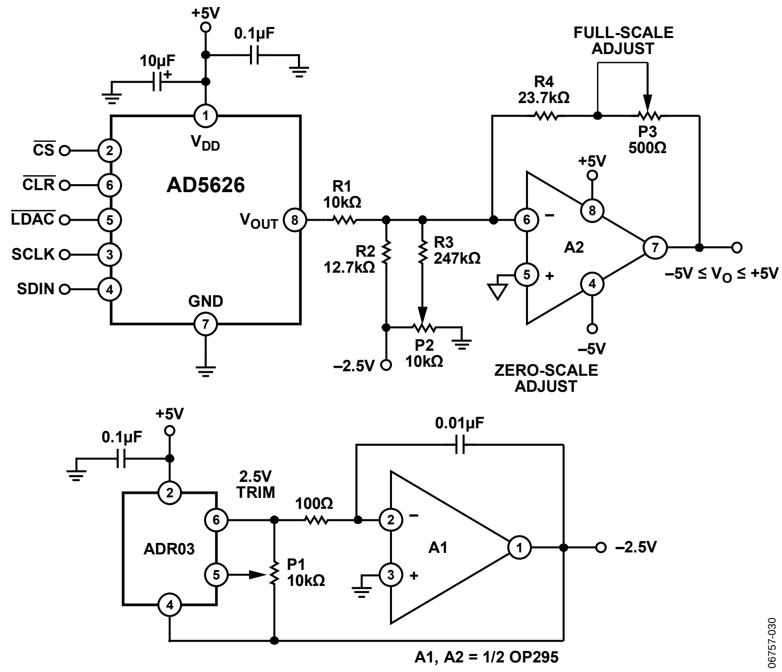
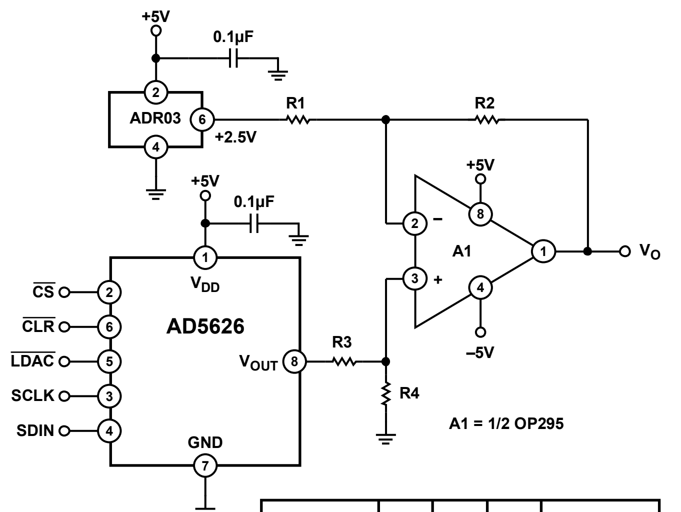


Figure 30. Bipolar Output Operation



V_{OUT} RANGE	R1	R2	R3	R4
±2.5V	10kΩ	10kΩ	10kΩ	15kΩ + 274Ω
±5V	10kΩ	20kΩ	10kΩ	43.2kΩ + 499Ω

06757-031

Figure 31. Bipolar Output Operation Without Trim

Table 7. Bipolar Code

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	−4.9976
801	2049	−2.44E − 3
800	2048	0
7FF	2047	+2.44E − 3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, and R4 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors whereas an R4 to R1 or R4 to R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 31 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim. The output voltage is coded in offset binary and is given by

$$V_O = 1\text{ mV} \times \textit{Digital Code} \times \left(\frac{R4}{R3 + R4}\right) \times \left(1 + \frac{R2}{R1}\right) - 2.5 \times \frac{R2}{R1}$$

For the ±2.5 V output range and the circuit values shown in the table in Figure 31, the transfer equation becomes

$$V_O = 1.22\text{ mV} \times \textit{Digital Code} - 2.5\text{ V}$$

Similarly, for the 5 V output range, the transfer equation becomes

$$V_O = 2.44\text{ mV} \times \textit{Digital Code} - 5\text{ V}$$

GENERATING A NEGATIVE SUPPLY VOLTAGE

Some applications may require bipolar output configuration but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, only 12 V, 15 V, and/or 5 V are available.

Figure 32 shows a method for generating a negative supply voltage using one CD4049, a CMOS hexadecimal inverter, and operating on 12 V or 15 V. The circuit is essentially a charge pump where two of the six inverters are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2.

The remaining four inverters are wired in parallel for higher output current. The square wave output is level translated by C2 to a negative-going signal rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump provides an output voltage of −5 V for currents loading in the range 0.5 mA ≤ I_{OUT} ≤ 10 mA with a 15 V supply and 0.5 mA ≤ I_{OUT} ≤ 7 mA with a 12 V supply.

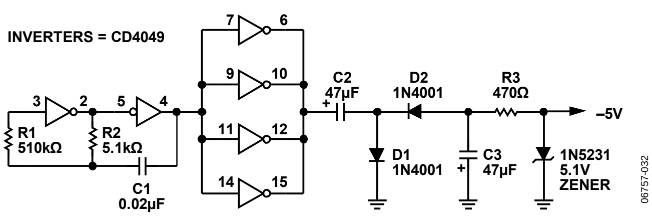


Figure 32. Generating a −5 V Supply When Only 12 V or 15 V Is Available

A SINGLE-SUPPLY, PROGRAMMABLE CURRENT SOURCE

The circuit in Figure 33 shows how the AD5626 can be used with an OP295 single-supply, rail-to-rail, output op amp to provide a digitally programmable current sink from V_{SOURCE} that consumes less than 3.8 mA, maximum. The DAC output voltage is applied across R1 by placing the 2N2222 transistor in the feedback loop of the OP295. For the circuit values shown, the full-scale output current is 1 mA, which is given by the following equation:

$$I_{OUT} = \frac{DW \times 4.095\text{V}}{R1}$$

where *DW* = the binary digital input code of the AD5626.

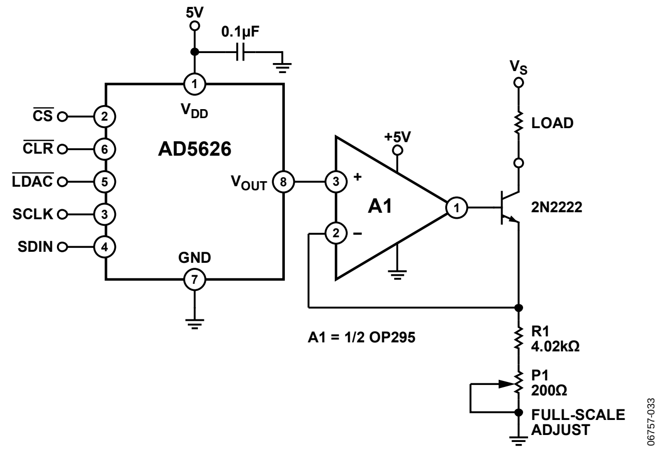


Figure 33. A Single-Supply, Programmable Current Source

The usable output voltage range of the current sink is 5 V to 60 V. The low limit of the range is controlled by transistor saturation, and the high limit is controlled by the collector-base breakdown voltage of the 2N2222.

GALVANICALLY-ISOLATED INTERFACE

In many process control type applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. An *i*Coupler® can provide isolation in excess of 2.5 kV. The serial loading structure of the AD5626 makes it ideal for isolated interfaces as the number of interface lines is kept to a minimum. Figure 34 illustrates a 4-channel isolated interface using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

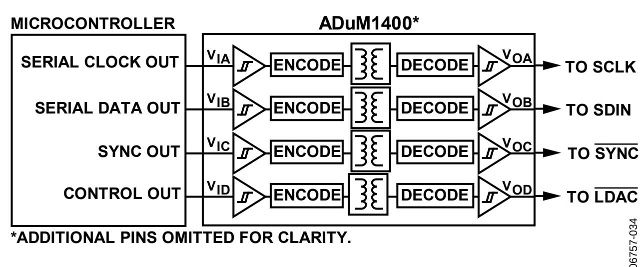


Figure 34. An iCoupler-Isolated DAC Interface

MICROPROCESSOR INTERFACING

AD5626 to MC68HC11 Interface

The circuit illustrated in Figure 35 shows a serial interface between the AD5626 and the MC68HC11 8-bit microcontroller. SCK of the MC68HC11 drives SCLK of the AD5626, whereas the MOSI output drives the serial data line, SDIN, of the AD5626. The $\overline{\text{CLR}}$, $\overline{\text{LDAC}}$, and $\overline{\text{CS}}$ signals of the DAC are derived from the PC1, PD5, and PC0 port lines, respectively, as shown.

For correct operation of the serial interface, configure the MC68HC11 such that its CPOL bit is set to 1 and its CPHA bit is also set to 1. When the serial data is to be transmitted to the DAC, PC0 is taken low, asserting the $\overline{\text{CS}}$ input of the DAC. When the MC68HC11 is configured in this manner, serial data on MOSI is valid on the rising edge of SCLK. The MC68HC11 transmits its serial data in 8-bit bytes (MSB first), with only eight rising clock edges occurring in the transmit cycle. To load data to the input serial register of the AD5626, PC0 is left low after the first eight bits are transferred, and a second byte of data is then transferred serially to the AD5626. During the second byte load, the first 4 MSBs of the first byte are pushed out of the input shift register of the DAC. At the end of the second byte load, PC0 is taken high. To prevent accidental advancing of the internal shift register, SCLK must already be asserted before PC0 is taken high. To transfer the contents of the input shift register to the DAC register, PD5 is taken low, asserting the $\overline{\text{LDAC}}$ input. The $\overline{\text{CLR}}$ input of the DAC, controlled by the MC68HC11 PC1 port, provides an asynchronous clear function, setting the DAC output to zero.

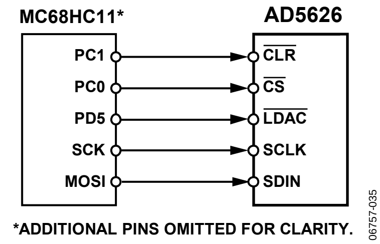
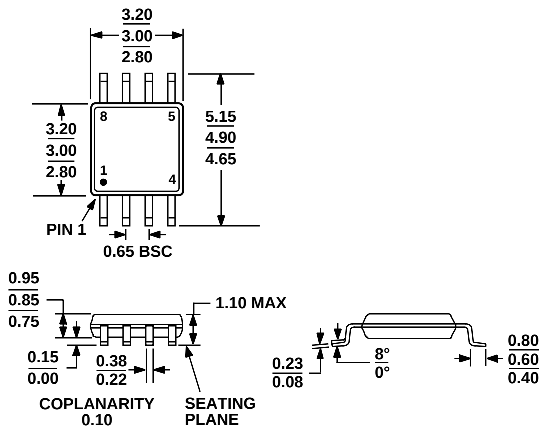


Figure 35. AD5626 to MC68HC11 Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

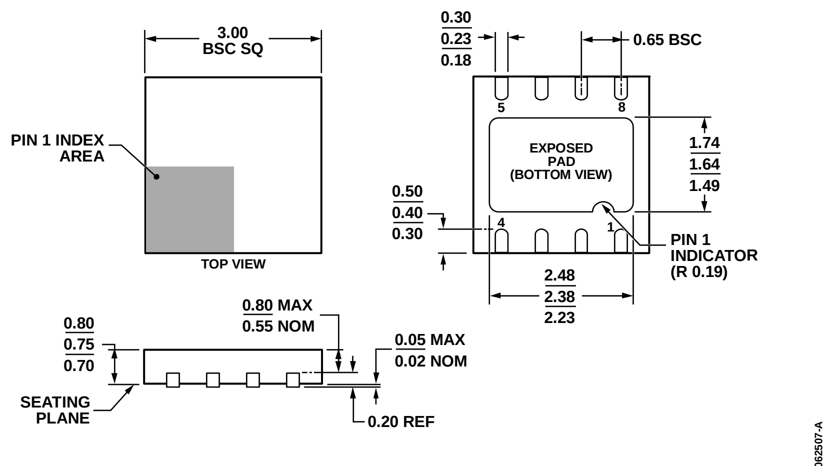


Figure 37. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm x 3 mm Body, Very Very Thin, Dual Lead
(CP-8-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Description	Package Option	Branding
AD5626BRMZ[1]	±1	−40°C to +85°C	8-Lead MSOP	RM-8	DAP
AD5626BRMZ-REEL7[1]	±1	−40°C to +85°C	8-Lead MSOP	RM-8	DAP
AD5626BCPZ[1]	±1	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-3	DAP
AD5626BCPZ-REEL7[1]	±1	−40°C to +85°C	8-Lead LFCSP_WD	CP-8-3	DAP

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D06757-0-12/07(0)