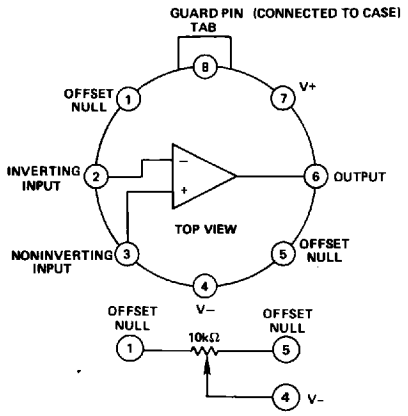
Monolithic Precision, Low Drift FET-Input Op Amp

AD545A*

FEATURES

Low Offset Voltage: 0.5mV max (AD545AL)
0.25mV max (AD545AM)
Low Offset Voltage Drift: 5μV/°C max (AD545AL), 3μV/°C max (AD545AM)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545AK, L, M)
Low Noise: 3μV p-p, 0.1Hz to 10Hz

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD545A is a monolithic precision FET-input operational amplifier. It is a successor to the AD545 and will replace the AD545 in most applications. Bias current is specified as 2pA max for the AD545AJ and 1pA max for the AD545AK, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545AL, 0.25mV max for the AD545AM. All devices also feature low voltage noise and power consumption. The AD545A is internally compensated, short circuit protected and free of latch-up.

The AD545A series offers a broad combination of performance features. For precision applications the AD545AM specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545AJ, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/pIon sensitive electrodes, photocurrent detectors, biological microprobes, long-term precision integrators and vacuum ion gage measurements. The versatility of the AD545A is further enhanced by its excellent low frequency noise (3μV p-p, 0.1Hz to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients.

The AD545A is available in four versions of bias current and offset voltage, the "J," "K," "L," and "M." All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

*Covered by U.S. Patent No. 4,639,683.

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545A is laser trimmed to a level typically less than 250μV. Offset voltage drift is only 3μV/°C max for the AD545AM. If additional external nulling is desired, the effect on drift is minimal (approximately 2.5μV/°C mV, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.6mA typical, and 1.5mA max keeps self-heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one MΩ up to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristics.

AD545A—SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc, unless otherwise specified)

Model	AD545AJ	AD545AK	AD545AL	AD545AM
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	40,000V/V min	40,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	50,000V/V min	50,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	25,000V/V min	40,000V/V min	40,000V/V min
OUTPUT CHARACTERISTICS				
Voltage@R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
@R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	10mA min (20mA typ)	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	5kHz min (30kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (2.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	1.0mV max	0.5mV max	0.25mV max
vs. Temperature, T_A = min to max	25μV/°C max	15μV/°C max	5μV/°C max	3μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	200μV/V max	200μV/V max	200μV/V max
INPUT BIAS CURRENT				
Either Input[4]	2pA max	1pA max	1pA max	1pA max
INPUT IMPEDANCE				
Differential V_{IN} = ±1V	1.6pF‖$10^{13}\Omega$	*	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	5μV (p-p) max
f = 10Hz	55nV/$\sqrt{Hz}$	*	*	*
f = 100Hz	45nV/$\sqrt{Hz}$	*	*	*
f = 1kHz	35nV/$\sqrt{Hz}$	*	*	*
Current, 0.1Hz to 10Hz	0.03pA (p-p)	*	*	*
10Hz to 10kHz	0.05pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	66dB min (80dB typ)	70dB min	76dB min	76dB min
Maximum Safe Input Voltages[5]	±V_S	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±5V min (±18V max)	*	*	*
Quiescent Current	1.5mA max (0.6mA typ)	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]	H-08A	*	*	*

NOTES

*Specifications same as AD545AJ.

[1]Open Loop Gain is specified with or without nulling of V_{OS}.

[2]A conservative design would not exceed 500pF of load capacitance.

[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage.

[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD545A is brought out separately to Pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.8pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical for achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545A but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board.

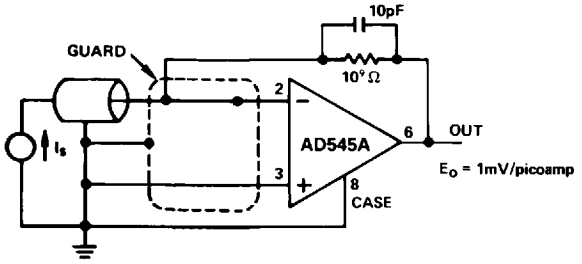


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

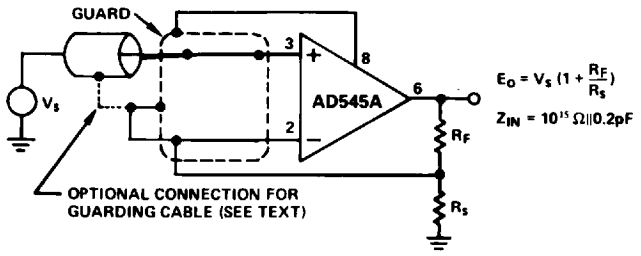


Figure 2. Very High Impedance Noninverting Amplifier

The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545A offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545A and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required voltage power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.
4. Figure 8 shows the AD545A's input currents versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1V to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

AD545A–Typical Performance Curves

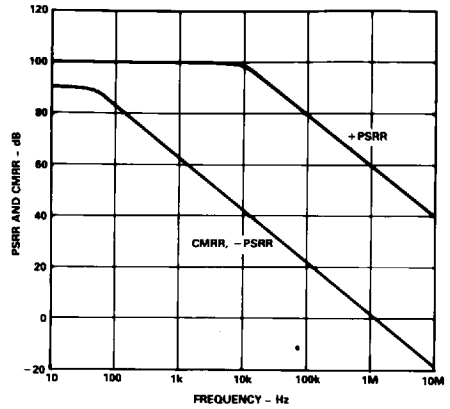


Figure 3. PSRR and CMRR vs. Frequency

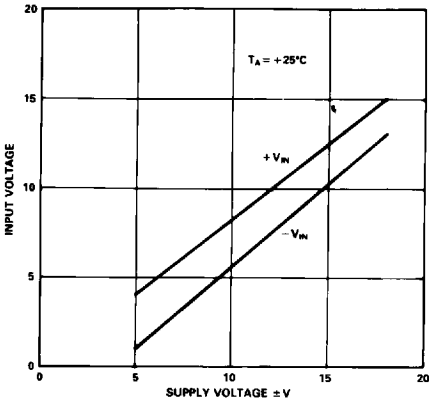


Figure 4. Input Common-Mode Range vs. Supply Voltage

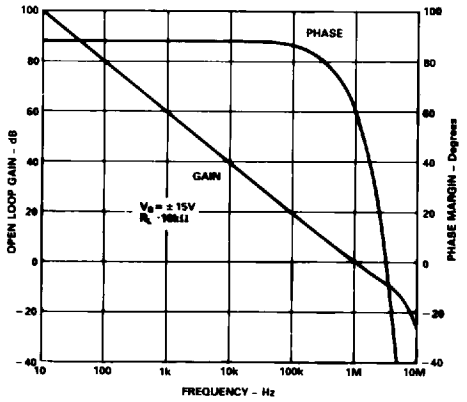


Figure 5. Open Loop Frequency Response

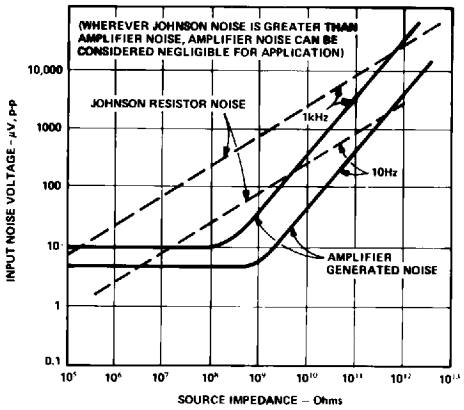


Figure 6. Total Input Noise Voltage vs. Source Impedance and Bandwidth

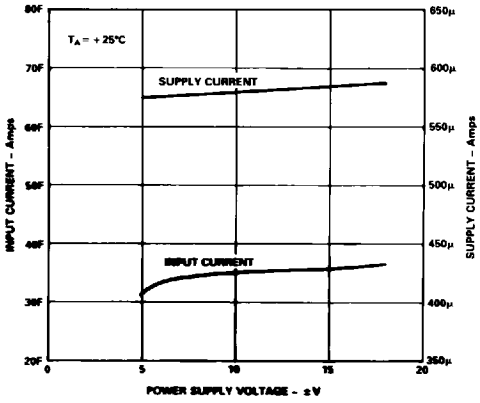


Figure 7. Input Bias Current and Supply Current vs. Supply Voltage

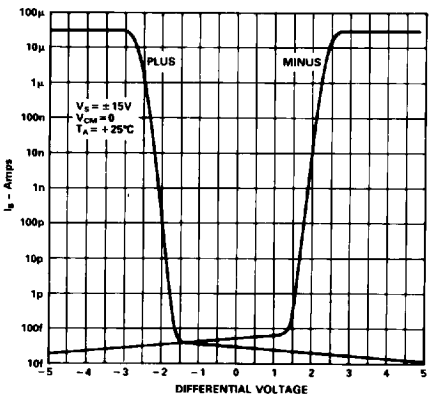


Figure 8. Input Bias Current vs. Differential Input Voltage

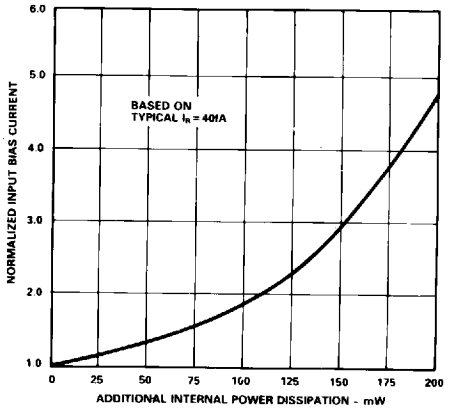


Figure 9. Input Bias Current vs. Additional Power Dissipation

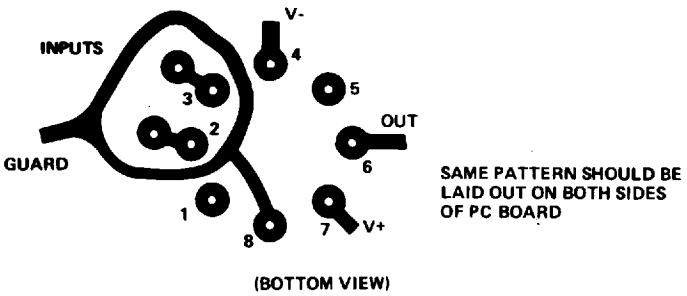


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package