AC101L

Ultra Low-Power 10/100 Ethernet Transceiver with Auto-MDIX

GENERAL DESCRIPTION

The AC101L is a single-channel, low-power, 10/100BASE-TX/FX transceiver. The AC101L transceiver has an integrated voltage regulator to allow operation from a single 3.3V or 2.5V supply source. The device contains a full-duplex 10BASE-T/100BASE-TX/100BASE-FX Fast Ethernet transceiver, which performs all of the physical layer interface functions.

The AC101L is a highly integrated solution combining an encoder/decoder, link monitor, auto-negotiation selection, parallel detection, adaptive equalization, clock/data recovery, baseline wander correction, multimode transmitter, scrambler/descrambler, far-end fault (FEF), and auto-MDI/MDIX circuitry.

FEATURES

- 3.3V tolerant and 2.5V capable
- Integrated voltage regulator to allow operation from a single 3.3V or 2.5V supply source
- 10/100 TX/FX
- Full-duplex or half-duplex
- FEFI on 100FX
- 48-pin TQFP
- Industrial temperature (–40°C to +85°C)
- 0.25 µm CMOS
- Fully compliant with IEEE 802.3/802.3u
- MII interface
- Baseline wander correction
- Multifunction LED outputs
- Cable length indicator
- HP auto-MDI/MDIX
- Eight programmable interrupts
- Diagnostic registers

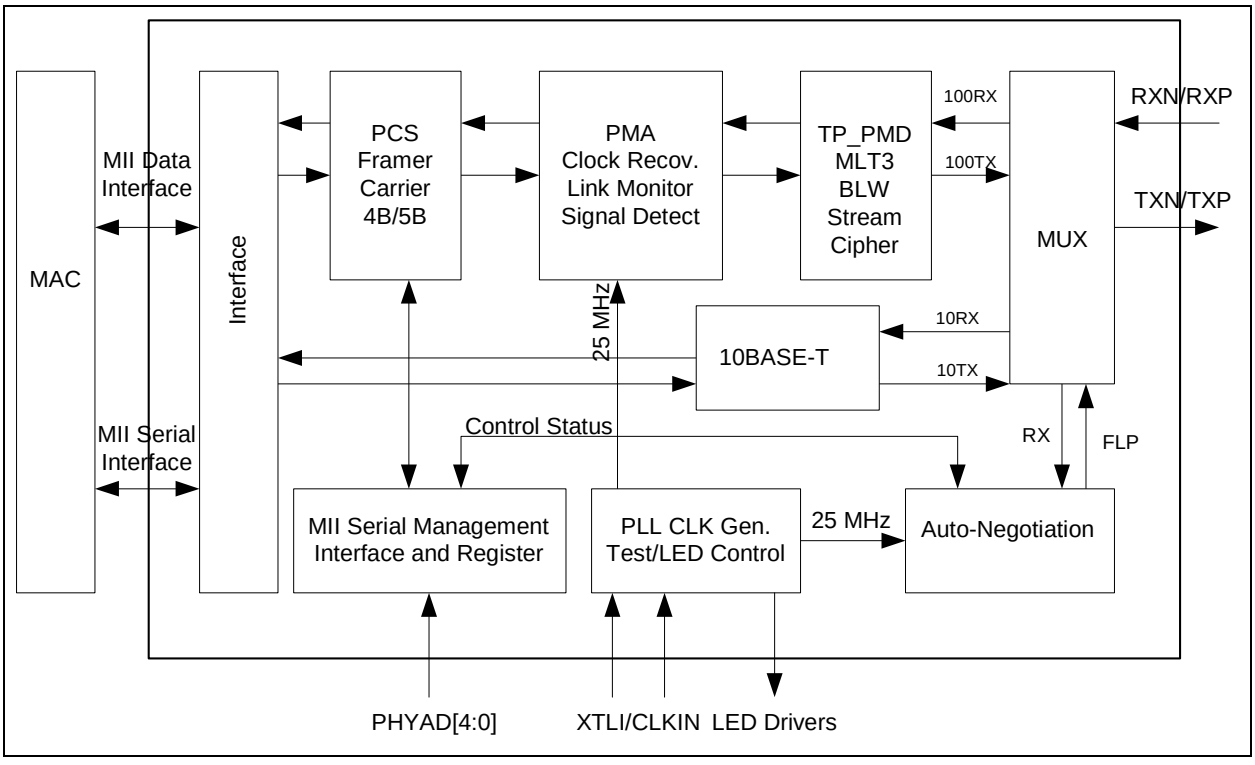

Figure 1: Functional Block Diagram

16215 Alton Parkway • P.O. Box 57013 • Irvine, California 92619-7013 • Phone: 949-450-8700 • Fax: 949-450-8710

REVISION HISTORY

Revision	*Date*	*Change Description*
AC101L-DS06-R	8/9/04	• Edits for consistency, minor error corrections
AC101L-DS05-R	3/10/03	• Replaced the # sign with an overline to indicate active low pins. • In Table 1, changed description of pin 24 ($\overline{\text{PDOWN}}$) from being pulled low externally to being pulled high externally for normal operation.
AC101L-DS04-R	1/29/03	• Updated Table 1, ”Pinout and Signal Definitions,” on page 7. • Updated Figure 2, ”AC101L Pinout Diagram,” on page 11. • Updated Table 19, ”Register 23: Operation Mode Register,” on page 25. • Updated Table 22, ”Common Register 1: (Map to Reg. 29, Page 0 A28.[15:12]=0000) Test Mode Register,” on page 26. • Updated Table 23, ”Common Register 4: (Map to Reg. 29, Page 1 A28.[15:12]=0001) LED Blink Rate,” on page 27. • Updated Table 44, ”Recommended Operating Conditions,” on page 46.
AC101L-DS03-R	9/18/02	• Updated Signal Types designations in Section 2 ”Pin Descriptions” on page 7. • Updated Table 35, ”Reset Timing,” on page 35. • Updated Table 37, ”100BASE-X MII Transmit System Timing,” on page 37. • Updated Table 38, ”100BASE-TX/FX MII Receive System Timing,” on page 38 and Figure 6, ”100BASE-T MII Receive Timing,” on page 39. • Updated Table 39, ”10BASE-T MII Transmit System Timing,” on page 40 and Figure 7, ”10BASE-T Transmit Timing,” on page 40. • Updated Table 40, ”10BASE-T MII Receive System Timing,” on page 41 and Figure 8, ”10BASE-T Receive Timing,” on page 42. • Removed Table 42,”RMII Receive Timing,” on page 39 and Figure 9,”RMII Receive Timing,” on page 39 as well as all references to RMII in the document. • Updated Table 44, ”Recommended Operating Conditions,” on page 46.
AC101L-DS02-R	6/6/02	• Added table showing current requirements at 2.5 V operation with LED disabled. • Added table showing current requirements at 3.3 V operation with LED disabled. • Added output voltage high values and output voltage low values (all digital pins). • Added input voltage high and low values (all digital input pins).
AC101L-DS01-R	02/20/02	Updated FX application figure and Power and ground filtering figure.
AC101L-DS00-R	01/02/02	Initial release.

Altima Communications, Inc.
A Wholly-Owned Subsidiary of Broadcom Corporation
P.O. Box 57013
16215 Alton Parkway
Irvine, California 92619-7013

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Section 1: Functional Description

The AC101L is a single-chip, Fast Ethernet transceiver. It performs all of the physical layer interface functions for 100BASE-TX full-duplex or half-duplex on Category 5 twisted-pair cable, and 10BASE-T full-duplex or half-duplex on Category 3 cable. It can be configured for 100BASE-FX full- or half-duplex transmission over fiber-optic cable when paired with an external fiber-optic line driver and receiver.

The chip performs 4B5B, MLT3, NRZI, encoder/decoder, link monitor, auto-negotiation selection, adaptive equalization, clock/data recovery, baseline wander correction, multimode transmitter, scrambler/descrambler, far-end fault (FEF), and auto-MDI/MDIX. It can be connected to a MAC switch controller through the MII on one side and directly to the media on the other side through a transformer for twisted-pair (TP) mode, or fiber-optic module for FX mode. It is fully compliant with the IEEE 802.3 and 803.3u standards.

ENCODER/DECODER

In 100BASE-TX and 100BASE-FX modes, the AC101L transmits and receives data stream on twisted-pair or fiber-optic cable. When the MII transmit enable is asserted, nibble wide (4-bit) data from transmit data pins is encoded into 5-bit code groups and inserted into transmit data stream. The 4B/5B encoding is shown in Section 6: “4B/5B Code Group” on page 26. The transmit packet is encapsulated by replacing the first 2 nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of packet. When the MII transmit error input is asserted during a packet, the error code group (H) is sent in place of the corresponding data code group. The transmitter sends repeatedly the idle code group between packets.

In 100BASE-TX mode, the encode data stream is first scrambled by a stream cipher block and then serialized and encoded into an MLT3 signal level. Second, a multimode transmit DAC (digital to analog converter) is used to drive the MLT3 data onto twisted-pair cable. Following baseline wander correction, adaptive equalization and clock/data recovery in 100BASE-TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data are descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

In 100BASE-FX mode, the scrambling function is bypassed and the data are NRZII-encoded. The multi mode transmit DAC drives differential Positive ECL (PECL) levels to an external fiber-optic transmitter. Baseline wander correction, adaptive equalization, stream cipher descrambling functions are bypassed and NRZI decoding is used instead of MLT3.

The 5-bit code groups are decoded into 4-bit data nibbles. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data are driven onto the MII receive data pins. When an invalid code group or bad SSD is detected in the data stream, the AC101L asserts the MII RXER signal.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multi mode transmit DAC performs pre-equalization for 100 meters of Category 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. The signal levels are qualified using squelch detect circuits. When no signal or certain valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the link pass state, and the transmit and receive functions are enabled.

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the SD signal (PIN 28).

In 10BASE-T mode, a link pulse detection circuit constantly monitors the RXP/RXN pins for the presence of valid link pulses.

CARRIER SENSE (CRS)/RXDV

Carrier sense is asserted asynchronously on the CRS pins as soon as activity is detected on the receive data stream. RXDV is asserted as soon as a valid SSD (Start-of-Stream Delimiter) is detected. Carrier sense and RXDV are de-asserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. However, if the carrier sense is asserted and a valid SSD is not detected immediately, RXER is asserted instead of RXDV.

In 10BASE-T mode, CRS is asserted asynchronously when the valid preamble and data activity is detected on the RXIP and RXIN pins.

In the half-duplex mode, the CRS is activated during data transmit. In the full-duplex mode, the CRS is activated during data receiving only.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted and transmission is in progress.

AUTO-NEGOTIATION

Auto-negotiation selection is on 100BASE twisted-pair PHY only; it is not operating in 100BASE fiber PHY.

In 100BASE-TX mode, auto-negotiation can be enabled or disabled by hardware or software control. When the auto-negotiation function is enabled, the 100BASE-TX PHY automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. 100BASE-TX PHY can be configured to advertise 100BASE-TX full-duplex or 100BASE-TX half-duplex.

The default auto-negotiation mode is configured via reset read value of ANEN/LED3 signal (pin 23) and SPD100/LED1.

Table 1: Auto-Negotiation Mode

Mode	*Mode Name*	*Link Settings*
0.13	Speed Select	The default value is SPD100.
0.12	ANEN Enable	1 = Enable Auto-negotiation. 0 = Disable Auto-negotiation.
0.8	Duplex	The default value is !ANEN && DUPLEX.
4.8/1.14	100BASE-TX Full-Duplex	The default value of this bit is SPD100 && DUPLEX.

Table 1: Auto-Negotiation Mode (Cont.)

Mode	*Mode Name*	*Link Settings*
4.7/1.13	100BASE-TX	The default value is SPD100 && (ANEN || !DUPLEX).
4.6/1.12	10BASE-T Full-Duplex	The default value of this bit is DUPLEX && (ANEN || !SPD100).
4.5/1.11	10BASE-T	The default value is ANEN || (!SPD100 && !DUPLEX).

PARALLEL DETECTION

Because there are many devices in the field that do not support the ANEN process, but must still be communicated with, it is necessary to detect and link through the parallel detection process. The parallel detection circuit is enabled in the absence of FLPs. The circuit is able to detect the following:

- Normal link pulse (NLP)
- 10BASE-T receive data
- 100BASE-TX idle

The mode of operation gets configured based on the technology of the incoming signal. If any of the above is detected, the device automatically configures to match the detected operating speed in the half-duplex mode. This ability allows the device to communicate with the legacy 10BASE-T and 100BASE-TX systems, while maintaining the flexibility of auto-negotiation.

ANALOG ADAPTIVE EQUALIZER

The analog adaptive equalizer removes InterSymbol Interference (ISI) created by the transmission channel media.

The PHY is designed to accommodate a maximum of 140 meters of UTP Category 5 cable. An AT&T 1061 Category 5 cable of this length typically has an attenuation of 31 dB at 100 MHz. A typical attenuation of 100-meter cable is 21 dB. The worst case cable attenuation is around 24–26 dB as defined by TP-PMD specification. The amplitude and phase distortion from the cable causes ISI which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pair cable. The equalizer has the ability to changes its equalizer frequency response according to the cable length. The equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

CLOCK RECOVERY

The equalized MLT3 signal passes through the slicer circuit and is converted to NRZI format. The PHY uses a proprietary mixed-signal Phase Locked Loop (PLL) to extract clock information from the incoming NRZI data. The extracted clock is used to retime the data stream and set the data boundaries. The transmit clock is locked to the 25-MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to the data stream, extracts the 125-MHz clock, and uses it for the bit framing for the recovered data. The recovered 125-MHz clock is also used to generate the 25-MHz RX_CLK signal. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase alignment and locks to data in one transition. Its data/clock acquisition time, after power-on, is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data are present (that is, when the SD is deasserted), the PLL switches and locks on to

TX_CLK. This provides a continuously running RX_CLK. At the PCS interface, the 5-bit data RXD[4:0] is synchronized to the 25-MHz RX_CLK.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The 100BASE-TX PHY automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the chance of a receive symbol error.

The baseline wander circuit is not required in 100BASE-FX PHY operation.

MULTIMODE TRANSMITTER

The multimode transmitter transmits MLT3 coded symbols in 100BASE-TX mode, and NRZI coded symbols in 100BASE-FX mode. It utilizes a current drive output, which is well balanced and produces very low noise transmit signals. PECL voltage levels are produced with resistive terminations in 100BASE-FX mode.

The serialized data bypasses the scrambler and 4B/5B encoder in FX mode. The output data are NRZI PECL signals. The PECL level signals are used to drive the fiber-optic transmitter.

STREAM CIPHER SCRAMBLER/DESCRAMBLER

In 100BASE-TX mode, the transmit data stream is scrambled to reduce radiated emissions on the twisted-pair cable. The data are scrambled by exclusive ORing the NRZ signal with the output of an 11-bit wide Linear Feedback Shift register (LFSR), which produces a 2047-bit nonrepeating sequence. The scrambler reduces peak emission by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle code group.

The receiver does not attempt to decode the data stream unless the descrambler is locked. When locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization.

The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle code within 724 μs, it becomes unlocked and the receive decoder is disabled. The descrambler is always forced into the unlock state when a link failure condition is detected.

Stream cipher descrambler is not used in the 100BASE-FX mode.

FEF (FAR-END FAULT)

Auto-negotiation provides the mechanism to inform the link partner that a remote fault has occurred. Auto-negotiation is disabled, however, in the 100BASE-FX applications. An alternative in-band signaling function (FEFI) is used to signal a remote fault condition.

FEFI is a stream of 84 consecutive ones followed by one logic zero. This pattern is repeated three times.

An FEFI signal is given under three conditions:

- When no activity is received from the link partner.
- When the clock recovery circuit detects a signal error or PLL lock error.
- When a management entity sets the Transmit Far-End Fault bit.

The FEFI mechanism is enabled by default in the 100BASE-FX mode and disabled in 100BASE-TX or 10BASE-T modes. The register setting can be changed by software after reset.

TRANSMIT DRIVER

In 100BASE-TX mode, the PHY transmit function converts synchronous 4-bit data nibbles from the MII to a pair of 125-Mbps differential serial data streams. The serial data are transmitted over network twisted-pair cables via an isolation transformer. Data conversion includes 4B/5B encoding, scrambling, parallel-to-serial, NRZ to NRZI, and MLT3 encoding. The entire operation is synchronous to the 25-MHz and 125-MHz clocks. Both clocks are generated by an on-chip PLL clock synthesizer that is locked on to an external 25-MHz clock source.

In 100BASE-FX, the transmit driver does not perform filtering; it utilizes a current drive output that is well balanced and produces a low noise PECL signal. PECL voltage levels are produced with resistive terminations.

In 10BASE-T mode, if the MII interface is used, parallel-to-serial logic is used to convert the 4-bit data into the serial stream through the output wave shaping driver. The wave shaper reduces any EMI emission by filtering out the harmonics, therefore eliminating the need for an external filter.

HP AUTO-MDI/MDIX

This feature is able to detect the required cable connection type (straight-through or crossed-over) and make correction automatically.

MAC INTERFACE

MII

The Media Independent Interface (MII) is an 18-wire MAC/PHY interface described in IEEE 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of physical layer devices through a common interface. MII operates at either 100 Mbps or 10 Mbps, depending on the speed of the physical layer. With clocks running at either 25 MHz or 2.5 MHz, 4-bit data are clocked between the MAC and PHY, synchronously with Enable and Error signals.

At the time of PLL lock on an incoming signal from the wire interface, the PHY generates RX_CLK at either 2.5 MHz for 10 Mbps or 25 MHz for 100 Mbps.

On receipt of valid data from the wire interface, RXDV goes active signaling the MAC that valid data will be presented on the RXD[3:0] pins at the speed of the RX_CLK.

On transmission of data from the MAC, TXEN is presented to the PHY, indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the PHY(synchronous to TX_CLK) during the time that TXEN is valid.

SMI

The PHYs internal registers are accessible only through the MII 2-wire Serial Management Interface (SMI). MDC is a clock input to the PHY, which is used to latch in or out data and instructions for the PHY. The clock can run at any speed from DC to 25 MHz. MDIO is a bidirectional connection used to write instructions to, write data to, or read data from the PHY. Each data bit is latched either in or out on the rising edge of the MDC. The MDC is not required to maintain any speed or duty cycle, provided no half cycle is less than 20 ns, and that data are presented synchronous to the MDC.

MDC/MDIO are a common signal pair to all PHYs on a design. Therefore, each PHY needs to have its own unique physical address. The physical address of the PHY is set using the pins defined as PHYAD[4:0]. These input signals are strapped externally, and are sampled as reset is negated. At idle, the PHY is responsible to pull the MDIO line to a high state. Therefore, a 1 kΩ resistor is required to connect the MDIO line to VCC.

PHYSICAL LAYER INTERFACES

The two supported interfaces are the twisted-pair (TP) interface with auto-MDI/MDIX selection, and the fiber-optic Interface with PECL signaling.

The selection of these two interfaces is performed at reset time by the SD/FXEN signal (pin 28). Pull pin 28 LOW to enable the TP interface, or connect pin 28 to the fiber module to enable FX interface.

Section 2: Pin Descriptions

Many pins perform multiple functions. These pins are designated by a **bold** pin number, and their descriptions are listed in the proper sections. Designers must verify that they have taken into account all modes of operation prior to final design.

Signal types:

- B = Bidirection pin
- P = Power pin
- G = Ground pin
- AI = Analog Input pin
- AO = Analog output pin
- D = Internal pull-down pin
- U = Internal pull-up pin
- Overline = Active low

All digital pins are bidirectional pins.

Table 2: Pinout and Signal Definitions

Pin Number	Pin Name	Type	Description
1	VCC	P	+2.5V power supply.
2	GND	G	Ground.
2	GND	G	Ground.
3	RXDV	B_D	RXDV (active HIGH output): Receive Data Valid is the output signal in the MII mode. RXDV is active HIGH to indicate that the receive frame is in progress, and that the data stream present on the RXD output pins is valid.
4	RX_CLK	B_D	Input function is reserved. This pin must be pulled low externally. RX_CLK (Output): Receive clock in MII mode. RX_CLK is 25-MHz output in 100BASE and 2.5 MHz output in 10BASE. This clock is recovered from the incoming data on the cable inputs.
5	RXER	B_D	Input function is reserved. This pin must be pulled low externally. RXER (active HIGH output): asserted to indicate that an invalid symbol or bad SSD is detected in MII modes.
6	GND	G	Ground.
7	VCC	P	+2.5V power supply.
8	TXER	B_D	TXER (active HIGH input): Transmits an error in the MII interface. When TXER is asserted for one or more TX_CLK periods while TXEN is also asserted, the PHY emits one or more symbols that are not part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.
9	TX_CLK	B_D	TX_CLK (output): Transmits the clock signal of the MII mode. TX_CLK is 25-MHz output in 100BASE operation and 2.5-MHz in 10BASE operation. This clock is a continuously-driven output, generated from the XI (crystal input) pin.
10	TXEN	B_D	TXEN (active HIGH input): Transmits the Enable signal in the MII interfaces. TXEN is asserted by the MAC to indicate that valid data are present on TXD[3:0].
11	TXD0	B_D	TXD0: Transmits data input for the MII interface.
12	TXD1	B_D	TXD1: Transmits data input for the MII interface.
13	TXD2	B_D	TXD2: Transmits data input for the MII interface.
14	TXD3	B_D	TXD3: Transmits data input for MII interface.
15	COL	B_D	COL (active HIGH output): This pin must be pulled low externally. It is the collision detect signal in the MII interface. In half-duplex mode, COL active HIGH output indicates that a collision has occurred. In full-duplex mode, COL remains low.
16	REPEATER/ CRS	B_D	REPEATER: Resets read input. Active HIGH puts the chip in repeater mode. CRS (active HIGH output): Carrier sense signal in the MII interface. CRS is asserted when the twisted-pair media is non-idle and is deasserted when idle, or when a valid end-of-stream delimiter is detected.
17	GND	G	Ground.
18	VCC	P	+2.5V power supply.
19	PHYAD0/ INTR	B_U	PHYAD0: Resets read input. Pull high or low to set the PHY Address bit 0 for the MII management function. INTR (output): Active low Interrupt output. Cleared by reading register 17.

Table 2: Pinout and Signal Definitions (Cont.)

Pin Number	Pin Name	Type	Description
20	$\overline{\text{BURNIN}}$/ LED0	B_U	$\overline{\text{BURNIN}}$: Resets read input. Set Active LOW to put the chip in burn-in test mode. LED0 (output): active LOW, the default behavior is ON when the chip is in link-up condition, and is BLINK when the chip detects transmit or receive activity.
21	SPD100/ LED1	B_U	SPD100: Resets read input. If ANEN is Low, SPD100 sets the TP port speed in register 0. If ANEN is High, SPD100 is used to set 100 Mbps half-duplex and 100 Mbps full-duplex bits in register 4. LED1 (output): active LOW. The default behavior is ON when the chip is operating at 100 Mbps and is OFF when the chip is operating at 10 Mbps.
22	DUPLEX/ LED2	B_U	DUPLEX: Resets read input. If ANEN is Low, DUPLEX sets the TP port in full-duplex mode in register 0. If ANEN is High, DUPLEX is used to set 10 Mbps FDX and 100 Mbps FDX bits in register 4. LED2 (output): active LOW. The default behavior is ON when the chip is operating in full-duplex mode and is OFF when the chip is operating in half-duplex mode.
23	ANEN/LED3	B_U	ANEN (resets read input): Auto-negotiation enable for the twisted-pair port. Pull high to enable auto-negotiation. Pull low to disable auto-negotiation. LED3 (output): active LOW. The default behavior is BLINK when the chip detect collision is in half-duplex mode.
24	$\overline{\text{PDOWN}}$	B_U	$\overline{\text{PDOWN}}$ (input): Power-down input. This pin must be pulled high externally for normal operation. Pulling this pin low puts both the TP and fiber port into power-down mode. This is a regular input, not a reset read signal.
25	VCC	P	+2.5V power supply.
26	RXN	A	Receive. For TP port in MDI mode. Transmit. For TP port in MDIX mode.
27	RXP	A	Receive +. For TP port in MDI mode. Transmit +. For TP port in MDIX mode.
28	SD/FXEN	AI	SD/FXEN (analog input): This pin must be pulled low externally for normal TP mode. Connect to fiber module to enable FX mode; also serves as signal detect input.
29	GND	G	Ground.
30	GND	G	Ground.
31	RBIAD	A	Bias resistor connection. Connect to a 10K 1% resistor to GND.
32	VCCPLL	P	+2.5V supply for analog bias, PLL modules.
33	GND	G	Ground.
34	TXN	A	Transmit. In MDI mode. Receive. In MDIX mode.
35	TXP	A	Transmit +. In MDI mode. Receive +. In MDIX mode.
36	VCC25OUT	P	+2.5VCC out from the on-chip regulator.
37	GND	G	Ground.
38	GND	G	Ground.
39	XO	A	XTAL output.
40	XI	A	XTAL input. In MII Mode: XI and XO is designed to connect to a 25 MHz., 50 PPM XTAL or 25 MHz OSC.
41	VCC33IN	P	3.3V Power supply input.
42	$\overline{\text{RST}}$	I_U	Reset input. active LOW.
43	MDIO	B_U	MDIO (input/ output): Management data I/O. This serial input/output pin is used to read from and write to the MII register. The data value on the MDIO pin is valid and latched on the rising edge of the MDC. This pin requires a 1 kΩ resistor pull-up.
44	MDC	I_D	MDC (input): Management data clock. This pin must be pulled low externally for normal operation. The MDC clock input must be provided to allow MII management function. This pin has a Schmitt trigger input.
45	PHYAD1/ RXD3	B_D	PHYAD1: Resets read input. Pull high or low to set the PHY Address bit 1 for MII management function. RXD3: Receives the data output signal in the MII interface.
46	PHYAD2/ RXD2	B_D	PHYAD2: Resets read input. Pull high or low to set the PHY Address bit 2 for MII management function. RXD2: Receives the data output signal in the MII interface.
47	PHYAD3/ RXD1	B_D	PHYAD3 (Reset Read Input): Pull High or Low to set the PHY Address bit 3 for MII management function. RXD1: Receive data output signal in MII interface.
48	PHYAD4/ RXD0	B_D	PHYAD4: Resets read input. Pull high or low to set the PHY Address bit 4 for MII management function. RXD0: Receives the data output signal in the MII interface.

Section 3: Pinout Diagram

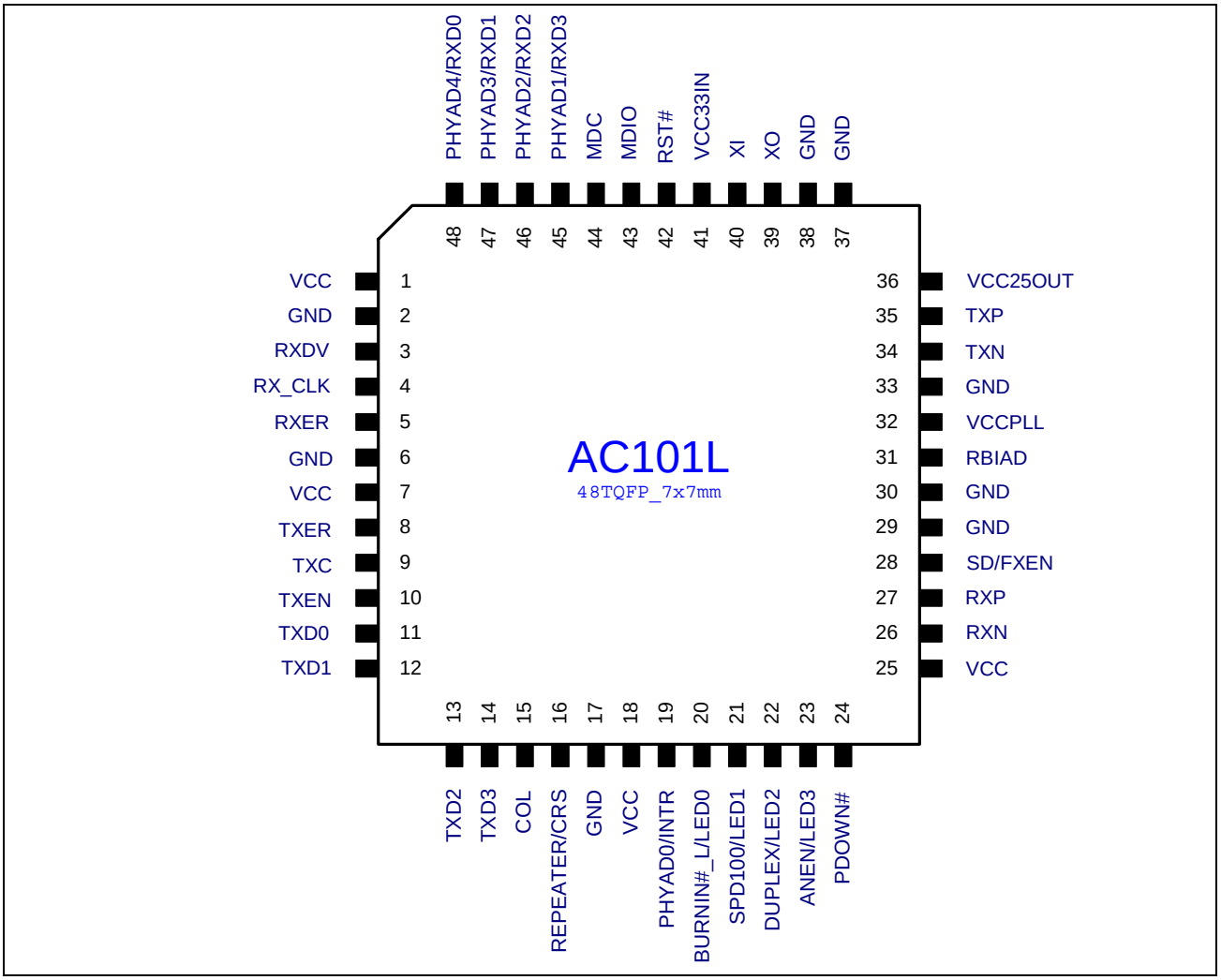


Figure 2: AC101L Pinout Diagram

Section 4: Operational Description

RESET

The PHY can be reset in two ways:

- Hardware reset: (See “Pin Descriptions” on page 7).
- Software reset: (See “Register Description” on page 13).

POWER SOURCE

The AC101L chip provides an onboard 3.3V ±5% input to 2.5V ±5% output regulator with the capability to drive 150 mA of current. The 2.5V output supplies the PHY operation, including the LEDs. It is recommended to limit the LED current below 10 mA per LED.

The 2.5V power should be decoupled to provide the digital and analog pins on the chip.

POWER SAVING MODE

The power consumption of the AC101L device is significantly reduced due to its built-in power management features. Separate power supply lines are used to power the 10BASE-T circuitry and the 100BASE-TX circuitry. Therefore, the two circuits can be turned on and turned off independently. When the PHY is set to operate in 100BASE-TX mode, 10BASE-T circuitry is powered down.

The following power management features are supported:

- **Power-down mode**: (see pin and register descriptions). During power down mode, the device is still able to interface through the management interface.
- **Energy detect/power saving mode**: Energy detect mode turns off the power to select internal circuitry when there is no live network connected. The energy detect (ED) circuit is always turned on to monitor if there is signal energy present on the media. The management circuitry is also powered on and ready to respond to any management transaction. The transmit circuit still sends out link pulses with minimum power consumption. If a valid signal is received from the media, the device powers up and resumes normal transmit/receive operations.
- **Valid data detection mode**: This can be achieved by writing to the Receive Clock Register control bit. During this mode, if there is no data other than incoming idles, the receive clock (RX_CLK) turns itself off. This could save the power of the attached media access controller. RX_CLK resumes operation one clock period prior to the assertion of RXDV. The receive clock again shuts off 64 clock cycles after RXDV is deasserted.

CLOCK SOURCE

The clock source for this chip is from the XI pin. In MII mode, it can connect to a 25 MHz 50 ppm (parts per million) OSC or a 25 MHz 50 ppm XTAL (crystal).

ISOLATE MODE

When the AC101L device is put into isolate mode, all MII inputs (TXD[3:0}, TXEN, TXER) are ignored, and all MII outputs (TX_CLK, COL, CRS, RX_CLK, RXDV, RXER, RXD[3:0] are set to high impedance. Only the MII management pins (MDC, MDIO) operate normally. Pull HIGH pin 4 at reset or write 1 to bit 10 register 0 to put the chip into isolate mode.

LOOPBACK MODE

Local loopback is provided for testing purpose. It can be enabled by writing a one to register 0 bit 14.

The local loopback routes transmitted data through the transmit path back to the clock and data recovery module of the receiving path. The loopback data are presented to the PCS in 5-bit symbol format. This loopback is used to check the operation of the 5-bit symbol decoder and the phase lock loop circuitry. In local loopback, the SD output is forced to a logical 1 and TXOP/N outputs are tristated.

INTERRUPT MODE

The INTR pin on the PHY is asserted whenever 1 of 8 selectable interrupt events occurs. The assertion state is high or low and is programmable through the INTR_LEVL register bit. The selection is made by setting the appropriate bit in the upper half of the Interrupt Control/Status register. When the INTR bit goes active, the MAC interface is required to read the Interrupt Control/Status register to determine which event caused the interrupt. The Status bits are read-only and clear-on-read. When INTR is not asserted, the pin is held in a high impedance state.

LED OPERATION

LED INTERFACE

The LED interface is fully configurable through register setting. The connection of LED (source/sink current) depends on the default setting.

The default LED modes are as shown below:

LED0	LED1	LED2	LED3
Link/Activity	Speed	Duplex	Collision

LED CONFIGURATION

The LEDs are fully configurable to other operational modes. Each LED has two 16-bit registers to define its operation. See “Common Registers” on page 22 and Table 3 below to configure the LEDs to work with operational modes other than default mode.

LED [3:0] EVENT TABLE

LED [3:0] are configurable. The following events are defined for AC101L operation:

Table 3: LED [3:0] Event Table

Bit#	***Description***
7	Duplex
6	Collision
5	Speed 100
4	Speed 10
3	Transmit activity
2	Transmit/Receive activity
1	Receive activity
0	Link

Section 5: Register Description

The first 7 registers of the MII register set are defined by the MII specification. In addition to these required registers there are several registers specific to Altima Communications Inc. There are reserved registers and/or bits that are for Altima internal use only. The following standard registers are supported (*register numbers are in decimal notation; the values are in hexadecimal notation*):

When writing to registers, it is recommended that a read/modify/write operation be performed, as unintended bits may get set to unwanted states. This applies to all registers, including those with reserved bits.

Legend:

- RW = Read and write access
- SC = Self-clearing
- LL = Latch low until cleared by reading
- RO = Read-only
- RC = Cleared on read
- LH = Latch high until cleared by reading

TP PHY Register Summary

Table 4: TP PHY Register Summary

Register	*Description*	*Default Value*
Registers 0–7		
0	Control register	3000
1	Status register	7849
2	PHY Identifier 1 register	0022
3	PHY Identifier 2 register	5521
4	Auto-Negotiation Advertisement register	01E1
5	Auto-Negotiation Link Partner Ability register	0001
6	Auto-Negotiation Expansion register	0004
7	Next Page Advertisement register	2001
Registers 8–31		
8–15	Reserved	XXXX
16	BT and Interrupt Level Control register	1800
17	Interrupt Control/Status register	0000
18,19	Reserved	XXXX
20	Cable Measurement Capability register	XXXX
21	Receive Error Counter register	0304
22–31	Reserved	XXXX

REGISTER 0: CONTROL REGISTER

Table 5: Register 0: Control Register

Bit	Name	Description	Mode	Default
0.15	Reset	1 = PHY reset. This bit is self-clearing.	RW/ SC	0
0.14	Loopback	1 = Enable loopback mode. This loops back TXD to RXD and ignores all of the activity on the cable media. 0 = Normal operation.	RW	0
0.13	Speed Select	1 = 100 Mbps. 0 = 10 Mbps. Default value: SPD100	RW	Set by SPD100
0.12	ANEN Enable	1 = Enable the auto-negotiate process (overrides 0.13 and 0.8). 0 = Disable the auto-negotiate process. Mode selection is controlled via bit 0.8, 0.13. Default value: ANEN	RW	Set by ANEN
0.11	Power Down	1 = Power down. All blocks except for SMI will be turned off. Setting $\overline{\text{PDOWN}}$ pin (24) to LOW will achieve the same result. 0 = Normal operation.	RW	0
0.10	Isolate	1 = N/A. 0 = Normal operation.	RW	0
0.9	Restart ANEN	1 = Restart auto-negotiation process. 0 = Normal operation.	RW/ SC	0
0.8	Duplex Mode	1 = Full-duplex operation. 0 = Half-duplex operation. Default value: !ANEN && DUPLEX	RW	See description
0.7	Collision Test	1 = Enable collision test that issues the COL signal in response to the assertion of the TXEN signal. Collision test is disabled if the PCSBP pin is high. Collision test is enabled regardless of the duplex mode. 0 = Disable COL test.	RW	0
0.[6:0]	Reserved	–	RW	0000000

REGISTER 1: STATUS REGISTER

Table 6: Register 1: Status Register

Bit	Name	Description	Mode	Default
1.15	100BASE-T4	Permanently tied to zero; indicates no 100BASE-T4 capability.	RO	0
1.14	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable. Default value: SPD100 && DUPLEX	RO	See description

Table 6: Register 1: Status Register (Cont.)

Bit	*Name*	*Description*	*Mode*	*Default*
1.13	100BASE-TX Half-Duplex	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable. Default value: SPD100 && (ANEN || !DUPLEX).	RO	See description
1.12	10BASE-T Full-Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable. Default value: DUPLEX && (ANEN || !SPD100).	RO	See description
1.11	10BASE-T Half-Duplex	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable. Default value: ANEN || (!SPD100 && !DUPLEX).	RO	See description
1.[10:7]	Reserved	–	RO	0000
1.6	MF Preamble Suppression	The PHY is able to perform management transaction without MDIO preamble. The management interface needs a minimum of 32 bits of preamble after reset.	RO	1
1.5	ANEN Complete	1 = Auto-negotiation process completed. Registers 4, 5, and 6 are valid after this bit is set. 0 = Auto-negotiation process is not completed.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit remains set until it is cleared by reading register 1.	RO/LH	0
1.3	ANEN Ability	1 = Able to perform the auto-negotiation function; default value is determined by the ANEN pin. 0 = Unable to perform the auto-negotiation function.	RO	Set by ANEN
1.2	Link Status	1 = Link is established. If the link fails, this bit clears and remains at 0 until the register is read again. 0 = Link is down.	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detected. 0 = No Jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capable. This bit is tied permanently to a value of 1.	RO	1

REGISTER 2: PHY IDENTIFIER 1 REGISTER

Table 7: Register 2: PHY Identifier 1 Register

Bit	Name	Description	Mode	Default
2.[15:0]	OUI[a]	Composed of bits 3 —18 of the Organizationally Unique Identifier (OUI), respectively.	RO	0022(H)

a. Based on an OUI of 0010A9 (hexadecimal)

REGISTER 3: PHY IDENTIFIER 2 REGISTER

Table 8: Register 3: PHY Identifier 2 Register

Bit	Name	Description	Mode	Default
3.[15:10]	OUI[a]	Assigned to bits 19 — 24 of the OUI.	RO	010101
3.[9:4]	Model Number	6-bit manufacturer's model number.	RO	010010
3.[3:0]	Revision Number	4-bit manufacturer's revision number.	RO	0001

a. Based on an OUI of 0010A9 (hexadecimal)

REGISTER 4: AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 9: Register 4: Auto-Negotiation Advertisement Register

Bit	Name	Description	Mode	Default
4.15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
4.14	Acknowledge	This bit is set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.[13:11]	Reserved	–		
4.10	FDFC	Full-duplex flow control. 1 = Advertise that the DTE (MAC) has implemented both the optional MAC control sublayer and the pause function as specified in Clause 31 and Annex 31B of IEEE 802.3u. 0 = MAC does not support flow control.		
4.9	100BASE-T4	Technology not supported. This bit is always 0.	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable. Default value: SPD100 && DUPLEX.	RW	See description
4.7	100BASE-TX	1 = 100BASE-TX half-duplex capable. 0 = Not TX half-duplex capable. Default value: SPD100 && (ANEN || !DUPLEX).	RW	See description
4.6	10BASE-T Full Duplex	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable. Default value: DUPLEX && (ANEN || !SPD100).	RW	See description

Table 9: Register 4: Auto-Negotiation Advertisement Register (Cont.)

Bit	Name	Description	Mode	Default
4.5	10BASE-T	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable. Default value: ANEN || (!SPD100 && !DUPLEX).	RW	See Description
4.[4:0]	Selector Field	Protocol selection [00001] = IEEE 802.3.	RO	00001

REGISTER 5: AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER/LINK PARTNER NEXT PAGE MESSAGE

Table 10: Register 5: Auto-Negotiation Link Partner Ability Register/Link Partner Next Page Message

Bit	Name	Description	Mode	Default
5.15	Next Page	1 = Link partner desires a Next Page transfer. 0 = Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	1 = Link Partner acknowledges reception of FLP words. 0 = Not acknowledged by the link partner.	RO	0
5.[13:10]	Reserved	–		
5.9	100BASE-T4	1 = 100BASE-T4 operation supported by the link partner. 0 = 100BASE-T4 operation not supported by the link partner.	RO	0
5.8	100BASE-TX Full Duplex	1 = 100BASE-TX full-duplex operation supported by the link partner. 0 = 100BASE-TX full-duplex operation not supported by the link partner.	RO	0
5.7	100BASE-TX	1 = 100BASE-TX half-duplex operation supported by the link partner. 0 = 100BASE-TX half-duplex operation not supported by the link partner.	RO	0
5.6	10BASE-T Full Duplex	1 = 10 Mbps full-duplex operation supported by the link partner. 0 = 10 Mbps full-duplex operation not supported by the link partner.	RO	0
5.5	10BASE-T	1 = 10 Mbps half-duplex operation supported by the link partner. 0 = 10 Mbps half-duplex operation not supported by the link partner.	RO	0
5.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

Note: When this register is used as the Next Page message, the bit definition is the same as that of register 7.

REGISTER 6: AUTO-NEGOTIATION EXPANSION REGISTER

Table 11: Register 6: Auto-Negotiation Expansion Register

Bit	Name	Description	Mode	Default
6.[15:5]	Reserved	–	RO	0

Table 11: Register 6: Auto-Negotiation Expansion Register (Cont.)

Bit	Name	Description	Mode	Default
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection logic; this fault is due to more than one technology detecting a concurrent link-up condition. This bit can only be cleared by reading register 6, using the management interface. 0 = No fault detected by parallel detection logic.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner supports Next Page function. 0 = Link partner does not support Next Page function.	RO	0
6.2	Next Page Able	Next page is supported.	RO	1
6.1	Page Received	This bit is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability register. This bit is cleared upon a read of this register.	RC	0
6.0	Link Partner ANEN-Able	1 = Link partner is auto-negotiation capable. 0 = Link partner is not auto-negotiation capable.	RO	0

REGISTER 7: AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 12: Register 7: Auto-Negotiation Next Page Transmit Register

Bit	Name	Description	Mode	Default
7.15	NP	1 = Another Next Page desired. 0 = No other Next Page transmit desired.	RW	0
7.14	Reserved	–	RO	0
7.13	MP	1 = Message page. 0 = Unformatted page.	RW	1
7.12	ACK2	1 = Will comply with message. 0 = Cannot comply with message.	RW	0
7.11	TOG_TX	1 = Previous value of transmitted link code word equals to 0. 0 = Previous value of transmitted link code word equals to 1.	RW	0
17.[10:0]	CODE	Message/Unformatted Code field.	RW	001

REGISTER 16: BT AND INTERRUPT LEVEL CONTROL REGISTER

Table 13: Register 16: BT and Interrupt Level Control Register

Bit	Name	Description	Mode	Default
16.15	Repeater	1 = Repeater mode. Full-duplex is inactive, and CRS only responds to receive activity. SQE test function is disabled.	RW	Set by Repeater
16.14	Reserved	-	RW	0
16.13	TXJAM	1 = Forces CIM to send JAM pattern. 0 = Normal operation.	RW	0
16.12	Reserved	-	RO	1
16.11	SQE Test Inhibit	1 = Disable 10BASE-T SQE testing. 0 = Enable 10BASE-T SQE testing, which generates a COL pulse following the completion of a packet transmission**.**	RW	0
16.[10:6]	Reserved	–	RO	0

Table 13: Register 16: BT and Interrupt Level Control Register (Cont.)

Bit	Name	Description	Mode	Default
16.5	Autopolarity Disable	1 = Disables autopolarity detection/correction. 0 = Enables autopolarity detection/correction.	RW	0
16.4	Reverse Polarity	1 = Reverses polarity when register 16.5 = 0. 0 = Normal polarity when register 16.5 = 0. If register 16.5 is set to 1, writing a 1 to this bit reverses the polarity of the transmitter.	RW	0
16.[3:0]	Reserved	–	RO	0

REGISTER 17: INTERRUPT CONTROL/STATUS REGISTER

Table 14: Register 17: Interrupt Control/Status Register

Bit	Name	Description	Mode	Default
17.15	Jabber_IE	Jabber interrupt enable.	RW	0
17.14	RXER_IE	Receive error interrupt enable.	RW	0
17.13	Page_Rx_IE	Page received interrupt enable.	RW	0
17.12	PD_Fault_IE	Parallel detection fault interrupt enable.	RW	0
17.11	LP_Ack_IE	Link partner acknowledge interrupt enable.	RW	0
17.10	Link_Status_Change_IE	Link status change interrupt enable.	RW	0
17.9	R_Fault_IE	Remote fault interrupt enable.	RW	0
17.8	ANEN_Comp_IE	Auto-negotiation complete interrupt enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	RXER_Int	This bit is set when RXER transitions HIGH.	RC	0
17.5	Page_Rx_Int	This bit is set when a new page is received during ANEN.	RC	0
17.4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Not_OK Int	This bit is set when link status switches from OK status to Non-OK status (fail or ready).	RC	0
17.1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17.0	ANEN _Comp Int	This bit is set when ANEN is complete.	RC	0

REGISTER 18: DIAGNOSTIC REGISTER

Table 15: Register 18: Diagnostic Register

Bit	Name	Description	Mode	Default
18.[15]	Reserved	Reserved.	RW	0
18.[14]	Reserved	Reserved.	RW	0
18.[13]	Force Link Pass 10BT	1 = Enables force link pass 10BASE-T. 0 = Disables force link pass 10BASE-T.	RW	0
18.[12]	Force Link Pass 100TX	1 = Force link pass 100BASE-TX. 0 = Disable Force link pass 100BASE-TX.	RW	0
18.11	Reserved	Reserved.	RO	0

Table 15: Register 18: Diagnostic Register (Cont.)

Bit	Name	Description	Mode	Default
18.10	Reserved	Reserved.	RO	0
18.9	Reserved	Reserved.	RO	0
18.8	Reserved	Reserved.	RO/RC	0
18.[7:0]	Reserved	Reserved.	RO	0

REGISTER 19: POWER/LOOPBACK REGISTER

Table 16: Register 19: Power/Loopback Register

Bit	Name	Description	Mode	Default
19.[14:7]	Reserved	Reserved.	RW	00
19.6	Reserved	Reserved.	RW	0
19.5	Disable Watchdog Timer for Decipher	1 = Disables watchdog timer. 0 = Enables advanced power saving mode.	RW	0
19.4	Low Power Mode Disable	0 = Enables advanced power saving mode. 1 = Disables advanced power saving mode. (Do not enable this bit during normal operation).	RW	0
19.3	Reserved	Reserved.	RW	0
19. 2	Reserved	Reserved.	RW	0
19.1	NLP Link Integrity Test	1 = In auto-negotiation test mode, sends NLP instead of FLP to test NLP receive integrity. 0 = Sends FLP in auto-negotiation test mode.	RW	0
19.0	Jabber Disable	1 = Disables jabber.	RW	0

REGISTER 20: CABLE MEASUREMENT CAPABILITY REGISTER

Table 17: Register 20: Cable Measurement Capability Register

Bit	Name	Description	Mode	Default
20.15	Reserved	Reserved.	RW	1
20.14	Reserved	1 = On. 0 = Off.	RW	1
20.[13:9]	Reserved	Reserved.	RO	0
[a]20.8	Adaptation Disable	1 = Disables adaptation. 0 = Enables adaptation.	RW	0
20.[7:4]	Cable Measurement Capability	These bits can be used as a cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100 MHz. The value is a read back from the equalizer, and the measured value is not absolute.	RW	X
20.[3:0]	Reserved	Reserved.	RO	X

a. To set the value of 20.[7:4], you must turn on bit 20.8 and turn off bit 20.14. Otherwise, this PHY rejects receive packets.

REGISTER 21: RECEIVE ERROR COUNTER

Table 18: Register 21: Receive Error Counter

Bit	Name	Description	Mode	Default
21.[15:0]	RXER Counter	Counts Receive Error events.	RO	0

REGISTER 22: POWER MANAGEMENT REGISTER

Table 19: Register 22: Power Management Register

Bit	Name	Description	Mode	Default
22.[15:14]	Reserved	–	RO	00
22.13	PD_PLL	1 = PLL circuit powers down.	RO	X
22.12	PD_EQUAL	1 = Equalizer circuit powers down.	RO	X
22.11	PD_BT_RCVR	1 = 10BASE-T receiver powers down.	RO	X
22.10	PD_LP	1 = Link pulse receiver powers down.	RO	X
22.9	PD_EN_DET	1 = Energy-detect circuit powers down.	RO	X
22.8	PD_FX	1 = FX circuit powers down.	RO	X
22.[7:6]	Reserved	–	RW	00
22.5	MSK_PLL	0 = Forces PLL circuit to power up. 1 = PLL circuit auto power-down.	RW	1
22.4	MSK_EQUAL	0 = Forces equalizer circuit to power up.	RW	X
22.3	MSK_BT_RCVR	0 = Forces 10BASE-T receiver to power up.	RW	X
22.2	MSK_LP	0 = Forces link pulse receiver to power up.	RW	X
22.1	MSK_EN_DET	0 = Forces energy-detect circuit to power up.	RW	X
22.0	MSK_FX	0 = Forces FX circuit to power up.	RW	X

REGISTER 23: OPERATION MODE REGISTER

Table 20: Register 23: Operation Mode Register

Bit	Name	Description	Mode	Default
23.[15:14]	Reserved	–		
23.13	Clk_rclk_save	1 = Sets rclk save mode. Rclk shuts off after 64 cycles of each packet.		0
23.12	Reserved	–		
23.11	Scramble Disable	1 = Disables scrambler. 0 = Enables scrambler.	RW	0
23.10	Reserved	–	RW	0
23.9	Pcsbp	1 = Enables PCS bypass mode. 0 = Disables PCS bypass mode.	RW	0
23:8	Reserved	–	RW	0
23.7	Auto-MDIX disable	0 = Auto-MDIX mode. 1 = Disable Auto-MDIX mode.	RW	0

Table 20: Register 23: Operation Mode Register (Cont.)

Bit	Name	Description	Mode	Default
23.6	MDIX state	Only valid when register 23.7 is set to 1. 0 = MDI 1= MDIX	RW	0
23.5	Reserved	–	RO	0
23.[4:0]	Reserved	–	RO	XXXXX

REGISTER 24: CRC FOR RECENT RECEIVED PACKET

Table 21: Register 24: CRC for Recent Received Packet

Bit	Name	Description	Mode	Default
24.[15:0]	CRC16	Displays CRC16 value. For system-level test purposes.	RC	0000H

COMMON REGISTERS

The following registers are mapped to Reg28-31 on the TP PHY. Reg28.[15:12] is used as page selection. There are multiple pages of Reg29-31, depends on the value of Reg28[15:12].

COMMON REGISTER 0 (MAP TO REG28) MODE CONTROL REGISTER

Table 22: Common Register 0 (Map to Reg. 28) Mode Control Register

Bit	Name	Description	Mode	Default
A.28.[15:12]	Page Selection	Selects multiple common register pages.	RW	0000
A.28.[11:7]	Reserved	Reserved.	RO	0000
A.28.6	MII_enable	1 = Enables MII interface.	RW	1
A.28.5	Reserved	Reserved.	RO	0
A.28.4	Reserved	Reserved.	RW	0
A.28.3	Reserved	Reserved.	RO	0
A.28.2	Act select	Selects activity event. 0 = Receive activity. 1 = TX or RX activity.	RW	1
A.28.1	Reserved	–	RO	0
A.28.0	Reserved	–	RO	0

COMMON REGISTER 1: (MAP TO REG. 29, PAGE 0 A28.[15:12]=0000) TEST MODE REGISTER

Table 23: Common Register 1: (Map to Reg. 29, Page 0 A28.[15:12]=0000) Test Mode Register

Bit	Name	Description	Mode	Default
A0.29.15	Reduce_mcount	Reduces millisecond counter to 256 microseconds.	RO	0
A0.29.[14:10]	Reserved	–	RO	00100
A0.29.[9:8]	Reserved	–	RW	00
A0.29.[7:4]	Test Mode	0000 = Normal operation.	RW	0000
A0.29.3	Burn In	1 = Enables burn-in test mode. 0 = Normal operation.	RW	0
A0.29.2	Output Disable	1 = Disables all digital output. 0 = Normal operation.	RW	0
A0.29.1	Reserved	0 = Normal operation.	RW	0
A0.29.0	Reduce Timer	1 = Reduces timer for auto-negotiation testing. 0 = Normal operation.	RW	0

COMMON REGISTER 4: (MAP TO REG. 29, PAGE 1 A28.[15:12]=0001) LED BLINK RATE

Table 24: Common Register 4: (Map to Reg. 29, Page 1 A28.[15:12]=0001) LED Blink Rate

Bit	Name	Description	Mode	Default
A1.29.[15:8]	Reserved	–	RO	00000000
A1.29.[7:0]	Blink Rate	Set LED blink rate. The blink rate is this number × 16 ms. Default value is 256 ms.	RW	00010000

COMMON REGISTER 5: (MAP TO REG. 30, PAGE 1 A.28.[15:12]=0001) LED0 SETTING1 REGISTER

Default operation for LED0 is ON when Link; BLINK when Activity.

Table 25: Common Register 5: (Map to Reg. 30, Page 1 A.28.[15:12]=0001) LED0 Setting1 Register

Bit	Name	Description	Mode	Default
A1.30.[15:13]	Reserved	–	RW	0000
A1.30.12	Force LED On	Forces LED0 on.	RW	0
A1.30.[11:9]	Reserved	–	RW	000
A1.30.8	Force LED Off	Forces LED0 off.	RW	0
A1.30.[7:0]	Msk Blink	Blink mask. When the bits are set to 1, a corresponding event causes the LED to blink.	RW	00000100

COMMON REGISTER 6: (MAP TO REG. 31, PAGE 1 A.28.[15:12]=0001) LED0 SETTING2 REGISTER

Table 26: Common Register 6: (Map to Reg. 31, Page 1 A.28.[15:12]=0001) LED0 Setting2 Register

Bit	Name	Description	Mode	Default
A1.31. [15:8]	Msk On	On mask. When the bits are set to 1, a corresponding event causes the LED to turn on.	RW	00000001
A1.31. [7:0]	Msk Off	Off mask. When the bits are set to 1, a corresponding event causes the LED to turn off.	RW	00000000

COMMON REGISTER 7: (MAP TO REG. 29, PAGE 2 A.28.[15:12]=0010) LED1 SETTING1 REGISTER

Table 27: Common Register 7: (Map to Reg. 29, Page 2 A.28.[15:12]=0010) LED1 Setting1 Register

Bit	Name	Description	Mode	Default
A2.29.[15:13]	Reserved	–	RO	000
A2.29.12	Force LED On	Forces LED1 on.	RW	0
A2.29.[11:9]	Reserved	–	RO	000
A2.29.8	Force LED Off	Forces LED1 off.	RW	0
A2.29.[7:0]	Msk Blink	Blink mask. When the bits are set to 1, a corresponding event causes the LED to blink.	RW	00000000

COMMON REGISTER 8: (MAP TO REG. 30, PAGE 2 A.28.[15:12]=0010) LED1 SETTING2 REGISTER

Default Operation for LED1 is ON during 100 Mbps operation.

Table 28: Common Register 8: (Map to Reg. 30, Page 2 A.28.[15:12]=0010) LED1 Setting2 Register

Bit	Name	Description	Mode	Default
A2.30.[15:8]	Msk On	On mask. When the bits are set to 1, a corresponding event causes the led to turn on.	RW	00100000
A2.30.[7:0]	Msk Off	Off mask. When the bits are set to one, a corresponding event causes the led to turn off.	RW	00000000

COMMON REGISTER 9: (MAP TO REG. 31, PAGE 2 A.28.[15:12]=0010) LED2 SETTING1 REGISTER

Table 29: Common Register 9: (Map to Reg. 31, Page 2 A.28.[15:12]=0010) LED2 Setting1 Register

Bit	Name	Description	Mode	Default
A2.31.[15:13]	Reserved	–	RO	000
A2.31.12	Force LED On	Forces LED2 on.	RW	0
A2.31.[11:9]	Reserved	–	RO	000
A2.31.8	Force LED Off	Forces LED2 off.	RW	0

Table 29: Common Register 9: (Map to Reg. 31, Page 2 A.28.[15:12]=0010) LED2 Setting1 Register (Cont.)

Bit	Name	Description	Mode	Default
A2.31.[7:0]	Msk Blink	Blink mask. When the bits are set to 1, a corresponding event causes the led to blink.	RW	00000000

COMMON REGISTER 10: (MAP TO REG. 29, PAGE 3 A.28.[15:12]=0011) LED2 SETTING2 REGISTER

Default operation for LED2 is ON during duplex mode operation.

Table 30: Common Register 10: (Map to Reg. 29, Page 3 A.28.[15:12]=0011) LED2 Setting2 Register

Bit	Name	Description	Mode	Default
A3.29.[15:8]	Msk On	On mask. When the bits are set to 1, a corresponding event causes the led to turn on.	RW	10000000
A3.29.[7:0]	Msk Off	Off mask. When the bits are set to 1, a corresponding event causes the led to turn off.	RW	00000000

COMMON REGISTER 11: (MAP TO REG. 30, PAGE 3 A.28[.15:12]=0011) LED3 SETTING1 REGISTER

Default operation for LED3 is BLINK when COL.

Table 31: Common Register 11: (Map to Reg. 30, Page 3 A.28[.15:12]=0011) LED3 Setting1 Register

Reg.bit	Name	Description	Mode	Default
A3.30.[15:13]	Reserved	–	RO	000
A3.30.12	Force LED On	Forces LED3 on.	RW	0
A3.30.[11:9]	Reserved	–	RO	000
A3.30.8	Force LED Off	Forces LED3 off.	RW	0
A3.30.[7:0]	Msk Blink	Blink mask. When the bits are set to 1, a corresponding event causes the led to blink.	RW	0100000

COMMON REGISTER 12: (MAP TO REG. 31, PAGE 3 A.28.[15:12]=0011) LED3 SETTING2 REGISTER

Table 32: Common Register 12: (Map to Reg. 31, Page 3 A.28.[15:12]=0011) LED3 Setting2 Register

Bit	Name	Description	Mode	Default
A3.31.[15:8]	Msk On	On mask. When the bits are set to 1, a corresponding event causes the led to turn on.	RW	00000000
A3.31.[7:0]	Msk Off	Off mask. When the bits are set to 1, a corresponding event causes the led to turn off.	RW	00000000

Section 6: 4B/5B Code Group

Table 33: 4B/5B Code Group

Symbol name	*4B code*	*5B code*	*Description*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
Idle and control codes			
I	0000	11111	Idle
J	0101	11000	Start-of-stream delimiter, part 1 of 2; always use in pair with K symbol
K	0101	10001	Start-of-stream delimiter, part 2 of 2; always use in pair with J symbol
T	Undefined	01101	End-of-stream delimiter, part 1 of 2; always use in pair with R symbol
R	Undefined	00111	End-of-stream delimiter, part 2 of 2; always use in pair with T symbol
Invalid code			
H	Undefined	00100	Transmit error; used to send HALT code group
V	Undefined	00000	Invalid code
V	Undefined	00001	Invalid code
V	Undefined	00010	Invalid code
V	Undefined	00011	Invalid code
V	Undefined	00101	Invalid code
V	Undefined	00110	Invalid code
V	Undefined	01000	Invalid code
V	Undefined	01100	Invalid code
V	Undefined	10000	Invalid code
V	Undefined	11001	Invalid code

Section 7: SMI Read/Write Sequence

Table 34: SMI Read/Write Sequence

SMI read/write sequence								
–	Pream (32 bits)	Start (2 bits)	Opcode (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	TurnAround (2 bits)	Data (16 bits)	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	D…D	Z
Write	1…1	01	01	AAAAA	RRRRR	10	D…D	Z

Section 8: Timing and AC Characteristics

CLOCK TIMING

Table 35: Clock Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
XTAL input cycle time	CK_CYCLE	–	40	–	ns
XTAL input high/low time	CK_HI CK_LO	–	20	–	ns
XTAL input rise/fall time	CK_EDGE	–	–	4	ns

RESET TIMING

Table 36: Reset Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
Reset pulse length low period with stable XTAL input	RESET_LEN	1	–	–	µs
Activity after end of hardware reset	RESET_WAIT	1	–	–	seconds
Reset rise/fall time	RESET_EDGE	–	5	10	ns

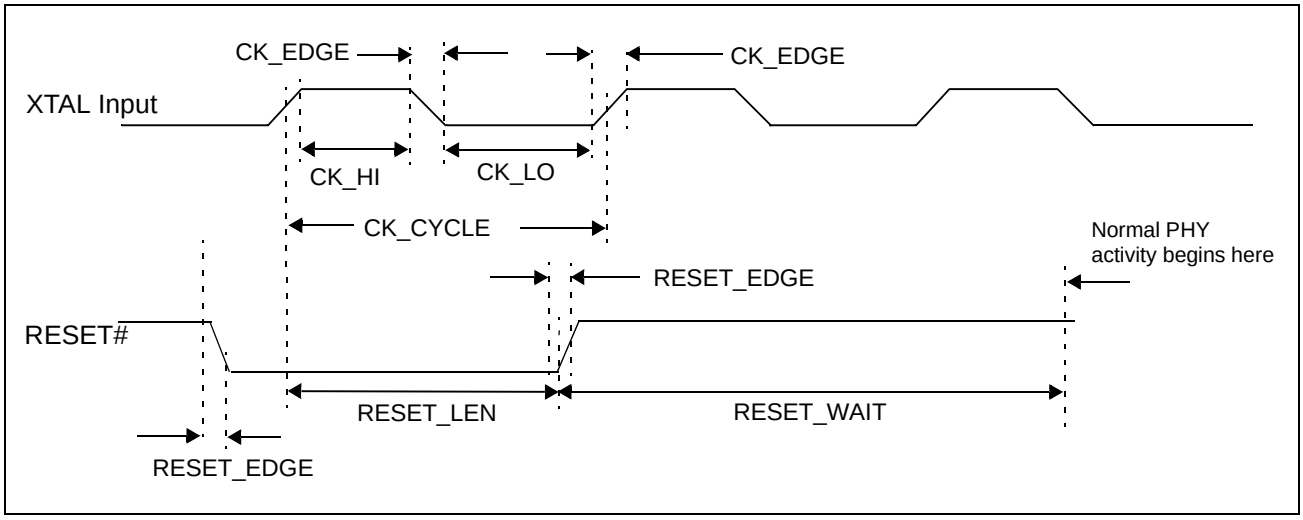


Figure 3: Reset Timing

MANAGEMENT DATA INTERFACE TIMING

Table 37: Management Interface Timing

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Units*
MDC cycle time	MDC_CYCLE	40	–	–	ns
MDC high/low	–	20	–	–	ns
MDC rise/fall time	MDC_RISE MDC_FALL	–	–	10	ns
MDIO input setup time to MDC rising	MDIO_SETUP	10	–	–	ns
MDIO input hold time from MDC rising	MDIO_HOLD	10	–	–	ns
MDIO output delay from MDC rising	MDIO_DELAY	0	–	30	ns

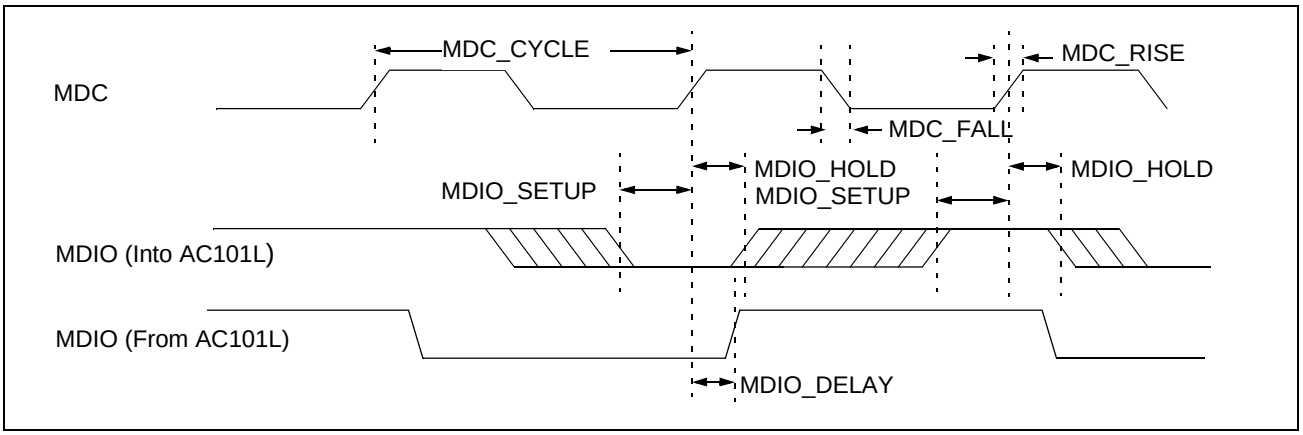


Figure 4: Management Interface Timing

100BASE-TX/FX MII TRANSMIT SYSTEM TIMING

Table 38: 100BASE-X MII Transmit System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
TX_CLK period	tCK	–	39.998	40.000	40.002	ns
TX_CLK high period	tCKH	–	18.000	20.000	22.000	ns
TX_CLK low period	tCKL	–	18.000	20.000	22.000	ns
TXEN to /J/	tTJ	–	–	60	140	ns
TXEN sampled to CRS	tCSA	RPTR is logic low	–	60	140	ns
TXEN sampled to COL	tCLA	RPTR is logic low	–	60	140	ns
!TXEN to /T/	tTT	–	–	60	140	ns
!TXEN sampled to !CRS	tCSD	RPTR is logic low	–	60	140	ns
!TXEN sampled to !COL	tCLD	RPTR is logic low	–	60	140	ns
TX propagation delay	tTJ	From TXD[3:0] to TXOP/N(FXTP/N)	–	60	140	ns

Table 38: 100BASE-X MII Transmit System Timing (Cont.)

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
TXD[3:0], TXEN, TXER setup	tTXS	From rising edge of TX_CLK	10	–	–	ns
TXD[3:0], TXEN, TXER hold	tTXH	From rising edge of TX_CLK	0	–	25	ns

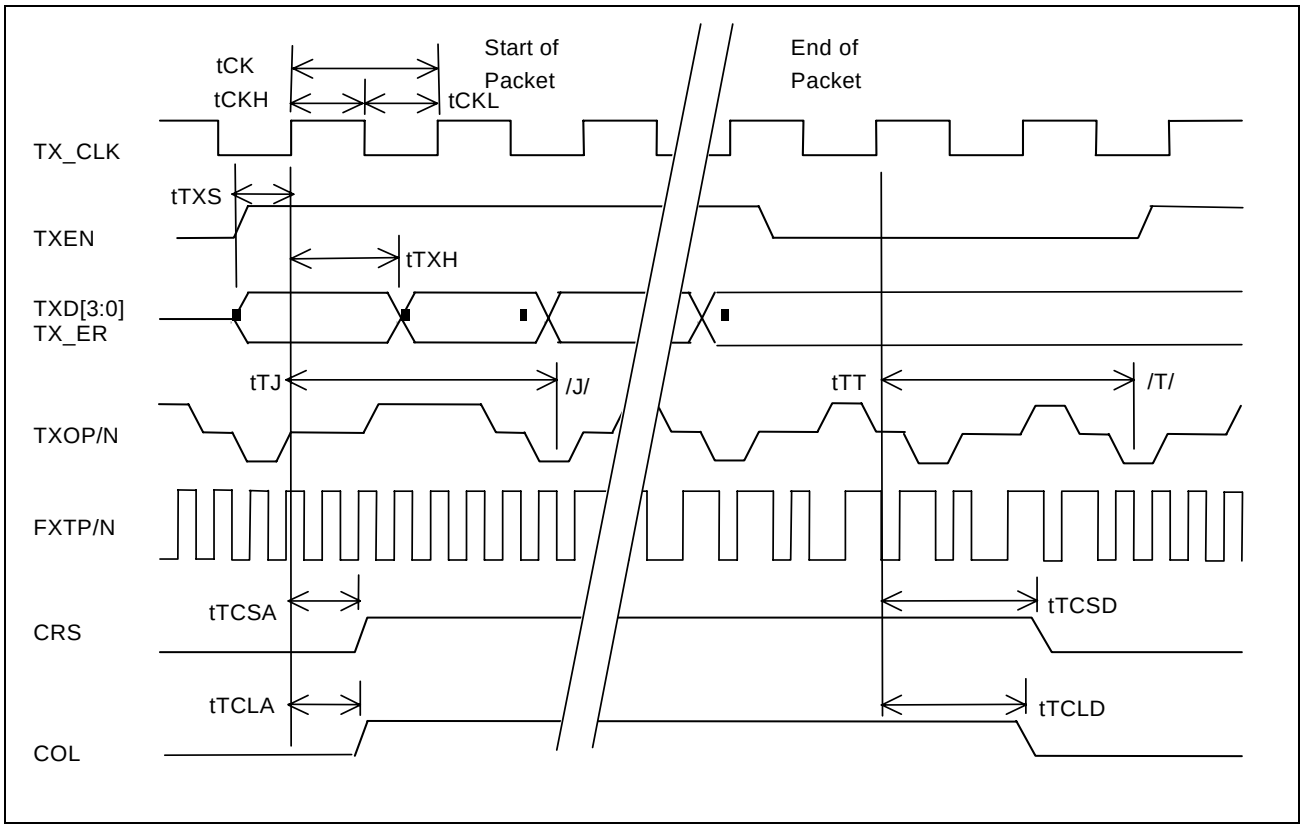


Figure 5: 100BASE-TX/FX MII Transmit Timing

100BASE-TX/FX MII RECEIVE SYSTEM TIMING

Table 39: 100BASE-TX/FX MII Receive System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RX_CLK period	tCK	–	39.998	40.000	40.002	ns
RX_CLK high period	tCKH	–	18.000	20.000	22.000	ns
RX_CLK low period	tCKL	–	18.000	20.000	22.000	ns
/J/K to RXDV assert	tRDVA	–	–	40	180	ns
/J/K to CRS assert	tRCSA	–	–	40	180	ns
/J/K to COL assert	tRCLA	RPTR is logic low.	–	40	180	ns
/T/R to !RXDV	tRDVD	RPTR is logic low.	–	40	180	ns
/T/R to !CRS	tRCSD	RPTR is logic low.	–	40	180	ns
/T/R to !COL	tRCLD	RPTR is logic low.	–	40	180	ns
RX propagation delay	tRDVA	From RXIP/N(FXRP/N) to RXD[3:0].	–	40	180	ns
RXD[3:0], RXDV assert: Output delay	$tpLH_{100}$	From rising edge RX_CLK.	10	–	30	ns
RXD[3:0], RXDV de-assert: invalid	$tpHL_{100}$	From rising edge RX_CLK.	10	–	30	ns

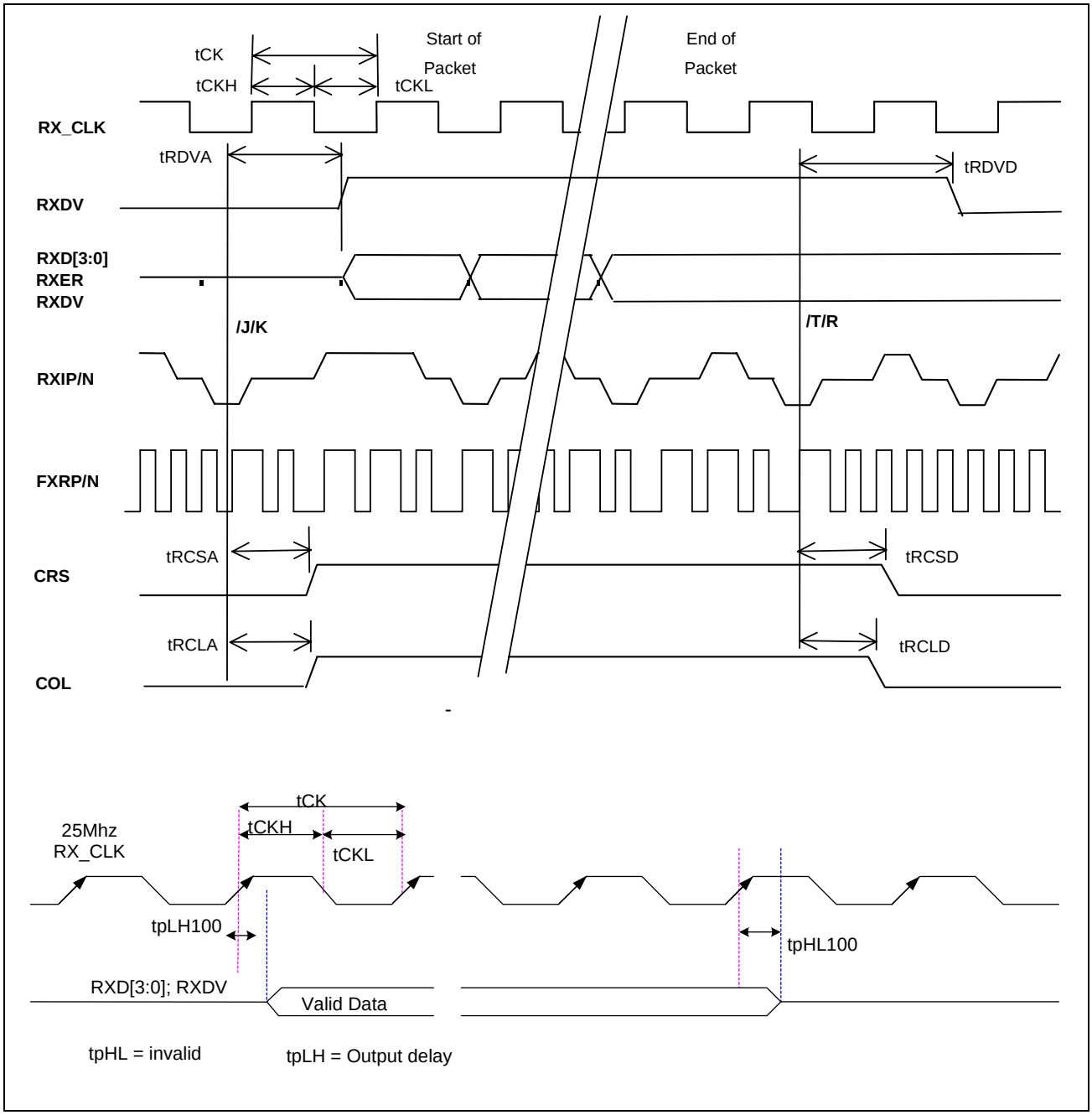


Figure 6: 100BASE-T MII Receive Timing

10BASE-T MII TRANSMIT SYSTEM TIMING

Table 40: 10BASE-T MII Transmit System Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
TX_CLK period	tCK	–	399.98	400.00	400.02	ns
TX_CLK high period	tCKH	–	180.00	200.00	220.00	ns
TX_CLK low period	tCKL	–	180.00	200.00	220.00	ns
TXEN to SOP	tTJ	–	240	–	360	ns
TXEN sampled to CRS	tTCSA	RPTR is logic low	–	–	130	ns
TXEN sampled to COL	tTCLA	RPTR is logic low	–	–	300	ns
!TXEN to EOP	tTJ	–	240	–	360	ns
!TXEN sampled to !CRS	tTCSD	RPTR is logic low	–	–	130	ns
!TXEN sampled to !COL	tTCLD	RPTR is logic low	–	–	300	ns
TX propagation delay	tTJ	From TXD[3:0] to TXOP/N	240	–	360	ns
TXD[3:0], TXEN, TXER setup	tTXS	From rising edge of TX_CLK	10	–	–	ns
TXD[3:0], TXEN, TXER hold	tTXH	From rising edge of TX_CLK	0	–	–	ns

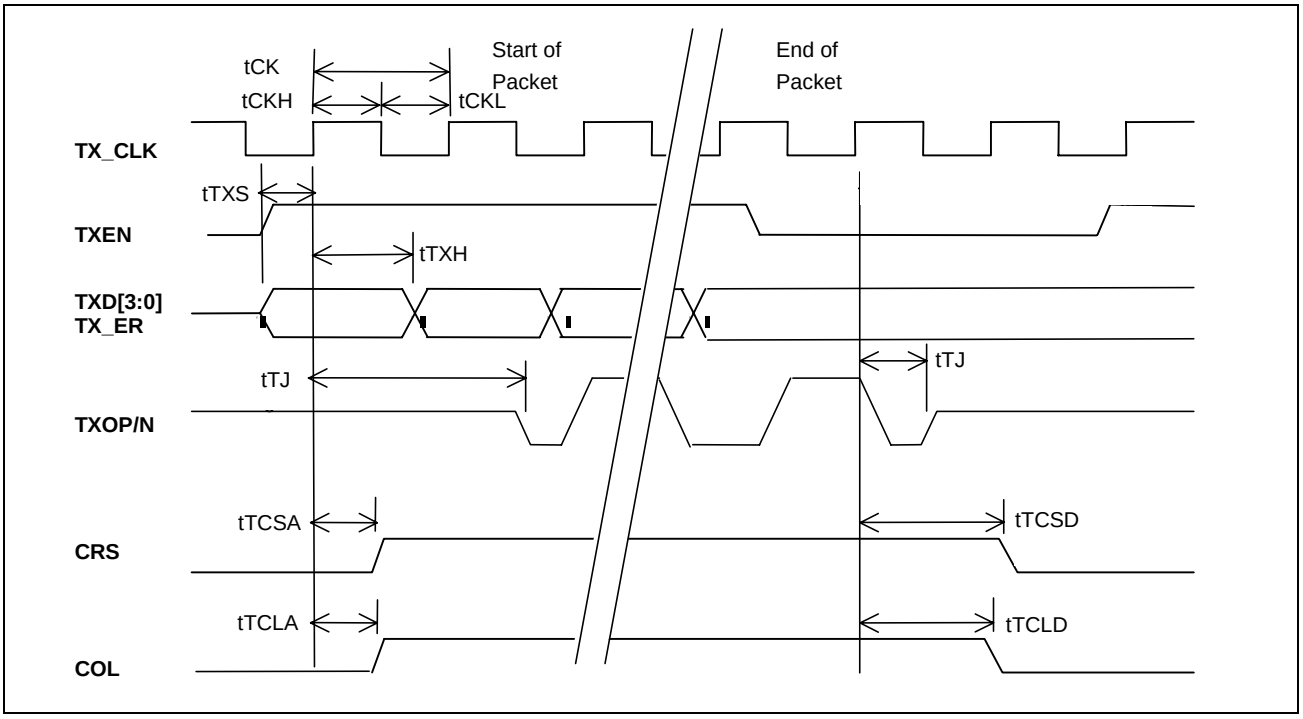


Figure 7: 10BASE-T Transmit Timing

10BASE-T MII RECEIVE SYSTEM TIMING

Table 41: 10BASE-T MII Receive System Timing

Parameter	*Symbol*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RX_CLK period	tCK	–	399.98	400.00	400.02	ns
RX_CLK high period	tCKH	–	180.00	200.00	220.00	ns
RX_CLK low period	tCKL	–	180.00	200.00	220.00	ns
SOP to CRS	tRCSA	–	80	–	150	ns
SOP to COL	tRCLA	RPTR is logic low.	80	–	150	ns
EOP to !RXDV	tRDVD	RPTR is logic low.	120	–	140	ns
EOP to !CRS	tRCSD	RPTR is logic low.	130	–	190	ns
EOP to !COL	tRCLD	RPTR is logic low.	125	–	185	ns
RX propagation delay	tRDVA	From RXIP/N to RXD[3:0].	180	–	250	ns
RXD[3:0], RXDV assert: Output delay	$tpLH_{10}$	From rising edge RX_CLK.	50	–	350	ns
RXD[3:0], RXDV de-assert: invalid	$tpHL_{10}$	From rising edge RX_CLK.	50	–	350	ns

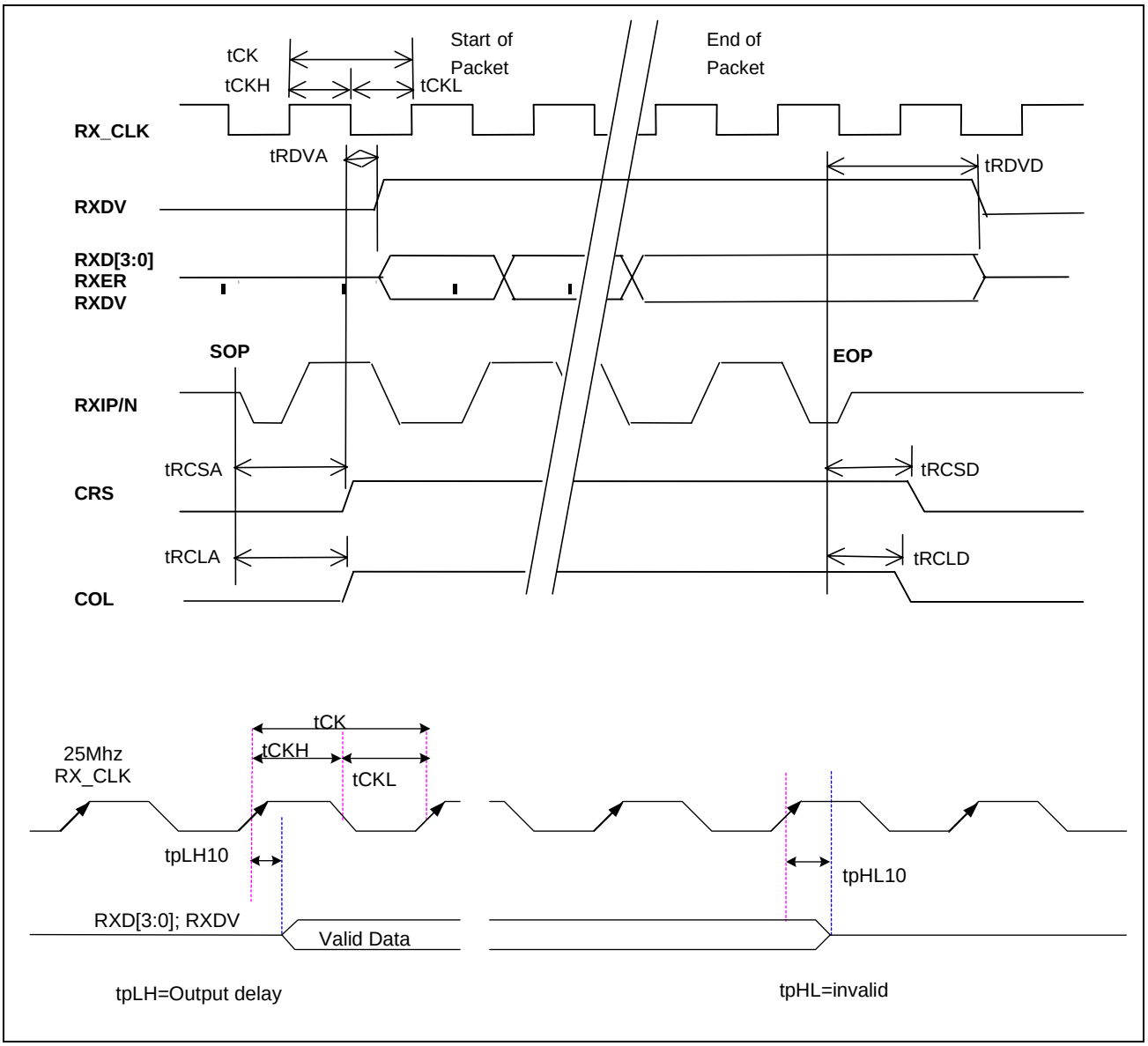


Figure 8: 10BASE-T Receive Timing

COPPER APPLICATION TERMINATION

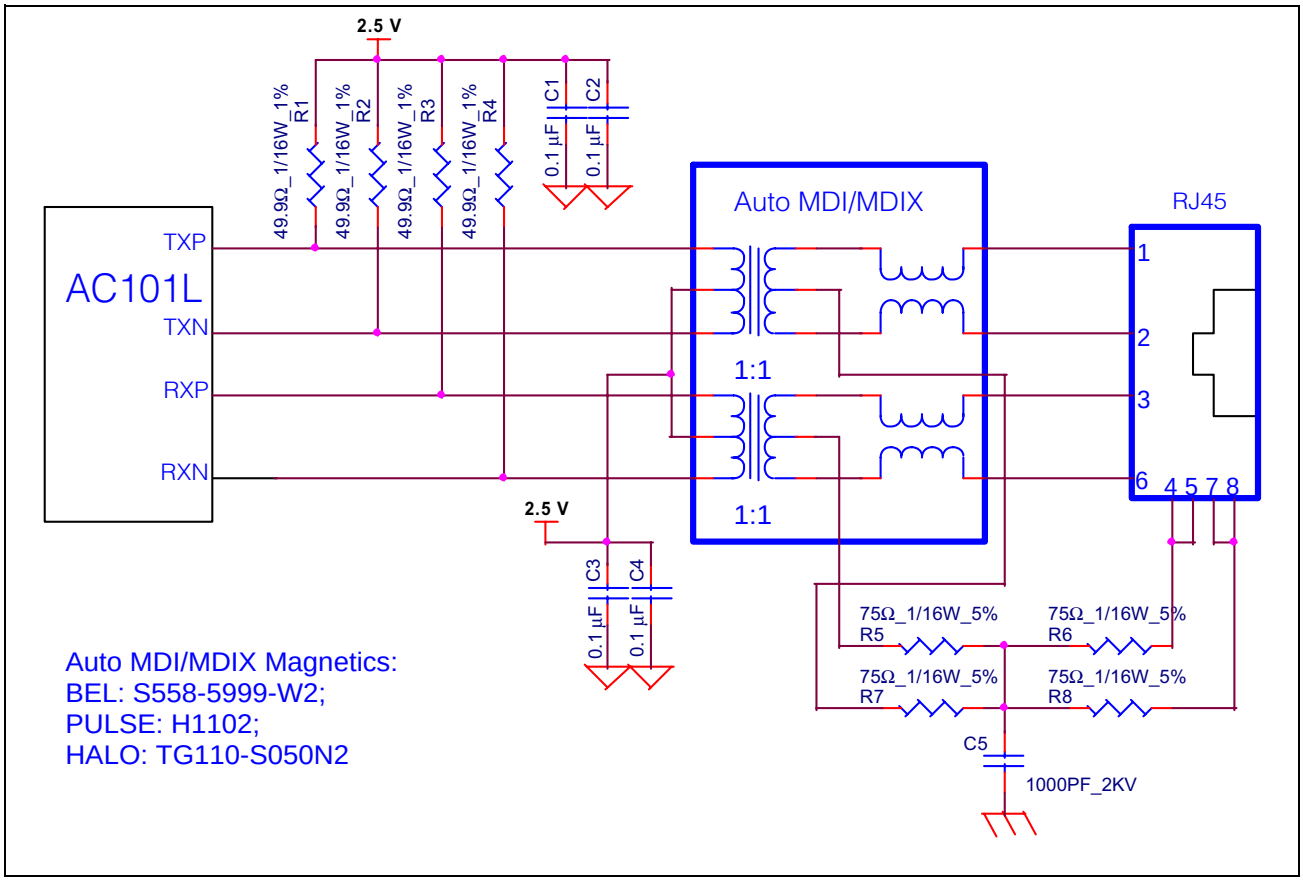


Figure 9: TX Application

Section 9: Electrical Characteristics

Note: The following electrical characteristics are design goals rather than characterized numbers.

ABSOLUTE MAXIMUM RATINGS

Table 42: Absolute Maximum Ratings

Parameter	*Symbol*	*Min*	*Max*	*Units*
Supply voltage	3V3	GND-0.3	3.465	V
Storage temperature	Ts	–40	+125	°C
Electrostatic discharge	VESD	–	1000	V

Table 43: Current Requirement at 2.5V Operation with LED Disabled

Operational Mode	*Current (mA)*	
	@V_{CC} = 2.5V	*@V_{CC} = 2.625V*
Traffic at 100 Mbps	90	100
Power-down	–	16
Standby	30	32

Table 44: Current Requirement at 3.3V Operation with LED Disabled

Operational Mode	*Current (mA)*	
	@V_{CC} = 3.3V	*@V_{CC} = 3.465V*
Traffic at 100 Mbps	92	102
Power-down	–	18
Standby	32	34

RECOMMENDED OPERATING CONDITIONS

Table 45: Recommended Operating Conditions

Parameter	*Symbol*	*Pins*	*Operating mode*	*Min*	*Typ*	*Max*	*Units*
Ambient operating temperature AC101L	T_A	–	–	–40	–	+85	°C
Bias voltage	V_{BIAS}	RBIAD	–	1.18	–	1.30	V
Common mode input voltage	V_{ICM}	RD±	100BASE-TX	1.8	–	VCC	V
Common mode input voltage	V_{ICM}	RD±	100BASE-FX	1.8	–	2.2	V
Differential input voltage	V_{IDIFF}	RD±	100BASE-FX (with 100 ohm load)	0.37	–	2.00	V
Differential output voltage	V_{ODIFF}	TD ±	100BASE-FX mode	1.5	–	1.7	V
Input current	I_I	Digital inputs with pull-up resistor	V_I = VCC	–	–	200	µA
Input voltage high	V_{IH}	SD	100BASE-FX	2.2	–	–	V
Input voltage high	V_{IH}	All digital input	V_{CC} = 2.5V ±5%	1.4	–	–	V
Input voltage low	V_{IL}	SD	100BASE-FX	–	–	1.7	V
Input voltage low	V_{IL}	All digital input	V_{CC} = 2.5V ±5%	–	–	1.1	V
Output voltage high	V_{OH}	All digital output	V_{CC} = 2.5V ±5% I_{OH} = –10 µA	2.3	–	–	V
Output voltage high	V_{OH}	All digital output	V_{CC} = 2.5V ±5% I_{OH} = –4 mA	2.0	–	–	–
Output voltage high	V_{OH}	TD±	Driving load magnetic module	–	–	VCC+1.5	V
Output voltage low	V_{OL}	All digital output	V_{CC} = 2.5 V ±5% I_{OL} = 10 µA	–	–	0.4	–
Output voltage low	V_{OL}	All digital output	V_{CC} = 2.5V ±5% I_{OL} = 4 mA	–	–	0.4	–
Output voltage low	V_{OL}	TD±	Driving load magnetic module	V_{CC}–1.5	–	–	–
Supply voltage AC101L	3V3	VCC33IN	–	3.135	3.3	3.465	V
Supply voltage AC101L	V_{CC}	VCC, VCCPLL, VCC25OUT	–	2.375	2.5	2.625	V

Section 10: Fiber Application Termination

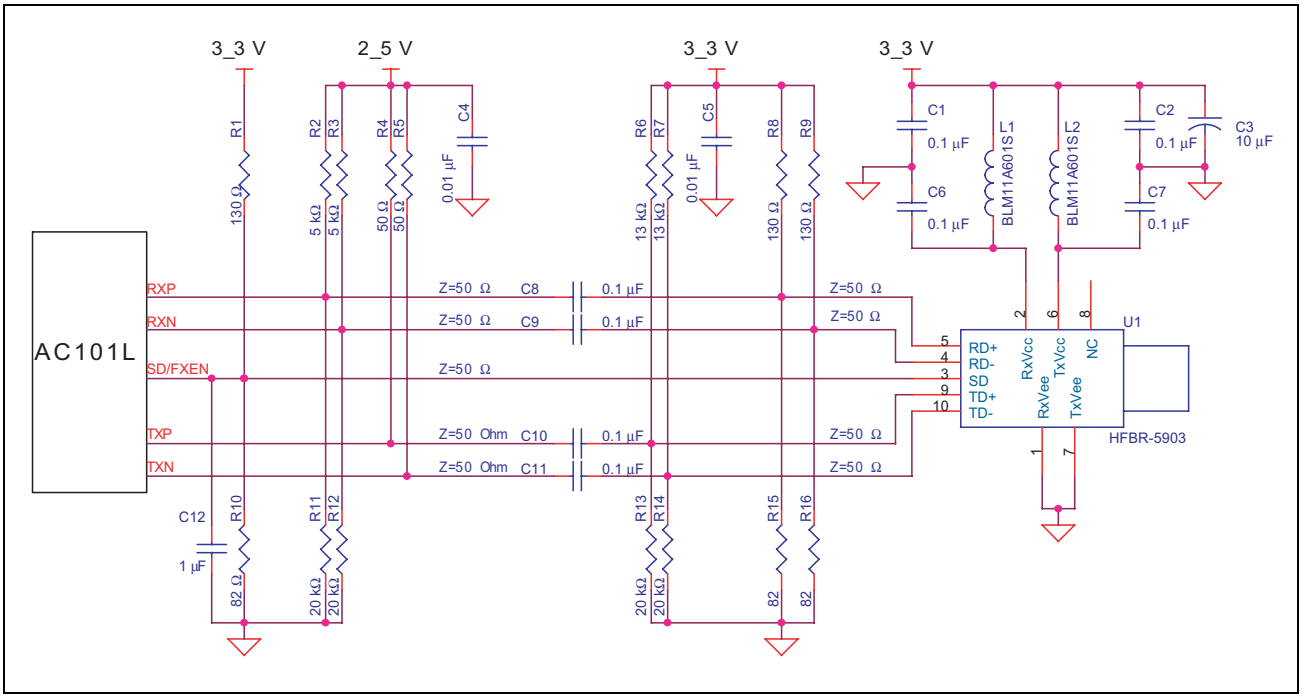


Figure 10: FX Application

Section 11: Power and Ground Filtering

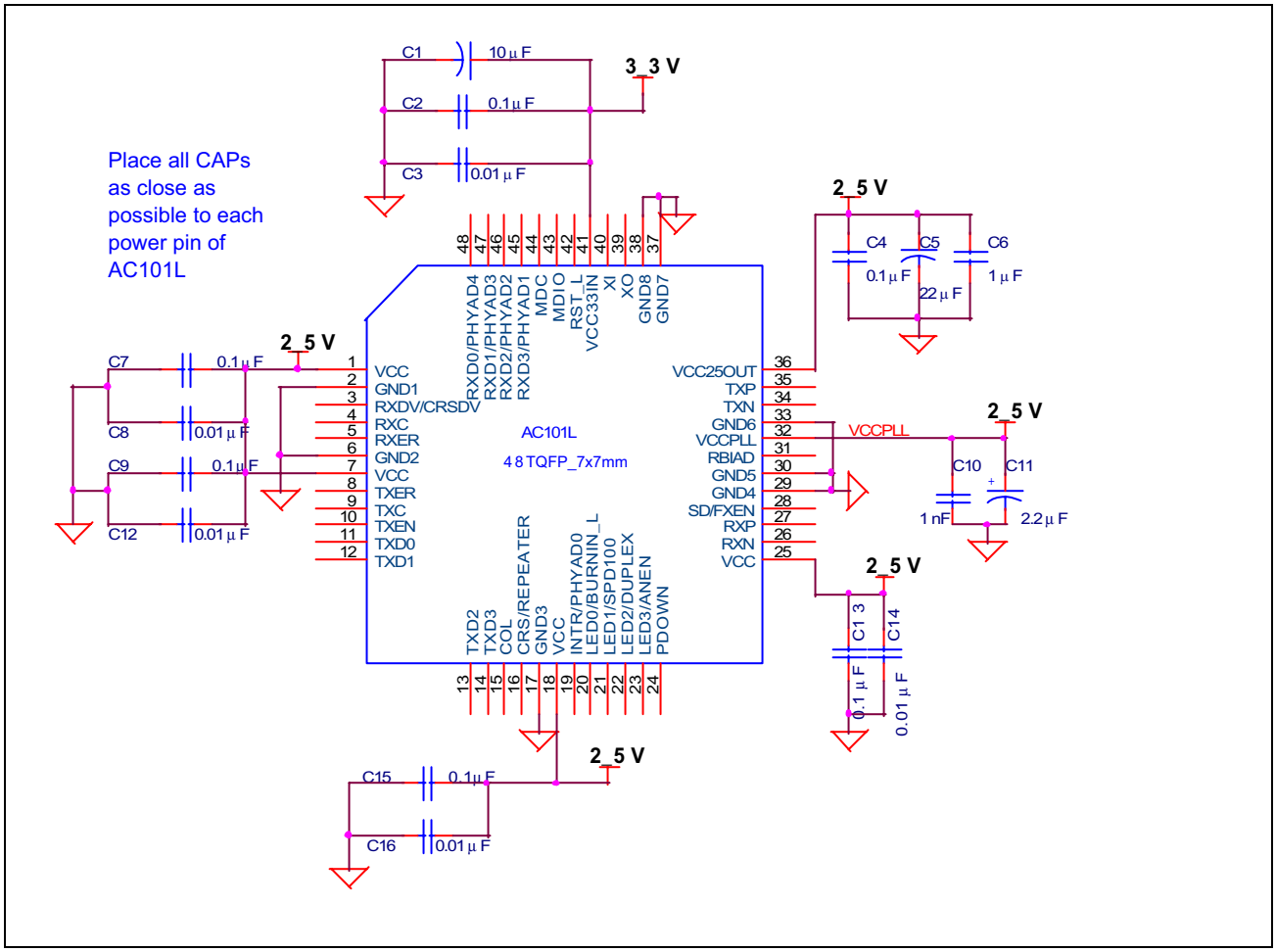
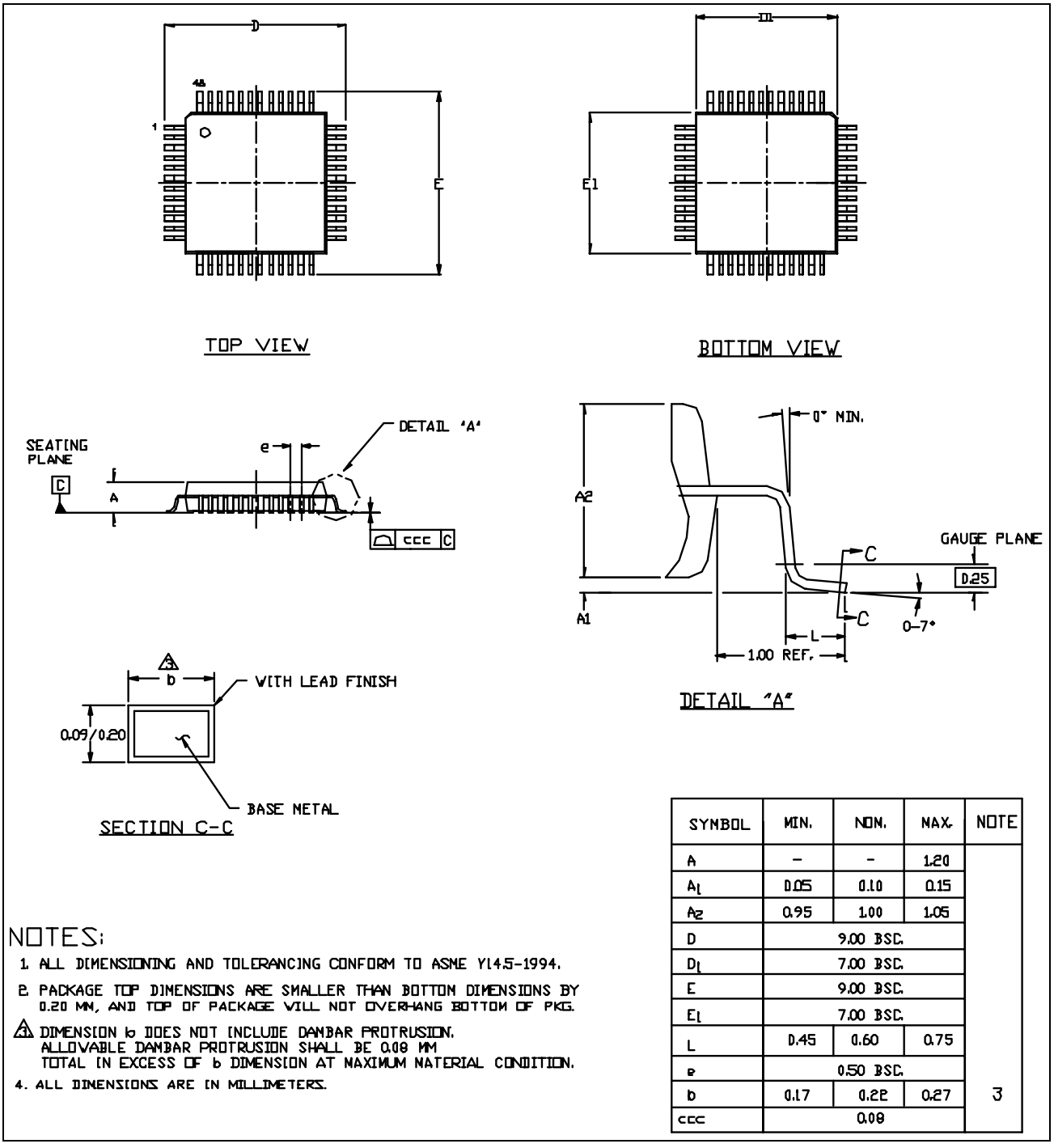


Figure 11: Power and Ground Filtering

Section 12: Mechanical Information



SYMBOL	MIN.	NOM.	MAX.	NOTE
A	–	–	1.20	
A_1	0.05	0.10	0.15	
A_2	0.95	1.00	1.05	
D		9.00 BSC.		
D_1		7.00 BSC.		
E		9.00 BSC.		
E_1		7.00 BSC.		
L	0.45	0.60	0.75	
e		0.50 BSC.		
b	0.17	0.22	0.27	3
ccc		0.08		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-1994.
2. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS BY 0.20 MM, AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PKG.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 12: Quad Flat Pack outline (7×7 mm)

Section 13: Thermal Parameters

Table 46: Thermal Parameters

Airflow (feet per minute)	***0***	***100***	***200***	***400***	***600***
$Theta_{JA}$ (°C/W)	53.9	51.2	50	48.6	47.5
$Theta_{JC}$ (°C/W) at maximum junction temperature of 125°C			24.7	–	–

Section 14: Ordering Information

Table 47: Ordering Information

Part number	*Package*	*Ambient temperature*
AC101LKQT	48TQFP	0°C to +70°C
AC101LIQT	48TQFP	–40°C to +85°C

Altima Communications, Inc.

A Wholly-Owned Subsidiary of Broadcom Corporation

16215 Alton Parkway
P.O. Box 57013
Irvine, California 92619-7013
Phone: 949-450-8700
Fax: 949-450-8710