

# 74VHC165FT

## 1. Functional Description

- 8-Bit Shift Register (P-IN, S-OUT)

## 2. General

The 74VHC165FT is an advanced high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.

When the SHIFT/LOAD input is held low, the parallel data is loaded synchronously into the register at positive going transition of the clock pulse.

The CK-INH input should be shifted high only when the CK input is held high.

An Input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

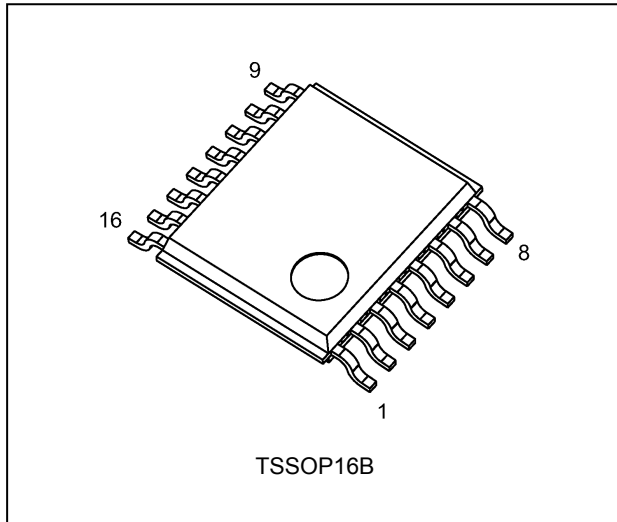
- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed:  $f_{MAX} = 150$  MHz (typ.) at  $V_{CC} = 5$  V
- (4) Low power dissipation:  $I_{CC} = 4.0$   $\mu$ A (max) at  $T_a = 25$  °C
- (5) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (6) Power-down protection is provided on all inputs.
- (7) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (8) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to  $5.5$  V
- (9) Pin and function compatible with 74 series (74AC/HC/AHC etc.) 165 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

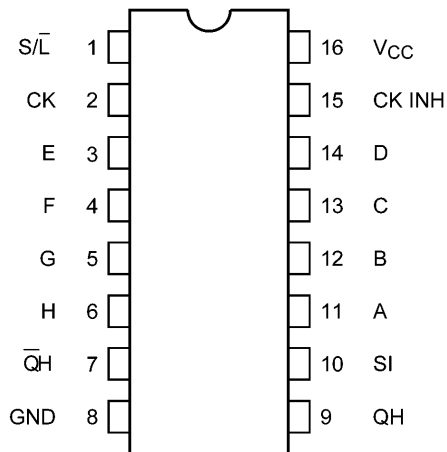
Start of commercial production

2013-05

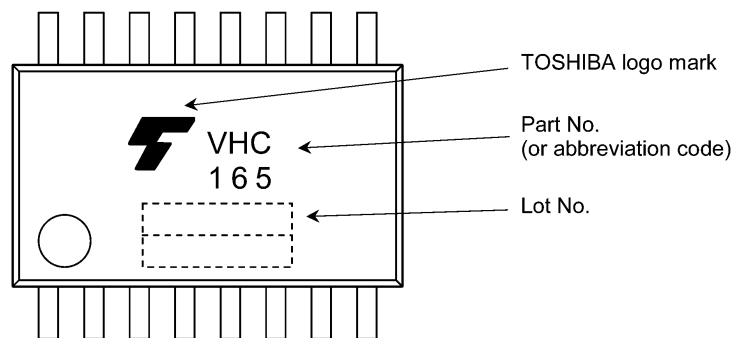
**4. Packaging**



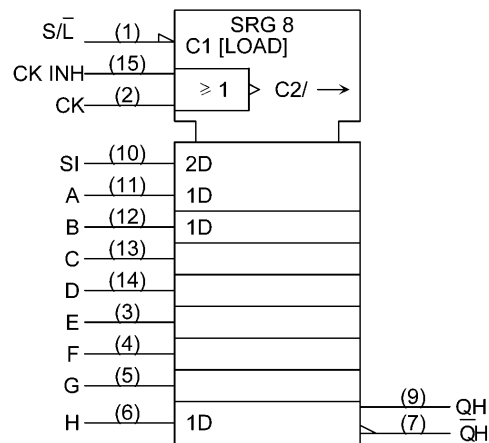
**5. Pin Assignment**



**6. Marking**



**7. IEC Logic Symbol**



**8. Truth Table**

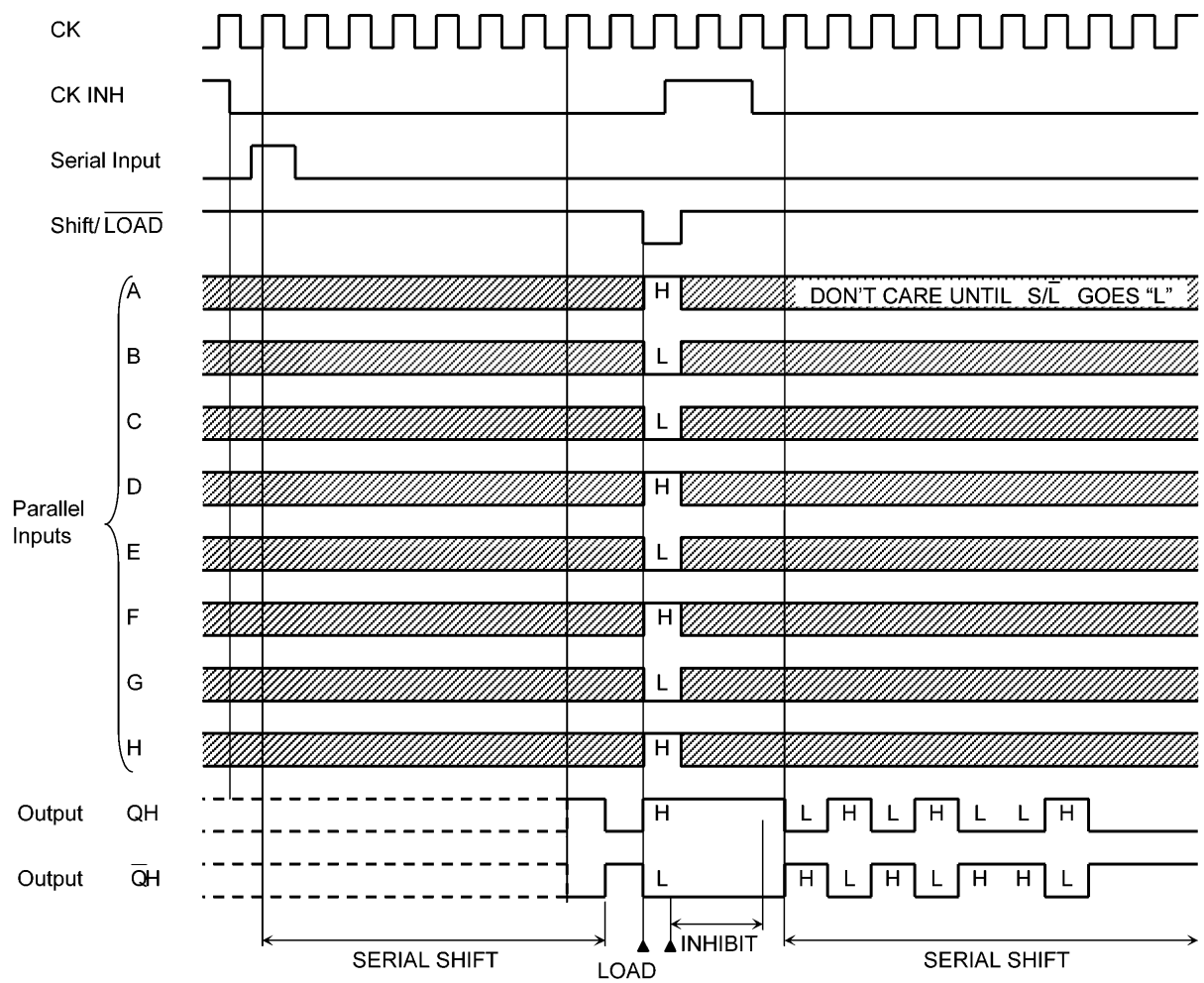
Inputs					Internal Outputs		Outputs	
SHIFT/LOAD	CK INH	CK	SERIAL IN	PARALLEL A.....H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a.....h	a	b	h	$\overline{h}$
H	L	$\uparrow$	H	X	H	QA <sub>n</sub>	QG <sub>n</sub>	$\overline{QG_n}$
H	L	$\uparrow$	L	X	L	QA <sub>n</sub>	QG <sub>n</sub>	$\overline{QG_n}$
H	$\uparrow$	L	H	X	H	QA <sub>n</sub>	QG <sub>n</sub>	$\overline{QG_n}$
H	$\uparrow$	L	L	X	L	QA <sub>n</sub>	QG <sub>n</sub>	$\overline{QG_n}$
H	X	H	X	X	No Change			
H	H	X	X	X	No Change			

X: Don't care

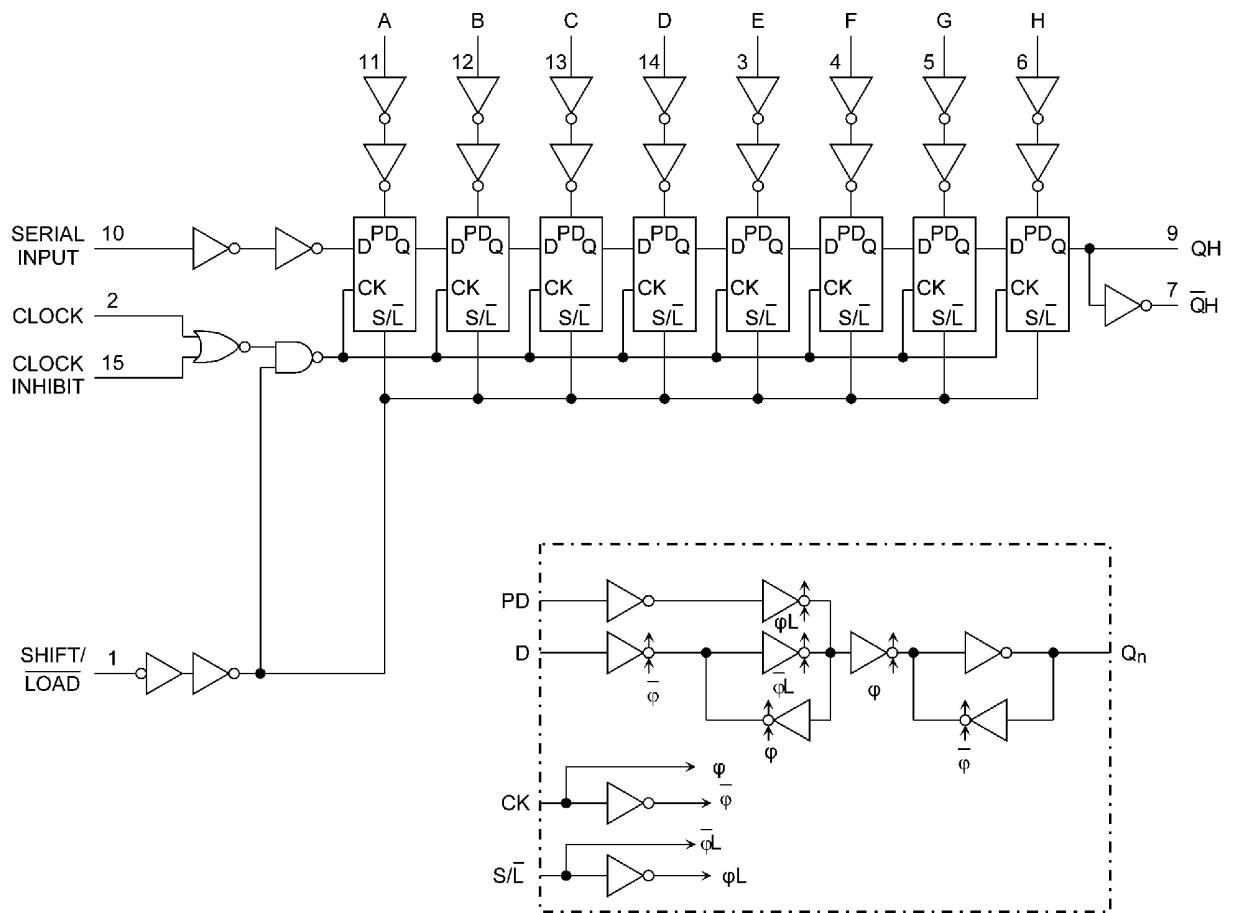
a.....h: The level of steady state input voltage at inputs A through H respectively.

QA<sub>n</sub> to QG<sub>n</sub>: The level of QA to QG, respectively, before the most recent positive transition of the CK.

**9. Timing Diagrams**



10. System Diagram



**11. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 50$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to  $85$  °C. From  $T_a = 85$  to  $125$  °C a derating factor of  $-3.25$  mW/°C shall be applied until 50 mW.

**12. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 125	°C
Input rise and fall times	$dt/dv$	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**13. Electrical Characteristics**

**13.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
4.5	3.94	—		—				
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
				4.5	—	—	0.36	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	

**13.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.5	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.5	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
				4.5	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
				4.5	—	0.44	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	$\mu\text{A}$	

**13.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V	
				3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V	
				3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V	
				3.0	2.9	—		
				4.5	4.4	—		
				$I_{OH} = -4$ mA	3.0	2.40		—
			$I_{OH} = -8$ mA	4.5	3.70	—		
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V	
				3.0	—	0.1		
				4.5	—	0.1		
				$I_{OL} = 4$ mA	3.0	—		0.55
				$I_{OL} = 8$ mA	4.5	—		0.55
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND		0 to 5.5	—	$\pm 2.0$	$\mu A$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	80.0	$\mu A$	

**13.4. Timing Requirements (Unless otherwise specified,  $T_a = 25$  °C, Input:  $t_r = t_f = 3$  ns)**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK, CK INH)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum pulse width (S/L)	$t_{w(L)}$	—	$3.3 \pm 0.3$	7.5	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time (PI-S/L)	$t_s$	—	$3.3 \pm 0.3$	7.5	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time (SI-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum setup time (S/L-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum hold time (PI-S/L)	$t_h$	—	$3.3 \pm 0.3$	0.5	ns
			$5.0 \pm 0.5$	1.0	
Minimum hold time (SI-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum hold time (S/L-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum removal time (CK INH-CK), (CK-CK INH)	$t_{rem}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	3.5	



**13.5. Timing Requirements**  
 (Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK, CK INH)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum pulse width (S/L)	$t_{w(L)}$	—	$3.3 \pm 0.3$	9.0	ns
			$5.0 \pm 0.5$	6.0	
Minimum setup time (PI-S/L)	$t_s$	—	$3.3 \pm 0.3$	8.5	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time (SI-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum setup time (S/L-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum hold time (PI-S/L)	$t_h$	—	$3.3 \pm 0.3$	0.5	ns
			$5.0 \pm 0.5$	1.0	
Minimum hold time (SI-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum hold time (S/L-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum removal time (CK INH-CK), (CK-CK INH)	$t_{rem}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	3.5	

**13.6. Timing Requirements**  
 (Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK, CK INH)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	7.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum pulse width (S/L)	$t_{w(L)}$	—	$3.3 \pm 0.3$	9.0	ns
			$5.0 \pm 0.5$	6.0	
Minimum setup time (PI-S/L)	$t_s$	—	$3.3 \pm 0.3$	8.5	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time (SI-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum setup time (S/L-CK, CK INH)	$t_s$	—	$3.3 \pm 0.3$	6.0	ns
			$5.0 \pm 0.5$	4.0	
Minimum hold time (PI-S/L)	$t_h$	—	$3.3 \pm 0.3$	0.5	ns
			$5.0 \pm 0.5$	1.0	
Minimum hold time (SI-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum hold time (S/L-CK, CK INH)	$t_h$	—	$3.3 \pm 0.3$	0.0	ns
			$5.0 \pm 0.5$	0.5	
Minimum removal time (CK INH-CK), (CK-CK INH)	$t_{rem}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	3.5	

**13.7. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK, CK INH-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	9.9	15.4	ns
					50	—	12.4	18.9	
				$5.0 \pm 0.5$	15	—	6.6	9.9	
					50	—	8.1	11.9	
Propagation delay time (S/L-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	9.9	15.8	ns
					50	—	12.4	19.3	
				$5.0 \pm 0.5$	15	—	6.7	9.9	
					50	—	8.2	11.9	
Propagation delay time (H-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	9.2	14.1	ns
					50	—	11.7	17.6	
				$5.0 \pm 0.5$	15	—	5.9	9.0	
					50	—	7.4	11.0	
Maximum clock frequency	$f_{MAX}$		—	$3.3 \pm 0.3$	15	65	85	—	MHz
					50	60	105	—	
				$5.0 \pm 0.5$	15	110	150	—	
					50	95	130	—	
Input capacitance	$C_{IN}$		—			—	4	10	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—			—	50	—	pF

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

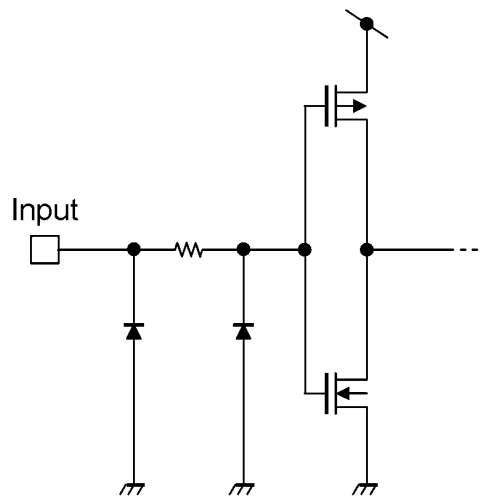
**13.8. AC Characteristics (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (CK, CK INH-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	18.0	ns
				50	1.0	21.5	
			$5.0 \pm 0.5$	15	1.0	11.5	
				50	1.0	13.5	
Propagation delay time (S/L-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	18.5	ns
				50	1.0	22.0	
			$5.0 \pm 0.5$	15	1.0	11.5	
				50	1.0	13.5	
Propagation delay time (H-QH, $\overline{QH}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	16.5	ns
				50	1.0	20.0	
			$5.0 \pm 0.5$	15	1.0	10.5	
				50	1.0	12.5	
Maximum clock frequency	$f_{MAX}$	—	$3.3 \pm 0.3$	15	55	—	MHz
				50	50	—	
			$5.0 \pm 0.5$	15	90	—	
				50	85	—	
Input capacitance	$C_{IN}$	—			—	10	pF

**13.9. AC Characteristics**  
 (Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

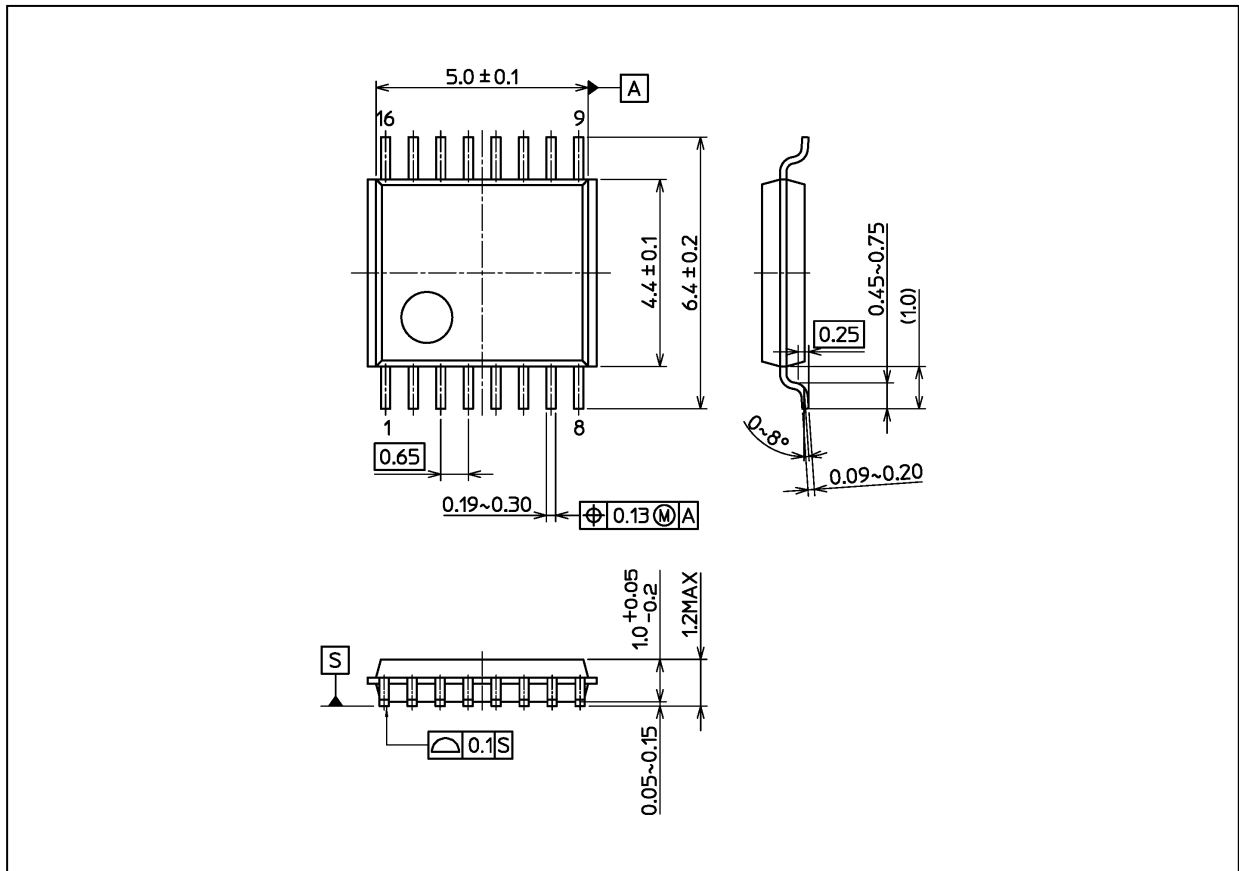
Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time (CK, CK INH-QH, $\bar{Q}H$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	20.5	ns
				50	1.0	24.0	
			$5.0 \pm 0.5$	15	1.0	13.0	
				50	1.0	15.0	
Propagation delay time (S/L-QH, $\bar{Q}H$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	21.0	ns
				50	1.0	24.5	
			$5.0 \pm 0.5$	15	1.0	13.0	
				50	1.0	15.0	
Propagation delay time (H-QH, QH)	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	18.5	ns
				50	1.0	22.0	
			$5.0 \pm 0.5$	15	1.0	12.0	
				50	1.0	14.0	
Maximum clock frequency	$f_{MAX}$	—	$3.3 \pm 0.3$	15	50	—	MHz
				50	45	—	
			$5.0 \pm 0.5$	15	85	—	
				50	75	—	
Input capacitance	$C_{IN}$	—			—	10	pF

**14. Internal Equivalent Circuit**



Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

Package Name(s)
Nickname: TSSOP16B

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