74LVT573

3.3 V octal D-type transparent latch; 3-state

Rev. 9 — 30 July 2021 Product data sheet

1. General description

The 74LVT573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- Wide supply voltage range from 2.7 to 3.6 V
- Inputs and outputs arranged for easy interfacing to microprocessors
- 3-state outputs for bus interfacing
- Common output enable control
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT573D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT573PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVT573BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

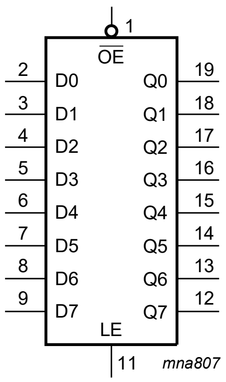


Fig. 1. Logic symbol

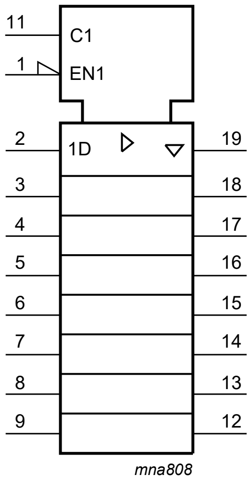


Fig. 2. IEC logic symbol

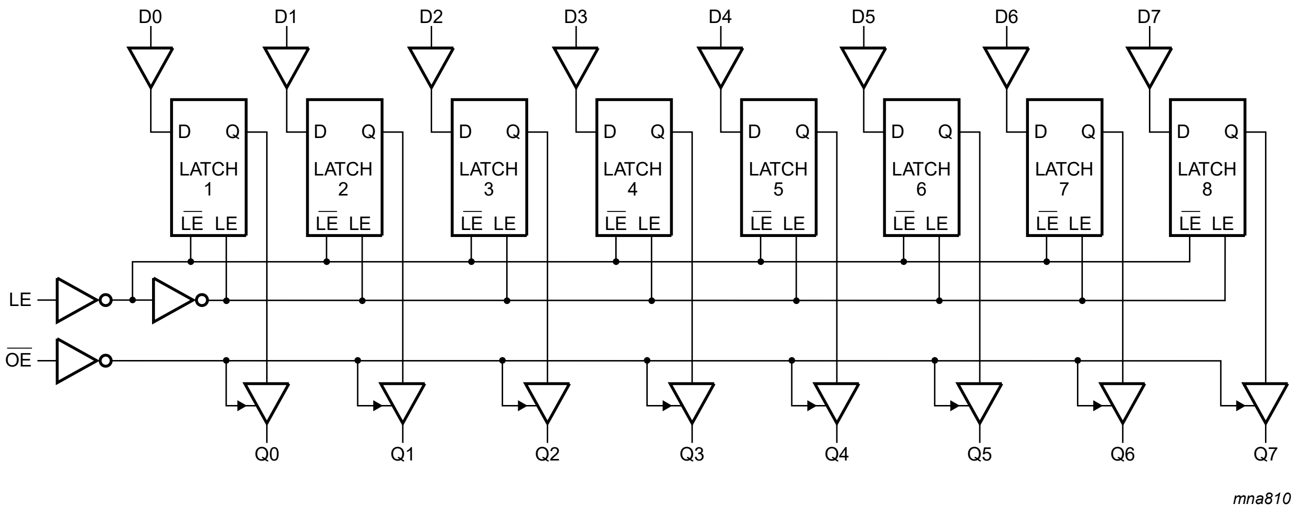


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

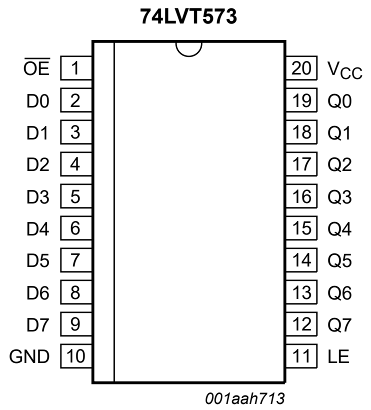
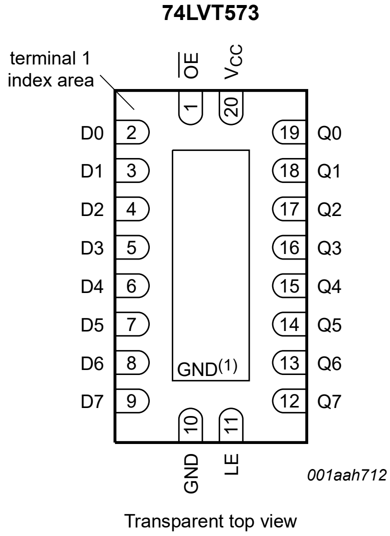


Fig. 4. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
LE	11	latch enable (active HIGH)
Q0, Q1, Q2, Q3, Q4 ,Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition;
↓ = HIGH-to-LOW latch enable transition;
Z = high-impedance OFF-state; NC = no change; X = don't care.

Operating mode	Control $\overline{OE}$	Control LE	Input Dn	Internal register	Output Qn
Load and read register enable	L	H	L	L	L
			H	H	H
Latch and read register	L	↓	l	L	L
			h	H	H
Hold	L	L	X	NC	NC
Disable outputs	H	L	X	NC	Z
		H	Dn	Dn	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage		[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-	-50	mA
I_{OK}	output clamping current	$V_O < 0$ V		-	-50	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	-64	mA
T_{stg}	storage temperature			-65	+150	°C
T_j	junction temperature		[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C		-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current		-	-	32	mA
		current duty cycle ≤ 50 %; f_i ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.9	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = -100 μA	V_{CC} - 0.2	V_{CC} - 0.1	-	V
		V_{CC} = 2.7 V; I_{OH} = -8 mA	2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = -32 mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 μA	-	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V I_{OL} = 16 mA	-	0.25	0.4	V
		V_{CC} = 3.0 V I_{OL} = 32 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V I_{OL} = 64 mA	-	0.4	0.55	V
$V_{OL(pu)}$	power-up LOW-level output voltage	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC} [2]	-	0.13	0.55	V
I_I	input leakage current	all input pins;				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	1	10	μA
		control pins;				
		V_{CC} = 3.6 V; V_{CC} or GND	-	±0.1	±1	μA
		data pins				
		V_{CC} = 3.6 V; V_I = V_{CC} [3]	-	0.1	1	μA
		V_{CC} = 3.6 V; V_I = 0 V	-5	-1	-	μA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	1	±100	μA
I_{BHL}	bus hold LOW current	Dn input; V_{CC} = 3 V; V_I = 0.8 V [4]	75	150	-	μA
I_{BHH}	bus hold HIGH current	Dn input; V_{CC} = 3 V; V_I = 2.0 V	-	-150	-75	μA
I_{BHHO}	bus hold HIGH overdrive current	Dn input; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [4]	-	-	500	μA
I_{BHLO}	bus hold LOW overdrive current	Dn input; V_{CC} = 3.6 V; V_I = 0 V to 3.6 V	-500	-	-	μA

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C			Unit
				Min	Typ [1]	Max	
I_{LO}	output leakage current	Qn output HIGH when V_O = 5.5 V and V_{CC} = 3.0 V		-	60	125	μA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = don't care	[5]	-	1	±100	μA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}					
		output HIGH: V_O = 3.0 V		-	1	5	μA
		output LOW: V_O = 0.5 V		-5	-1	-	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.13	0.19	mA
		outputs LOW		-	3	12	mA
		outputs disabled	[6]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V and other inputs at V_{CC} or GND	[7]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or 3.0 V		-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	8	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
[3] Unused pins at V_{CC} or GND.
[4] This is the bus hold overdrive current required to force the input to the opposite logic state.
[5] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[6] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[7] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

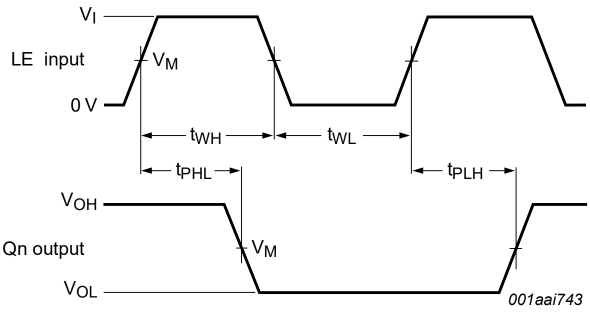
Table 7. Dynamic characteristics

Voltages are referenced to ground (GND = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions		T_{amb} = -40 °C to +85 °C			Unit
				Min	Typ [1]	Max	
t_{PLH}	LOW to HIGH propagation delay	LE to Qn; see Fig. 6					
		V_{CC} = 3.0 V to 3.6 V		1.6	3.5	5.6	ns
		V_{CC} = 2.7 V		-	-	6.3	ns
		Dn to Qn; see Fig. 7					
		V_{CC} = 3.0 V to 3.6 V		1.0	2.5	4.2	ns
		V_{CC} = 2.7 V		-	-	4.7	ns
t_{PHL}	HIGH to LOW propagation delay	LE to Qn; see Fig. 6					
		V_{CC} = 3.0 V to 3.6 V		2.5	4.3	6.5	ns
		V_{CC} = 2.7 V		-	-	7.2	ns
		Dn to Qn; see Fig. 7					
		V_{CC} = 3.0 V to 3.6 V		1.0	2.7	4.3	ns
		V_{CC} = 2.7 V		-	-	5.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{OE}$ to Qn; see Fig. 8					
		V_{CC} = 3.0 V to 3.6 V		1.0	2.8	5.1	ns
		V_{CC} = 2.7 V		-	-	6.2	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{OE}$ to Qn; see Fig. 9					
		V_{CC} = 3.0 V to 3.6 V		1.3	3.3	5.5	ns
		V_{CC} = 2.7 V		-	-	6.6	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{OE}$ to Qn; see Fig. 8					
		V_{CC} = 3.0 V to 3.6 V		2.0	3.7	5.7	ns
		V_{CC} = 2.7 V		-	-	6.7	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{OE}$ to Qn; see Fig. 9					
		V_{CC} = 3.0 V to 3.6 V		1.5	3.0	4.6	ns
		V_{CC} = 2.7 V		-	-	5.1	ns
t_{su}	set-up time	Dn to LE; see Fig. 10	[2]				
		V_{CC} = 3.0 V to 3.6 V		0.7	-	-	ns
		V_{CC} = 2.7 V		0.6	-	-	ns
t_h	hold time	Dn to LE; see Fig. 10	[3]				
		V_{CC} = 3.0 V to 3.6 V		1.6	-	-	ns
		V_{CC} = 2.7 V		1.8	-	-	ns
t_W	pulse width	LE input HIGH; see Fig. 6	[4]				
		V_{CC} = 3.0 V to 3.6 V		3.3	-	-	ns
		V_{CC} = 2.7 V		3.3	-	-	ns

[1] Typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] t_{su} is the same as $t_{su(L)}$ and $t_{su(H)}$.
[3] t_h is the same as $t_{h(L)}$ and $t_{h(H)}$.
[4] t_W is the same as t_{WL} and t_{WH}.

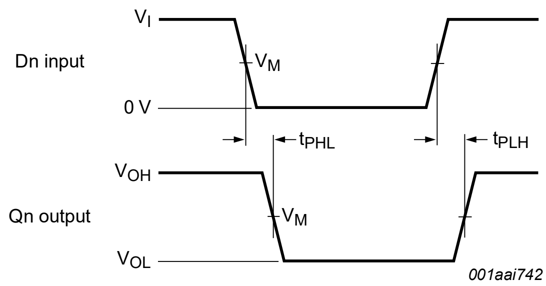
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

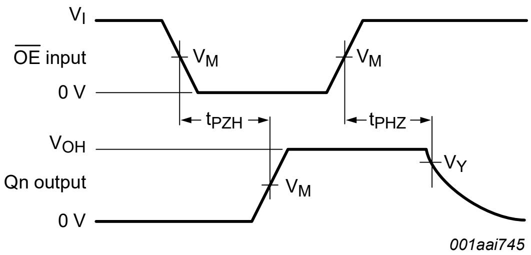
Fig. 6. Propagation delays latch enable input (LE) to output (Qn), and latch enable (LE) pulse width



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

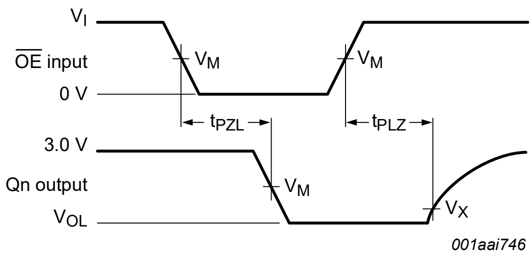
Fig. 7. Propagation delay data input (Dn) to output (Qn)



Measurement points are given in Table 8.

V_{OH} is a typical voltage output level that occurs with the output load.

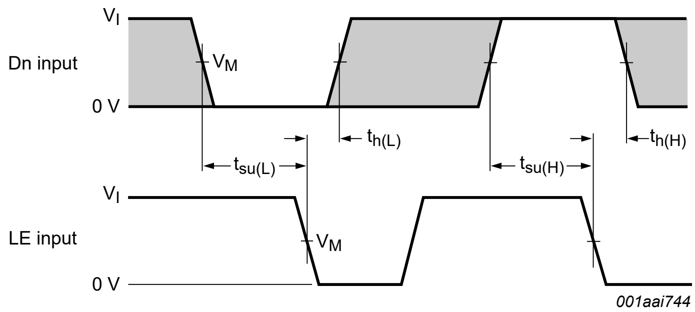
Fig. 8. Output enable time to HIGH-state and output disable time from HIGH-state



Measurement points are given in Table 8.

V_{OL} is a typical voltage output level that occurs with the output load.

Fig. 9. Output enable time to LOW-state and output disable time from LOW-state



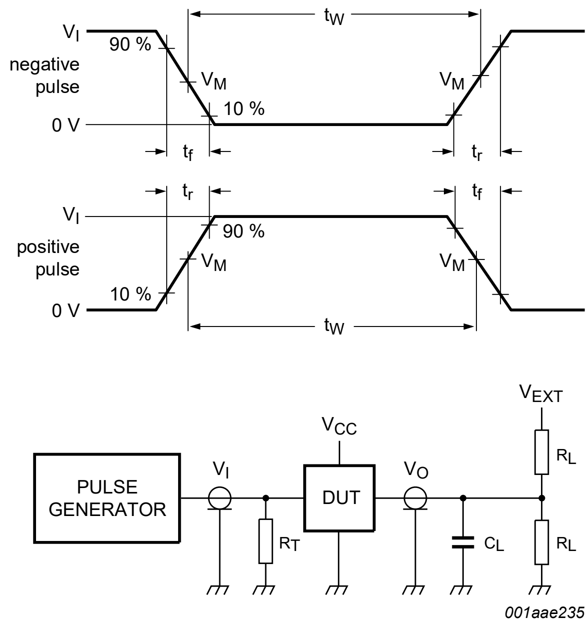
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 10. Data setup and hold times for data (Dn) and latch enable (LE) inputs

Table 8. Measurement points

Input	Output		
V_M	**V_M**	**V_X**	**V_Y**
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

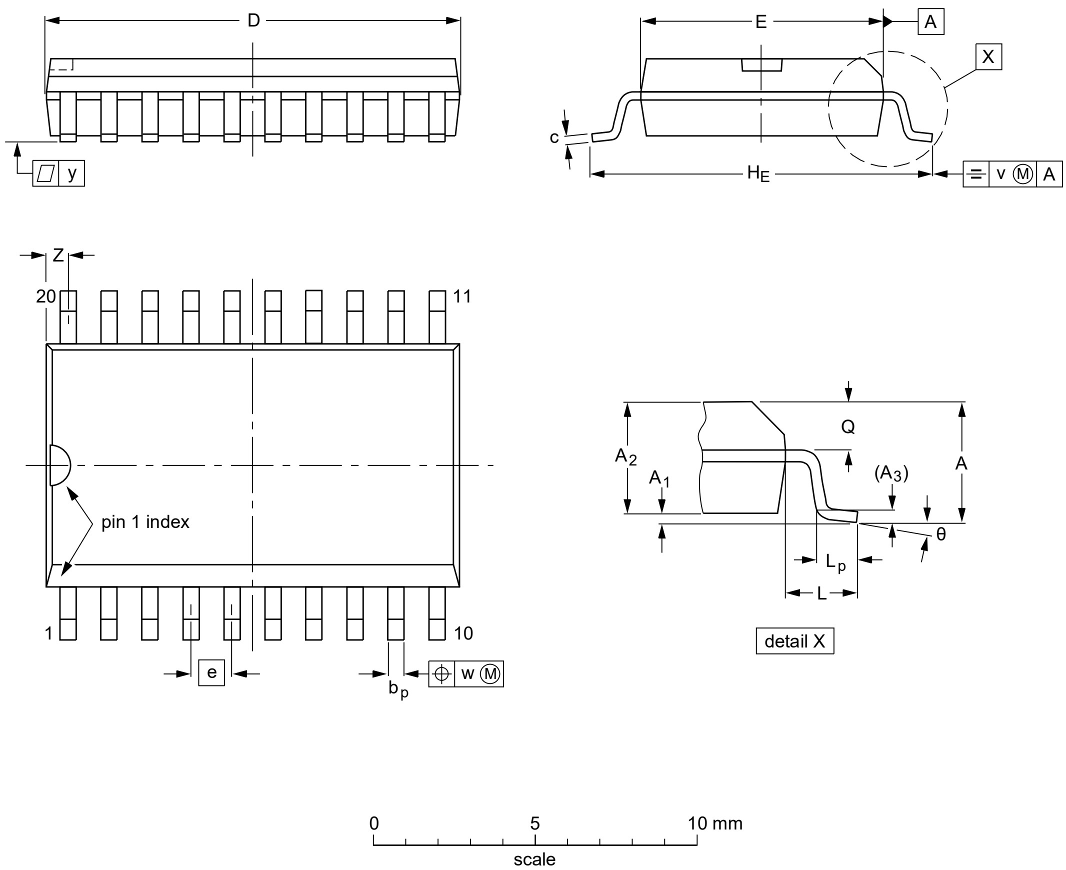
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(1)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

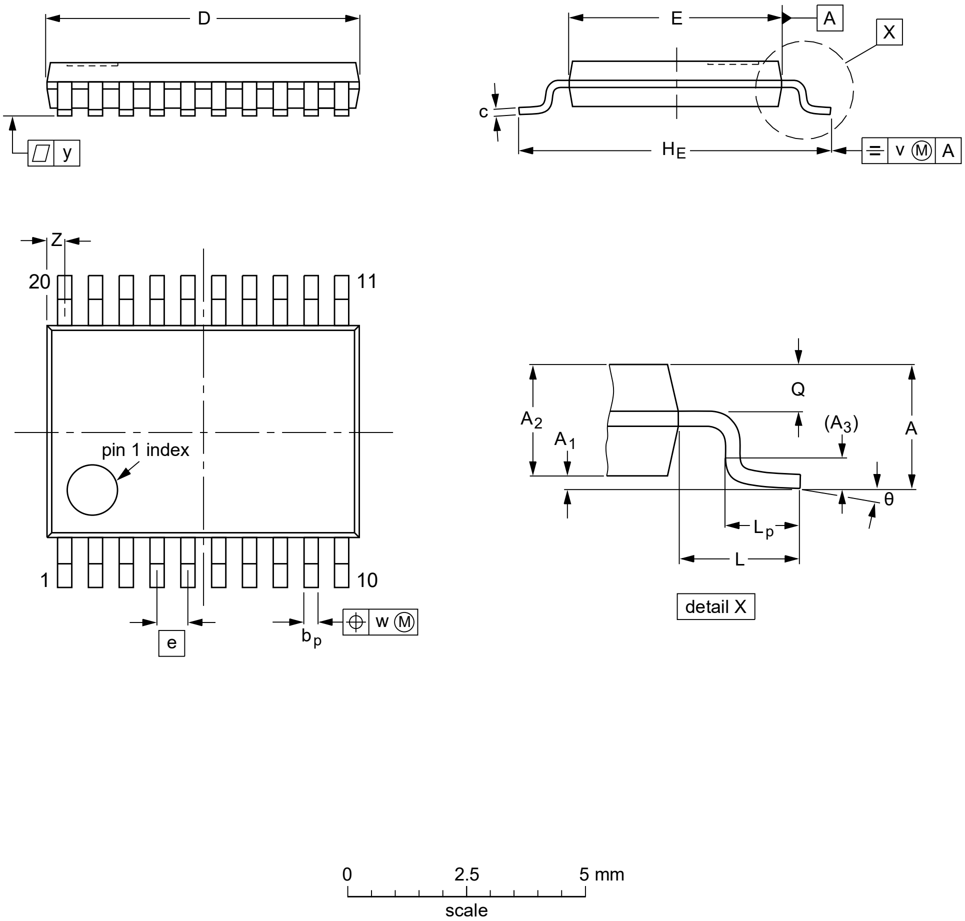
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 12. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

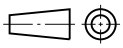
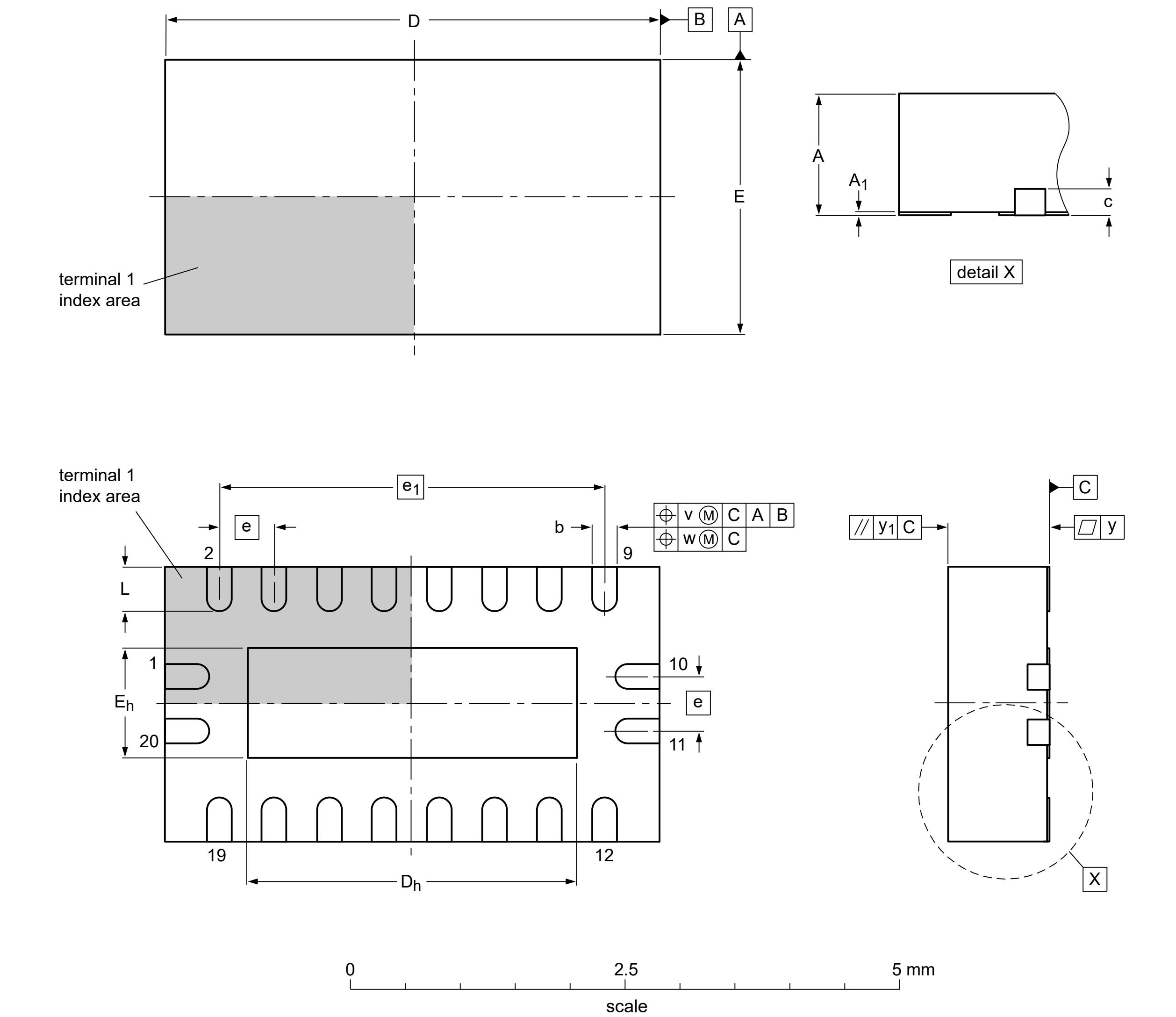
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 13. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm **SOT764-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
	max	1.00	0.05	0.30		4.6	3.15	2.6	1.15			0.5				
mm	nom	0.90	0.02	0.25	0.2	4.5	3.00	2.5	1.00	0.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.4	2.85	2.4	0.85			0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot764-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT764-1	- - -	MO-241	- - -			~~03-01-27~~ 14-12-12

Fig. 14. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT573 v.9	20210730	Product data sheet	-	74LVT573 v.8
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74LVT573DB (SOT339-1/SSOP20) removed. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation removed. • Fig. 14: Package outline drawing SOT764-1 (DHVQFN20) updated.			
74LVT573 v.8	20111122	Product data sheet	-	74LVT573 v.7
Modifications:	• Legal pages updated.			
74LVT573 v.7	20110912	Product data sheet	-	74LVT573 v.6
74LVT573 v.6	20110727	Product data sheet	-	74LVT573 v.5
74LVT573 v.5	20110629	Product data sheet	-	74LVT573 v.4
74LVT573 v.4	20080915	Product data sheet	-	74LVT573 v.3
74LVT573 v.3	20011217	Product data sheet	-	74LVT573 v.2
74LVT573 v.2	19980219	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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