

# 74LV393

## Dual 4-bit binary ripple counter

Rev. 6 — 19 March 2021

Product data sheet

### 1. General description

The 74LV393 is a dual 4-stage binary ripple counter. Each counter features a clock input ( $n\overline{CP}$ ), an overriding asynchronous master reset input ( $nMR$ ) and 4 buffered parallel outputs ( $nQ0$  to  $nQ3$ ). The counter advances on the HIGH-to-LOW transition of  $n\overline{CP}$ . A HIGH on  $nMR$  clears the counter stages and forces the outputs LOW, independent of the state of  $n\overline{CP}$ . Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess  $V_{CC}$ .

### 2. Features and benefits

- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce) 0.8 V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot) 2 V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV393D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV393PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

### 4. Functional diagram

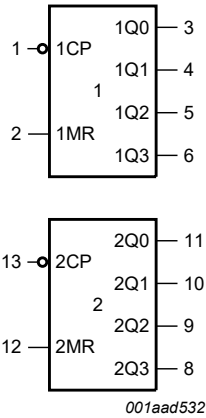


Fig. 1. Logic symbol

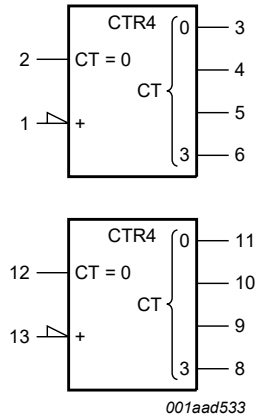


Fig. 2. IEC logic symbol

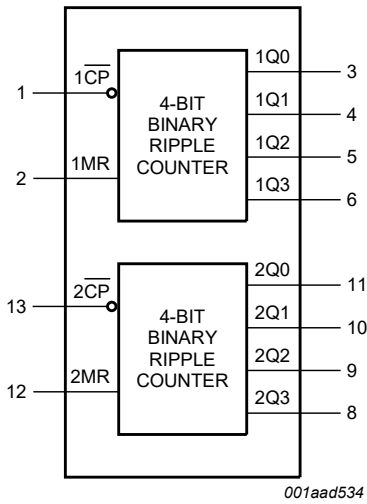


Fig. 3. Functional diagram

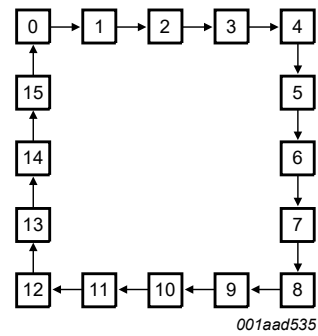


Fig. 4. State diagram

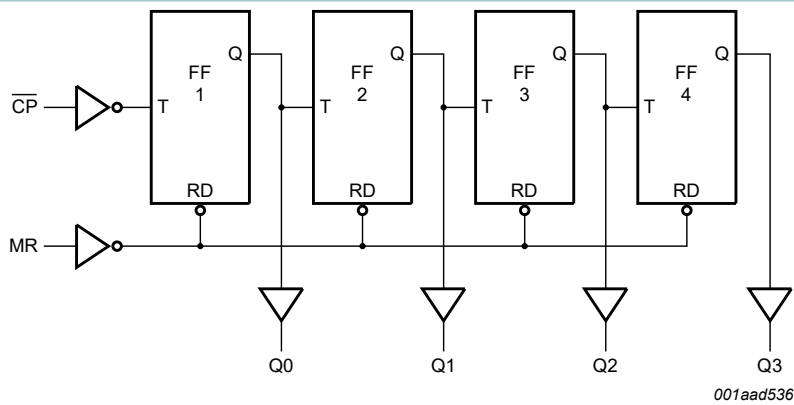


Fig. 5. Logic diagram (one counter)

## 5. Pinning information

### 5.1. Pinning

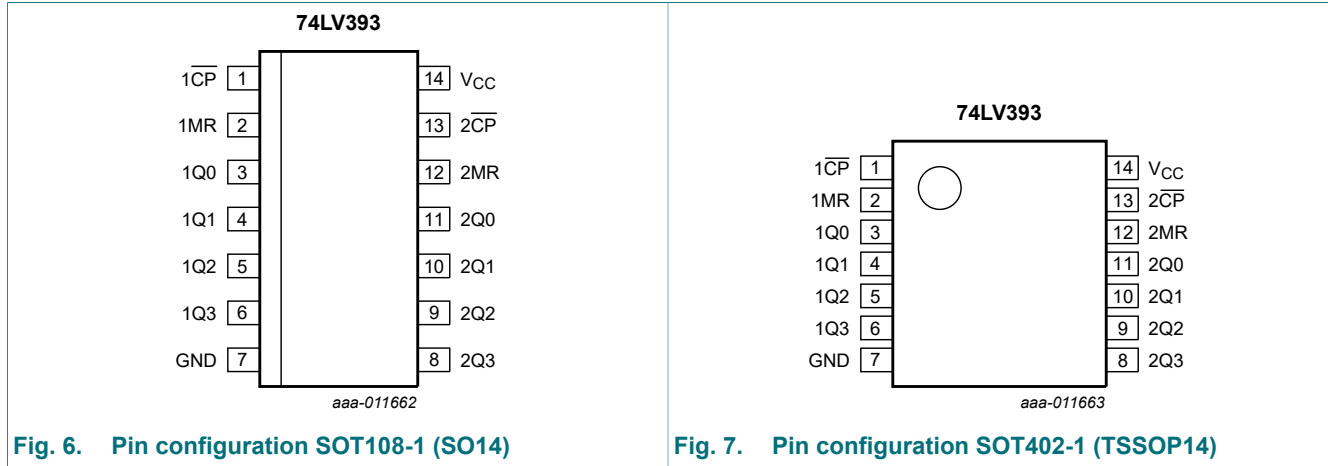


Fig. 6. Pin configuration SOT108-1 (SO14)

Fig. 7. Pin configuration SOT402-1 (TSSOP14)

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 13	clock input (HIGH-to-LOW, edge-triggered)
1MR, 2MR	2, 12	asynchronous master reset input (active HIGH)
1Q0, 1Q1, 1Q2, 1Q3	3, 4, 5, 6	flip-flop output
GND	7	ground (0 V)
2Q0, 2Q1, 2Q2, 2Q3	11, 10, 9, 8	flip-flop output
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Count sequence for one counter**

*H = HIGH voltage level; L = LOW voltage level.*

Count	Output			
	nQ0	nQ1	nQ2	nQ3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 50$	mA
$I_O$	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]	-	500	mW

- [1] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.  
 For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.0	3.3	3.6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	100	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	0.9	-	-	0.9	-	V
		$V_{CC} = 2.0\text{ V}$	1.4	-	-	1.4	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.3	-	0.3	V
		$V_{CC} = 2.0\text{ V}$	-	-	0.6	-	0.6	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = -100\ \mu\text{A}; V_{CC} = 1.2\text{ V}$	-	1.2	-	-	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 2.7\text{ V}$	2.5	2.7	-	2.5	-	V
		$I_O = -100\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.80	3.0	-	2.8	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = 100\ \mu\text{A}; V_{CC} = 1.2\text{ V}$	-	0	-	-	-	V
		$I_O = 100\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.2	-	0.2	V
		$I_O = 100\ \mu\text{A}; V_{CC} = 2.7\text{ V}$	-	0	0.2	-	0.2	V
		$I_O = 100\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.2	-	0.2	V
$I_I$	input leakage current	$V_I = V_{CC}\text{ or GND}; V_{CC} = 3.6\text{ V}$	-	-	1.0	-	1.0	$\mu\text{A}$
		$V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}; V_{CC} = 3.6\text{ V}$	-	-	20.0	-	160	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_I = V_{CC} - 0.6\text{ V}; V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	500	-	850	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

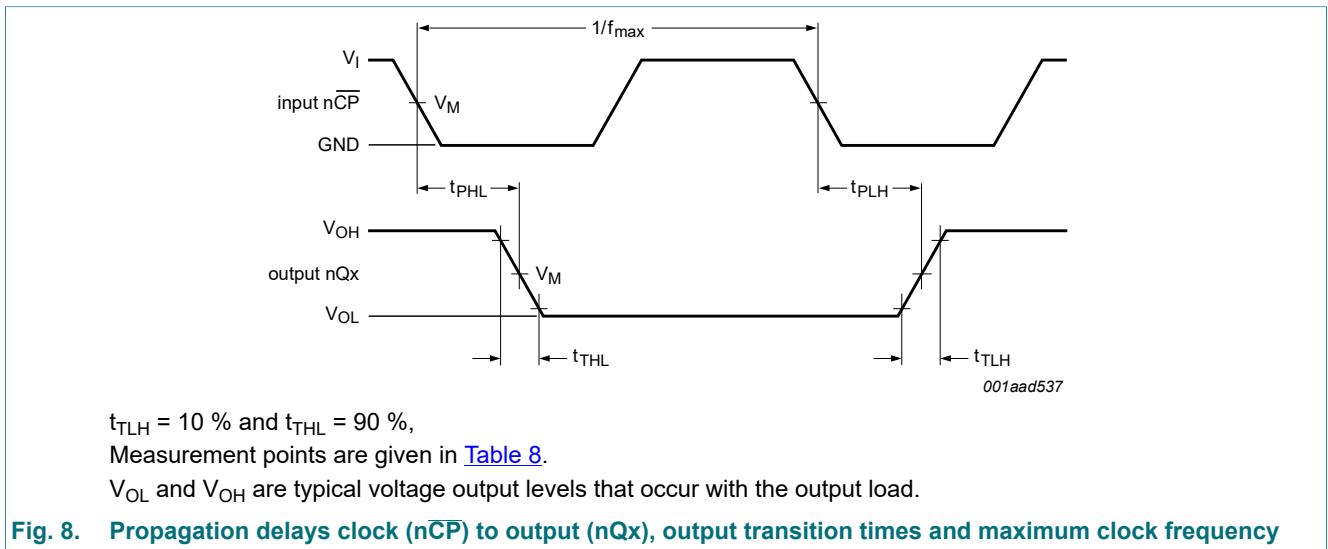
Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{pd}$	propagation delay	n $\overline{CP}$ to nQ0; see Fig. 8 [2]						
		$V_{CC} = 1.2$ V	-	75	-	-	-	ns
		$V_{CC} = 2.0$ V	-	26	49	-	60	ns
		$V_{CC} = 2.7$ V	-	19	36	-	44	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	12	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	14	29	-	35	ns
		nQ to nQn+1; see Fig. 8 [2]						
		$V_{CC} = 1.2$ V	-	25	-	-	-	ns
		$V_{CC} = 2.0$ V	-	9	17	-	20	ns
		$V_{CC} = 2.7$ V	-	6	13	-	15	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	4	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	5	10	-	12	ns
$t_{PHL}$	HIGH to LOW propagation delay	nMR to nQx; see Fig. 9						
		$V_{CC} = 1.2$ V	-	70	-	-	-	ns
		$V_{CC} = 2.0$ V	-	24	44	-	54	ns
		$V_{CC} = 2.7$ V	-	18	33	-	40	ns
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	11	-	-	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	-	13	26	-	32	ns
$t_w$	pulse width	n $\overline{CP}$ HIGH or LOW; see Fig. 8						
		$V_{CC} = 2.0$ V	34	10	-	41	-	ns
		$V_{CC} = 2.7$ V	25	8	-	30	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	20	6	-	24	-	ns
		nMR HIGH; see Fig. 9						
		$V_{CC} = 2.0$ V	34	12	-	41	-	ns
		$V_{CC} = 2.7$ V	25	9	-	30	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	20	7	-	24	-	ns
$t_{rec}$	recovery time	nMR to n $\overline{CP}$ ; see Fig. 9						
		$V_{CC} = 1.2$ V	-	5	-	-	-	ns
		$V_{CC} = 2.0$ V	5	2	-	5	-	ns
		$V_{CC} = 2.7$ V	5	2	-	5	-	ns
		$V_{CC} = 3.0$ V to 3.6 V [3]	5	1	-	5	-	ns
$f_{max}$	maximum frequency	see Fig. 8						
		$V_{CC} = 2.0$ V	14	53	-	12	-	MHz
		$V_{CC} = 2.7$ V	19	72	-	16	-	MHz
		$V_{CC} = 3.3$ V, $C_L = 15$ pF	-	99	-	-	-	MHz
		$V_{CC} = 3.0$ V to 3.6 V [3]	24	90	-	20	-	MHz

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> [3] [4]	-	23	-	-	-	pF

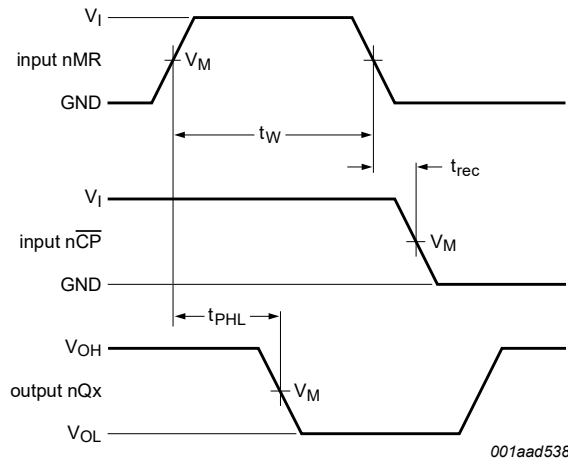
- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 10.1. Waveforms and test circuit



**Table 8. Measurement points**

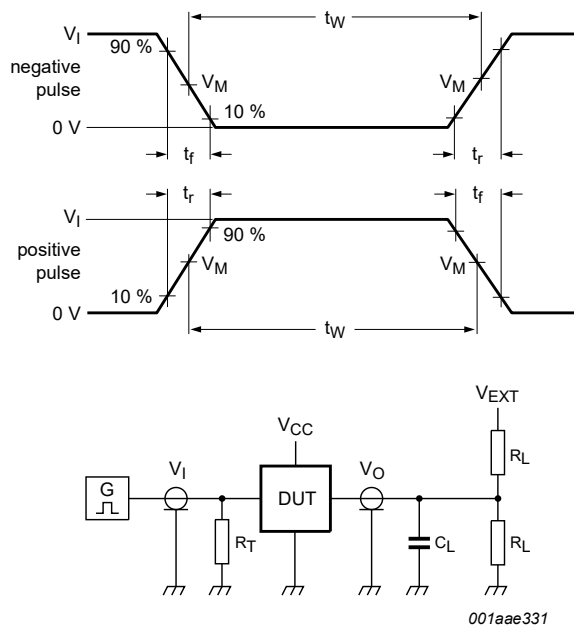
Supply voltage V <sub>CC</sub>	Input		Output	
	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
< 2.7 V	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	V <sub>OL</sub> + 0.1V <sub>CC</sub>	V <sub>OH</sub> - 0.1V <sub>CC</sub>
2.7 V to 3.6 V	1.5V <sub>CC</sub>	1.5V <sub>CC</sub>	V <sub>OL</sub> + 0.3V <sub>CC</sub>	V <sub>OH</sub> - 0.3V <sub>CC</sub>



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 9. Propagation delays clock (nCP) to output (nQx), pulse width master reset (nMR), and recovery time master reset (nMR) to clock (nCP)**



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

S1 = Test selection switch.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input	Load			$V_{EXT}$
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
< 2.7 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	1 k $\Omega$	open
2.7 V to 3.6 V	2.7 V	$\leq 2.5$ ns	15 pF, 50 pF	1 k $\Omega$	open



### 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

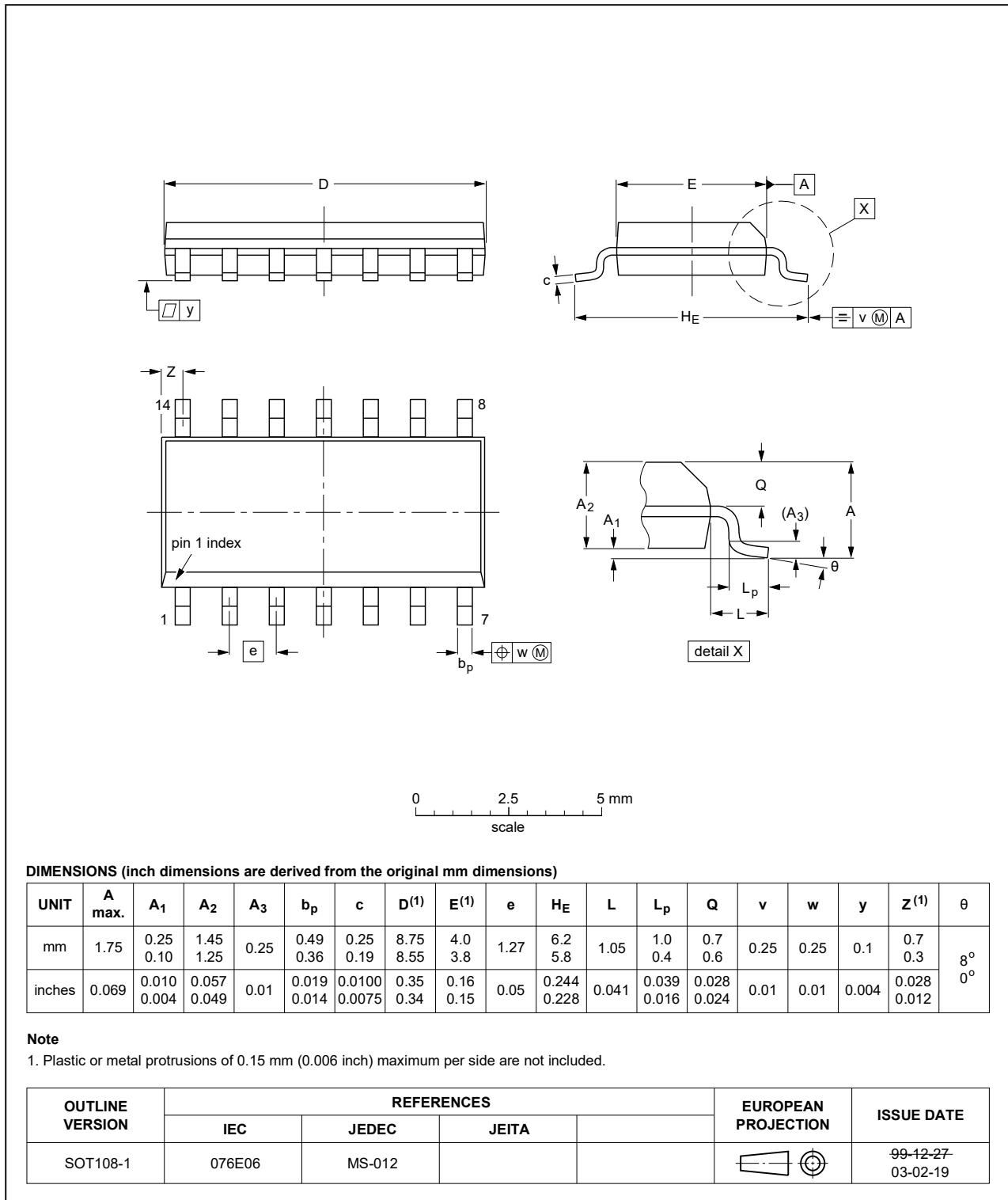


Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 12. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV393 v.6	20210319	Product data sheet	-	74LV393 v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> updated.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li>Type number 74LV393DB (SOT337-1 / SSOP14) removed.</li> </ul>			
74LV393 v.5	20151208	Product data sheet	-	74LV393 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LV393N (SOT27-1) removed.</li> </ul>			
74LV393 v.4	20140918	Product data sheet	-	74LV393 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 4</a> minus sign added to the minimum ground current.</li> <li><a href="#">Fig. 10</a> and <a href="#">Table 9</a> updated because of a missing load resistance in the test circuit.</li> </ul>			
74LV393 v.3	20140428	Product data sheet	-	74LV393 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LV393 v.2	19970610	Product specification	-	74LV393 v.1
74LV393 v.1	19970304	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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