74HCT14

Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The 74HCT14 may be used as a level converter for interfacing TTL or NMOS outputs to high−speed CMOS inputs.

The HCT14 is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14 finds applications in noisy environments.

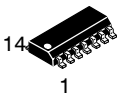
Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb−Free Devices

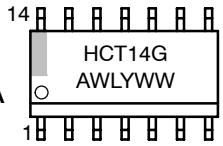
ON Semiconductor®

http://onsemi.com

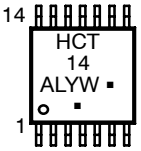
MARKING DIAGRAMS



SOIC−14
D SUFFIX
CASE 751A



TSSOP−14
DT SUFFIX
CASE 948G



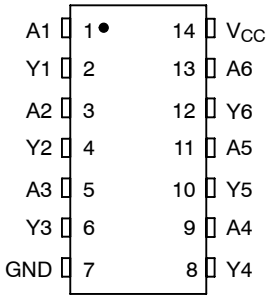
HCT14	= Device Code
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

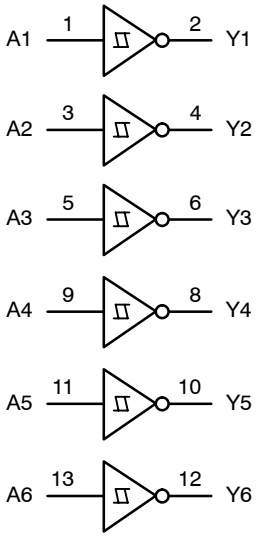
PIN ASSIGNMENT



FUNCTION TABLE

Input A	Output Y
L	H
H	L

LOGIC DIAGRAM



$Y = \overline{A}$ PIN 14 = V_{CC}
PIN 7 = GND

ORDERING INFORMATION

Device	Package	Shipping†
74HCT14DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
74HCT14DTR2G	TSSOP−14*	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	−0.5 to +7.0	V
V_I	DC Input Voltage	(Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_O	DC Output Voltage	(Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current		±20	mA
I_{OK}	DC Output Diode Current		±25	mA
I_O	DC Output Sink Current		±25	mA
I_{CC}	DC Supply Current per Supply Pin		±50	mA
I_{GND}	DC Ground Current per Ground Pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOIC TSSOP	125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC TSSOP	500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2)	>2000 >200	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 3)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to EIA/JESD78.
4. For high frequency or heavy load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	4.5	5.5	V
V_I, V_O	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)		−	(Note 5)	ns

5. No Limit when $V_I \approx 50\%$ V_{CC}, I_{CC} > 1 mA.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Temperature Limit						Unit
				−55°C to 25°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
V_{T+} max	Maximum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V_{T+} min	Minimum Positive−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
V_{T-} max	Maximum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
V_{T-} min	Minimum Negative−Going Input Threshold Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V_H max	Maximum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V_H min	Minimum Hysteresis Voltage	V_O = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0 4		
V_{OH}	Minimum High−Level Output Voltage	$V_I < V_{T-}$ min $\|I_{out}\| \le 20$ μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		$V_I < V_{T-}$ min $\|I_{out}\| \le 4.0$ mA	4.5	3.98		3.84		3.7		
V_{OL}	Maximum Low−Level Output Voltage	$V_I \ge V_{T+}$ max $\|I_{out}\| \le 20$ μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		$V_I \ge V_{T+}$ max $\|I_{out}\| \le 4.0$ mA	4.5		0.26		0.33		0.4	
I_{IK}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per package)	V_I = V_{CC} or GND I_{out} = 0 μA	5.5		2.0		20		40	μA
				≥ −55°C		25°C to 125°C				
ΔI_{CC}	Additional Quiescent Supply Current	V_I = 2.4 V, Any One Input V_I = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	2.9		2.4				mA

7. Information on typical parametric values can be found in the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Test Conditions	Figures	Guaranteed Limit						Unit
				−55°C to 25°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V_{CC} = 5.0 V ±10% C_L = 50 pF, Input t_r = t_f = 6.0 ns	1 & 2		32		40		48	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	V_{CC} = 5.0 V ±10% C_L = 50 pF, Input t_r = t_f = 6.0 ns	1 & 2		15		19		22	ns

8. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance, per Inverter (Note 9)	32	pF

9. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

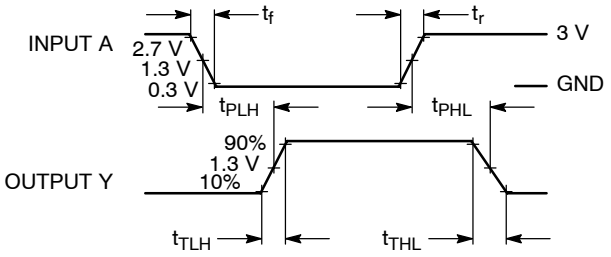
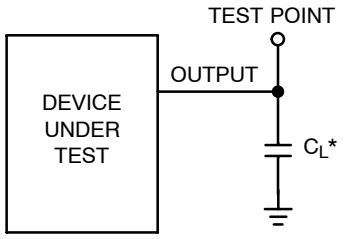


Figure 1. Switching Waveforms

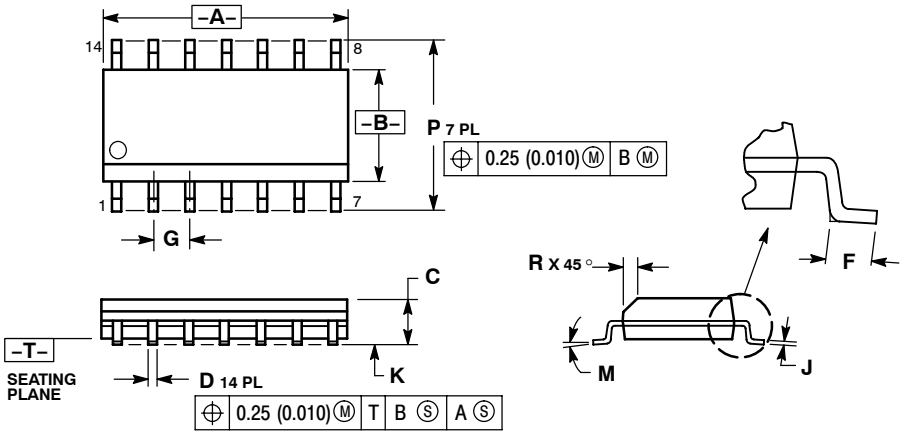


*Includes all probe and jig capacitance.

Figure 2. Test Circuit

PACKAGE DIMENSIONS

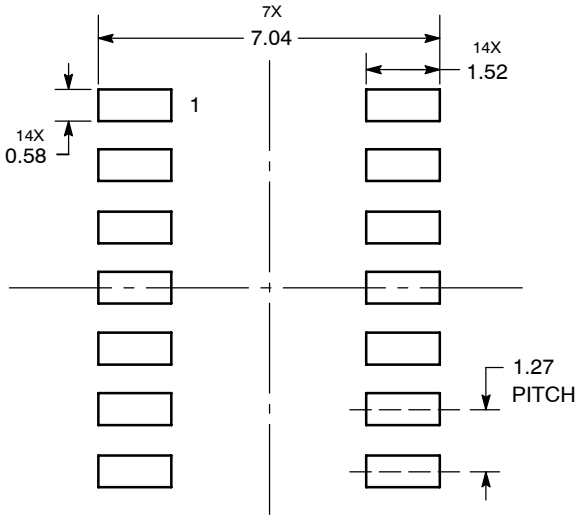
SOIC−14
CASE 751A−03
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

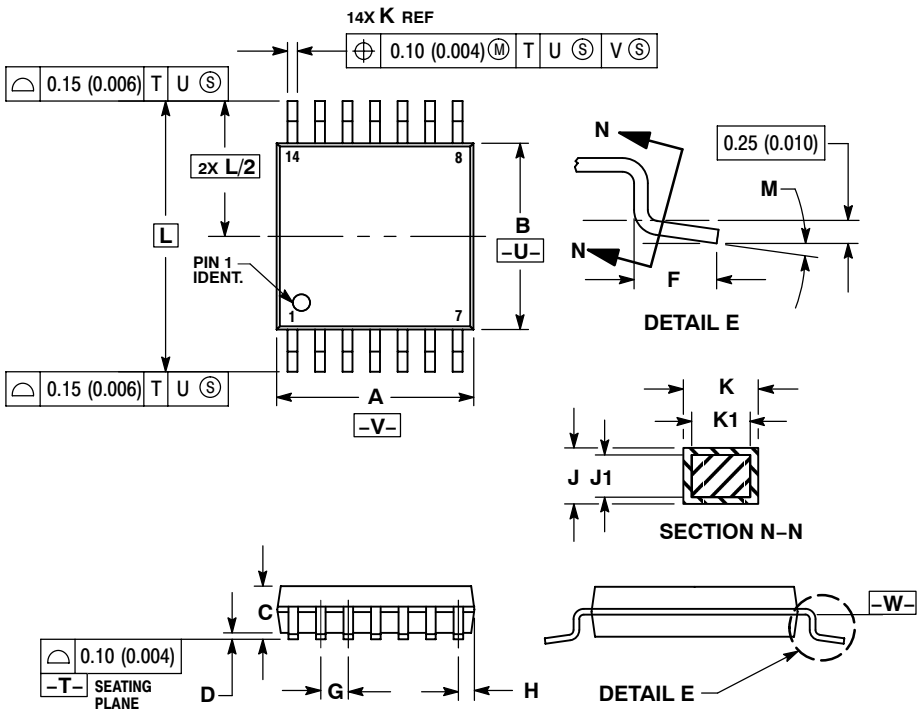


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

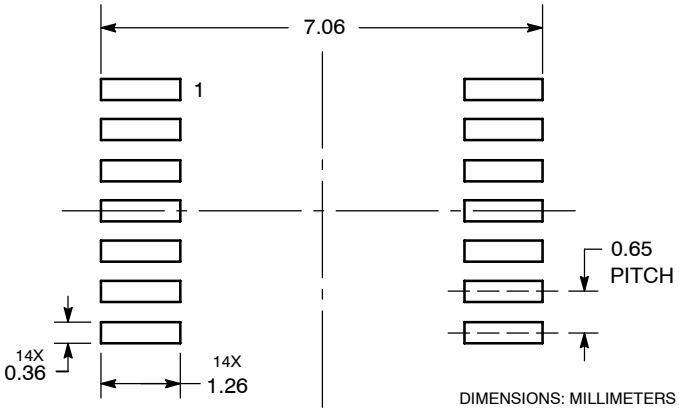
TSSOP−14
CASE 948G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

74HCT14/D