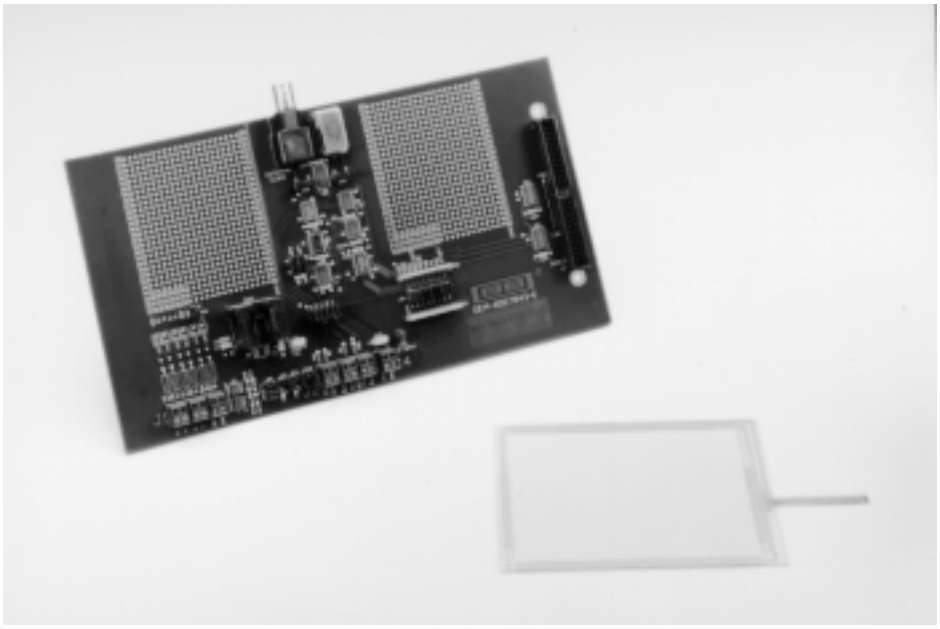
BURR-BROWN®

DEM-ADS7843E/45E

EVALUATION FIXTURE



FEATURES

- STAND-ALONE CAPABILITY
- FLEXIBLE CLOCK PROGRAMMING
- USER-CONFIGURABLE A/D CONVERTER OPERATION
- ANALOG BREADBOARD AREA
- DIGITAL BREADBOARD AREA
- FLEXIBLE REFERENCE VOLTAGE PROGRAMMING

APPLICATIONS

- DATA ACQUISTION
- PERSONAL DIGITAL ASSISTANTS
- 4- OR 5-WIRE RESISTIVE TOUCH SCREEN
- PORTABLE INSTRUMENTS

DESCRIPTION

The DEM-ADS7843E/45E evaluation fixture is designed for quick evaluation of Burr-Brown's ADS7843E (4-wire) and ADS7845E (5-wire) touch-panel controllers. The board has features that allow the user to evaluate all the functions of the analog-to-digital converter. The options offered to the user include a flexible clock generator circuit, an analog breadboard area, a digital breadboard area, and an easily-configurable voltage reference. The DEM-ADS7843E/45E has been designed to accommodate stand-alone operation, allowing the user to easily connect directly to 4-wire (ADS7843E) or 5-wire (ADS7845E) touch-screen panels and to an external processor. This evaluation fixture has a quick-release socket for easy evaluation of mulitiple converters or a solder footprint to allow the user to solder the DUT directly to the board.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

LI-522A
Printed in U.S.A.March, 1999
SBAU004

INSTALLATION

The DEM-ADS7843E/45E evaluation fixture is designed for stand-alone evaluation or evaluation using the clocking network on the board. Stand-alone evaluations imply that the A/D converter is powered by J4 (power supply connector) and the user is put to the task to provide analog and digital input excitation. This is achieved by removing all five jumper tops of JP4 and using J1 and J2 for direct connections to the device under test (DUT).

In contrast, the DEM-ADS7843E/45E/45E board has the appropriate digital interface circuitry to drive the DUT data clock, chip select, and serial data in which is coordinated with the BUSY and PENIRQ to provide serial and parallel output data.

This kit includes the following items:

ADS7843E Evaluation Fixture—A2518

DEM-ADS7843E/45E Documentation (LI-522)

ADS7843E (5 samples)

ADS7845E (5 samples)

The DEM-ADS7843E evaluation fixture has two positions on the board for the A/D converter to be installed in. The first position is the socket, DUT1 on the board. This spring-loaded socket allows the user to quickly swap in or out the device that is being evaluated. The other option on the board is the position X1, which is a solder location for the DUT. If this option is chosen, the user must solder the DUT directly to the board. This position is only useful for 2 or 3 solder cycles.

CAUTION: DO NOT connect the a device into the DUT1 socket and have another device soldered to the board in position X1 at the same time.

The additional equipment required to do a complete evaluation of the performance of the ADS7843E or ADS7845E comprises of:

+5VDC power supply

Voltage or current signal source

4-Wire (ADS7843E) or 5-Wire (ADS7845E) Resistive Touch Screen

To install the DEM-ADS7843E/45E evaluation fixture, connect the appropriate power supply to J4. When power is applied to the DEM-ADS7843E/45E, the red LED on the board should light.

J1	Analog Input Interface. Each connector is labeled.
J2	Digital I/O Interface. Each connector is labeled.
J3	Parallel Output Port.
J4	Power Supply Connector. This connector powers the DUT and digital network. Refer to the ADS7843 or ADS7845 product data sheet for power supply restrictions. All digital chips on the DEM-ADS7843E/45E board are capable of operating with supply voltage from 2.7V to 5.25V.
P1	External DCLK Connector.

TABLE I. Connectors (Jx and P1) Assignments.

USER CONFIGURATIONS

The DEM-ADS7843E/45E evaluation fixture provides the right combination of jumper options and support circuitry to allow for a variety of evaluation configurations. Throughout this data sheet, numerous references are made to the ADS7843 and ADS7845 A/D converters. For more information concerning these devices, refer to the ADS7843 or ADS7845 data sheet. The circuit is laid out with a four-layer board. The two outside layers are for circuit traces and the inner layers are the ground and power planes. The analog and digital planes of the circuit is separated through the middle of the board all the way to the power supply connector, where they are joined. The circuit diagram and layout diagrams for the DEM-ADS7843E/45E is shown in Figure 1 and Figures 4 through 7.

JUMPER NUMBER	FACTORY SETTING	DESCRIPTION
JP1	B	Voltage reference. This setting connects A/D converter reference to $+V_{CC}$.
JP2, JP11, JP10	JP2 = Not Installed JP11 = Not Installed JP10 = Not Installed	Inverted or non-inverted option for PENIRQ of the ADS7843 or ADS7845 when driving this pin through pin 2. This setting sets this pin HIGH and connects this pin to J2.
JP3	D, F, G	Hardwire digital jumpers for DIN serial code. This setting configures the A/D converter for S = HIGH, A2-A0 = 001, MODE = LOW, SGL/DIF = HIGH, PD1-PD0 = 11.
JP4	A, B, C, D, E	This jumper connects the clocking network to the DUT.
JP5, JP6	JP5 = A JP6 = B	Clock speed options. This configuration sets the board using Y1/10 as the DCLK frequency.
JP7, JP8	JP7 = B JP8 = A	Optional 16- or 24-bit operation. This configuration sets the board for 16 DCLK per conversion cycle.
JP9	B	Used to personalize the board for the ADS7843 or ADS7845. Position B = ADS7843 or ADS7845.

TABLE II. Jumper (JPx) Assignments.

DUT CONNECTIONS

The DEM-ADS7843E/45E DUT Board has a socket for the DUT which is positioned in the DUT1 position. Additionally, it has a solder footprint in the event that the user chooses to solder the DUT directly to the board. This footprint is poisitioned in X1, just below the DUT1 socket. If the solder footprint is used, care should be taken to preserve the solder pads for repeated soldering. Bad X1 solder pads do not interfere with the operation or connections of the DUT1 socket.

The DEM-ADS7843E/45E evaluation fixture is designed to evaluate both the ADS7843 and ADS7845 A/D converters. JP9 must be in position B to evaluate either the ADS7843 or ADS7845.

Space for an R/C input filter has been provided to allow user customization for the particular application. Shorting bars have been installed in R_3, R_5, R_7, R_9, R_{10}, and R_{12} positions on the board. These are positioned betwen the input of the DUT and the pin connector, P1. Shorting bars were used to allow for immediate evaluation of a four-wire touch screen. In this situation, the touch screen would provide the source resistance. If resistors are desired in positions R_3, R_5, R_7, R_9, R_{10}, and R_{12}, the user can solder in the desired values. Additionally, positions for capacitors at the input of the DUT are provided with C_3, C_4, C_5, C_6, C_9 and C_{10}. Once again, the user must install appropriate values for the application under evaluation.

The voltage reference to the DUT is programmed in the JP1. The JP1 options are given in Table III.

POSITION	RESULTING CONFIGURATION
A	1.2V is configured to pin 9 (V_{REF}) of the DUT.
B	The power supply from J4 is configured to pin 9 (V_{REF}) of the DUT.
C	2.5V is configured to pin 9 (V_{REF}) of the DUT.

TABLE III. V_{REF} is Programmed Using JP1 Position Options.

The combination of JP2 allows jumper programmable settings of the PENIRQ of the ADS7843 or ADS7845 pin of the DUT. Additionally, this pin can be accessed through J2 and a combination of JP10 and JP11. Refer to Table IV for jumper position details. Refer to the ADS7845 data sheet for additional options.

The digital I/O pins of the DUT may be driven or monitored with the J2 connector. The assignment of these pins are summarized in Table V.

J2 PIN NUMBER (From Left to Right)	ADS7843 PIN DESCRIPTION
1	$\overline{CS}$
2	DCLK
3	BUSY
4	DIN
5	PENIRQ
6	DOUT

TABLE V. J2 Connector Contacts versus DUT Pins. (NOTE: If you have a DEM-ADS7843E/45E, Revision A, the silkscreen is in error. The above description is correct.)

STAND-ALONE OPERATION

The DUT can be evaluated in a stand-alone configuration by removing all of the jumper tops of JP4. JP4 connects pins 12, 13, 14, 15, and 16 of the DUT to the digital interface circuitry of the board. If the array of jumper tops are not removed, the user may find significant conflicts on the digital I/O lines of the DUT. The details of this interface circuitry is discussed in detail in the “Digital Interface” section of this data sheet.

DIGITAL INTERFACE CIRCUITRY

The DUT can be evaluated using the digital clocking circuitry on the board by installing all of the jumper tops of JP4 and removing any signal present on the J2 connector. This digital circuit uses the clock signal from P1 (External Clock) or Y1 to create the DUT clock (DCLK), CS, and the DIN code to the device while providing a serial or parallel output signal from the DOUT pin of the DUT.

Clock Control

The master clock to the board is set with the JP6 jumper. Position A of the JP6 jumper configures the External Clock (P1) coax connector into the circuit. It is recommended that this signal be a logic square wave. The signal from this connector will be used directly for the DCLK signal to the

JP2 POSITION	JP10 POSITION	JP11 POSITION	RESULTING CONFIGURATION
Not Installed	Not Installed	Not Installed	Pin 11 of the DUT is HIGH.
Not Installed	Installed	Not Installed	Pin 11 of the DUT is connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default HIGH.
Not Installed	Not Installed	Installed	Pin 11 of the DUT is inverted and connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default HIGH.
Installed	Not Installed	Not Installed	Pin 11 of the DUT is LOW.
Installed	Installed	Not Installed	Pin 11 of the DUT is connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default LOW.
Installed	Not Installed	Installed	Pin 11 of the DUT is inverted and connected to position 5 of J2. If there is no connection to position 5 of J2, pin 11 of the DUT will default LOW.

TABLE IV. PENIRQ (ADS7843 or ADS7845) Jumper Settings.

DUT. Refer to the ADS7843 or ADS7845 data sheet for the proper restrictions on this clock. Alternatively, a clock oscillator that is installed in Y1 can be used as the master clock. The signal from this device is either divided by 10 or divided by 20 per JP5. The settings from JP5 are listed in Table VI.

JUMPER SETTING	RESULTING CONFIGURATION
A	Y1 Frequency divided by 10. In conjunction with JP6 = B, this frequency becomes DCLK for the DUT.
B	Y1 frequency divided by 20. In conjunction with JP6 = B, this frequency becomes DCLK for the DUT.

TABLE VI. Jumper Settings for Using Y1 as Master Clock.

Clocks per Conversion Control

Once DCLK is set (per clock control instructions) the conversion cycle of the DUT can be configured to either take 16 or 24 clock cycles. The jumper configuration for these two modes of operation are shown in Table VII. Additionally, the timing diagram of these two modes of operation are shown in Figures 2 and 3.

JP7	JP8	RESULTING CONFIGURATION
A	B	24 DCLK cycles per conversion
B	A	16 DCLK cycles per conversion

TABLE VII. The Digital Support Circuitry Can be Operated in a 16 Clocks per Conversion or a 24 Clocks per Conversion with the Jumper Settings Described in the Table. Refer to Figures 2 and 3 for specific timing.

DIN Programming

The DIN input (DUT, pin 14) receives an 8-bit serial input data stream which programs the ADS7843 or ADS7845 X or Y input channel, mode and power-down options. This serial stream can be programmed with JP3. JP3 is essentailly an 8-bit parallel configuration which is processed by a parallel-to-serial converter (U8) and then transmitted to the DUT at the appropriate time. Even when a position on JP3 is jumper top configured, digital gates can over drive their settings. Consequently, these lines are also connected to the digital breadboard area, which gives the user more flexibility in terms of programming this serial command byte.

Parallel Output

The combination of U13 and U14 converts the digital output of the DUT into a parallel word. This parallel word appears on the connector J3. A DVALID trigger is also provided on J3. Refer to Table VIII for the J3 connector configuration.

J3 PIN	DESCRIPTION
1	$\overline{\text{DVALID}}$
11	LSB
13	LSB + 1
15	LSB + 2
17	LSB + 3
19	LSB + 4
21	LSB + 5
23	LSB + 6
25	LSB + 7
27	LSB + 8
29	LSB + 9
31	LSB + 10
33	MSB
3, 5, 7, 9	Digital LOW
35 through 50	Open
All Even Pins	GND

TABLE VIII. J3 Configuration.

PART LOCATION	NUMBER PER KIT	PART NUMBER	VENDOR	DESCRIPTION
	1	A-2518 Rev B		ADS7843E Bare Board
X1 (not installed)	1	Accepts ADS7843E and ADS7845E	Burr-Brown	12-bit A/D converter solder land area, parts not installed
U1	1	REF1004C-1.2	Burr-Brown	1.235V Reference, SOIC
U2	1	REF1004C-2.5	Burr-Brown	2.5V Reference, SOIC
DUT	5	ADS7843E	Burr-Brown	12-bit Touch Screen A/D Converter (4-wire panel)
DUT	5	ADS7845E	Burr-Brown	12-bit Touch Screen A/D Converter (5-wire panel)
DUT (socket)	1	OTS-16(24)-0.635-01	Enplas (TESCO)	16-lead SSOP socket
U3, U5, U7	3	74HC393D	TI(1)	Dual, 4-bit, binary counter
U4	1	74HC08D	TI(1)	Quadruple two-input positive AND gates
U6	1	74HC04D	TI(1)	Hex Inverters
U8	1	74HC166D	TI(1)	8-bit parallel-load shift register
U13, U14	2	SN74HC594D	TI(1)	8-bit shift registers with output registers
U15	1	MC74HC390D	TI(1)	Decade counter, dual 4-bit
Y1	1	CTX129-ND	DigiKey	32MHz clock oscillator, (CTS)
Y1 (socket)	1	1107741	Aries	14-pin oscillator socket, DIP
D1	1	HLMP-3201	Hewlett Packard(1)	Red LED
R_3, R_5, R_7, R_9, R_{10}, R_{12}				Optional. Provided with shorts. Resistors not included.
R_{13}	1	CRCW12062001F	Dale	2kΩ, 1%, 0.125W, metal-film resistor
R_{14}	1	CRCW12061001F	Dale	1kΩ, 1%, 0.125W, metal-film resistor
R_{15}, R_{16}	2	CRCW120622R1F	Dale	22.1kΩ, 1%, 0.125W, metal-film resistor
R_1, R_{11}	2	CRCW12061002F	Dale	10kΩ, 1%, 0.125W, metal-film resistor
R_8, R_{18}	2	CECW12061003F	Dale	100kΩ, 1%, 0.125W, metal-film resistor
R_2, R_4, R_6	3	CRCW12061000F	Dale	100Ω, 1%, 0.125W, metal-film resistor
R_{17}	1	CRCW12066810F	Dale	681Ω, 1%, 0.125W, metal-film resistor
C_1	1	T491B225K016AS	Kemet	2.2µF capacitor, 16V
C_3 through C_6, C_9, C_{10}				Optional. Capacitor not included.
C_{12}, C_{14} through C_{25}	13	C1206C104K5RAC	Kemet	0.1µF surface-mount capacitor, X7R
C_{11}, C_{13}	2	T491C106K016AS	Kemet	10µF polarized capacitors, 16V, 10%
C_2	1	C1206C103K5RAC	Kemet	0.01µF, 50V, 10%, chip-ceramic, X7R
C_8	1	C320C104K5R5CA	Kemet	0.1µF, 50V, 10%, ceramic
JP1	1	TSW-103-07-T-D	Samtec	2 x 3
JP2	1	TSW-101-07-T-D	Samtec	2 x 1
JP3	1	TSW-108-07-T-D	Samtec	2 x 8
JP4	1	TSW-105-07-T-D	Samtec	2 x 5
JP5 through JP9	5	TSW-103-07-T-S	Samtec	1 x 3
JP1, JP2, JP3 tops	3	SNT-100-BK-T	Samtec	Jumper Tops
J1, J2, J4 pins	7	31024102	RIACON	2-pin terminal block pins, 3.5mm centers
J1, J2, J4 tops	7	31165102	RIACON	2-pin terminal block tops, 3.5mm centers
J3	1	IDH-50LP-S3-TG	Robinson Nugent	2 x 25, straight-through header w/shroud, 0.1" center spacing
P1	1	47788	Pamona	BNC right-angle, PC mount connector
RN2	1	CSC10A-01-104F	Dale	10-pin SIP resistor network (100kΩ, 9R, 1C)
RN1	1	CSC10A-01-103F	Dale	10-pin SIP resistor network (10kΩ, 9R, 1C)
Rubber Feet	6	SJ5523-O-ND	3M	Bumpons

NOTE: (1) Or equivalent.

TABLE IX. Parts List for the DEM-ADS7843E/45E.

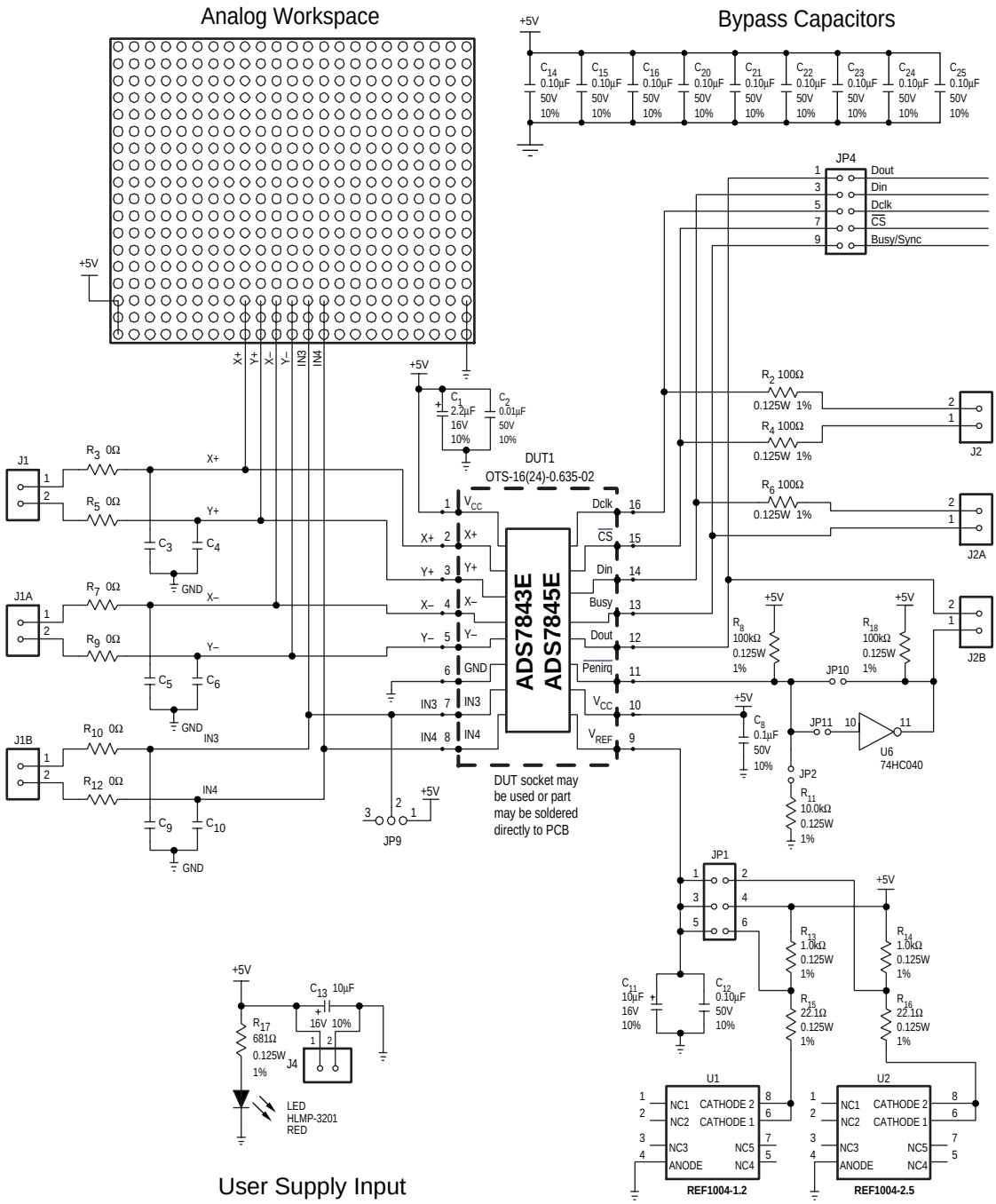
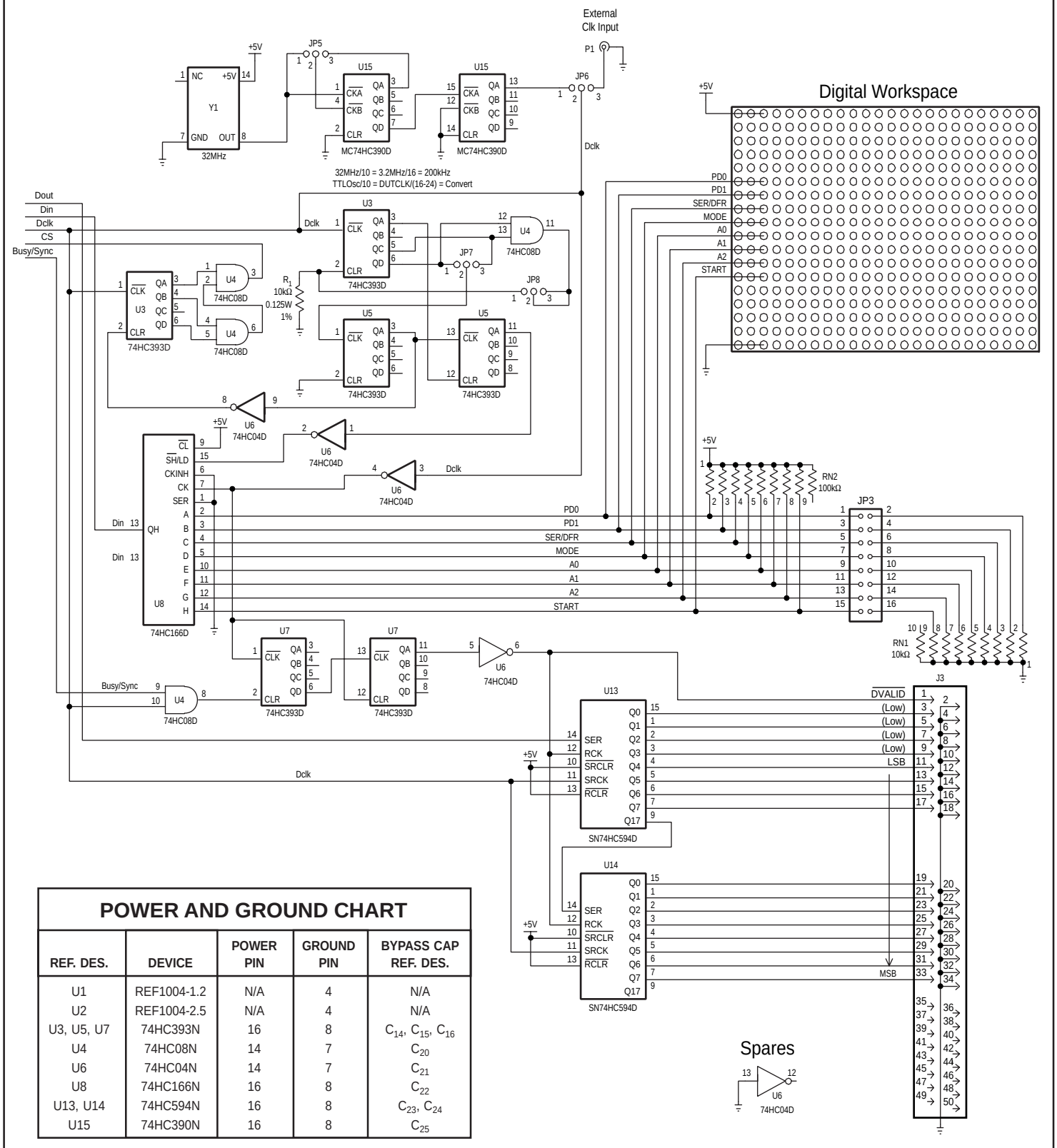


FIGURE 1a. ADS7843E and ADS7845E Evaluation Demo Board Analog Circuit Diagram.



POWER AND GROUND CHART

REF. DES.	DEVICE	POWER PIN	GROUND PIN	BYPASS CAP REF. DES.
U1	REF1004-1.2	N/A	4	N/A
U2	REF1004-2.5	N/A	4	N/A
U3, U5, U7	74HC393N	16	8	C_{14}, C_{15}, C_{16}
U4	74HC08N	14	7	C_{20}
U6	74HC04N	14	7	C_{21}
U8	74HC166N	16	8	C_{22}
U13, U14	74HC594N	16	8	C_{23}, C_{24}
U15	74HC390N	16	8	C_{25}

FIGURE 1b. ADS7843E and ADS7845E Evaluation Demo Board Digital Circuit Diagram.

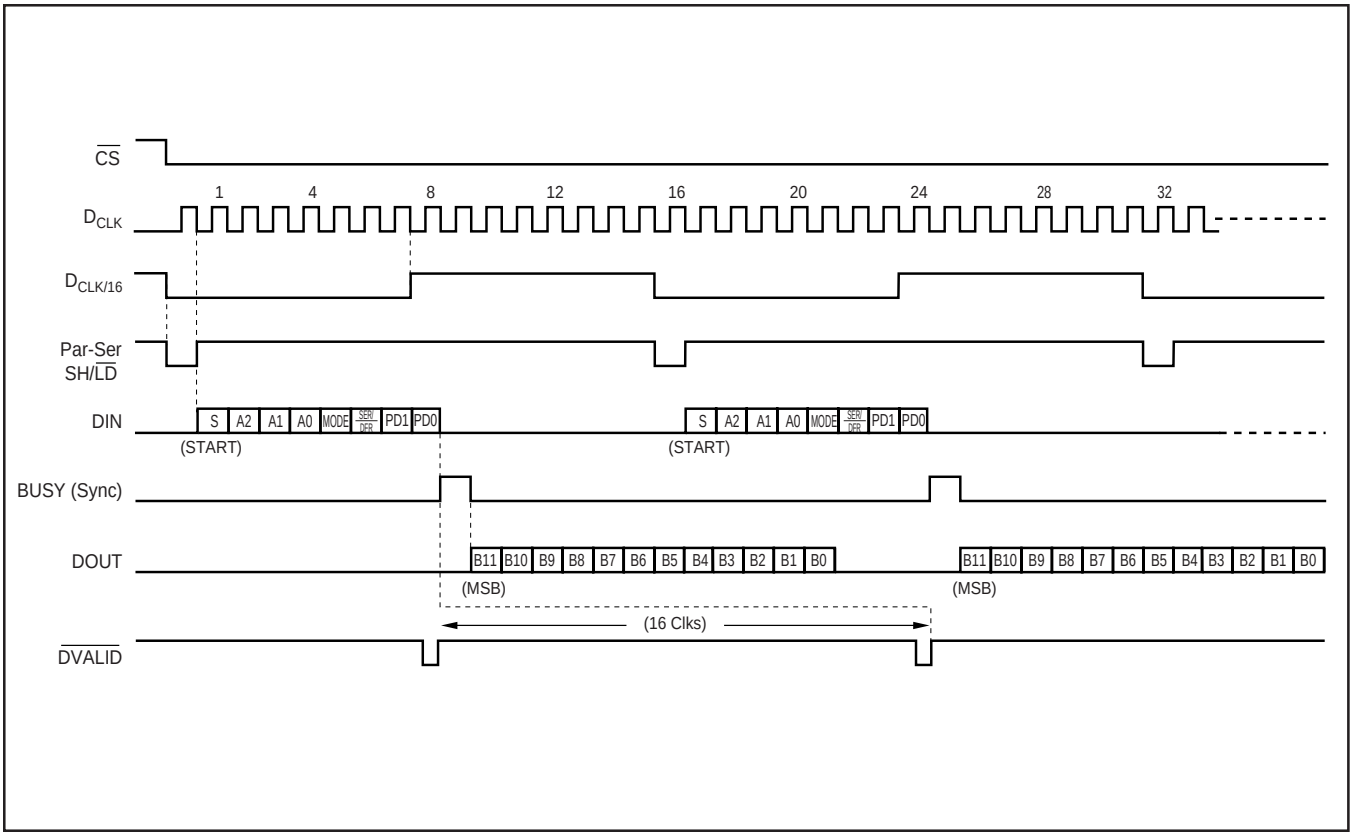


FIGURE 2. ADS7843E and ADS7845E Conversion Timing Diagram, 16 Clocks per Conversion.

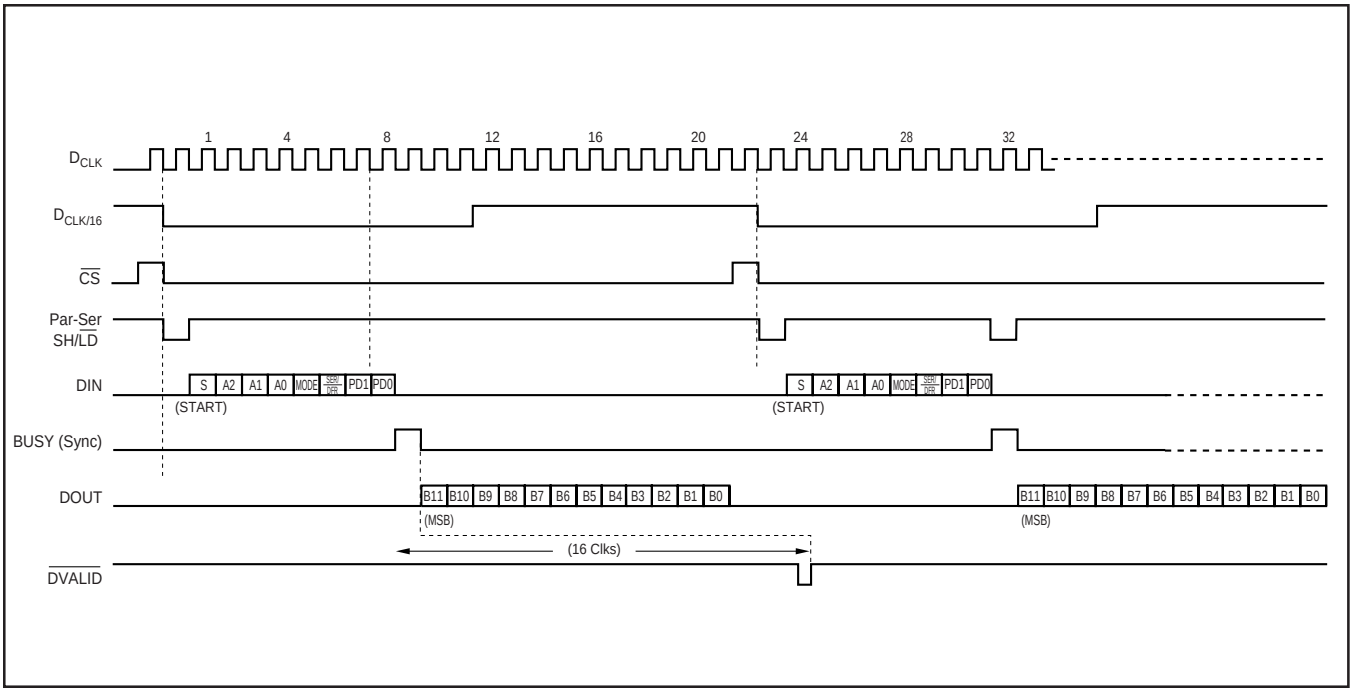


FIGURE 3. ADS7843E and ADS7845E Conversion Timing Diagram, 24 Clocks per Conversion.

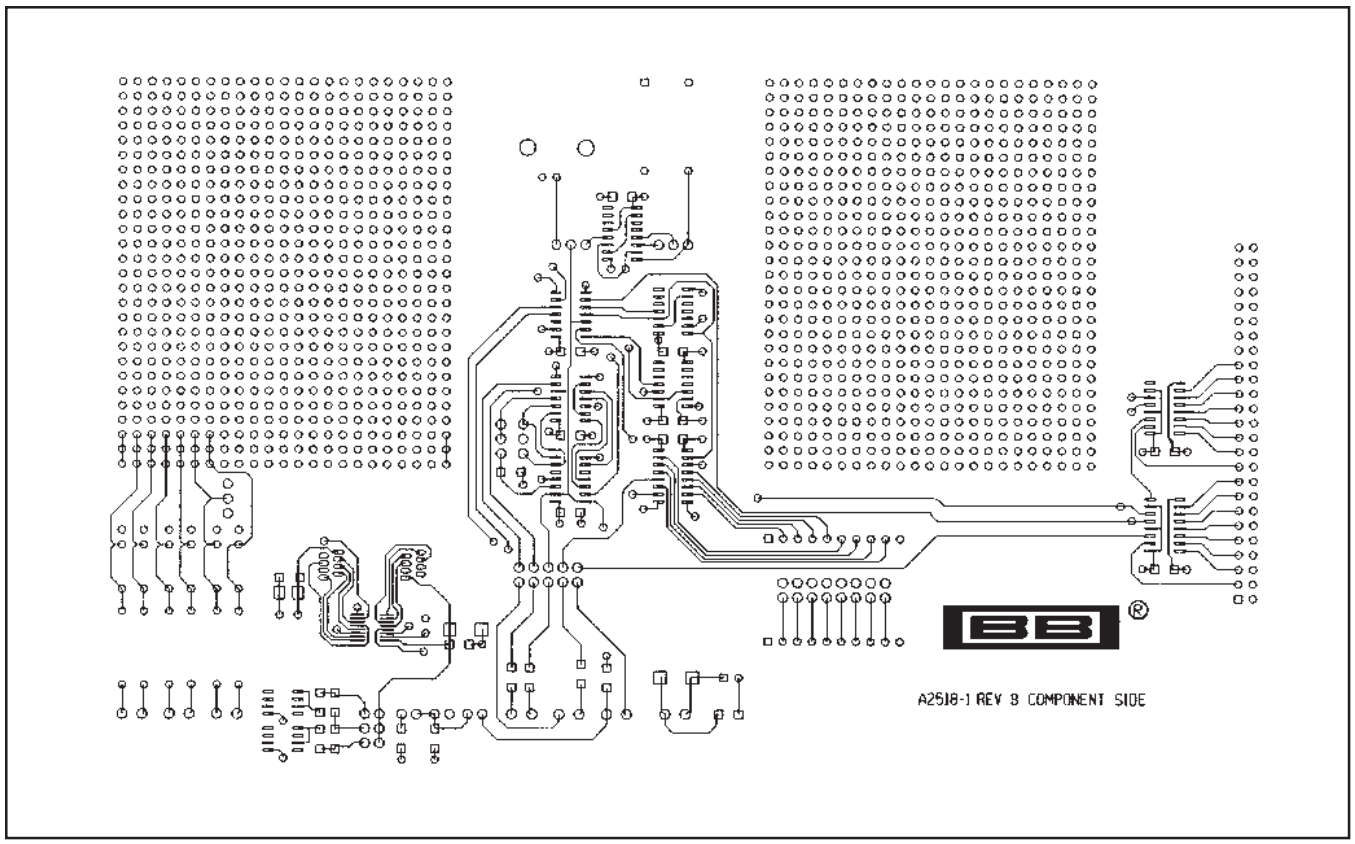


FIGURE 4. Component Side of the DEM-ADS7843E/45E Demonstration Board.

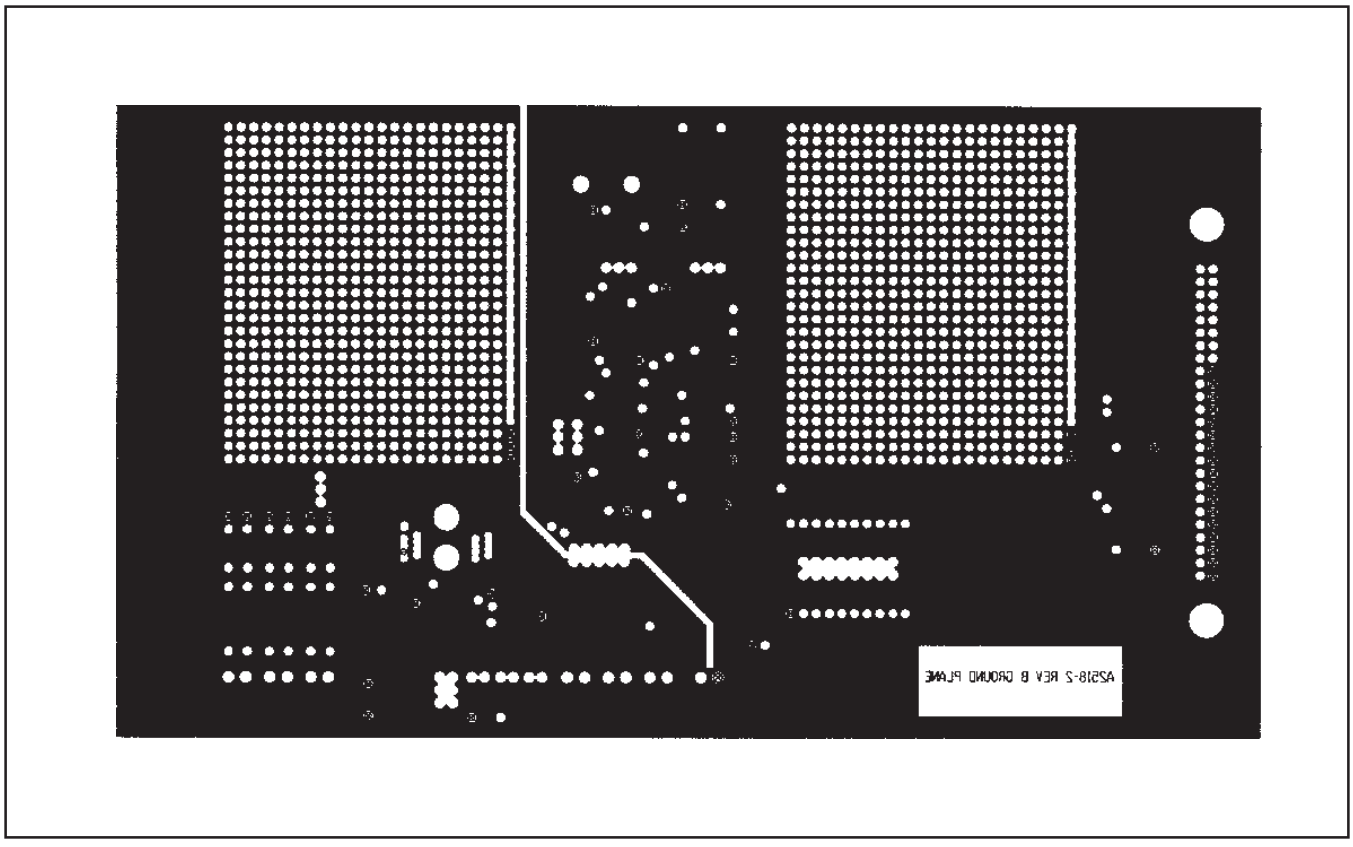


FIGURE 5. Ground Plane of the DEM-ADS7843E/45E Demonstration Board.

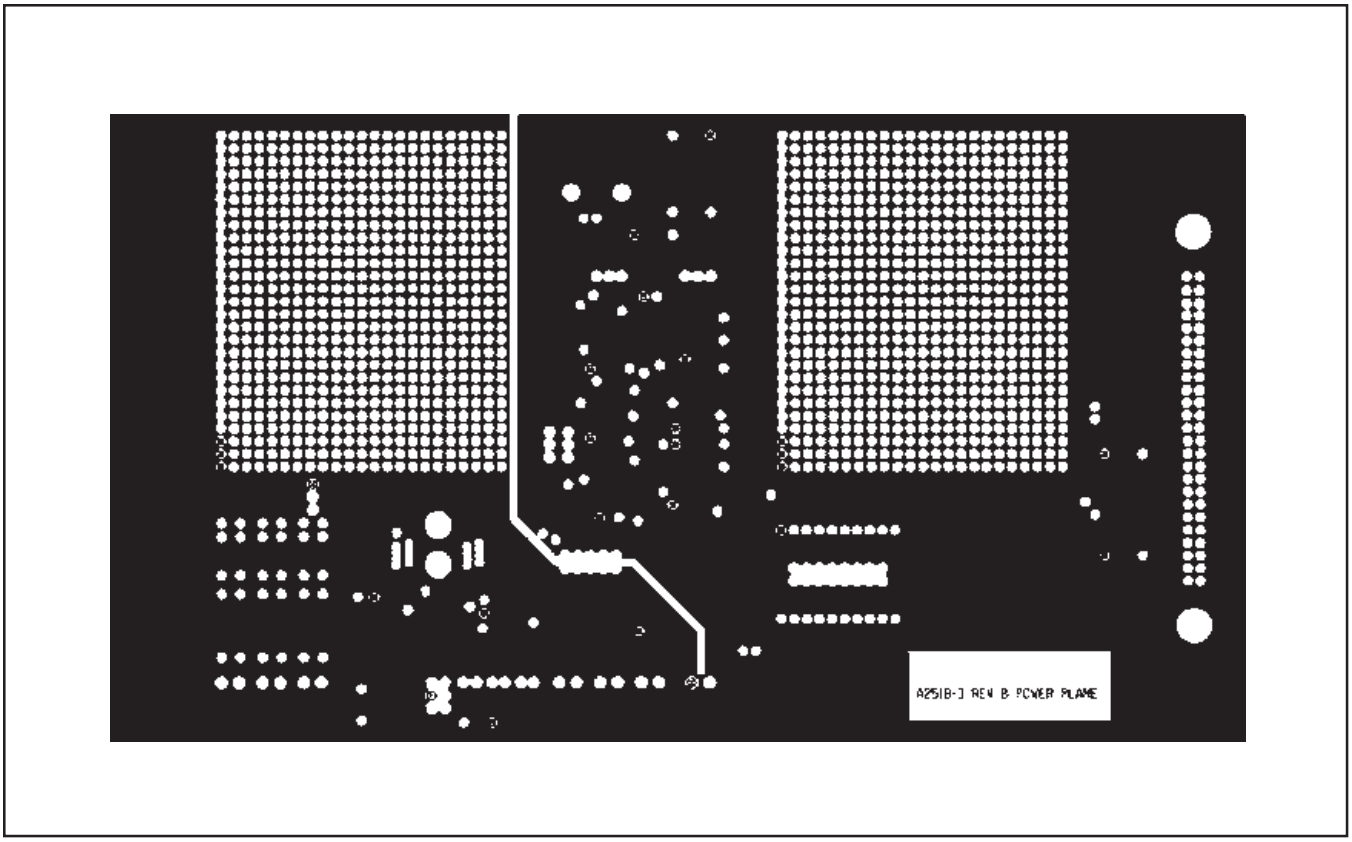


FIGURE 6. Power Plane of the DEM-ADS7843E/45E Demonstration Board.

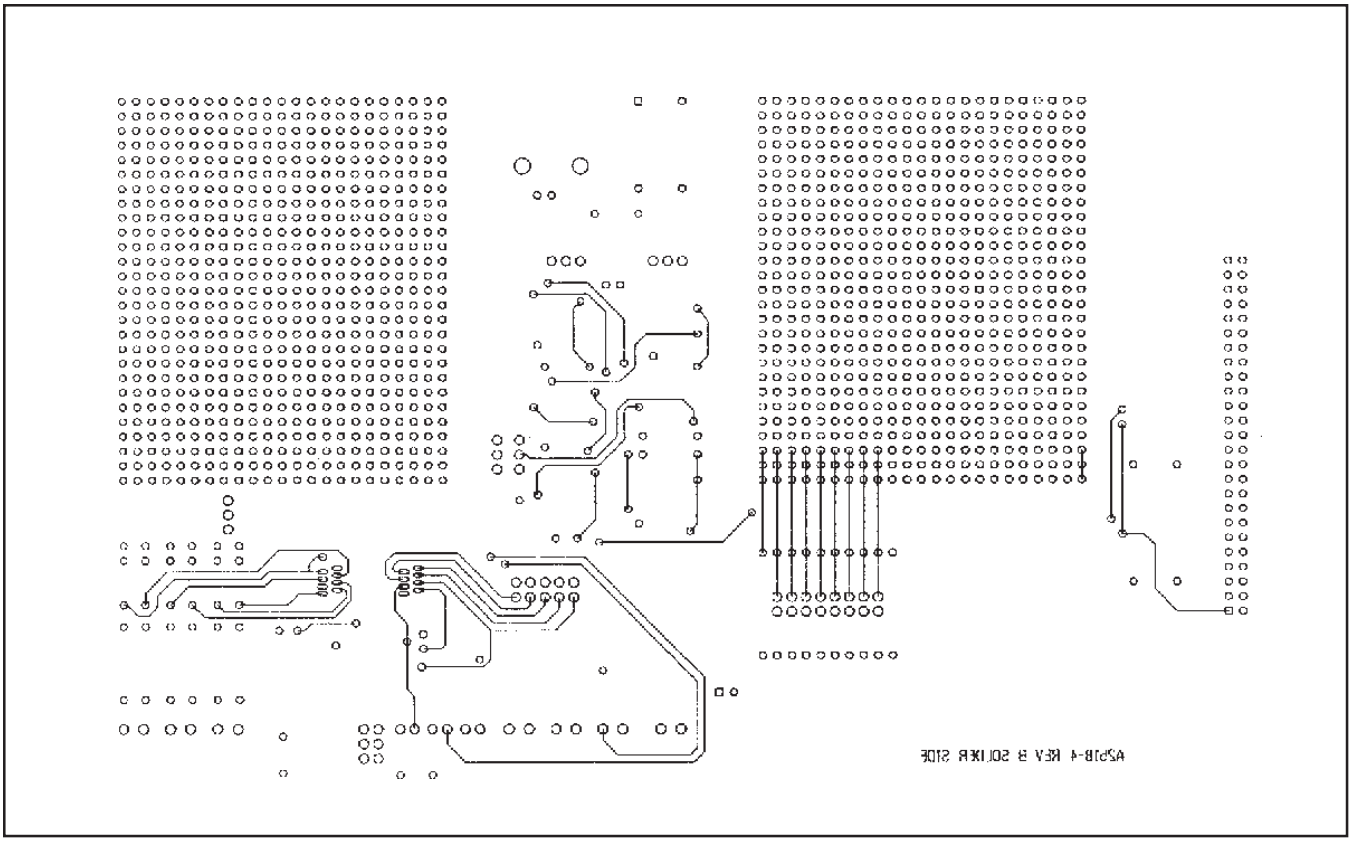


FIGURE 7. Solder Side of the DEM-ADS7843E/45E Demonstration Board.

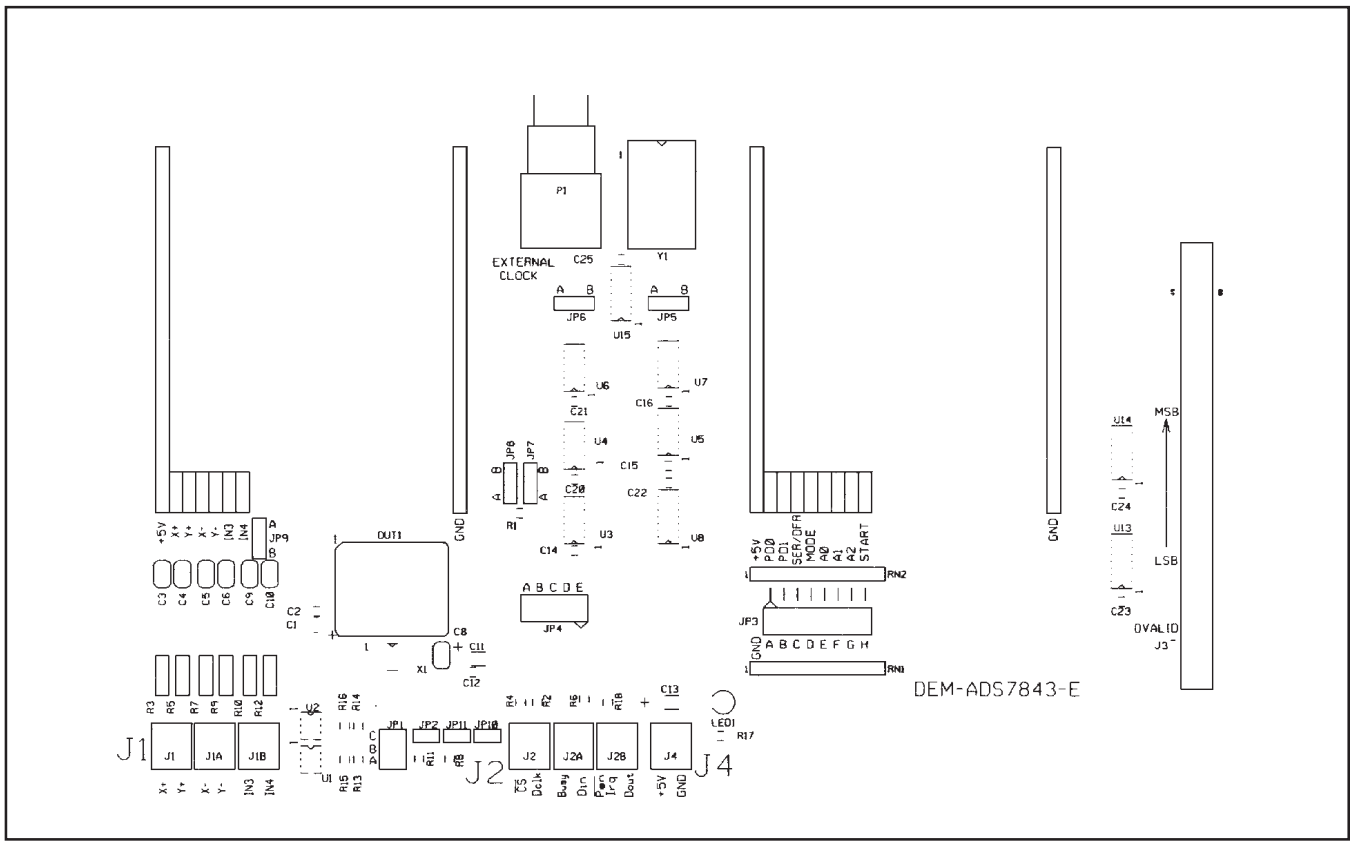


FIGURE 8. Component Side Silkscreen of the DEM-ADS7843E/45E Demonstration Board.

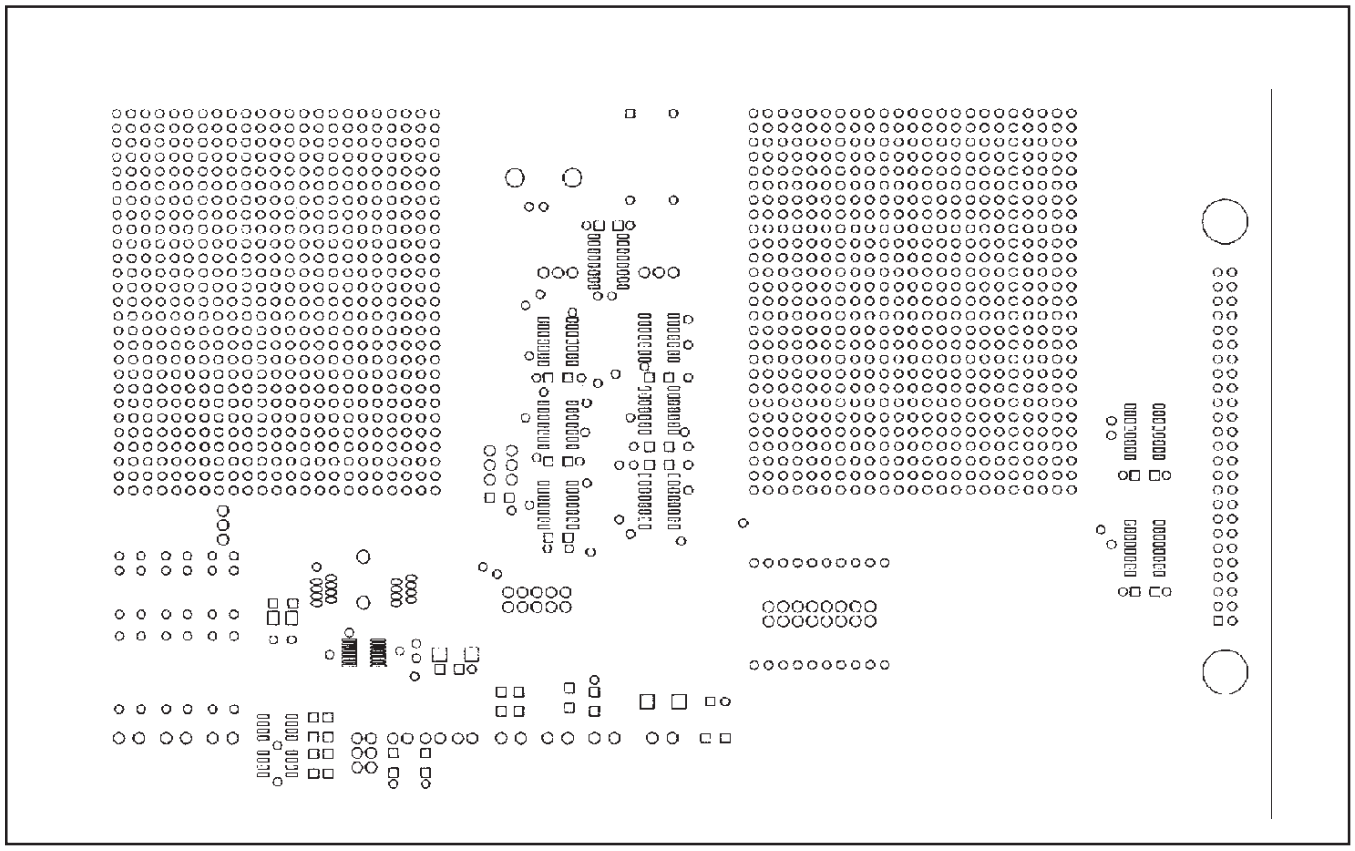


FIGURE 9. Component Side Soldermask of the DEM-ADS7843E/45E Demonstration Board.

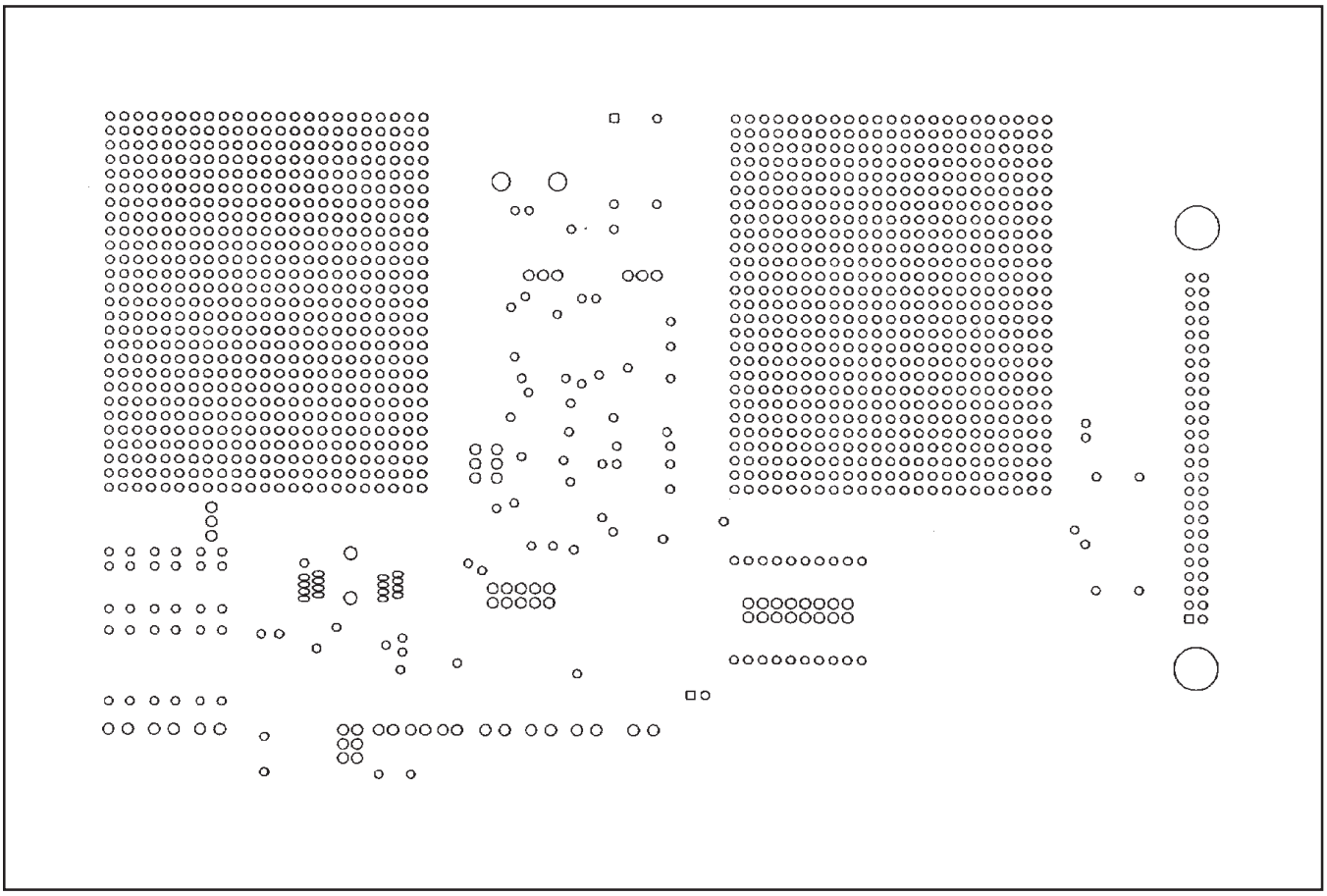


FIGURE 10. Bottom Side Soldermask of the DEM-ADS7843E/45E Demonstration Board.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.