

# 74LVC594A

## 8-bit shift register with output register

Rev. 4 — 3 September 2020

Product data sheet

### 1. General description

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The 74LVC594A is an 8-bit serial-in/serial or parallel-out shift register with a storage register. Separate clock and reset inputs are provided on both shift and storage registers. The device features a serial input (DS) and a serial output (Q7S) to enable cascading. Data is shifted on the LOW-to-HIGH transitions of the SHCP input, and the data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. A LOW level on one of the two register reset pins (SHR and STR) will clear the corresponding register. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

### 2. Features and benefits

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- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- Direct interface with TTL levels
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Applications

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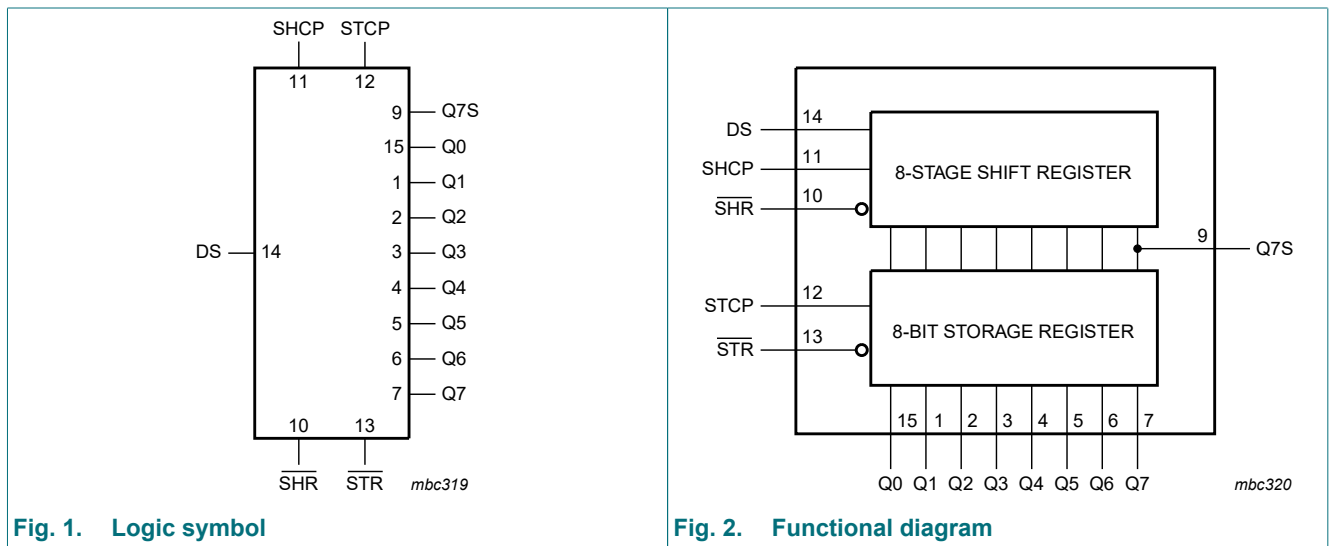
- Serial-to-parallel data conversion
- Remote control holding register

## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC594AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC594APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC594ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

## 5. Functional diagram



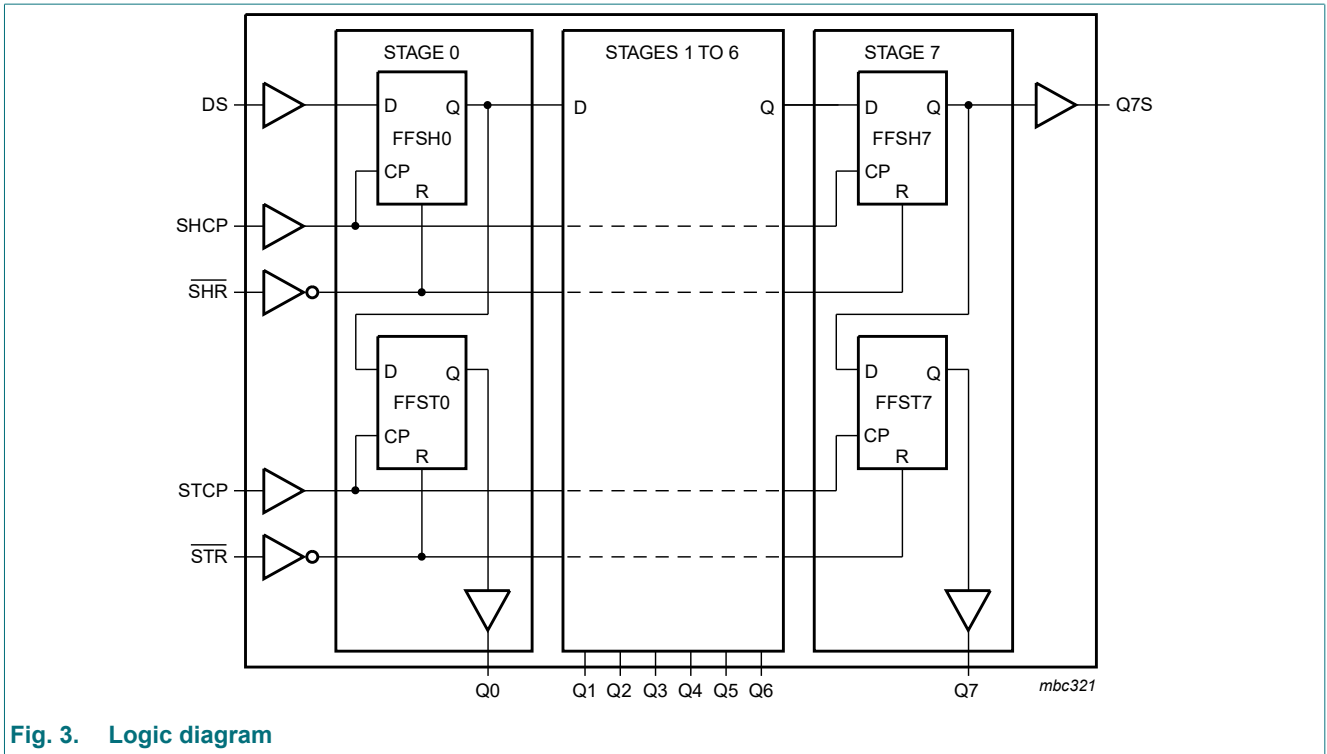


Fig. 3. Logic diagram

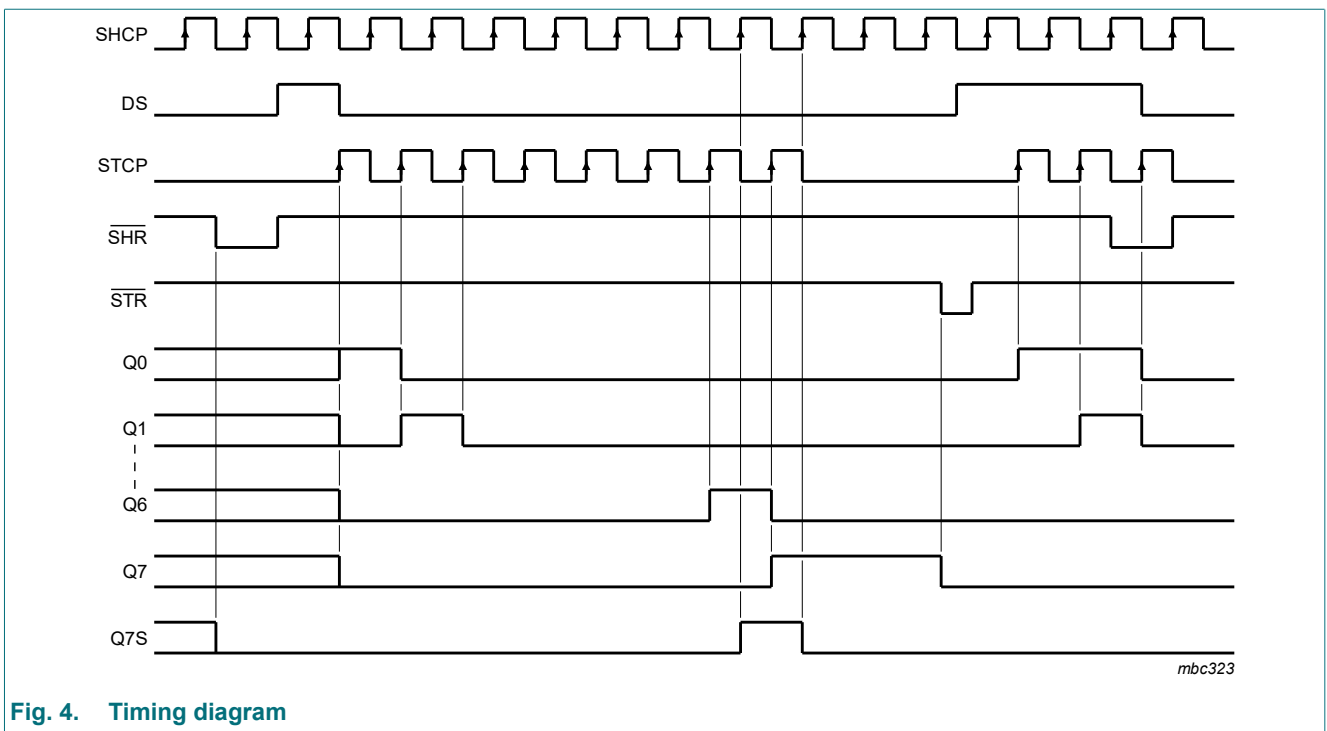
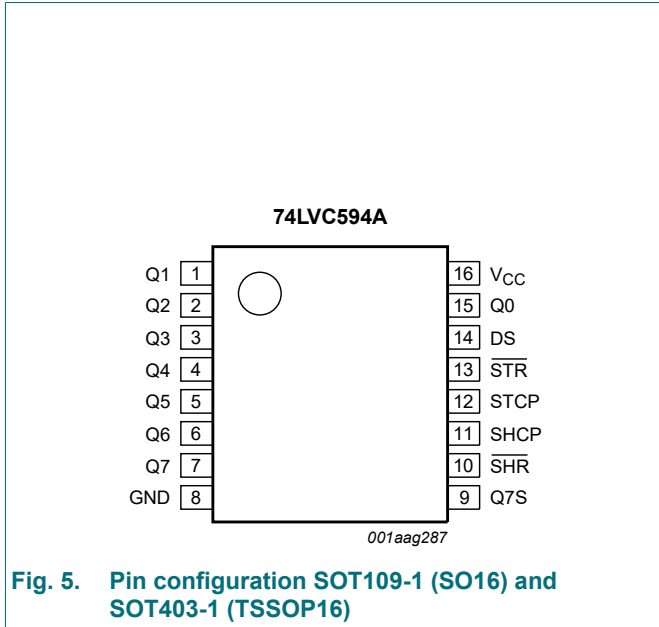


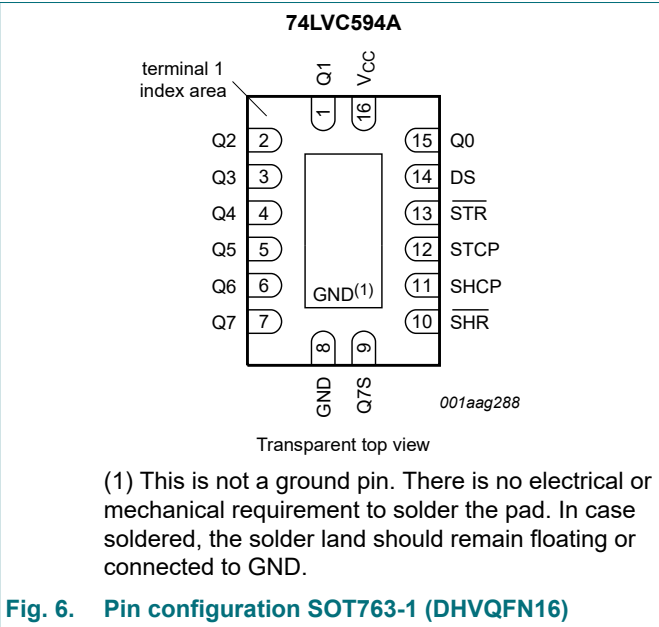
Fig. 4. Timing diagram

## 6. Pinning information

### 6.1. Pinning



**Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)**



**Fig. 6. Pin configuration SOT763-1 (DHVQFN16)**

### 6.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
SHR	10	shift register reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
STR	13	storage register reset (active LOW)
DS	14	serial data input
V <sub>CC</sub>	16	supply voltage

## 7. Functional description

**Table 3. Function table**

*H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change*

Input					Output		Function
SHCP	STCP	SHR	STR	DS	Q7S	Qn	
X	X	L	X	X	L	NC	a LOW-state on $\overline{\text{SHR}}$ only affects the shift register
X	X	X	L	X	NC	L	a LOW-state on $\overline{\text{STR}}$ only affects the storage register
X	↑	L	H	X	L	L	empty shift register loaded into storage register
↑	X	H	X	H	Q6S	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S)
X	↑	H	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	H	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	3-state [1]	-0.5	6.5	V
		output HIGH or LOW state [1]	-0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	3-state	0	-	5.5	V
		output HIGH or LOW state	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	-	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	10	ns/V

## 10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> -0.2	-	-	V <sub>CC</sub> -0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V

8-bit shift register with output register

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	0.1	10	-	20	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	-	40	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 1.65 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	µA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 13.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	SHCP to Q7S; see Fig. 7 [2] [3]						
		V <sub>CC</sub> = 1.2 V	-	17.5	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	5.2	15.8	2.0	18.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.2	8.1	1.5	9.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.5	7.6	1.5	8.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	3.1	6.7	1.5	7.7	ns
		STCP to Qn; see Fig. 8 [2]						
		V <sub>CC</sub> = 1.2 V	-	19.3	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	7.6	15.8	2.0	18.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.8	8.1	1.5	9.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	5.2	7.6	1.5	8.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	4.5	6.7	1.2	7.7	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	SHR to Q7S; see Fig. 11						
		V <sub>CC</sub> = 1.2 V	-	12.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	5.0	15.8	2.0	18.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.8	8.1	1.5	9.3	ns
		V <sub>CC</sub> = 2.7 V	1.2	3.9	7.6	1.2	8.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	3.3	6.7	1.2	7.7	ns
		STR to Qn; see Fig. 12						
		V <sub>CC</sub> = 1.2 V	-	20.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.0	7.7	15.8	2.0	18.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	5.0	8.1	1.5	9.3	ns
		V <sub>CC</sub> = 2.7 V	1.2	5.3	7.6	1.2	8.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	4.4	6.7	1.2	7.7	ns

## 8-bit shift register with output register

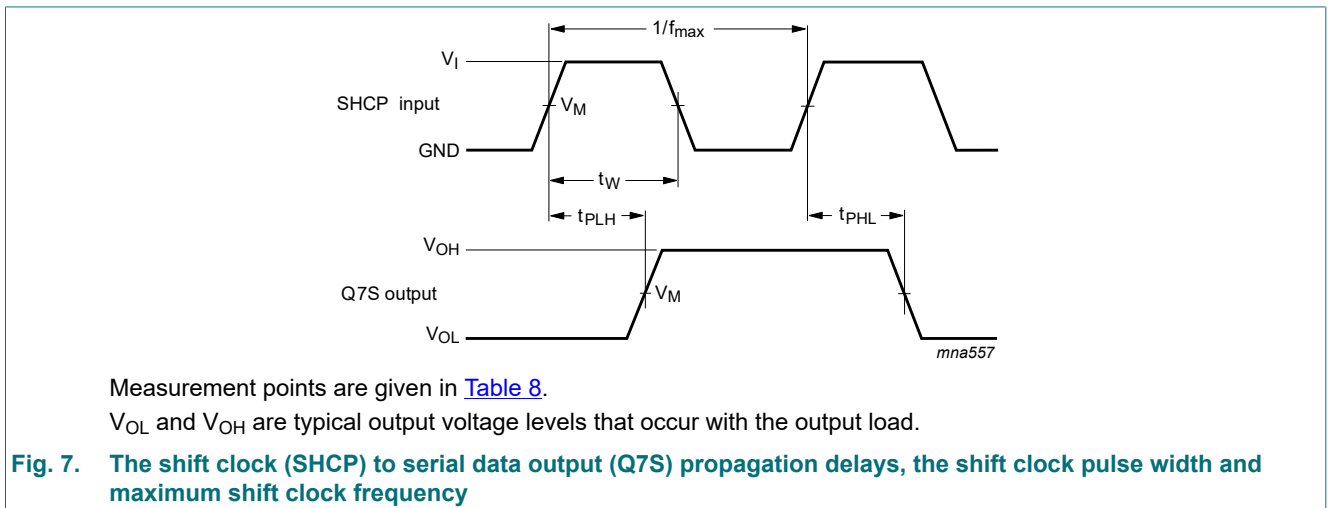
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_w$	pulse width	SHCP, STCP HIGH or LOW; see <a href="#">Fig. 7</a> and <a href="#">Fig. 8</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.0	2.5	-	7.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	5.0	2.0	-	5.5	-	ns
		$V_{CC} = 2.7\text{ V}$	4.5	1.5	-	5.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	1.5	-	4.5	-	ns
		SHR, STR LOW; see <a href="#">Fig. 11</a> and <a href="#">Fig. 12</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	6.0	2.5	-	5.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.0	2.0	-	4.5	-	ns
		$V_{CC} = 2.7\text{ V}$	2.5	1.5	-	3.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.5	1.5	-	3.0	-	ns
$t_{su}$	set-up time	DS to SHCP; see <a href="#">Fig. 9</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	5.0	1.0	-	5.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.0	0.8	-	4.5	-	ns
		$V_{CC} = 2.7\text{ V}$	2.0	0.6	-	2.5	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	0.6	-	2.5	-	ns
		SHR to STCP; see <a href="#">Fig. 10</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	8.0	3.5	-	8.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	5.0	2.1	-	5.5	-	ns
		$V_{CC} = 2.7\text{ V}$	4.0	1.8	-	4.5	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	1.7	-	4.5	-	ns
		SHCP to STCP; see <a href="#">Fig. 8</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	8.0	3.5	-	8.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	5.0	2.1	-	5.5	-	ns
		$V_{CC} = 2.7\text{ V}$	4.0	1.8	-	4.5	-	ns
$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	1.7	-	4.5	-	ns		
$t_h$	hold time	DS to SHCP; see <a href="#">Fig. 9</a> [3]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	1.5	0.2	-	2.0	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.5	0.1	-	2.0	-	ns
		$V_{CC} = 2.7\text{ V}$	1.5	-0.1	-	2.0	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	-0.2	-	1.5	-	ns
$t_{rec}$	recovery time	SHR to SHCP, STR to STCP; see <a href="#">Fig. 11</a> and <a href="#">Fig. 12</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	5.0	-2.7	-	5.5	-	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	4.0	-1.5	-	4.5	-	ns
		$V_{CC} = 2.7\text{ V}$	2.0	-1.0	-	2.5	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-1.0	-	2.5	-	ns
$f_{max}$	maximum frequency	SHCP or STCP; see <a href="#">Fig. 7</a> and <a href="#">Fig. 8</a>						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	80	130	-	70	-	MHz
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	100	140	-	90	-	MHz
		$V_{CC} = 2.7\text{ V}$	110	150	-	100	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	130	180	-	115	-	MHz

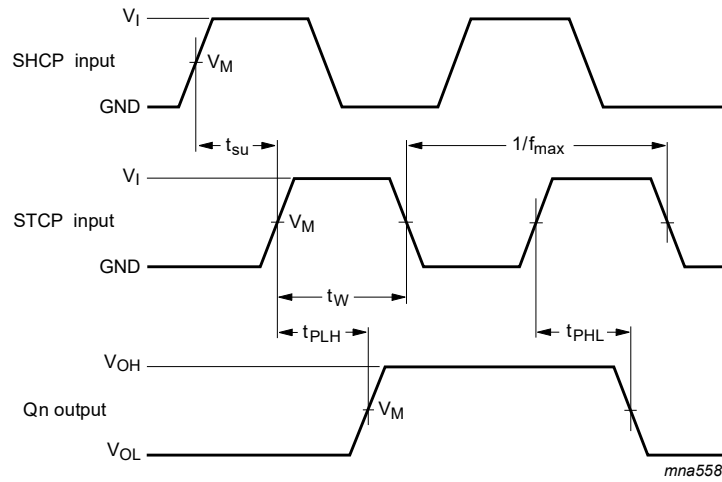


Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [4]	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [5]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	50	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	45	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	44	-	-	-	pF

- [1] Typical values are measured at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V},$  and  $3.3\text{ V}$  respectively.
- [2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [3] Cascadability is guaranteed under identical  $V_{CC}$  and temperature conditions.
- [4] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $N$  = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 11.1. Waveforms and test circuit

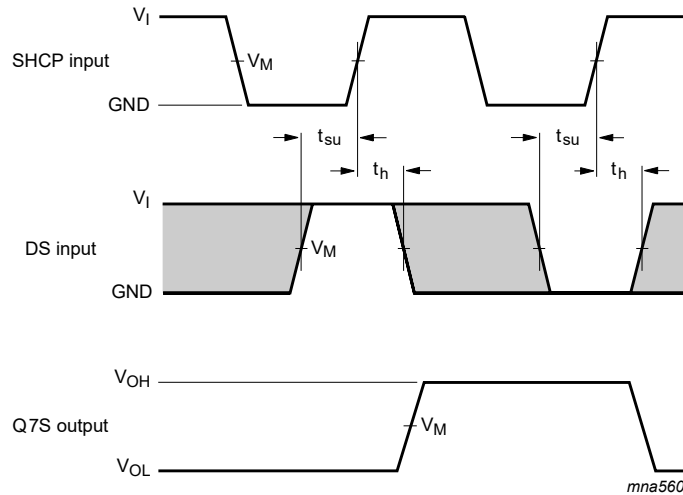




Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 8.** The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time

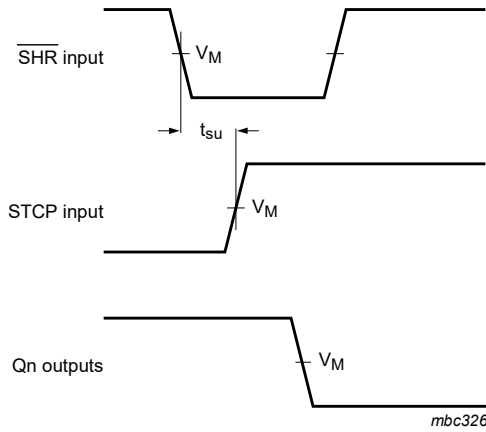


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

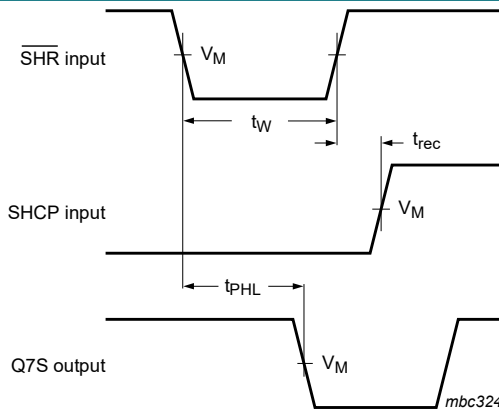
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 9.** The data set-up and hold times for the serial data input (DS)



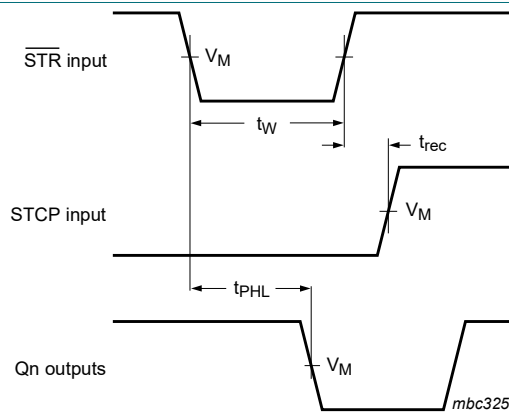
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 10. The shift reset ( $\overline{SHR}$ ) to storage clock (STCP) set-up times**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 11. The shift reset ( $\overline{SHR}$ ) pulse width, the shift reset to serial data output (Q7S) propagation delays and the shift reset to shift clock (SHCP) recovery time**

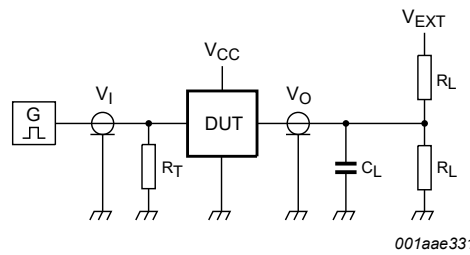
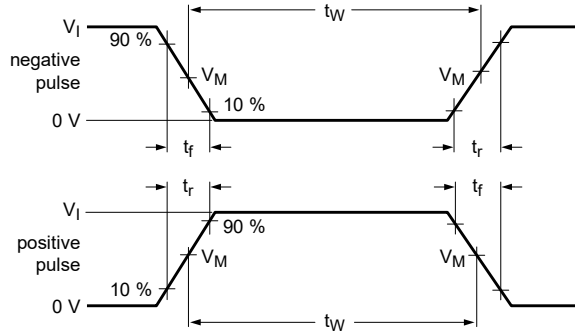


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 12. The storage reset ( $\overline{STR}$ ) pulse width, the storage reset to parallel data output (Qn) propagation delays and the storage reset to storage clock (STCP) recovery time**

Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
$V_{CC} < 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
$V_{CC} \geq 2.7\text{ V}$	1.5 V	1.5 V



Test data is given in [Table 9](#). Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

Fig. 13. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2\text{ ns}$	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2\text{ ns}$	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2\text{ ns}$	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5\text{ ns}$	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

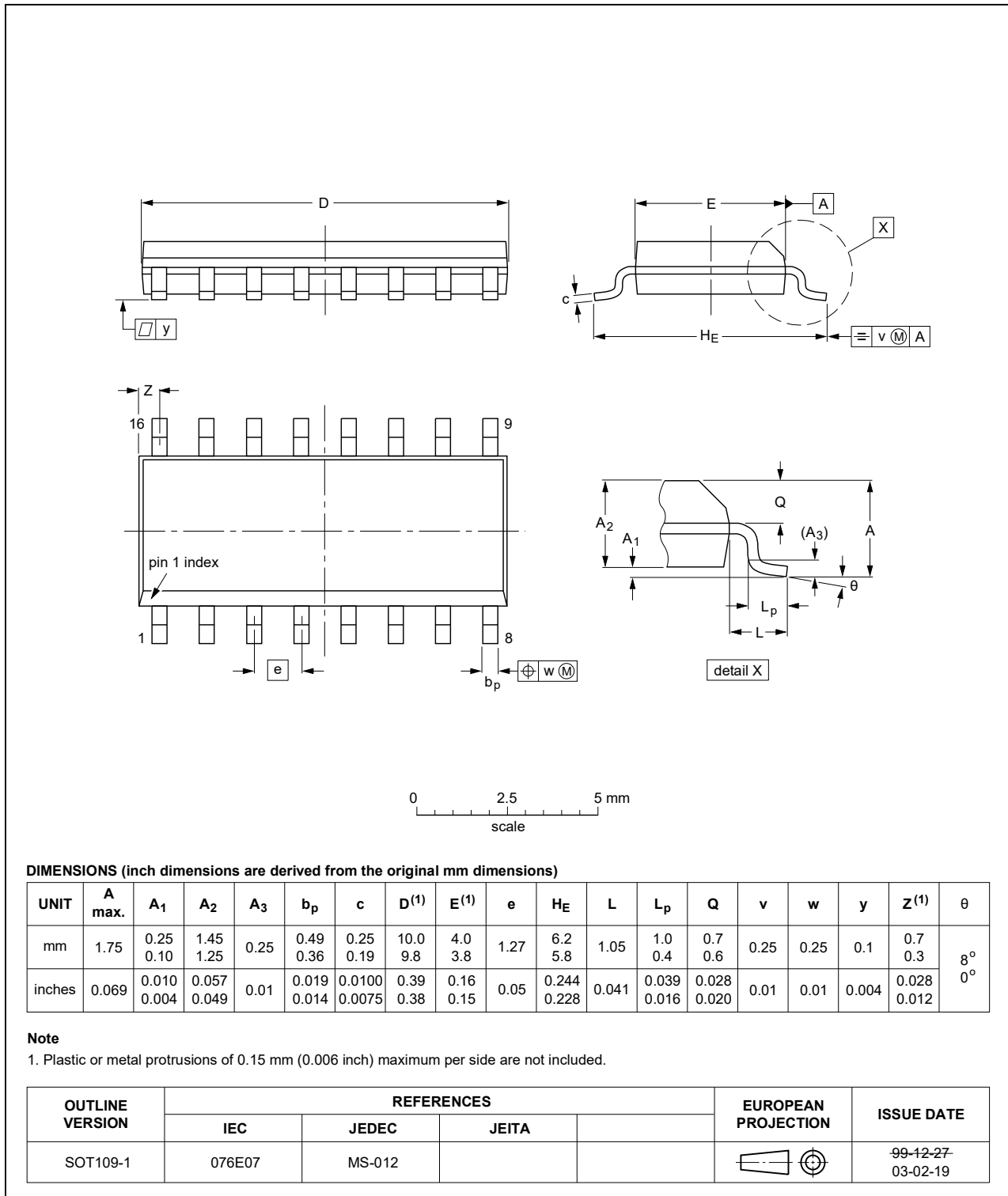


Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

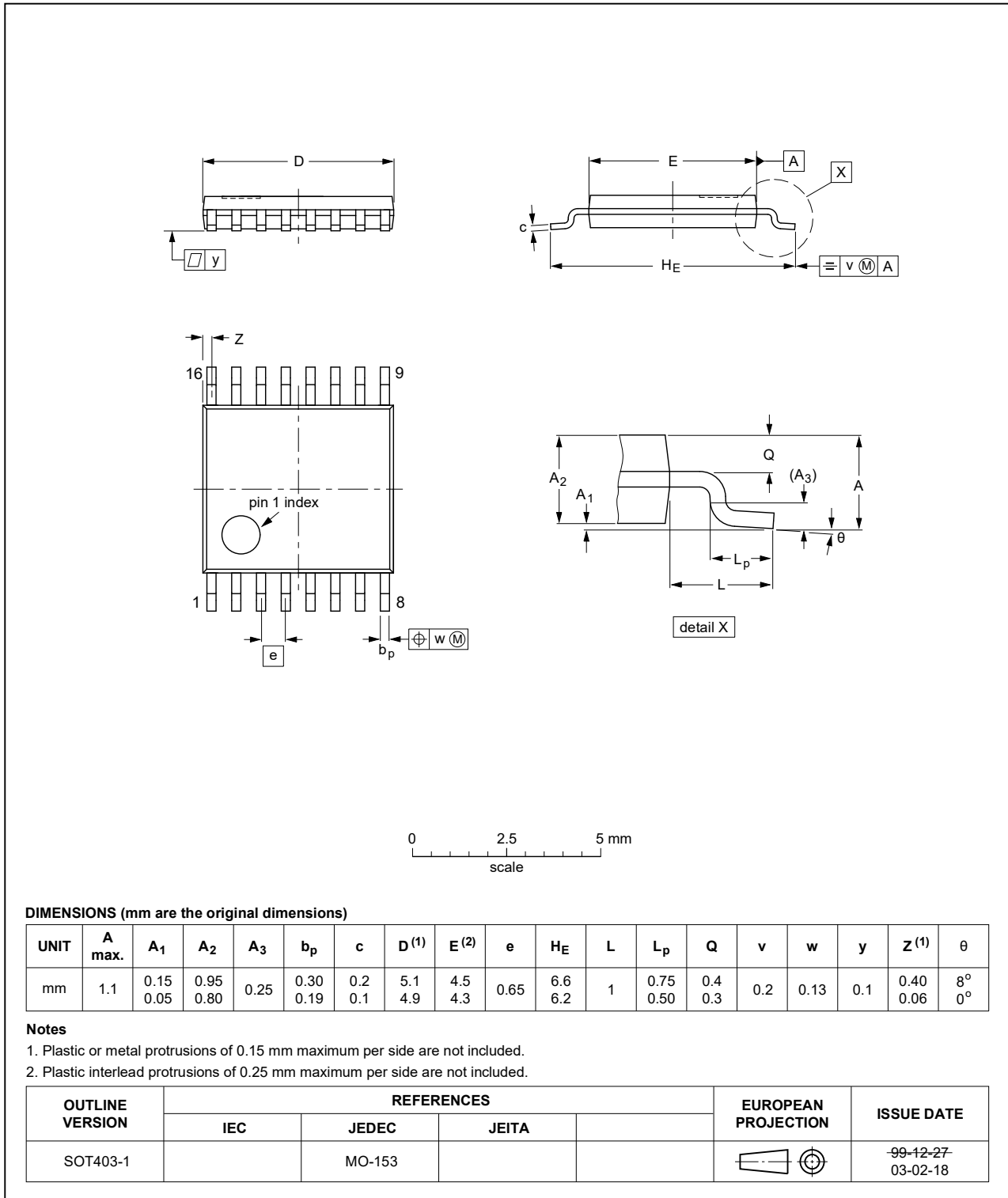


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

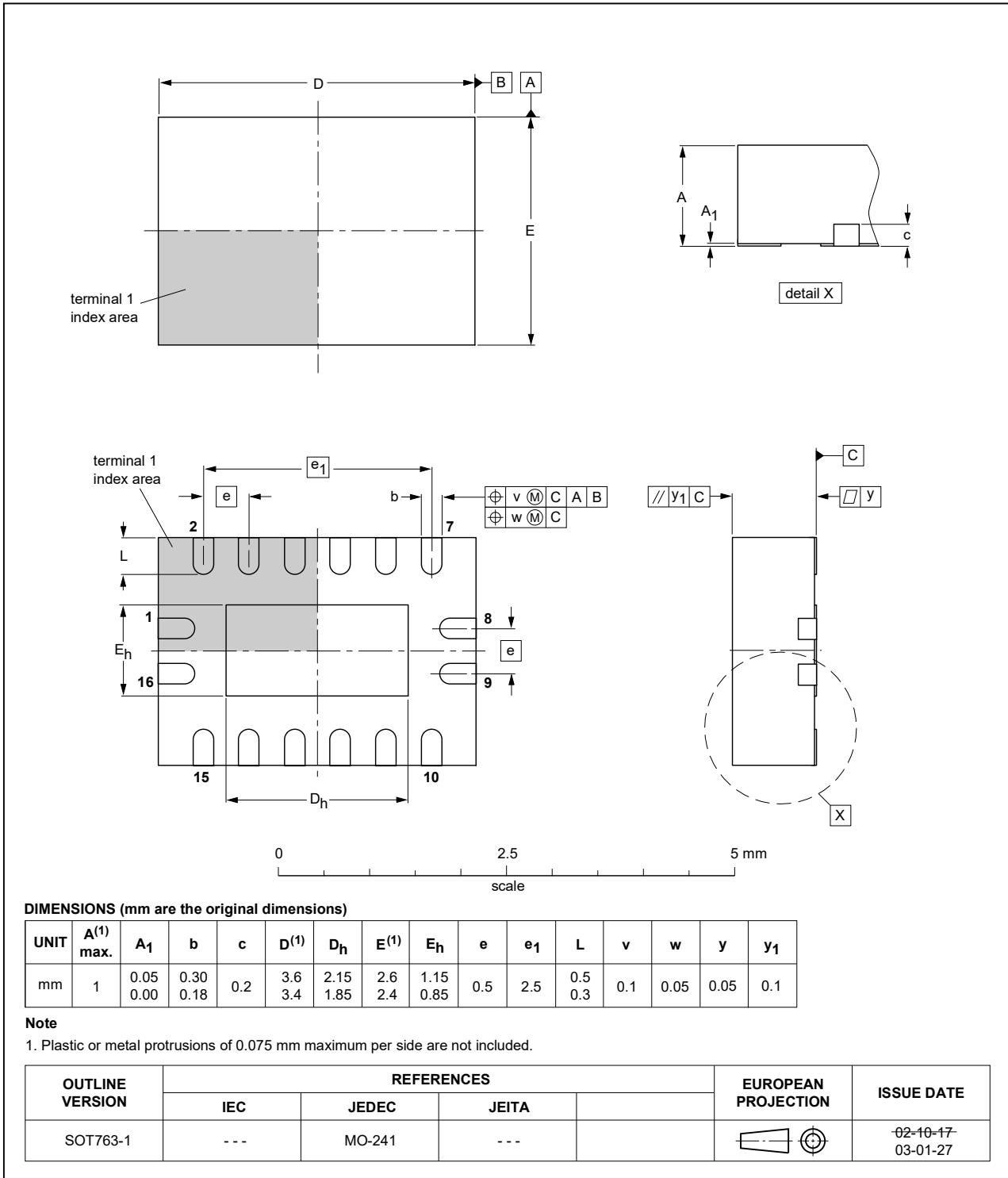


Fig. 16. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC594A v.4	20200903	Product data sheet	-	74LVC594A v.3
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• <a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74LVC594A v.3	20170720	Product data sheet	-	74LVC594A v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 7</a>: table note added for cascading purposes.</li> </ul>			
74LVC594A v.2	20131021	Product data sheet	-	74LVC594A v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVC594A v.1	20070524	Product data sheet	-	-



## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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