

# 74HC2G66; 74HCT2G66

## Dual single-pole single-throw analog switch

Rev. 11 — 6 November 2018

Product data sheet

### 1. General description

The 74HC2G66; 74HCT2G66 is a dual single pole, single-throw analog switch. Each switch has two input/output terminals (nY and nZ) and a digital enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 10.0 V for 74HC2G66
- Very low ON resistance:
  - 41  $\Omega$  (typ.) at  $V_{CC} = 4.5$  V
  - 30  $\Omega$  (typ.) at  $V_{CC} = 6.0$  V
  - 21  $\Omega$  (typ.) at  $V_{CC} = 9.0$  V
- High noise immunity
- Low power dissipation
- 25 mA continuous switch current
- Multiple package options
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC2G66DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HCT2G66DP				
74HC2G66DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74HCT2G66DC				
74HC2G66GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74HCT2G66GT				

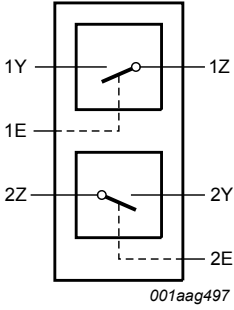
### 4. Marking

Table 2. Marking codes

Type number	Marking [1]
74HC2G66DP	H66
74HCT2G66DP	T66
74HC2G66DC	H66
74HCT2G66DC	T66
74HC2G66GT	H66
74HCT2G66GT	T66

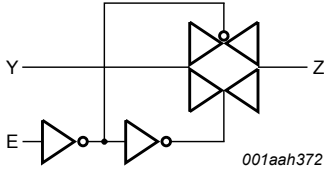
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram



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**Fig. 1. Logic symbol**

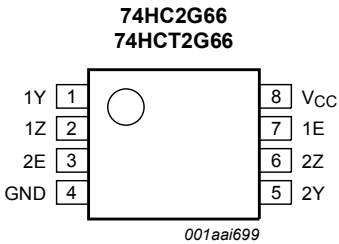


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**Fig. 2. Logic diagram for 1 switch**

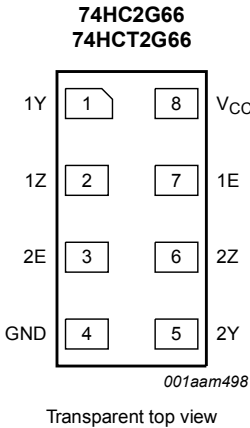
### 6. Pinning information

#### 6.1. Pinning



001aai699

**Fig. 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)**



001aam498

Transparent top view

**Fig. 4. Pin configuration SOT833-1 (XSON8)**

## 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1Y, 2Y	1, 5	independent input or output
1Z, 2Z	2, 6	independent input or output
GND	4	ground (0 V)
1E, 2E	7, 3	enable input (active HIGH)
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
L	OFF
H	ON

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+11.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>SK</sub>	switch clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V [1]	-	±20	mA
I <sub>SW</sub>	switch current	V <sub>SW</sub> > -0.5 V or V <sub>SW</sub> < V <sub>CC</sub> + 0.5 V	-	±20	mA
I <sub>CC</sub>	supply current		-	30	mA
I <sub>GND</sub>	ground current		-30	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		per package [2]	-	300	mW
		per switch [2]	-	100	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 packages: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.  
 For VSSOP8 packages: above 110 °C the value of P<sub>tot</sub> derates linearly with 8.0 mW/K.  
 For XSON8 packages: above 118 °C the value of P<sub>tot</sub> derates linearly with 7.8 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G66			74HCT2G66			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_{SW}$	switch voltage	[1]	0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V
		$V_{CC} = 10.0\text{ V}$	-	-	35	-	-	-	ns/V

[1] To avoid drawing  $V_{CC}$  current out of pin nZ, when switch current flows in pin nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin nZ, no  $V_{CC}$  current will flow out of terminal nY. In this case there is no limit for the voltage drop across the switch, but the voltage at pins nY and nZ may not exceed  $V_{CC}$  or GND.

## 10. Static characteristics

**Table 7. Static characteristics**

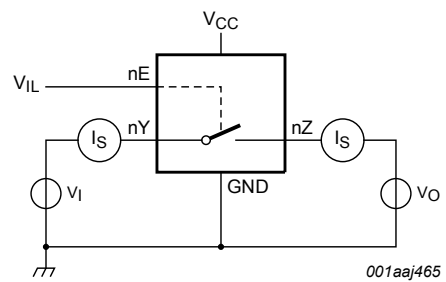
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
<b>74HC2G66</b>								
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	V
		$V_{CC} = 9.0\text{ V}$	6.3	4.7	-	6.3	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	V
		$V_{CC} = 9.0\text{ V}$	-	4.3	2.7	-	2.7	V
$I_I$	input leakage current	nE; $V_I = V_{CC}$ or GND						
		$V_{CC} = 6.0\text{ V}$	-	-	±0.1	-	±0.1	µA
		$V_{CC} = 9.0\text{ V}$	-	-	±0.2	-	±0.2	µA
$I_{S(OFF)}$	OFF-state leakage current	nY or nZ; $V_{CC} = 9.0\text{ V}$ ; see Fig. 5	-	0.1	1.0	-	1.0	µA
$I_{S(ON)}$	ON-state leakage current	nY or nZ; $V_{CC} = 9.0\text{ V}$ ; see Fig. 6	-	0.1	1.0	-	1.0	µA
$I_{CC}$	supply current	nE, nY and nZ = $V_{CC}$ or GND						
		$V_{CC} = 6.0\text{ V}$	-	-	10	-	20	µA
		$V_{CC} = 9.0\text{ V}$	-	-	20	-	40	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$C_I$	input capacitance		-	3.5	-	-	-	pF
$C_{PD}$	power dissipation capacitance		-	9	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF
<b>74HCT2G66</b>								
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	1.6	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	1.2	0.8	-	0.8	V
$I_I$	input leakage current	$nE; V_I = V_{CC}\text{ or GND}; V_{CC} = 5.5\text{ V}$	-	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{S(OFF)}$	OFF-state leakage current	$nY\text{ or }nZ; V_{CC} = 5.5\text{ V};$ see Fig. 5	-	0.1	1.0	-	1.0	$\mu\text{A}$
$I_{S(ON)}$	ON-state leakage current	$nY\text{ or }nZ; V_{CC} = 5.5\text{ V};$ see Fig. 6	-	0.1	1.0	-	1.0	$\mu\text{A}$
$I_{CC}$	supply current	$nE, nY\text{ and }nZ = V_{CC}\text{ or GND}; V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	10	-	20	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	$nE = V_{CC} - 2.1\text{ V}; I_O = 0\text{ A}; V_{CC} = 4.5\text{ V to }5.5\text{ V};$	-	-	375	-	410	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	-	-	pF
$C_{PD}$	power dissipation capacitance		-	9	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	8	-	-	-	pF

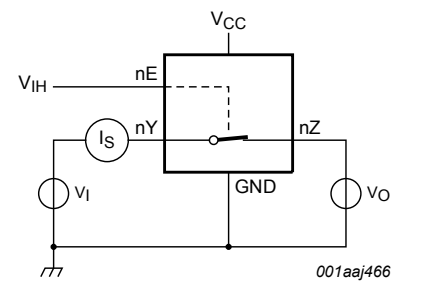
[1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ .

### 10.1. Test circuits



$V_I = V_{CC}\text{ or GND and }V_O = \text{GND or }V_{CC}.$

**Fig. 5. Test circuit for measuring OFF-state leakage current**



$V_I = V_{CC}\text{ or GND and }V_O = \text{open circuit.}$

**Fig. 6. Test circuit for measuring ON-state leakage current**

## 10.2. ON resistance

Table 8. ON resistance for 74HC2G66 and 74HCT2G66

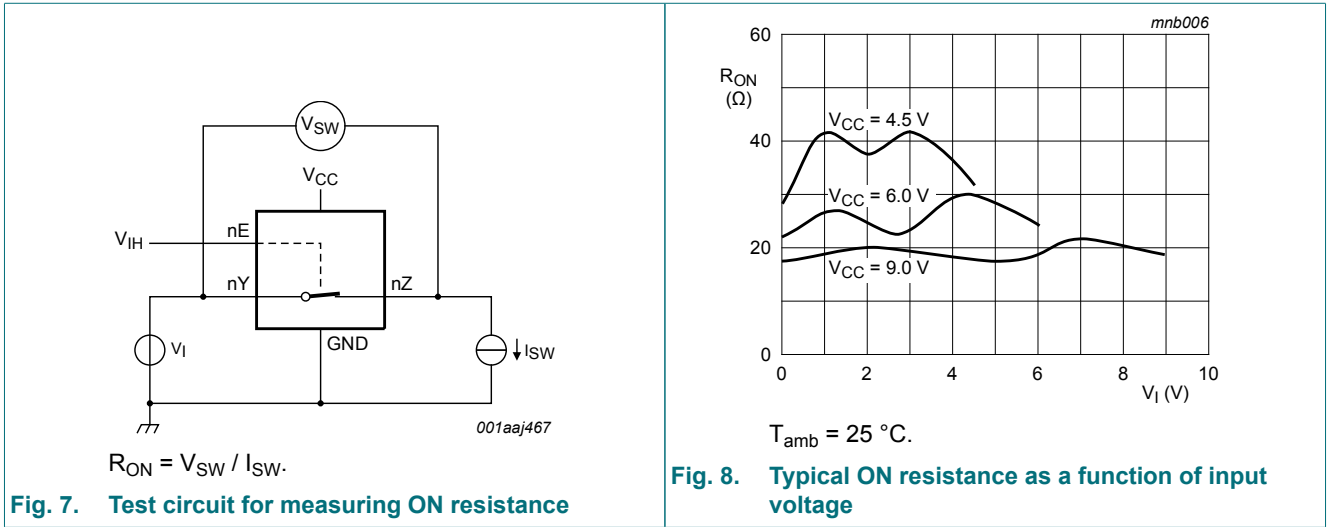
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see Fig. 8.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
<b>74HC2G66 [2]</b>								
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = GND to V <sub>CC</sub> ; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 0.1 mA; V <sub>CC</sub> = 2.0 V	-	250	-	-	-	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	41	118	-	142	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 6.0 V	-	30	105	-	126	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 9.0 V	-	21	88	-	105	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 0.1 mA; V <sub>CC</sub> = 2.0 V	-	65	-	-	-	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	28	95	-	115	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 6.0 V	-	22	82	-	100	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 9.0 V	-	18	70	-	80	Ω
		V <sub>I</sub> = V <sub>CC</sub> ; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 0.1 mA; V <sub>CC</sub> = 2.0 V	-	65	-	-	-	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	31	106	-	128	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 6.0 V	-	23	94	-	113	Ω
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 9.0 V	-	19	78	-	95	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = V <sub>CC</sub> to GND; see Fig. 7 and Fig. 8						
		V <sub>CC</sub> = 4.5 V	-	5	-	-	-	Ω
		V <sub>CC</sub> = 6.0 V	-	4	-	-	-	Ω
		V <sub>CC</sub> = 9.0 V	-	3	-	-	-	Ω
<b>74HCT2G66</b>								
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = GND to V <sub>CC</sub> ; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	41	118	-	142	Ω
R <sub>ON(rail)</sub>	ON resistance (rail)	V <sub>I</sub> = GND; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	28	95	-	115	Ω
		V <sub>I</sub> = V <sub>CC</sub> ; see Fig. 7 and Fig. 8						
		I <sub>SW</sub> = 1.0 mA; V <sub>CC</sub> = 4.5 V	-	31	106	-	128	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = V <sub>CC</sub> to GND; see Fig. 7 and Fig. 8						
		V <sub>CC</sub> = 4.5 V	-	5	-	-	-	Ω

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2] At supply voltages approaching 2 V, the ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

10.3. ON resistance test circuit and graphs



## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 11.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
<b>74HC2G66</b>								
t <sub>pd</sub>	propagation delay	nY to nZ or nZ to nY; R <sub>L</sub> = ∞ Ω; see Fig. 9 [2]						
		V <sub>CC</sub> = 2.0 V	-	6.5	65	-	80	ns
		V <sub>CC</sub> = 4.5 V	-	2	13	-	15	ns
		V <sub>CC</sub> = 6.0 V	-	1.5	11	-	14	ns
		V <sub>CC</sub> = 9.0 V	-	1.2	10	-	12	ns
t <sub>en</sub>	enable time	nE to nY or nZ; see Fig. 10 [2]						
		V <sub>CC</sub> = 2.0 V	-	40	125	-	150	ns
		V <sub>CC</sub> = 4.5 V	-	12	29	-	30	ns
		V <sub>CC</sub> = 6.0 V	-	10	21	-	26	ns
		V <sub>CC</sub> = 9.0 V	-	7	16	-	20	ns
t <sub>dis</sub>	disable time	nE to nY or nZ; see Fig. 10 [2]						
		V <sub>CC</sub> = 2.0 V	-	21	145	-	175	ns
		V <sub>CC</sub> = 4.5 V	-	12	29	-	35	ns
		V <sub>CC</sub> = 6.0 V	-	11	28	-	33	ns
		V <sub>CC</sub> = 9.0 V	-	10	23	-	27	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> [3]	-	9	-	-	-	pF
<b>74HCT2G66</b>								
t <sub>pd</sub>	propagation delay	nY to nZ or nZ to nY; R <sub>L</sub> = ∞ Ω; V <sub>CC</sub> = 4.5 V; see Fig. 9 [2]	-	2	15	-	18	ns
t <sub>en</sub>	enable time	nE to nY or nZ; V <sub>CC</sub> = 4.5; see Fig. 10 [2]	-	13	30	-	36	ns
t <sub>dis</sub>	disable time	nE to nY or nZ; V <sub>CC</sub> = 4.5 V; see Fig. 10 [2]	-	13	44	-	53	ns
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V [3]	-	9	-	-	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation P<sub>D</sub> (μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

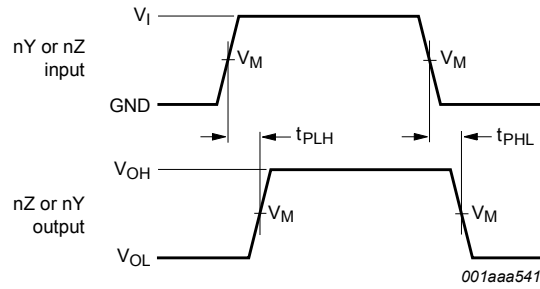
C<sub>SW</sub> = maximum switch capacitance in pF (see Table 7);

V<sub>CC</sub> = supply voltage in volts;

$\Sigma((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$  = sum of outputs.



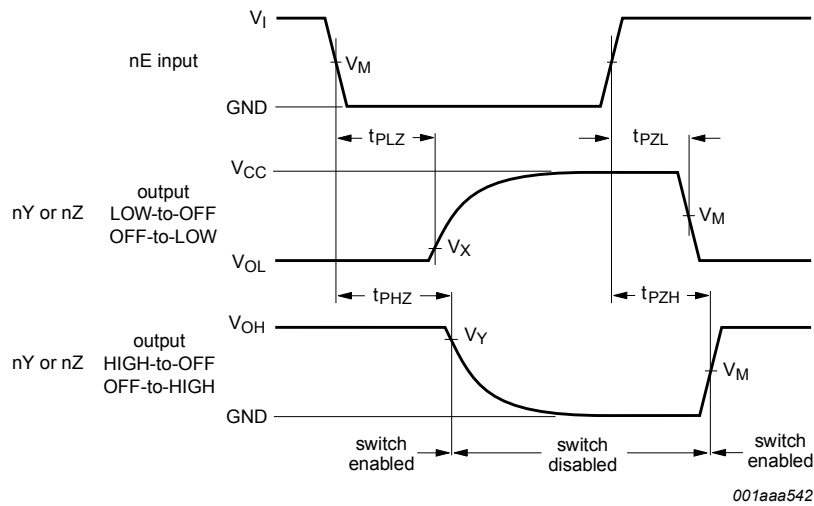
11.1. Waveforms and test circuit



Measurement points are given in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 9. Input (nY or nZ) to output (nZ or nY) propagation delays**



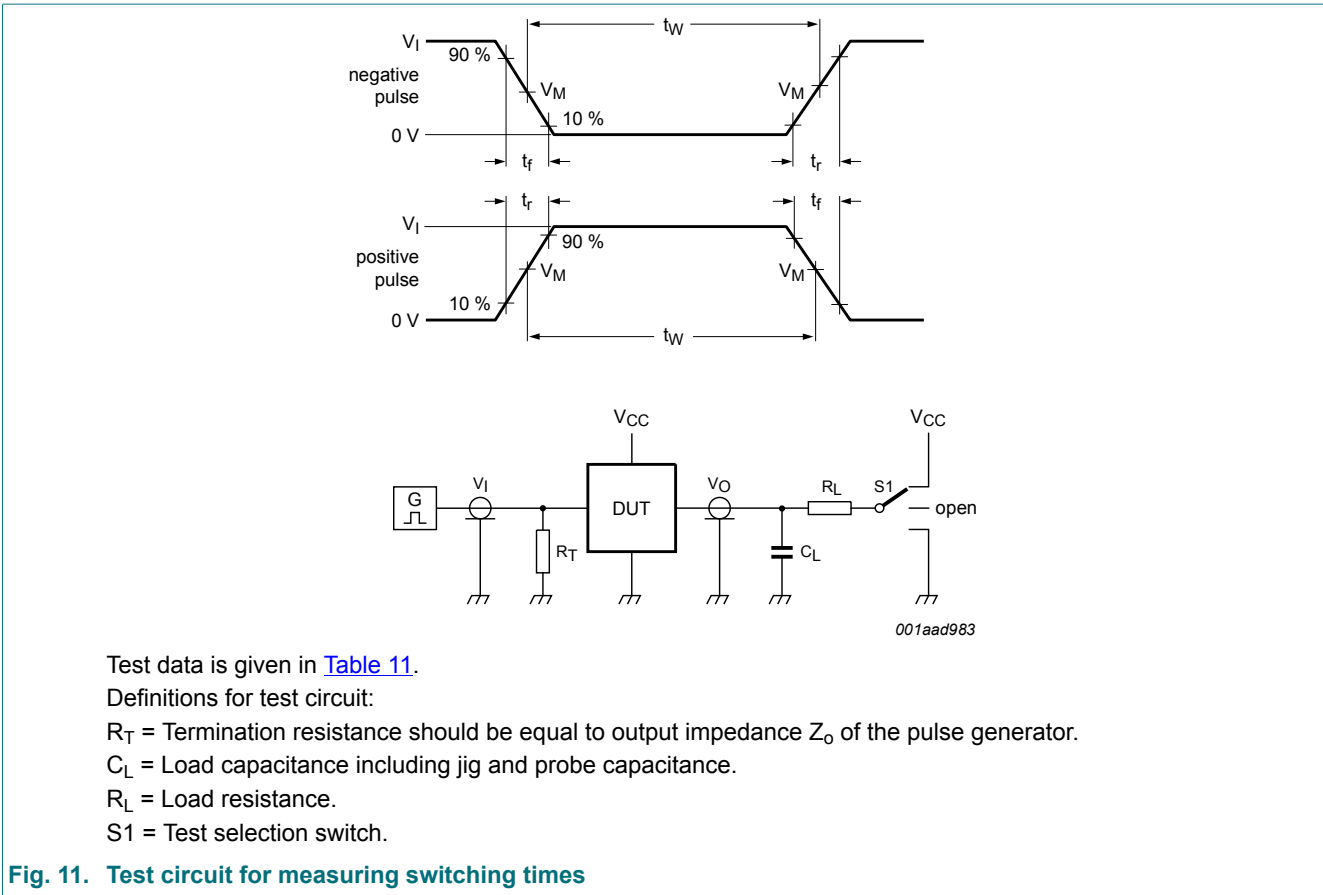
Measurement points are given in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 10. Enable and disable times**

**Table 10. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74HC2G66	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 10\%$	$V_{OH} - 10\%$
74HCT2G66	1.3 V	1.3 V	$V_{OL} + 10\%$	$V_{OH} - 10\%$



**Fig. 11. Test circuit for measuring switching times**

**Table 11. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$ [1]	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74HC2G66	GND to $V_{CC}$	6 ns	50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74HCT2G66	GND to 3 V	6 ns	50 pF	1 k $\Omega$	open	GND	$V_{CC}$

[1] There is no constraint on  $t_r, t_f$  with a 50 % duty factor when measuring  $f_{max}$ .

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74HC2G66 and 74HCT2G66

$GND = 0\text{ V}$ ;  $t_r = t_f = 6.0\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; unless otherwise specified. All typical values are measured at  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	$f_i = 1\text{ kHz}$ ; $R_L = 10\text{ k}\Omega$ ; see Fig. 12				
		$V_{CC} = 4.5\text{ V}$ ; $V_I = 4.0\text{ V (p-p)}$	-	0.04	-	%
		$V_{CC} = 9.0\text{ V}$ ; $V_I = 8.0\text{ V (p-p)}$	-	0.02	-	%
		$f_i = 10\text{ kHz}$ ; $R_L = 10\text{ k}\Omega$ ; see Fig. 12				
		$V_{CC} = 4.5\text{ V}$ ; $V_I = 4.0\text{ V (p-p)}$	-	0.12	-	%
		$V_{CC} = 9.0\text{ V}$ ; $V_I = 8.0\text{ V (p-p)}$	-	0.06	-	%
$f_{(-3\text{dB})}$	-3 dB frequency response	$R_L = 50\text{ }\Omega$ ; $C_L = 10\text{ pF}$ ; see Fig. 13 and Fig. 14				
		$V_{CC} = 4.5\text{ V}$	-	180	-	MHz
		$V_{CC} = 9.0\text{ V}$	-	200	-	MHz
$\alpha_{iso}$	isolation (OFF-state)	$R_L = 600\text{ }\Omega$ ; $f_i = 1\text{ MHz}$ ; see Fig. 15 and Fig. 16				
		$V_{CC} = 4.5\text{ V}$	-	-50	-	dB
		$V_{CC} = 9.0\text{ V}$	-	-50	-	dB
$V_{ct}$	crosstalk voltage	between digital input and switch (peak to peak value); $R_L = 600\text{ }\Omega$ ; $f_i = 1\text{ MHz}$ ; see Fig. 17				
		$V_{CC} = 4.5\text{ V}$	-	110	-	mV
		$V_{CC} = 9.0\text{ V}$	-	220	-	mV
Xtalk	crosstalk	between switches; $R_L = 600\text{ }\Omega$ ; $f_i = 1\text{ MHz}$ ; see Fig. 18				
		$V_{CC} = 4.5\text{ V}$	-	-60	-	dB
		$V_{CC} = 9.0\text{ V}$	-	-60	-	dB

11.3. Test circuits and graphs

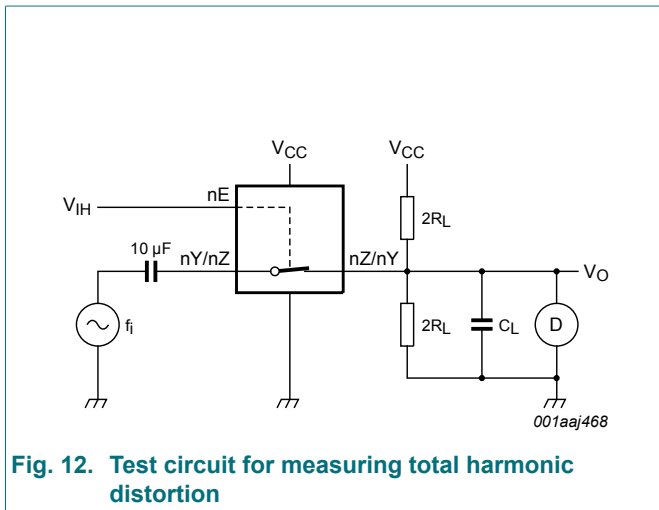


Fig. 12. Test circuit for measuring total harmonic distortion

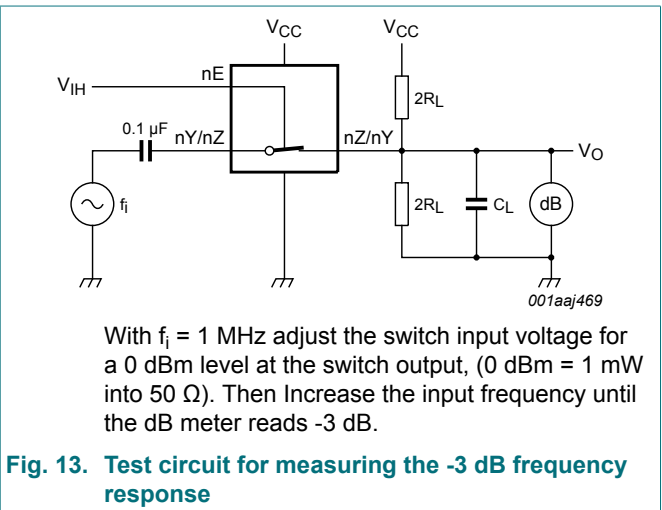
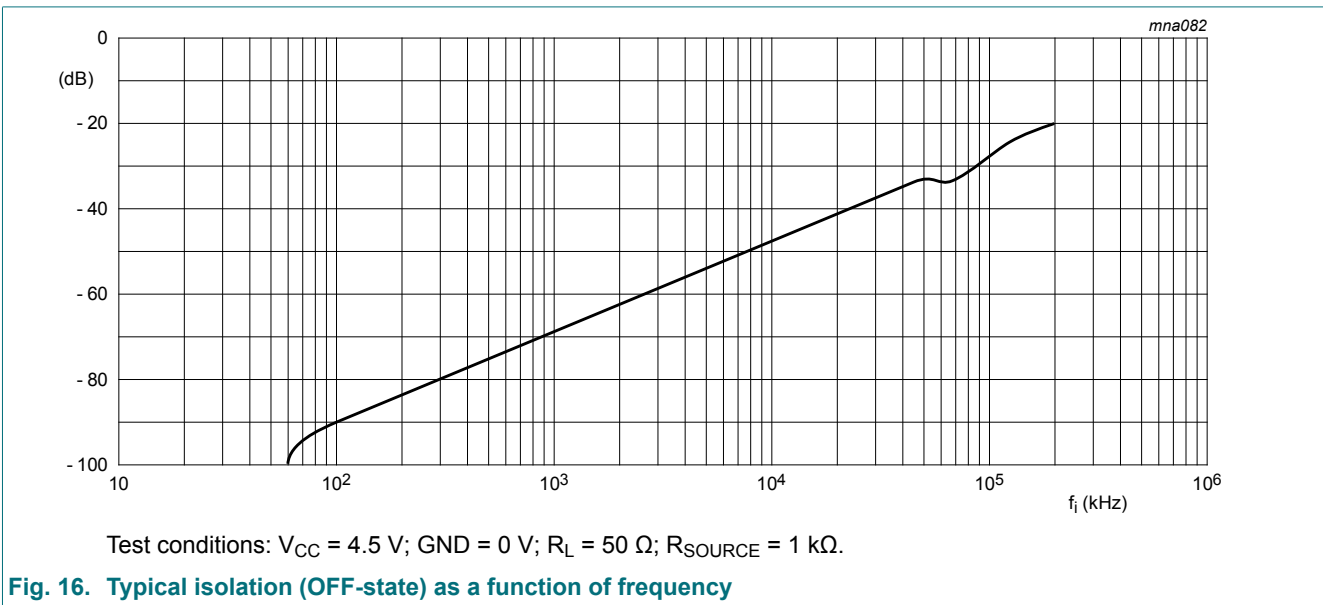
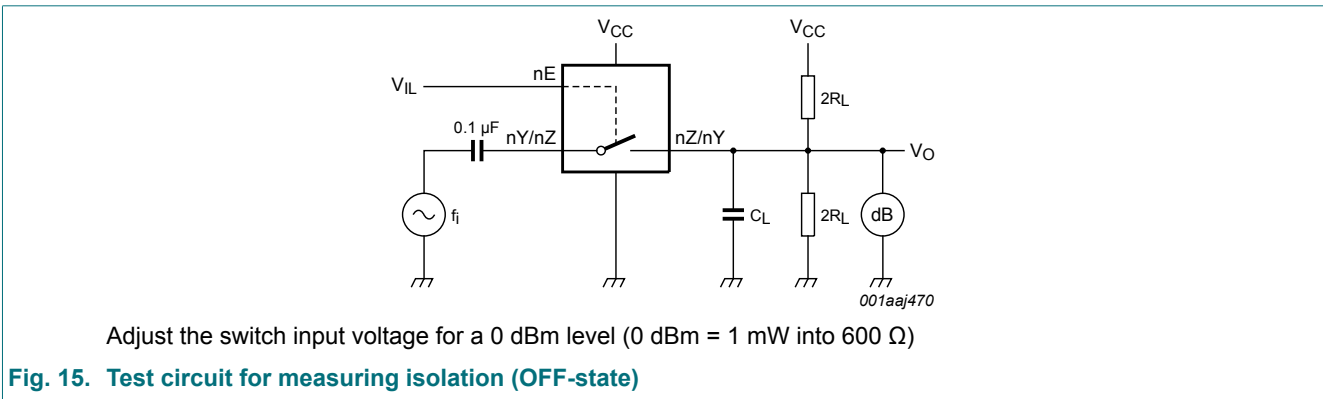
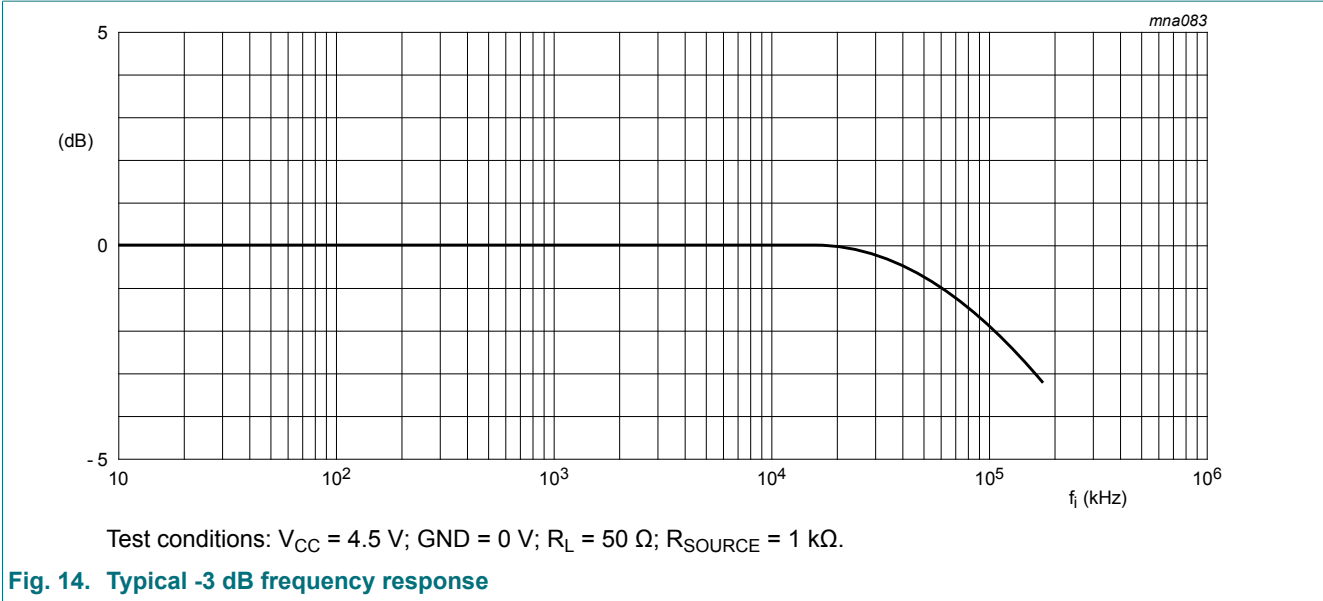
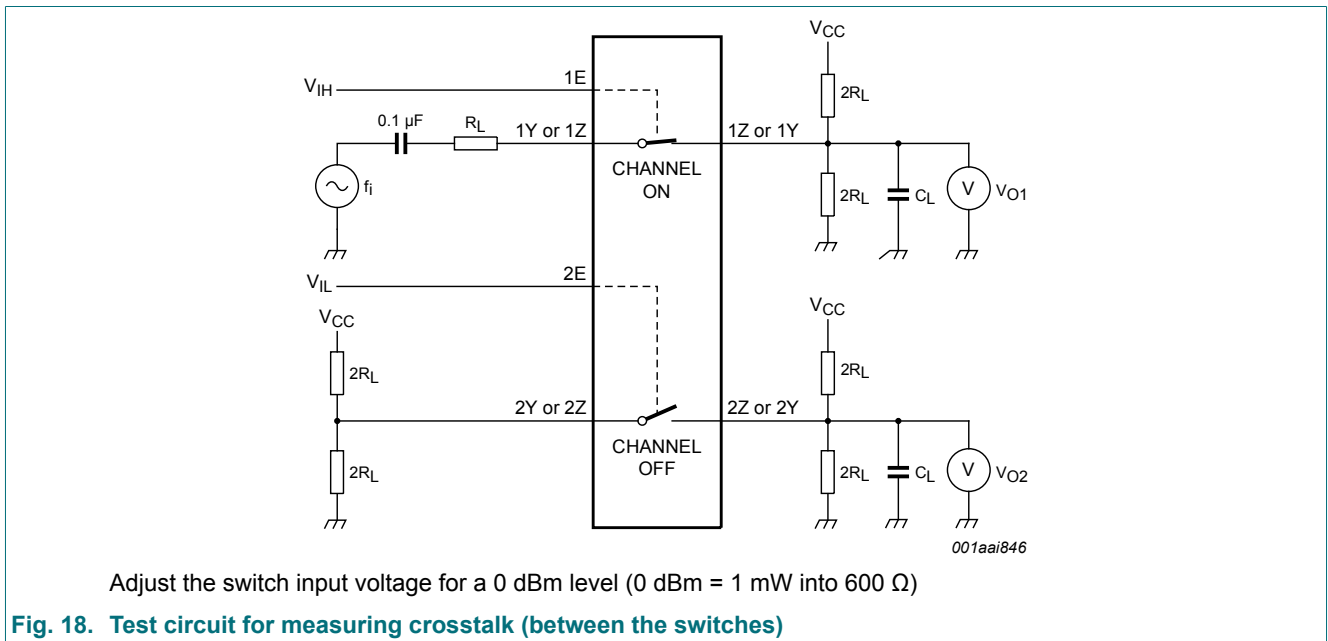
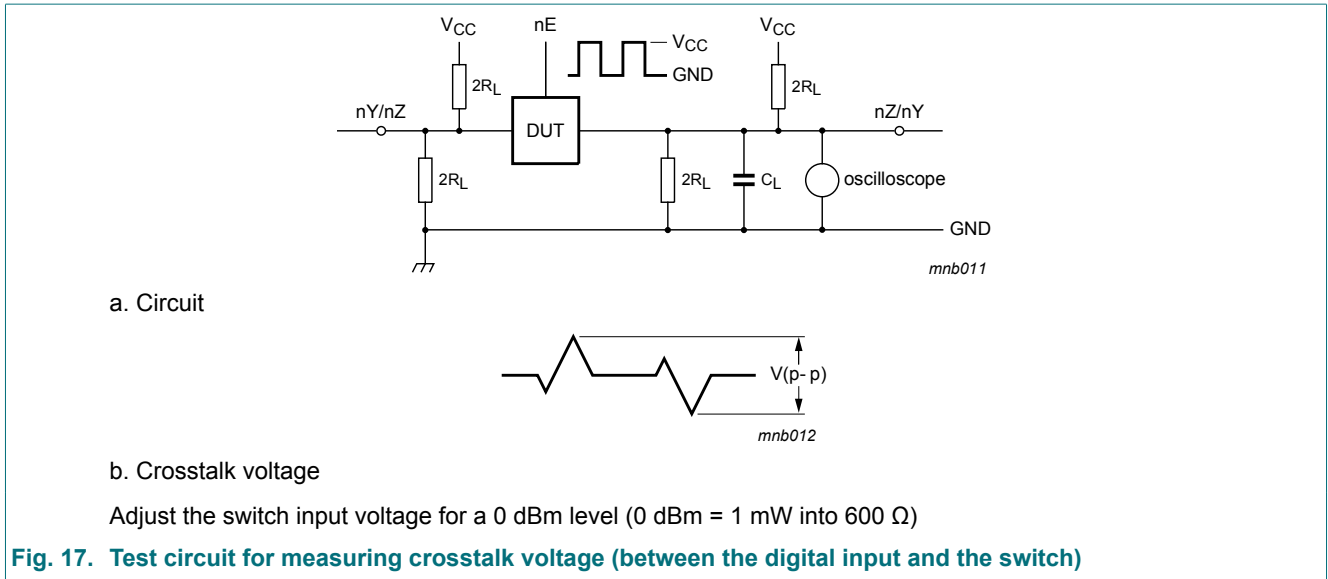


Fig. 13. Test circuit for measuring the -3 dB frequency response

With  $f_i = 1\text{ MHz}$  adjust the switch input voltage for a 0 dBm level at the switch output, (0 dBm = 1 mW into 50  $\Omega$ ). Then increase the input frequency until the dB meter reads -3 dB.





12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

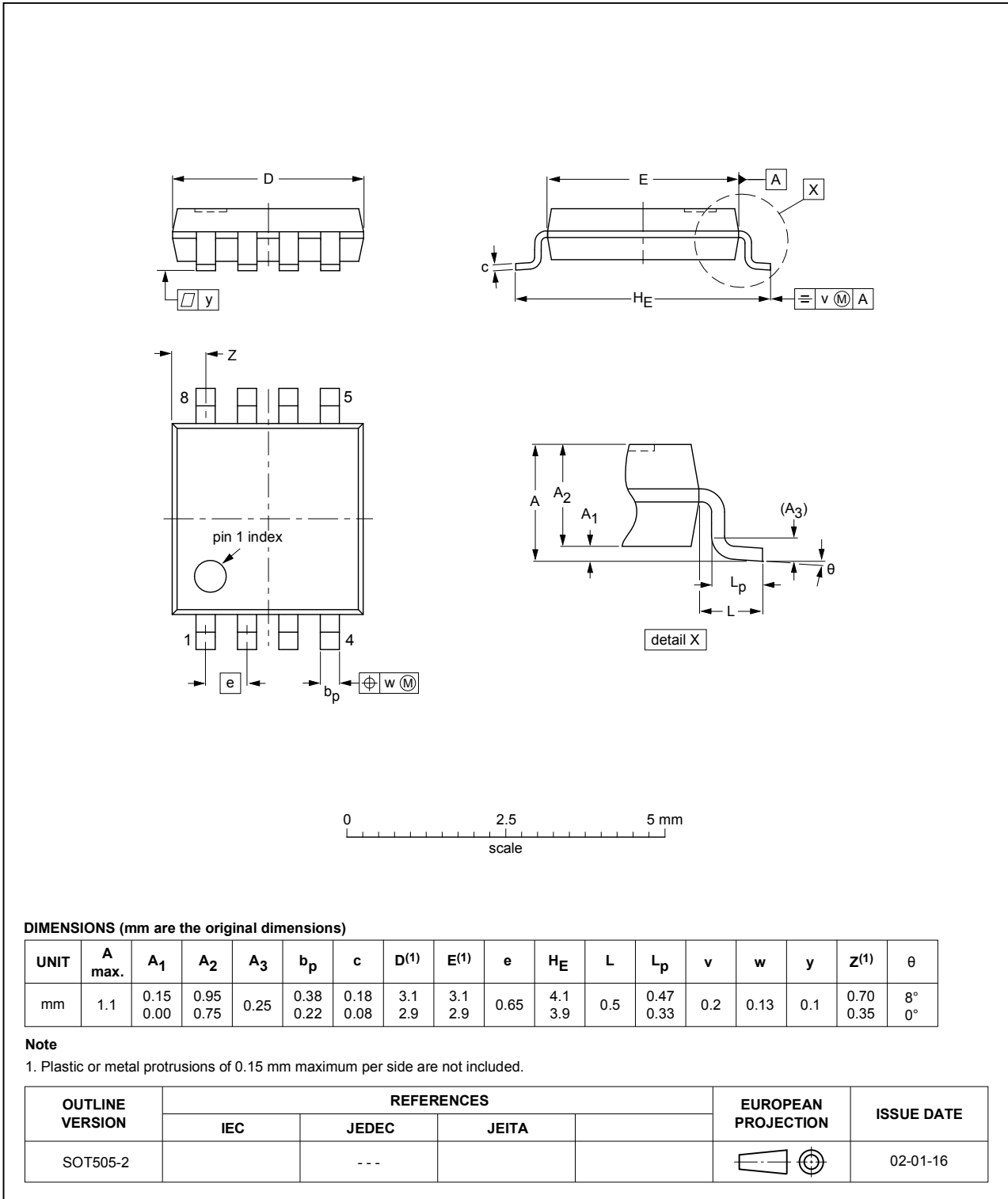


Fig. 19. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

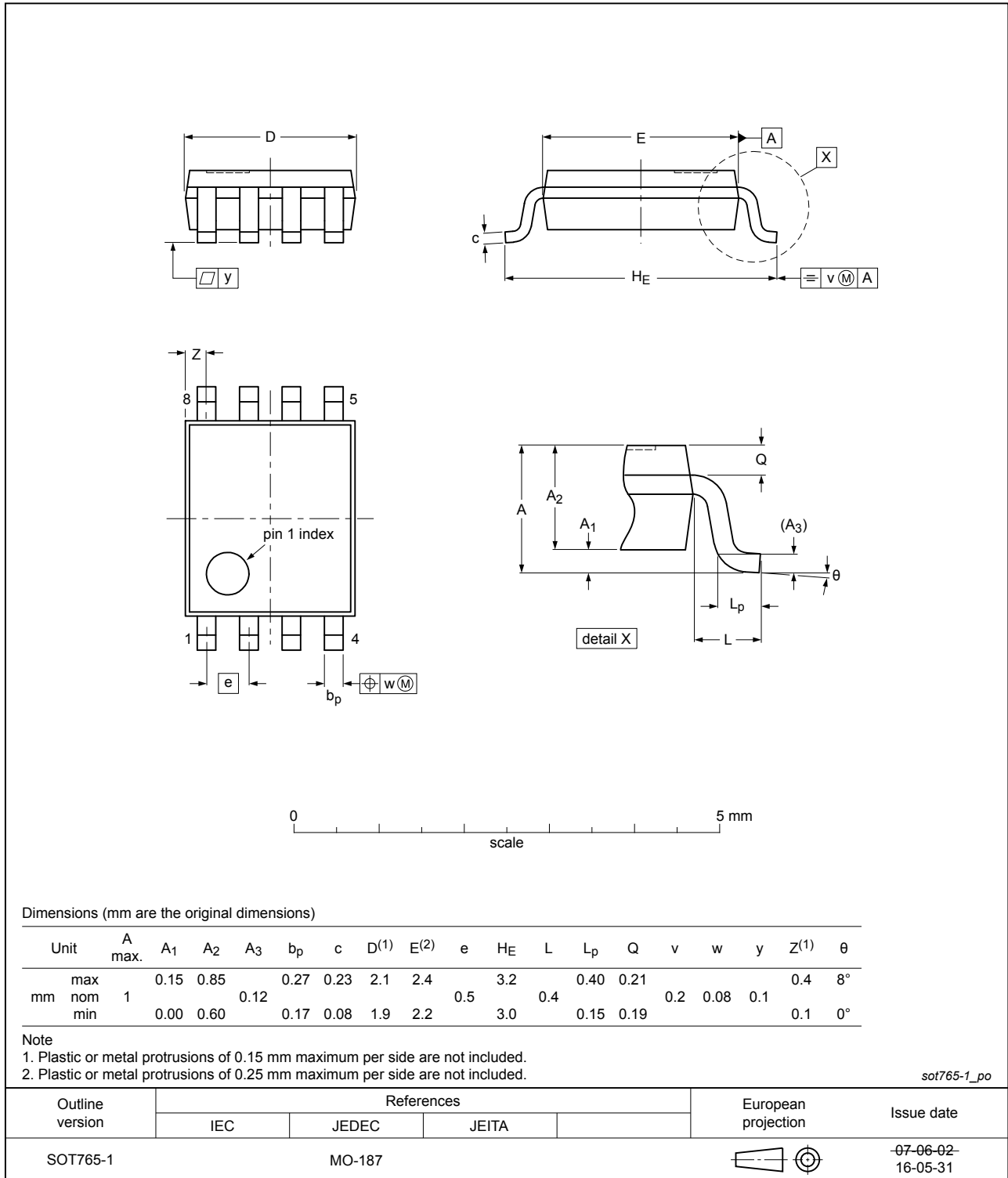


Fig. 20. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

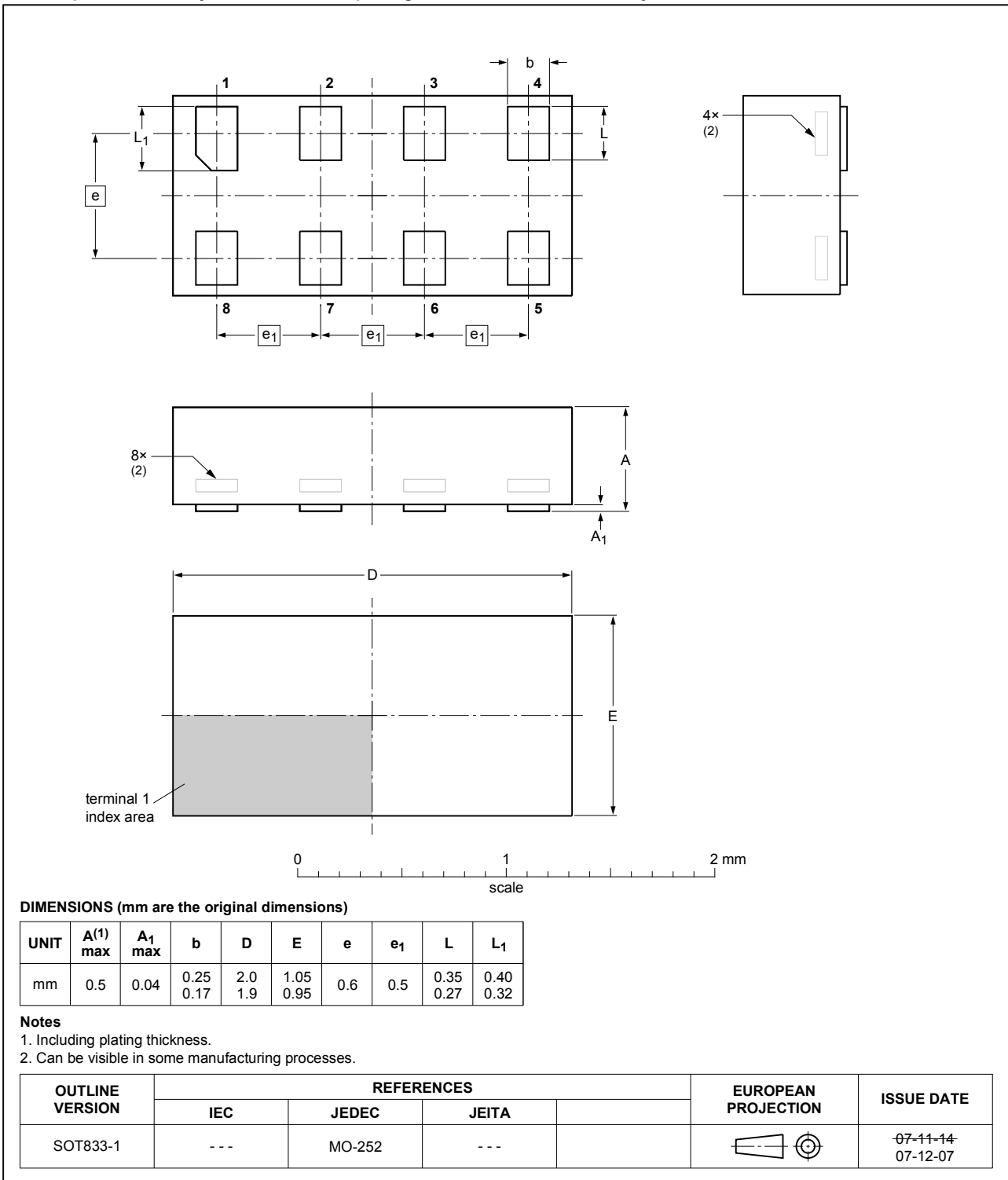


Fig. 21. Package outline SOT833-1 (XSON8)



## 13. Abbreviations

Table 13. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G66 v.11	20181106	Product data sheet	-	74HC_HCT2G66 v.10
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC2G66GD and 74HCT2G66GD (SOT996-2) removed.</li> <li>Corrected <a href="#">Fig. 2</a></li> <li>Package outline drawing <a href="#">SOT765-1</a> updated</li> </ul>			
74HC_HCT2G66 v.10	20131003	Product data sheet	-	74HC_HCT2G66 v.9
Modifications:	<ul style="list-style-type: none"> <li>For type numbers 74HC2G66GD and 74HCT2G66GD XSON8U has changed to XSON8.</li> </ul>			
74HC_HCT2G66 v.9	20111213	Product data sheet	-	74HC_HCT2G66 v.8
74HC_HCT2G66 v.8	20100923	Product data sheet	-	74HC_HCT2G66 v.7
74HC_HCT2G66 v.7	20100914	Product data sheet	-	74HC_HCT2G66 v.6
74HC_HCT2G66 v.6	20100402	Product data sheet	-	74HC_HCT2G66 v.5
74HC_HCT2G66 v.5	20090126	Product data sheet	-	74HC_HCT2G66 v.4
74HC_HCT2G66 v.4	20040519	Product specification	-	74HC_HCT2G66 v.3
74HC_HCT2G66 v.3	20031126	Product specification	-	74HC_HCT2G66 v.2
74HC_HCT2G66 v.2	20030808	Product specification	-	74HC_HCT2G66 v.1
74HC_HCT2G66 v.1	20030625	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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