

74HC240; 74HCT240

Octal buffer/line driver; 3-state; inverting

Rev. 03 — 2 August 2007

Product data sheet

1. General description

The 74HC240; 74HCT240 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL).

The 74HC240; 74HCT240 is a dual octal inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{1OE}$ and $\overline{2OE}$. A HIGH on \overline{nOE} causes the outputs to assume a high impedance OFF-state.

The 74HC240; 74HCT240 is similar to the 74HC244; 74HCT244 but has inverting outputs.

2. Features

- Inverting 3-state outputs
- Multiple package options
- Complies with JEDEC standard no. 7 A
- ESD protection:
 - ◆ HBM JESD22-A114-D exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

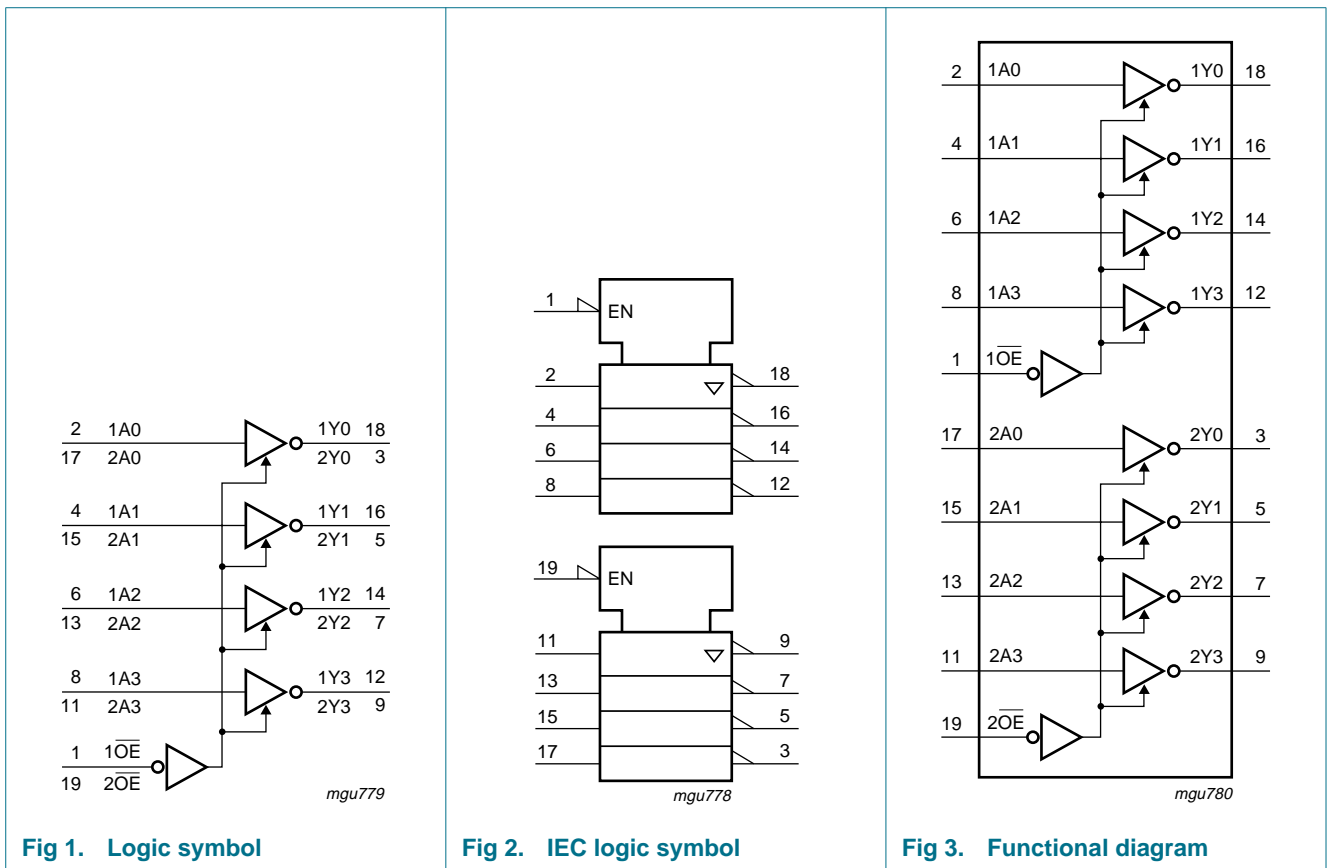
Table 1. Ordering information

| Type number | Package | | | |
|-----------------|---|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC240 | | | | |
| 74HC240N | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |
| 74HC240D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HC240DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74HC240PW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HC240BQ | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DHVQFN20 | plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm | SOT764-1 |
| 74HCT240 | | | | |
| 74HCT240N | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |

Table 1. Ordering information ...continued

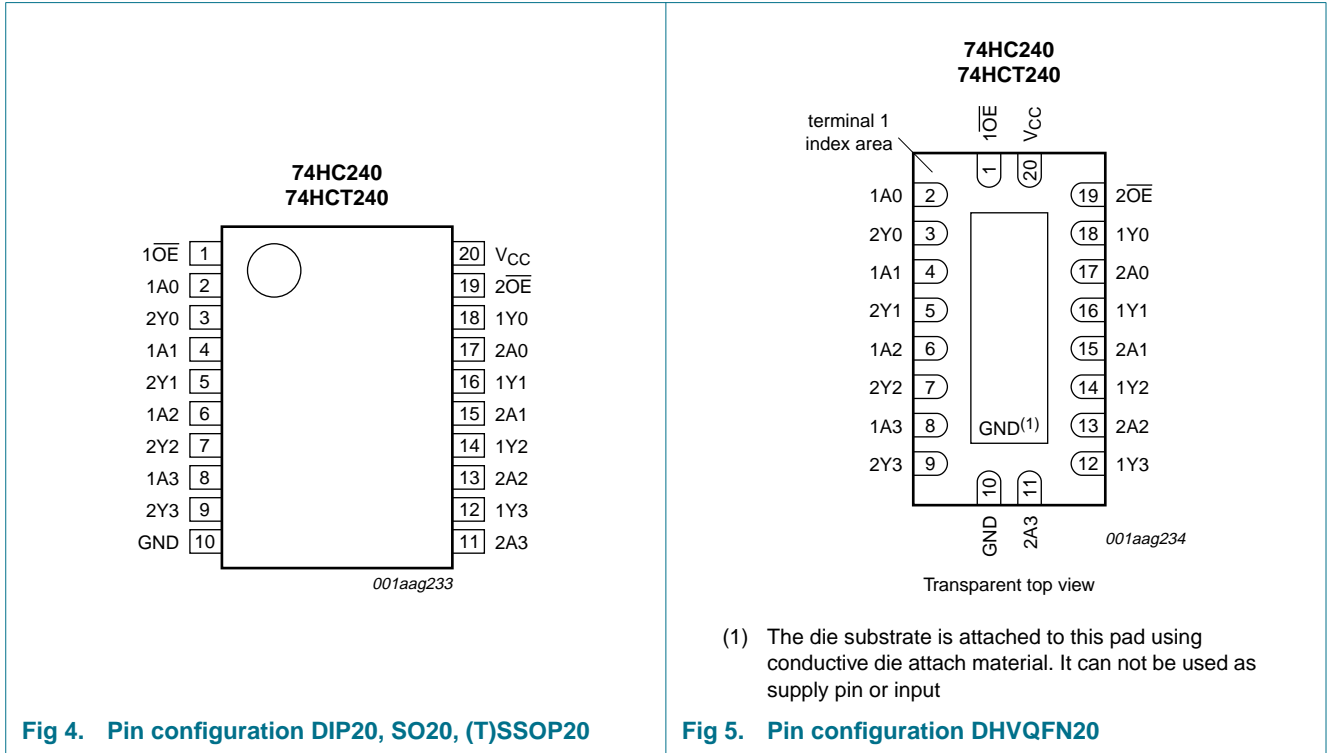
| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HCT240D | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HCT240DB | -40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74HCT240PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HCT240BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------|-----|----------------------------------|
| 1OE | 1 | output enable input (active LOW) |
| 1A0 | 2 | data input |
| 2Y0 | 3 | bus output |
| 1A1 | 4 | data input |
| 2Y1 | 5 | bus output |
| 1A2 | 6 | data input |
| 2Y2 | 7 | bus output |
| 1A3 | 8 | data input |
| 2Y3 | 9 | bus output |
| GND | 10 | ground (0 V) |
| 2A3 | 11 | data input |
| 1Y3 | 12 | bus output |
| 2A2 | 13 | data input |
| 1Y2 | 14 | bus output |
| 2A1 | 15 | data input |
| 1Y1 | 16 | bus output |

Table 2. Pin description ...continued

| Symbol | Pin | Description |
|------------------|-----|----------------------------------|
| 2A0 | 17 | data input |
| 1Y0 | 18 | bus output |
| $\overline{2OE}$ | 19 | output enable input (active LOW) |
| V_{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | Output | |
|-------|-----|--------|--|
| nOE | nAn | nYn | |
| L | L | H | |
| L | H | L | |
| H | X | Z | |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---|--|----------------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_O | output current | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ | - | ± 35 | mA |
| I_{CC} | supply current | | - | 70 | mA |
| I_{GND} | ground current | | -70 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | | ^[1] | | |
| | DIP20 package | | - | 750 | mW |
| | SO20, SSOP20, TSSOP20 and DHVQFN20 packages | | - | 500 | mW |

- [1] For DIP20 packages: above 70 °C, P_{tot} derates linearly with 12 mW/K.
 For SO20 packages: above 70 °C, P_{tot} derates linearly with 8 mW/K.
 For SSOP20 and TSSOP20 packages: above 60 °C, P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C, P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------------------|-----|------|----------|------|
| 74HC240 | | | | | | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | ns/V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| 74HCT240 | | | | | | |
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | ns/V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------|---|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC240 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0\text{ V}$ | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC} = 4.5\text{ V}$ | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC} = 6.0\text{ V}$ | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0\text{ V}$ | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC} = 6.0\text{ V}$ | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = -20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$ | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O = -20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$ | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O = -6.0\text{ mA}; V_{CC} = 4.5\text{ V}$ | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| | $I_O = -7.8\text{ mA}; V_{CC} = 6.0\text{ V}$ | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V | |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | I _O = 7.8 mA; V _{CC} = 6.0 V | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V; I _O = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |
| 74HCT240 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -6 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | per input pin; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; other inputs at V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; V _{CC} = 5.5 V; I _O = 0 A | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | | | | | |
| | | nAn or inputs | - | 150 | 540 | - | 675 | - | 735 | μA |
| | | nOE input | - | 70 | 252 | - | 315 | - | 343 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; for load circuit see Figure 8.

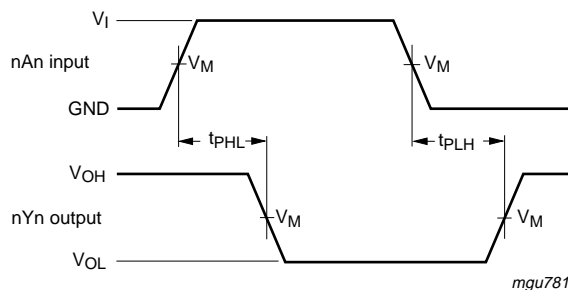
| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +125 °C | | Unit | |
|------------------|-------------------------------|--|-------|-----|-----|-------------------|--------------|------|----|
| | | | Min | Typ | Max | Max (85 °C) | Max (125 °C) | | |
| 74HC240 | | | | | | | | | |
| t _{pd} | propagation delay | nAn to nYn; see Figure 6 | [1] | | | | | | |
| | | V _{CC} = 2.0 V | - | 30 | 100 | 125 | 150 | ns | |
| | | V _{CC} = 4.5 V | - | 11 | 20 | 25 | 30 | ns | |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 9 | - | - | - | ns | |
| | | V _{CC} = 6.0 V | - | 9 | 17 | 21 | 26 | ns | |
| t _{en} | enable time | n $\overline{O}E$ to nYn; see Figure 7 | [2] | | | | | | |
| | | V _{CC} = 2.0 V | - | 39 | 150 | 190 | 225 | ns | |
| | | V _{CC} = 4.5 V | - | 14 | 30 | 38 | 45 | ns | |
| | | V _{CC} = 6.0 V | - | 11 | 26 | 33 | 38 | ns | |
| t _{dis} | disable time | n $\overline{O}E$ to nYn or see Figure 7 | [3] | | | | | | |
| | | V _{CC} = 2.0 V | - | 41 | 150 | 190 | 225 | ns | |
| | | V _{CC} = 4.5 V | - | 15 | 30 | 38 | 45 | ns | |
| | | V _{CC} = 6.0 V | - | 12 | 26 | 33 | 38 | ns | |
| t _t | transition time | see Figure 6 | [4] | | | | | | |
| | | V _{CC} = 2.0 V | - | 14 | 60 | 75 | 90 | ns | |
| | | V _{CC} = 4.5 V | - | 5 | 12 | 15 | 18 | ns | |
| | | V _{CC} = 6.0 V | - | 4 | 10 | 13 | 15 | ns | |
| C _{PD} | power dissipation capacitance | per transceiver; V _I = GND to V _{CC} | [5] | - | 30 | - | - | - | pF |

Table 7. Dynamic characteristics ...continued
GND = 0 V; for load circuit see Figure 8.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +125 °C | | Unit | |
|-----------------|-------------------------------|--|-------|-----|-----|-------------------|--------------|------|----|
| | | | Min | Typ | Max | Max (85 °C) | Max (125 °C) | | |
| 74HCT240 | | | | | | | | | |
| t_{pd} | propagation delay | nAn to nYn; see Figure 6 | [1] | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 11 | 20 | 25 | 30 | ns | |
| | | $V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$ | - | 9 | - | - | - | ns | |
| t_{en} | enable time | nOE to nYn; $V_{CC} = 4.5\text{ V}$; see Figure 7 | [2] | - | 13 | 30 | 38 | 45 | ns |
| t_{dis} | disable time | nOE to nYn; $V_{CC} = 4.5\text{ V}$; see Figure 7 | [3] | - | 13 | 25 | 31 | 38 | ns |
| t_t | transition time | $V_{CC} = 4.5\text{ V}$; see Figure 6 | [4] | - | 5 | 12 | 15 | 18 | ns |
| C_{PD} | power dissipation capacitance | per transceiver; $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ | [5] | - | 30 | - | - | - | pF |

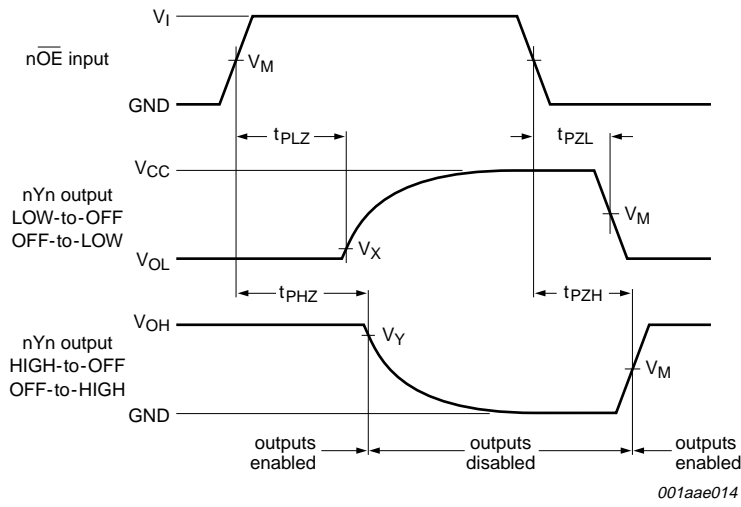
- [1] t_{pd} is the same as t_{PHL} and t_{PLH} .
- [2] t_{en} is the same as t_{PZH} and t_{PZL} .
- [3] t_{dis} is the same as t_{PHZ} and t_{PLZ} .
- [4] t_t is the same as t_{THL} and t_{TLH} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Input (nAn) to output (nYn) propagation delays and output transition times



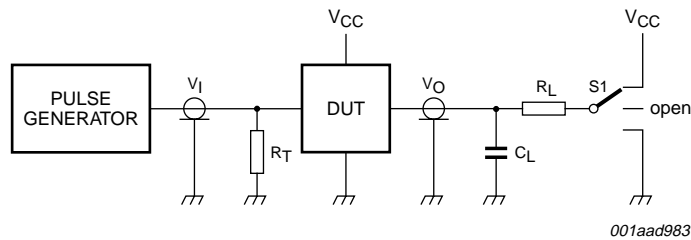
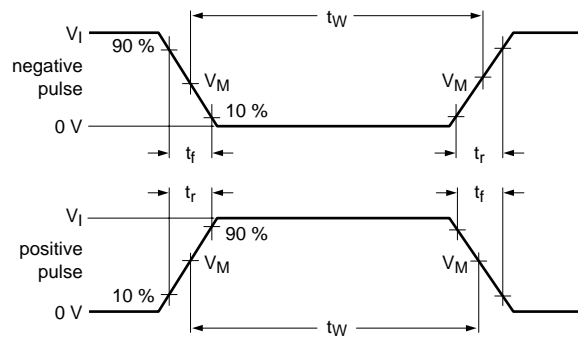
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

| Type | Input | Output | | |
|----------|---------------------|---------------------|---------------------|---------------------|
| | V_M | V_M | V_X | V_Y |
| 74HC240 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $0.1 \times V_{CC}$ | $0.9 \times V_{CC}$ |
| 74HCT240 | 1.3 V | 1.3 V | $0.1 \times V_{CC}$ | $0.9 \times V_{CC}$ |



001aad983

Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 8. Load circuitry for measuring switching times

Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC240 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT240 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

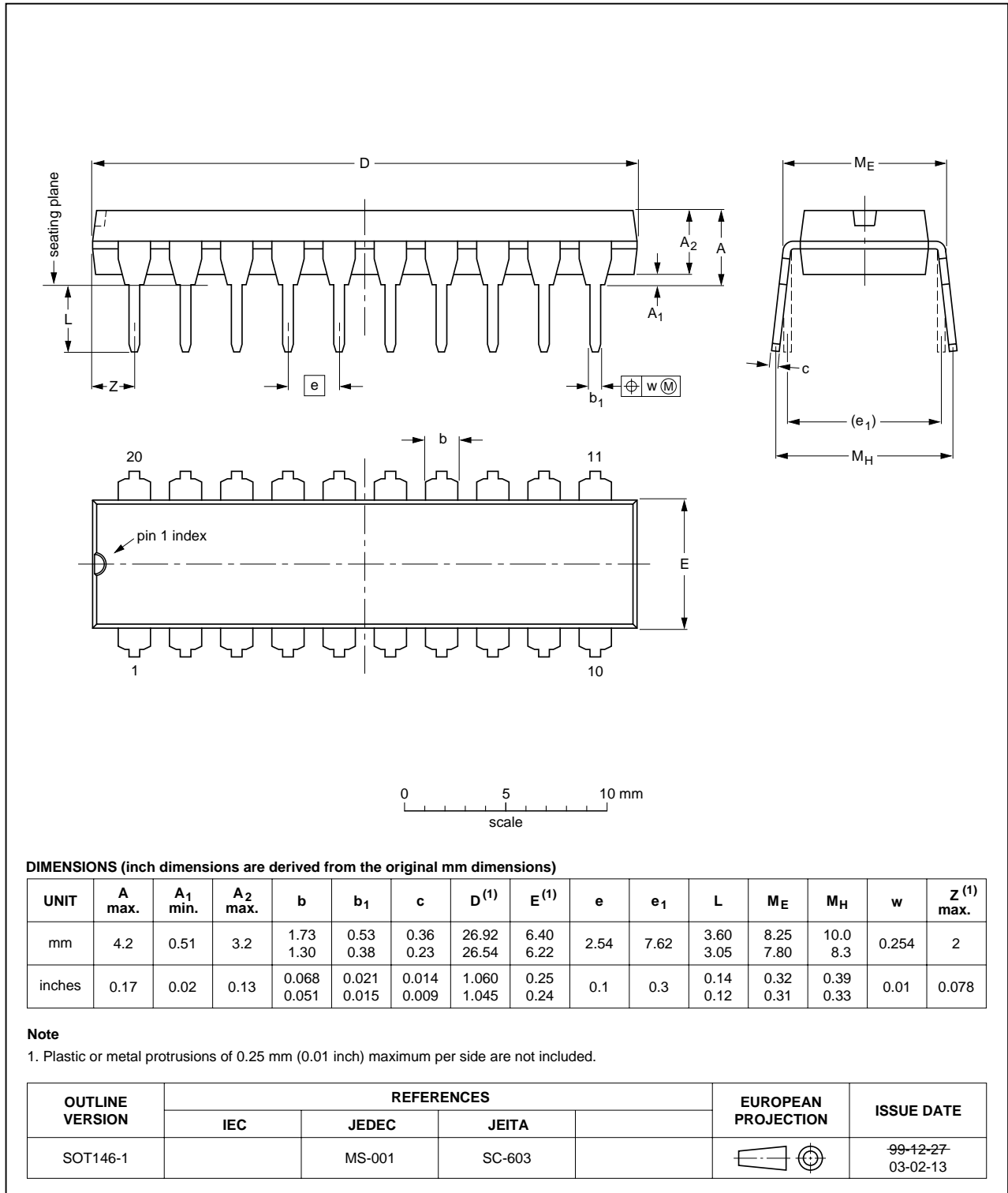


Fig 9. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

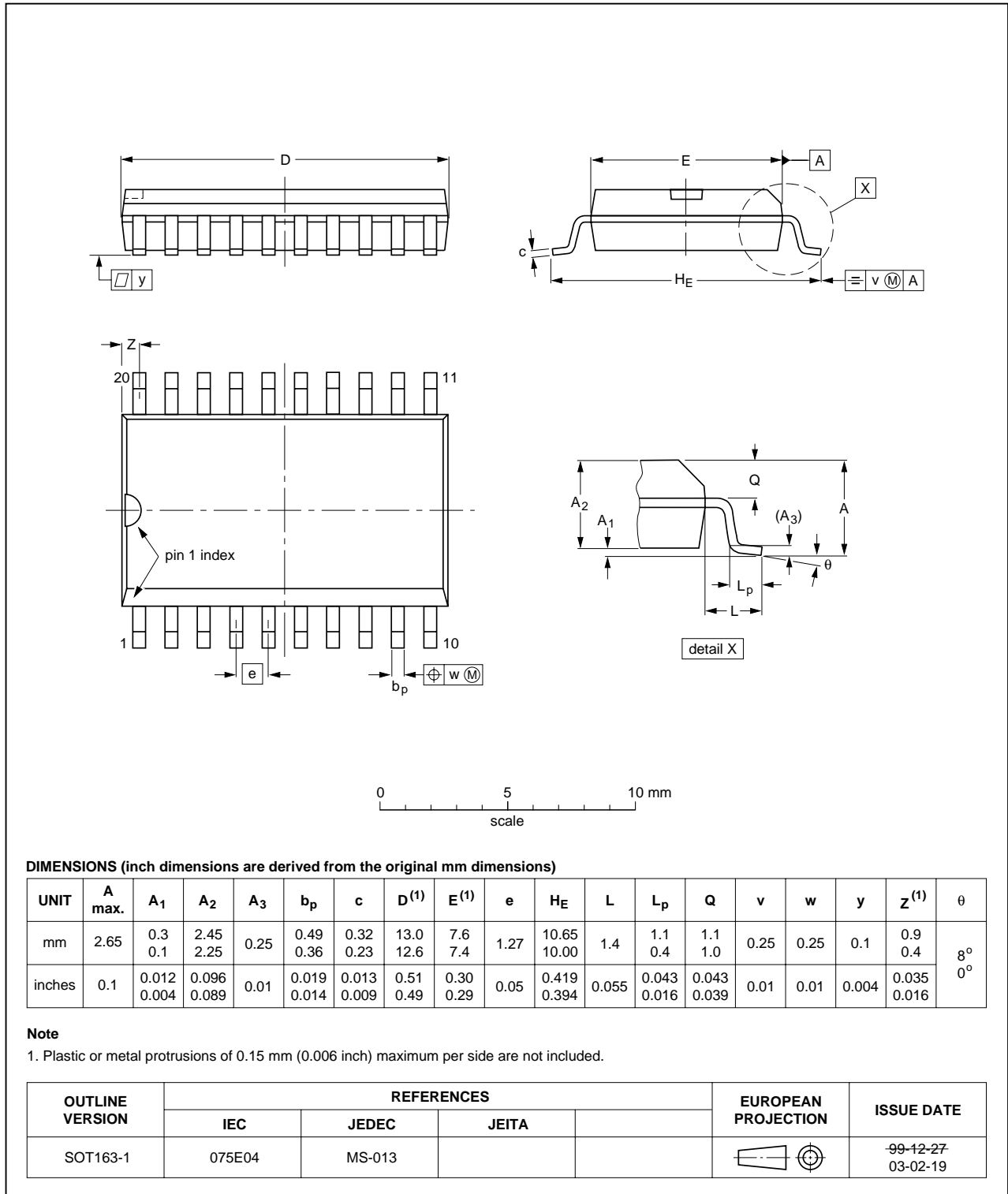


Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

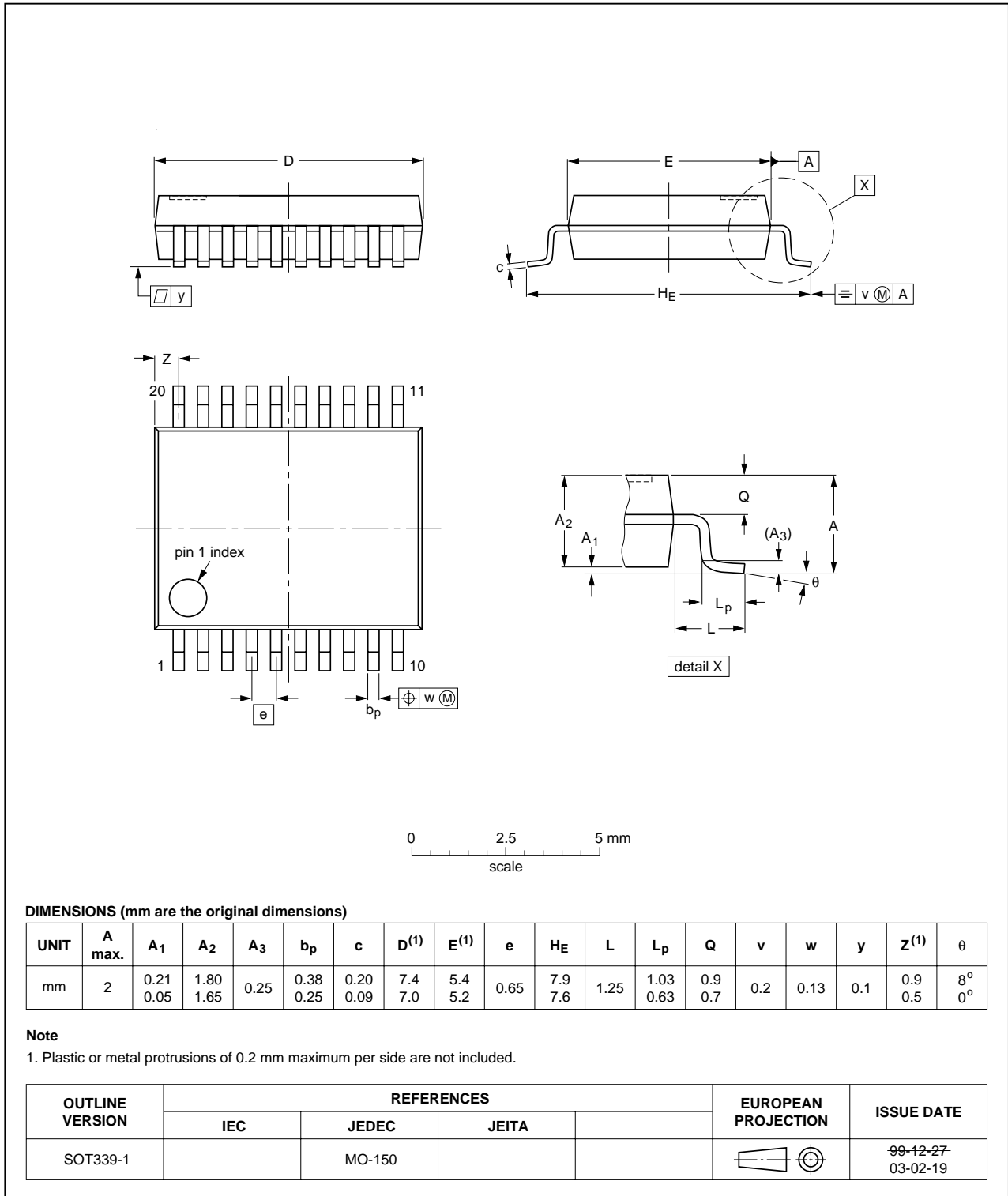


Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

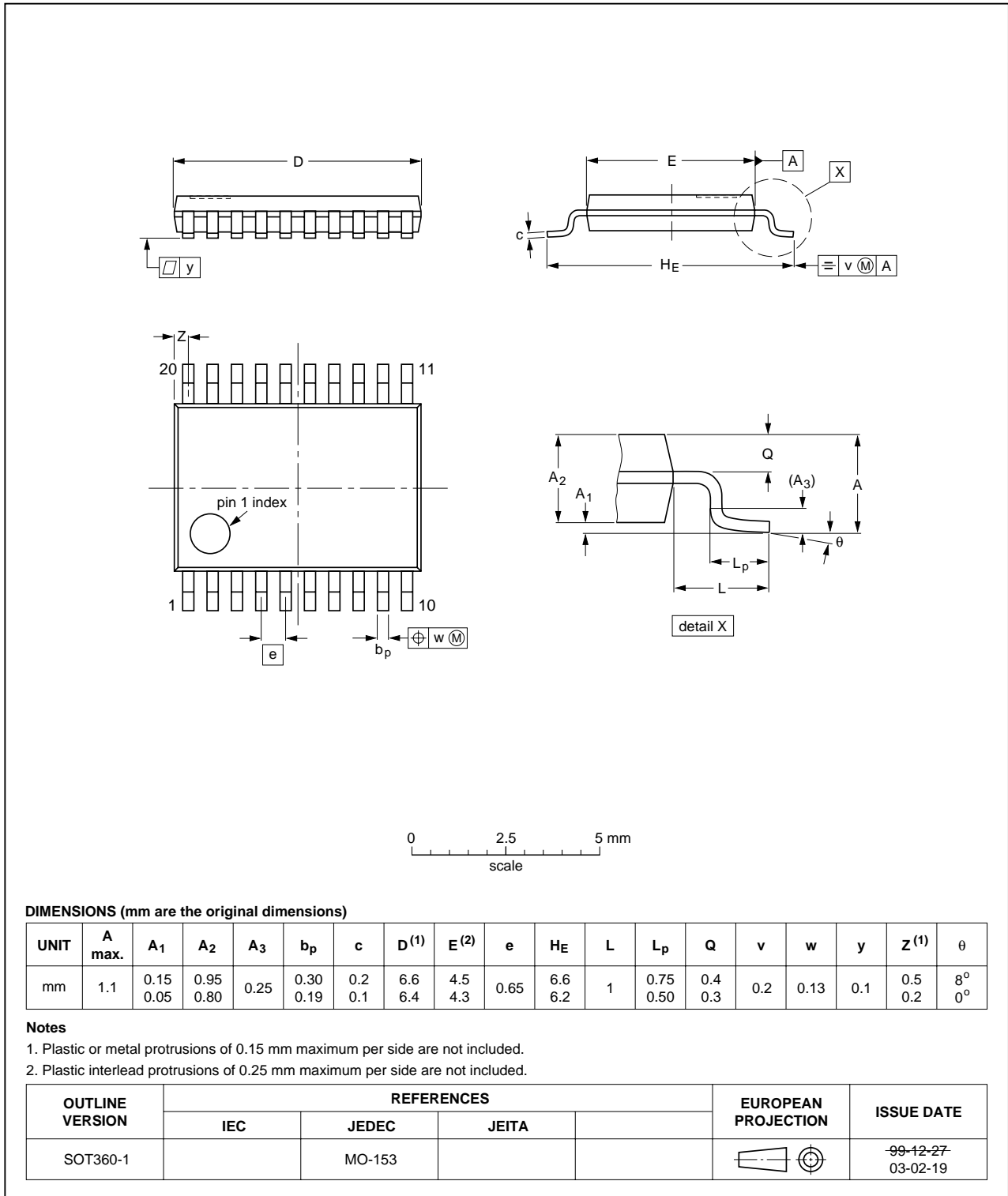


Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

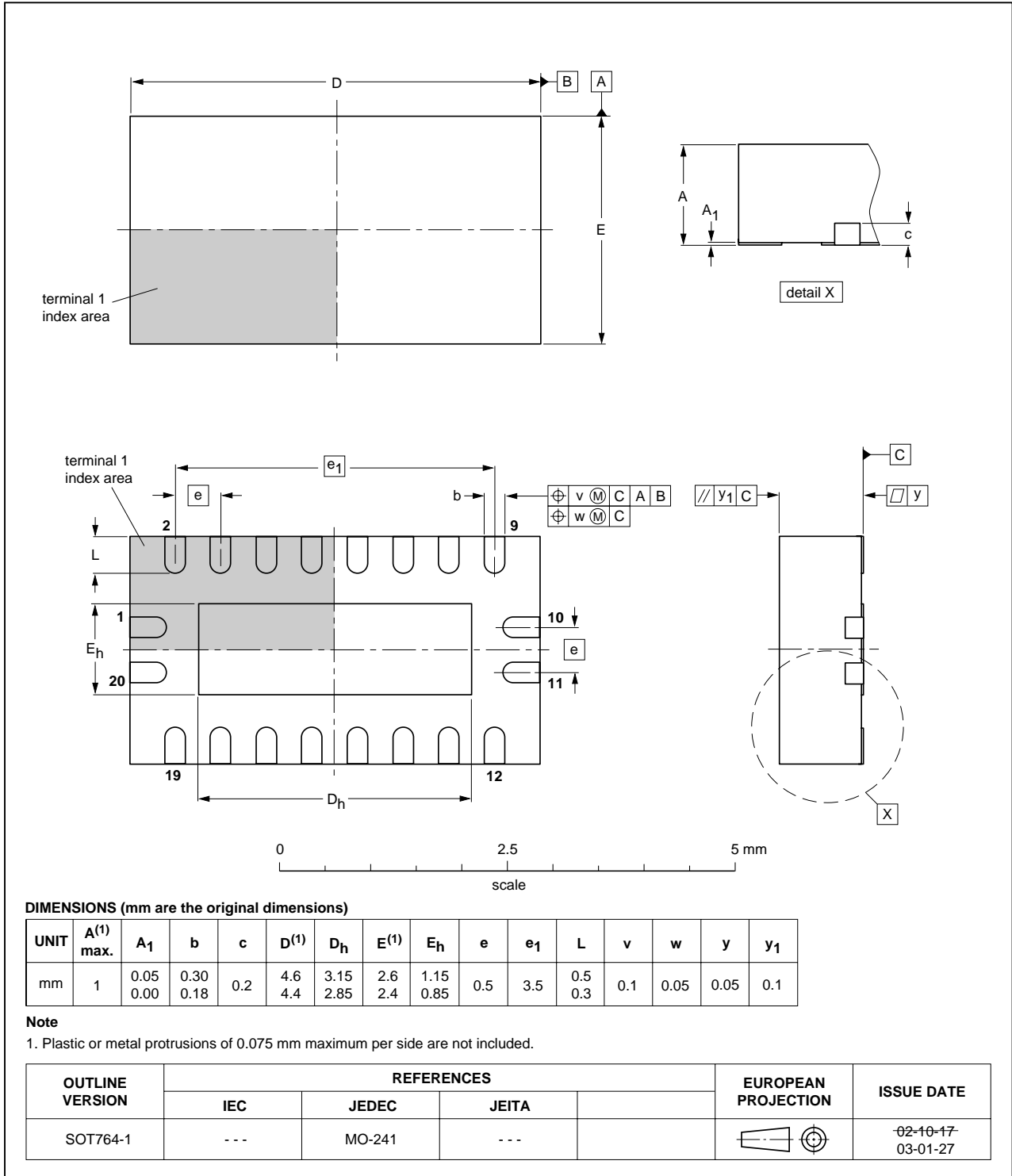


Fig 13. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|-----------------------|---------------|-------------------|
| 74HC_HCT240_3 | 20070802 | Product data sheet | - | 74HC_HCT240_CNV_2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Added type number 74HC240BQ and 74HCT240BQ (DHVQFN20 package) | | | |
| 74HC_HCT240_CNV_2 | 19970828 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features | 1 |
| 3 | Ordering information | 1 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 3 |
| 5.1 | Pinning | 3 |
| 5.2 | Pin description | 3 |
| 6 | Functional description | 4 |
| 7 | Limiting values | 4 |
| 8 | Recommended operating conditions | 5 |
| 9 | Static characteristics | 5 |
| 10 | Dynamic characteristics | 7 |
| 11 | Waveforms | 8 |
| 12 | Package outline | 11 |
| 13 | Abbreviations | 16 |
| 14 | Revision history | 16 |
| 15 | Legal information | 17 |
| 15.1 | Data sheet status | 17 |
| 15.2 | Definitions | 17 |
| 15.3 | Disclaimers | 17 |
| 15.4 | Trademarks | 17 |
| 16 | Contact information | 17 |
| 17 | Contents | 18 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2 August 2007

Document identifier: 74HC_HCT240_3