

74CBTLV3126

4-bit bus switch

Rev. 5 — 9 October 2018

Product data sheet

1. General description

The 74CBTLV3126 provides a 4-bit high-speed bus switch with separate output enable inputs (1OE to 4OE). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable (nOE) input is LOW.

To ensure the high-impedance OFF-state during power-up or power-down, nOE should be tied to the GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- Standard '126'-type pinout
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74CBTLV3126DS	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3126PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74CBTLV3126BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

[1] Also known as QSOP16.

4. Functional diagram

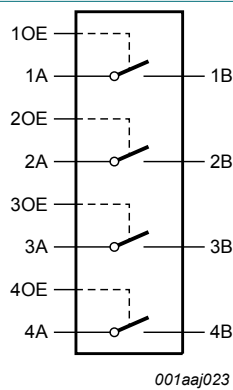


Fig. 1. Logic symbol

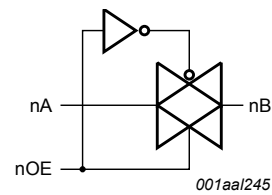
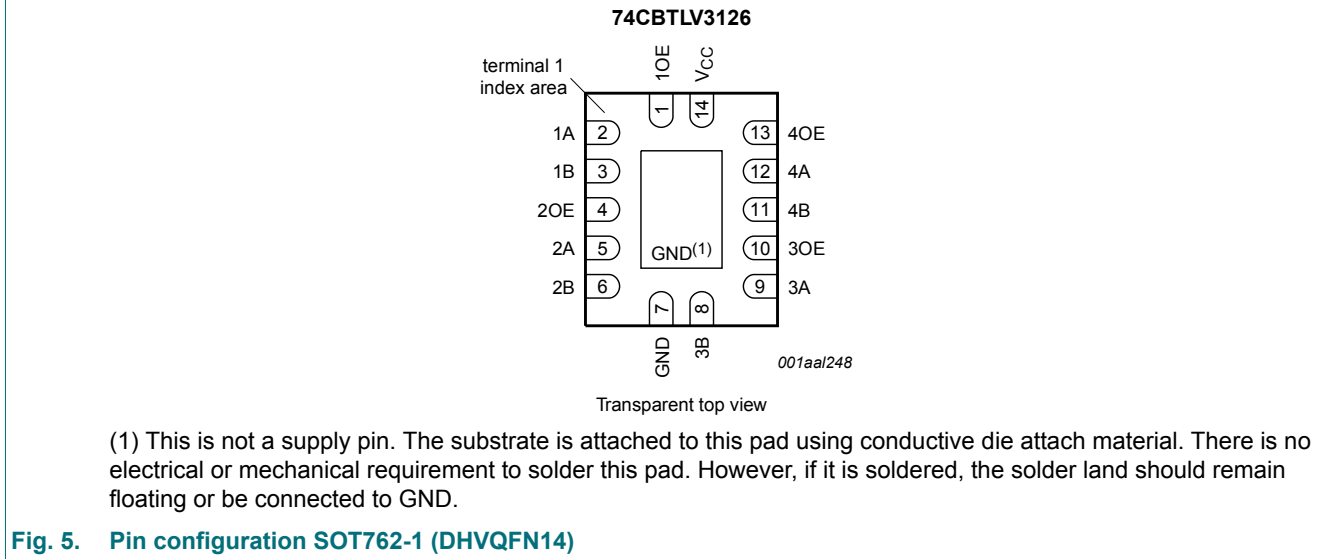
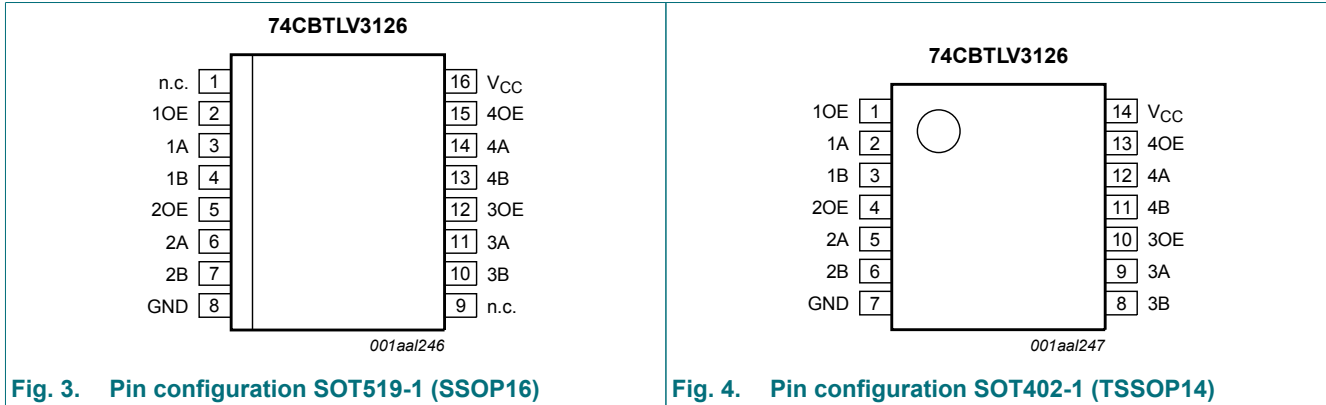


Fig. 2. Logic diagram (one switch)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin		Description
	SOT519-1	SOT402-1 and SOT762-1	
10E, 20E, 30E, 40E	2, 5, 12, 15	1, 4, 10, 13	output enable input
1A, 2A, 3A, 4A	3, 6, 11, 14	2, 5, 9, 12	A input/output
1B, 2B, 3B, 4B	4, 7, 10, 13	3, 6, 8, 11	B output/input
GND	8	7	ground (0 V)
V _{CC}	16	14	supply voltage
n.c.	1, 9	-	not connected

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Output enable input nOE	Function switch
L	OFF-state
H	ON-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	control inputs [1]	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current	$V_{SW} = 0$ V to V_{CC}	-	± 128	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For SSOP16 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage	control inputs	0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	pin nOE; $V_{CC} = 2.3$ V to 3.6 V	0	200	ns/V

9. Static characteristics

Table 6. Static characteristics

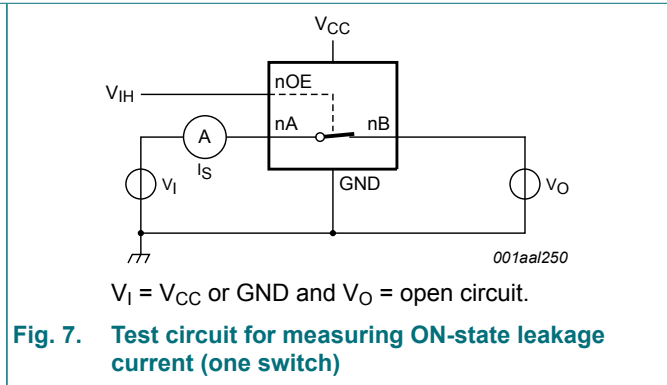
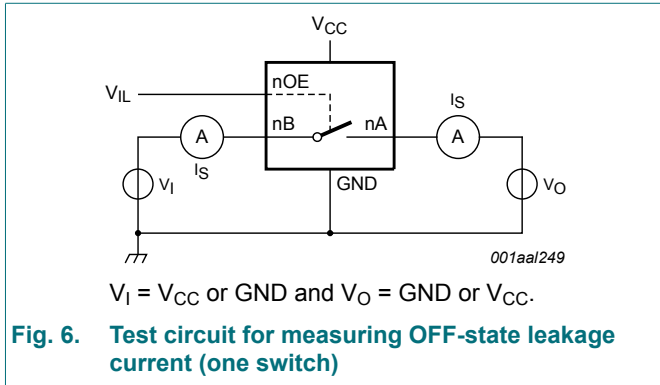
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin nOE; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1.0	-	±20	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Fig. 6	-	-	±1	-	±20	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Fig. 7	-	-	±1	-	±20	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	-	10	-	50	µA
ΔI _{CC}	additional supply current	pin nOE; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	[2]	-	300	-	2000	µA
C _I	input capacitance	pin nOE; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	14.3	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits



9.2. ON resistance

Table 7. Resistance R_{ON}

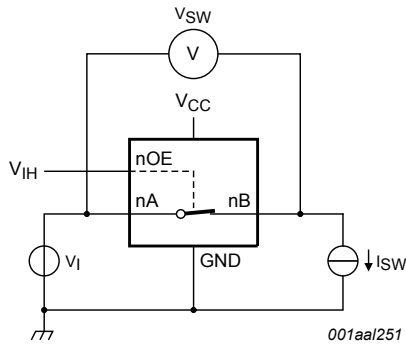
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ [1]	Max	Min	Max	
R_{ON}	ON resistance	$V_{CC} = 2.3\text{ V to }2.7\text{ V};$ see Fig. 9 to Fig. 11 [2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 15\text{ mA}; V_I = 1.7\text{ V}$	-	8.4	40.0	-	60.0	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V};$ see Fig. 12 to Fig. 14						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
$I_{SW} = 15\text{ mA}; V_I = 2.4\text{ V}$	-	6.2	15.0	-	25.5	Ω		

[1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and nominal V_{CC} .

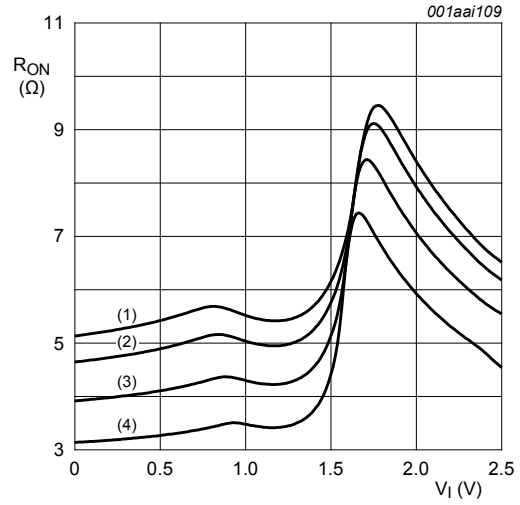
[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs



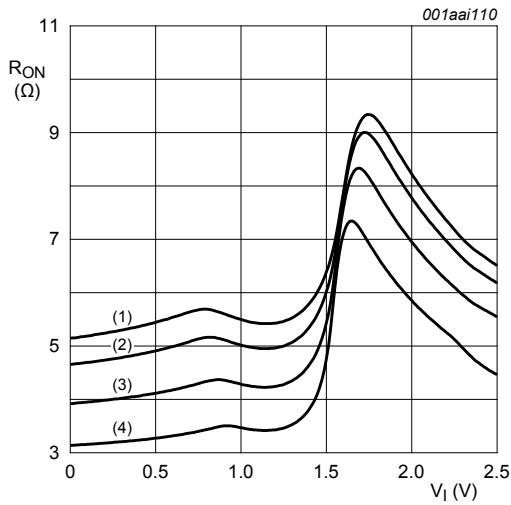
$R_{ON} = V_{SW} / I_{SW}$.

Fig. 8. Test circuit for measuring ON resistance (one switch)



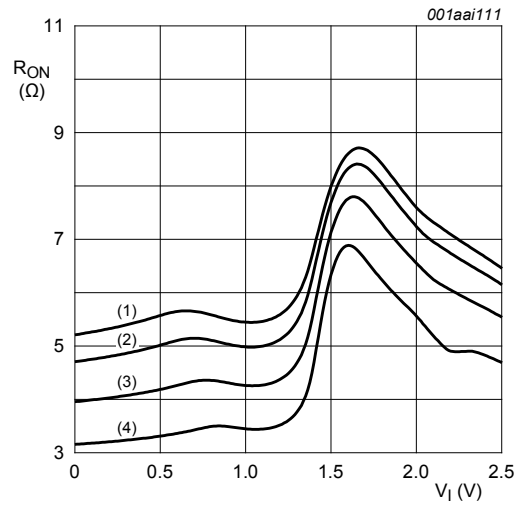
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig. 9. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$; $I_{SW} = 15\text{ mA}$



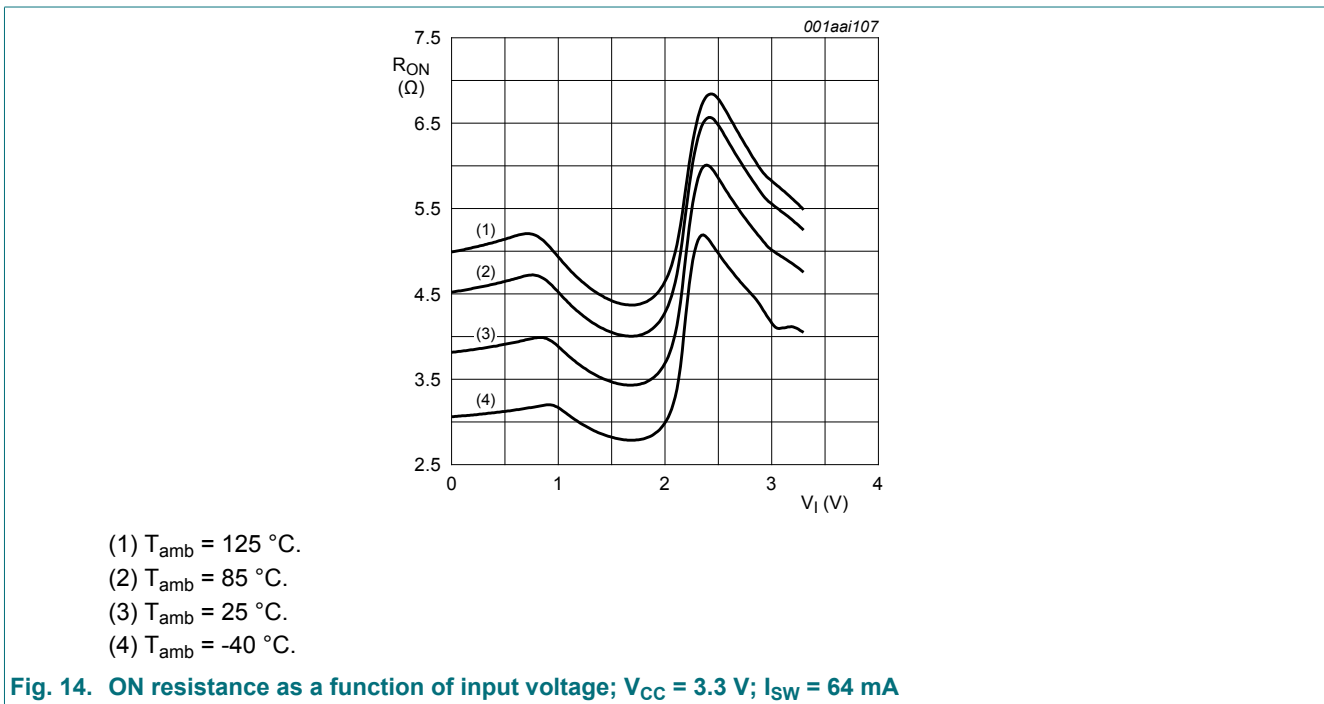
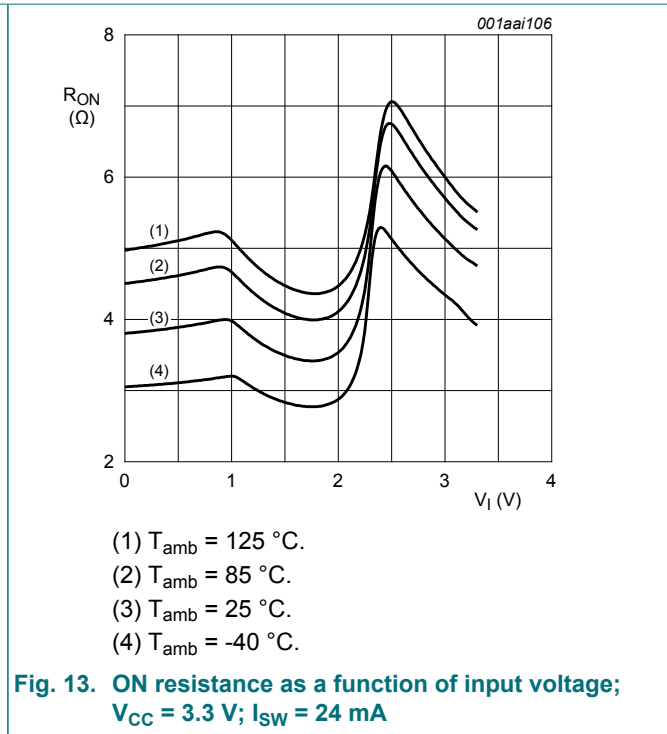
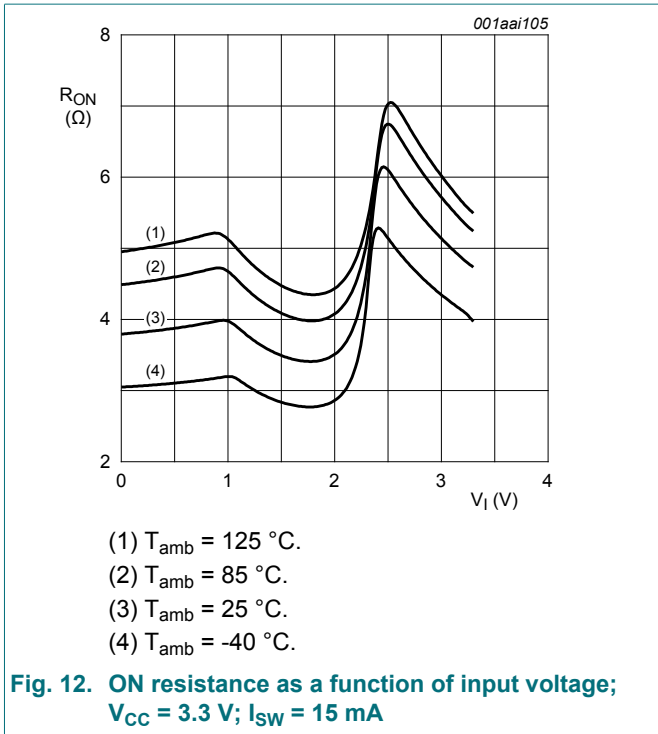
- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$; $I_{SW} = 24\text{ mA}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig. 11. ON resistance as a function of input voltage; $V_{CC} = 2.5\text{ V}$; $I_{SW} = 64\text{ mA}$



10. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 18

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nB or nB to nA; see Fig. 16 [2][3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.13	-	0.20	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.20	-	0.31	ns
t_{en}	enable time	nOE to nA or nB; see Fig. 17 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.5	4.5	1.0	6.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.2	4.2	1.0	6.0	ns
t_{dis}	disable time	nOE to nA or nB; see Fig. 17 [5]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.6	4.7	1.0	6.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.4	4.8	1.0	6.5	ns

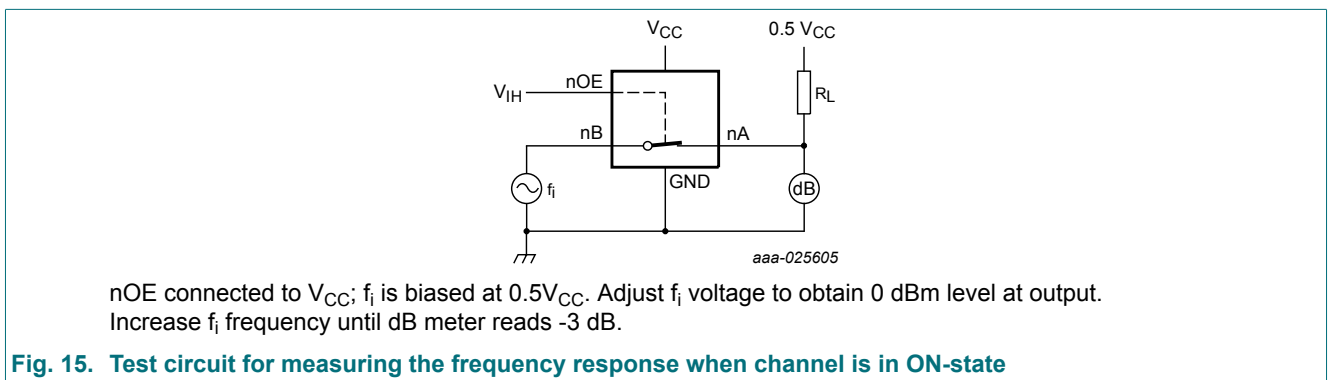
- [1] All typical values are measured at $T_{amb} = 25\text{ °C}$ and at nominal V_{CC} .
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [4] t_{en} is the same as t_{PZH} and t_{PZL} .
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

10.1. Additional dynamic characteristics

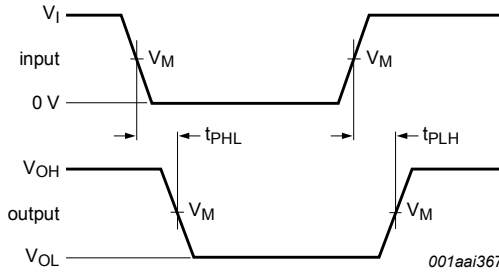
Table 9. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			Unit
			Min	Typ	Max	
$f_{(-3dB)}$	-3 dB frequency response	$V_I = GND\text{ or }V_{CC}$; $t_r = t_f \leq 2.5\text{ ns}$; $V_{CC} = 3.3\text{ V}$; $R_L = 50\text{ }\Omega$; see Fig. 15	-	406	-	MHz



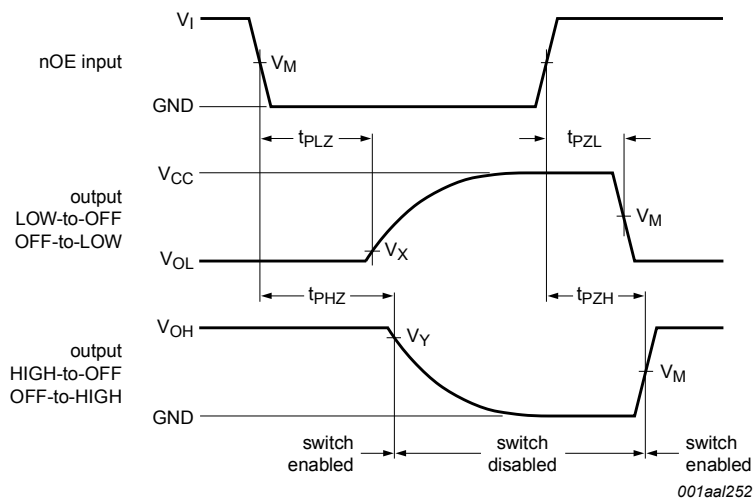
10.2. Waveforms and test circuit



Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 16. The data input (nA or nB) to output (nB or nA) propagation delays



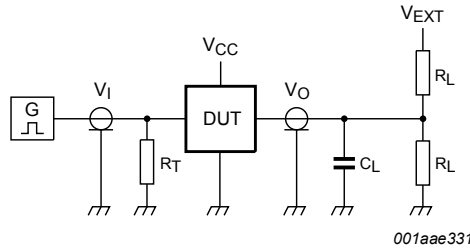
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 17. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_M	V_I	V_M	V_X	V_Y
2.3 V to 2.7 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



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Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load			V_{EXT}		
V_{CC}	C_L	R_L	$t_r = t_f$	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	≤ 2.0 ns	open	GND	$2V_{CC}$
3.0 V to 3.6 V	50 pF	500 Ω	≤ 2.0 ns	open	GND	$2V_{CC}$

11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

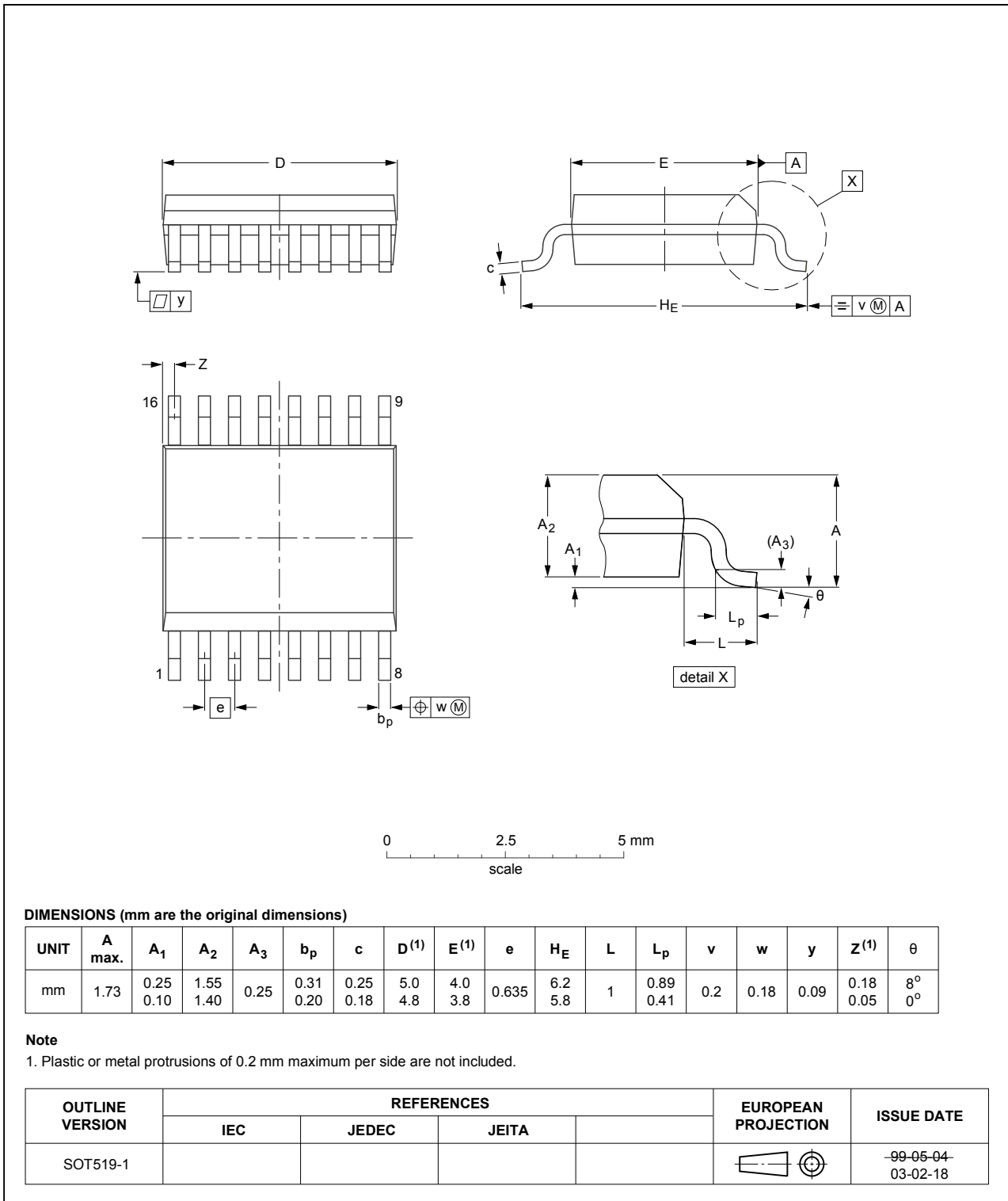


Fig. 19. Package outline SOT519-1 (SSOP16)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

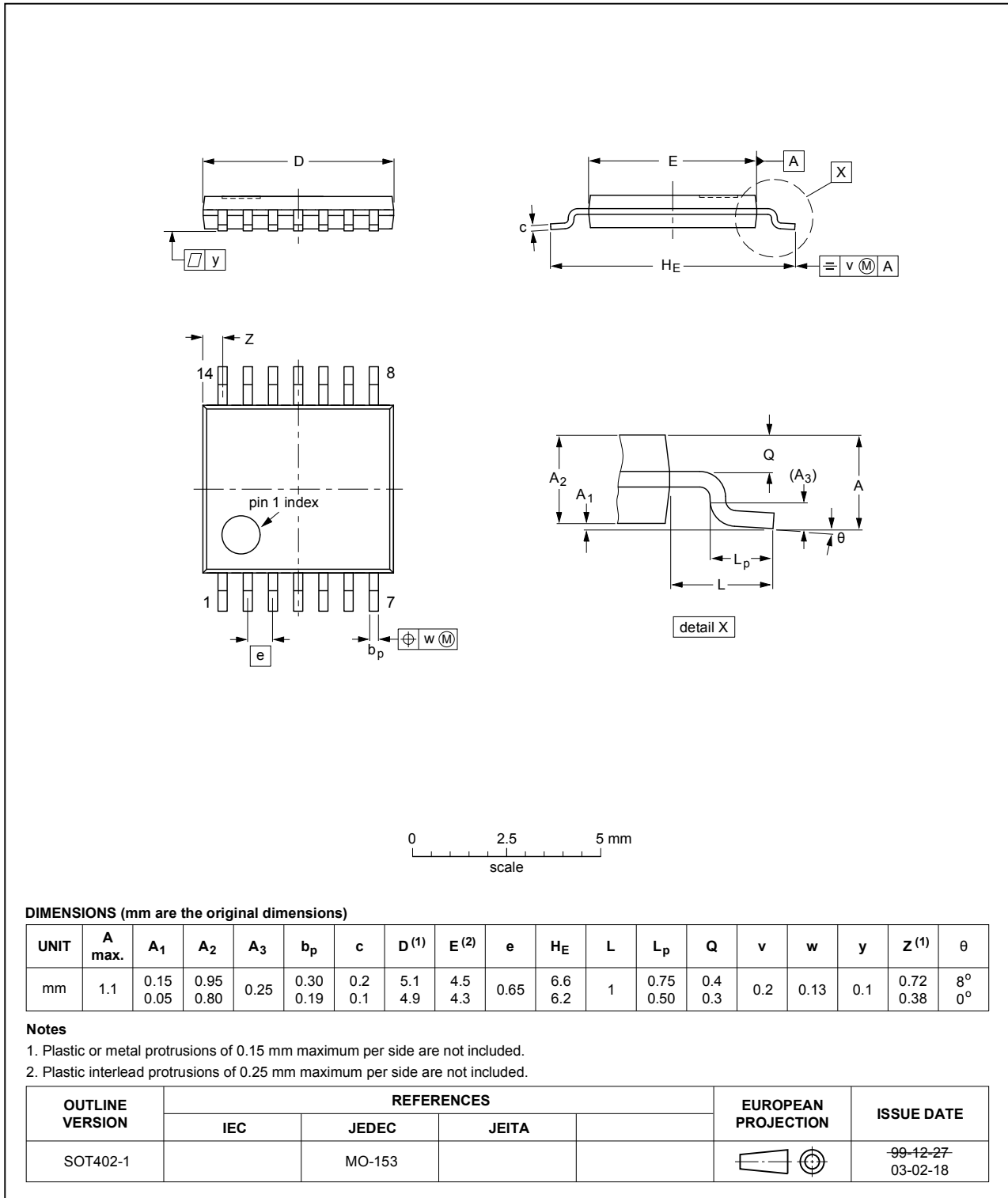


Fig. 20. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

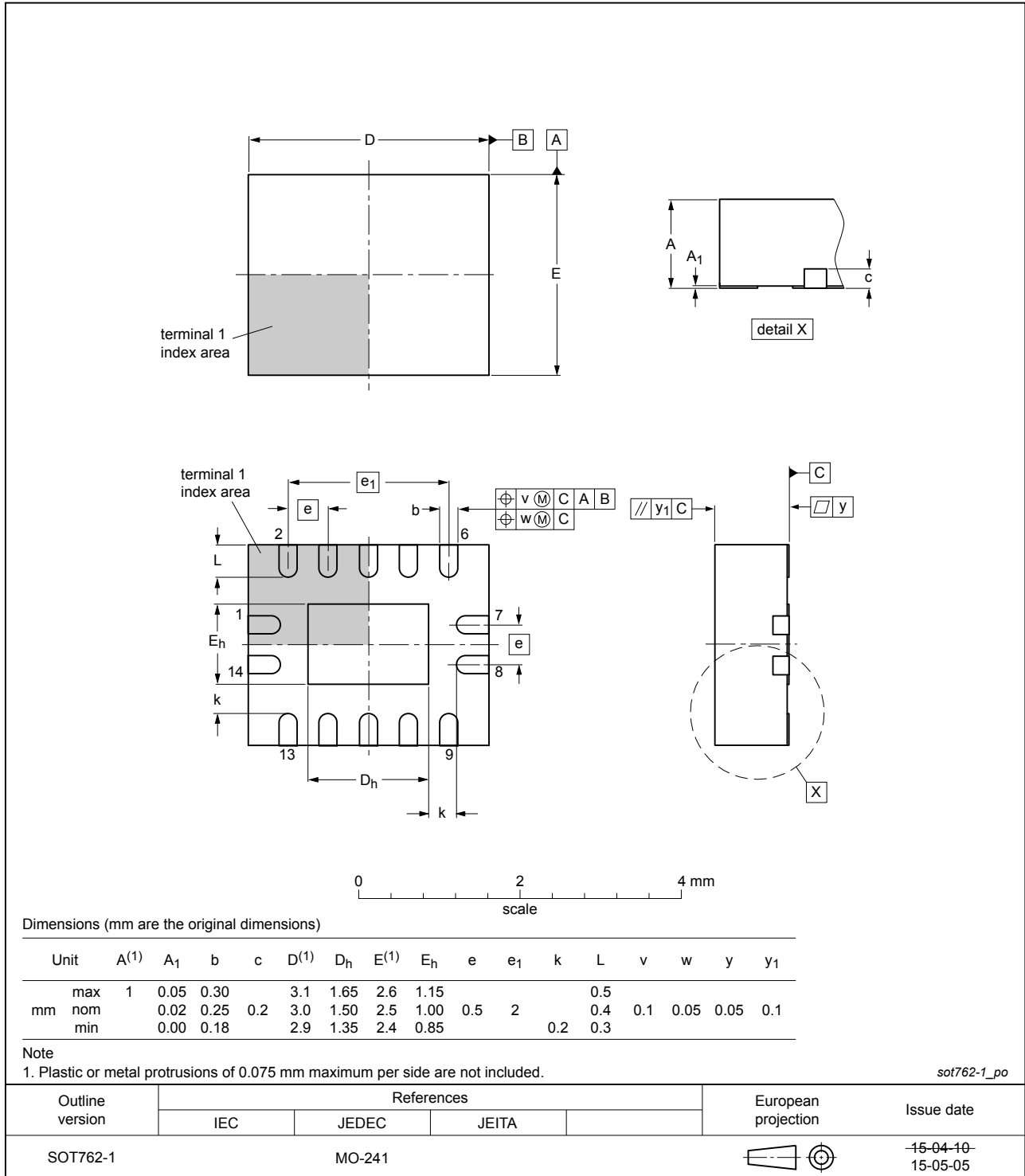


Fig. 21. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3126 v.5	20181009	Product data sheet	-	74CBTLV3126 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74CBTLV3126 v.4	20161108	Product data sheet	-	74CBTLV3126 v.3
Modifications:	<ul style="list-style-type: none"> Section 10.1 added. 			
74CBTLV3126 v.3	20111215	Product data sheet	-	74CBTLV3126 v.2
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74CBTLV3126 v.2	20110104	Product data sheet	-	74CBTLV3126 v.1
74CBTLV3126 v.1	20100105	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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