74ALVC16244; 74ALVCH16244

2.5 V / 3.3 V 16-bit buffer/line driver; 3-state

Rev. 6 — 22 July 2021 **Product data sheet**

1. General description

The 74ALVC16244; 74ALVCH16244 is a 16-bit buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$ and 4$\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

The 74ALVCH16244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Overvoltage tolerant inputs to 5.5 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- All data inputs have bushold (74ALVCH16244 only)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at 3.0 V
- ESD protection:
  - HBM JESD22-A114-A exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC16244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ALVCH16244DGG				

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4. Functional diagram

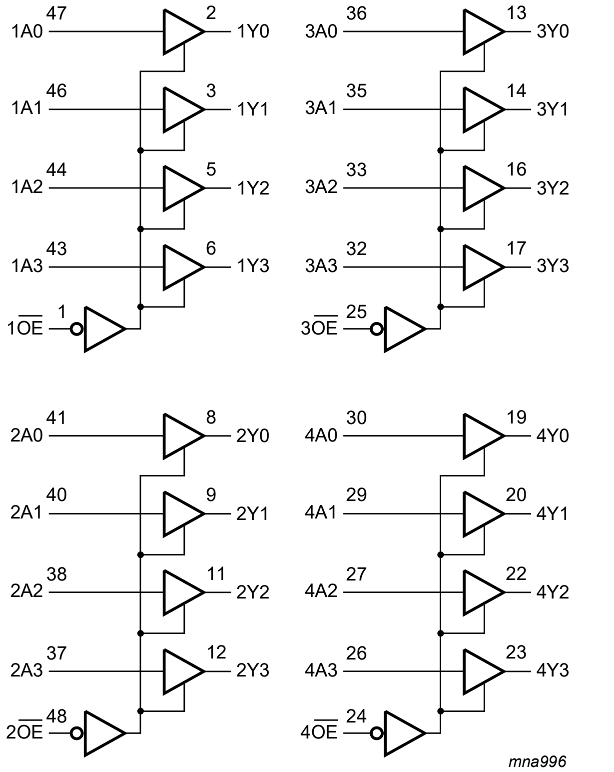


Fig. 1. Logic symbol

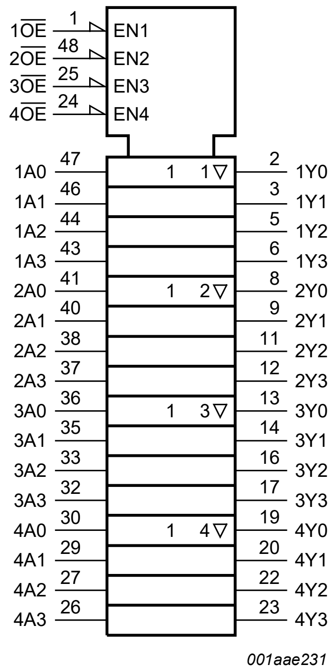


Fig. 2. IEC logic symbol

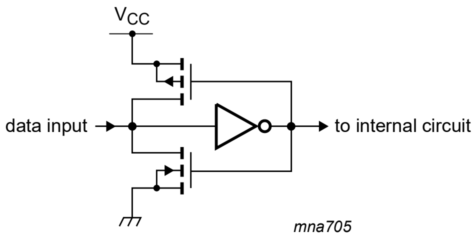


Fig. 3. Bus hold circuit

5. Pinning information

5.1. Pinning

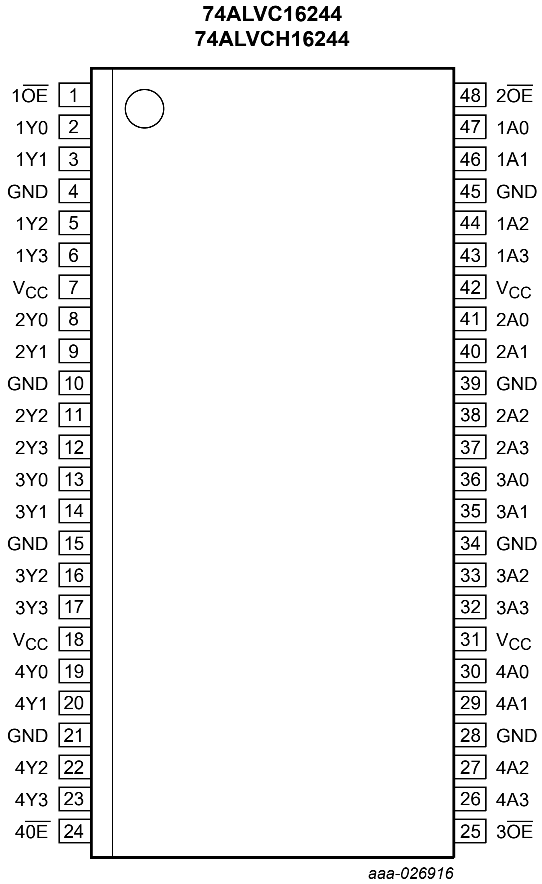


Fig. 4. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
$n\overline{OE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	74ALVCH16244; data inputs	[1]	-0.5	V_{CC} + 0.5	V
		74ALVC16244; data inputs	[1]	-0.5	+5.5	V
		control inputs	[1]	-0.5	+5.5	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	maximum speed performance			
		V_{CC} = 2.5 V: C_L = 30 pF	2.3	2.7	V
		V_{CC} = 3.3 V: C_L = 50 pF	3.0	3.6	V
		LOW-voltage applications	1.2	3.6	V
V_I	input voltage	74ALVCH16244; data inputs	0	V_{CC}	V
		74ALVC16244; data inputs	0	5.5	V
		control inputs	0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.8 V	0.7 × V_{CC}	0.9	-	V
		V_{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 1.8 V	-	0.9	0.2 × V_{CC}	V
		V_{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 μA; V_{CC} = 1.8 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 1.8 V	V_{CC} - 0.4	V_{CC} - 0.10	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.5	V_{CC} - 0.17	-	V
		I_O = -18 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.8 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 1.8 V	-	0.09	0.30	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.20	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.40	V
		I_O = 18 mA; V_{CC} = 2.3 V	-	0.23	0.60	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_I	input leakage current	74ALVCH16244; data inputs; $V_I = V_{CC}$ or GND; V_{CC} = 1.8 V to 3.6 V		-	0.1	5	μA
		74ALVC16244; data inputs; V_I = 5.5 V or GND; V_{CC} = 1.8 V to 3.6 V		-	0.1	5	μA
		control inputs; V_I = 5.5 V or GND; V_{CC} = 1.8 V to 3.6 V		-	0.1	5	μA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	[2]	45	-	-	μA
		V_{CC} = 3.0 V; V_I = 0.8 V	[2]	75	150	-	μA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	[2]	-45	-	-	μA
		V_{CC} = 3.0 V; V_I = 2.0 V	[2]	-75	-175	-	μA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 2.7 V	[2]	300	-	-	μA
		V_{CC} = 3.6 V	[2]	450	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 2.7 V	[2]	-300	-	-	μA
		V_{CC} = 3.6 V	[2]	-450	-	-	μA
I_{OZ}	OFF-state output current	V_{CC} = 1.8 to 2.7 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		-	0.1	5	μA
		V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND		-	0.1	10	μA
I_{CC}	supply current	V_{CC} = 1.8 to 2.7 V; $V_I = V_{CC}$ or GND; I_O = 0 A		-	0.1	20	μA
		V_{CC} = 2.3 to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A		-	0.2	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V					
		74ALVCH16244; data inputs		-	150	750	μA
		74ALVC16244; data inputs		-	5	500	μA
		control pins		-	5	500	μA
C_I	input capacitance			-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Valid for data inputs of bus hold parts.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 7.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	nAn to nYn; see Fig. 5 [2]				
		V_{CC} = 1.2 V	-	5.8	-	ns
		V_{CC} = 1.8 V	1.5	2.8	5.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	1.9	3.7	ns
		V_{CC} = 2.7 V	1.0	2.1	3.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	1.9	3.0	ns
t_{en}	enable time	$n\overline{OE}$ to nYn; see Fig. 6 [3]				
		V_{CC} = 1.2 V	-	8.4	-	ns
		V_{CC} = 1.8 V	1.5	3.8	7.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.5	4.9	ns
		V_{CC} = 2.7 V	1.0	2.9	4.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nYn; see Fig. 6 [4]				
		V_{CC} = 1.2 V	-	5.9	-	ns
		V_{CC} = 1.8 V	1.5	3.1	5.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.1	4.1	ns
		V_{CC} = 2.7 V	1.0	3.0	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.7	4.1	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [5]				
		outputs enabled	-	25	-	pF
		outputs disabled	-	4	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

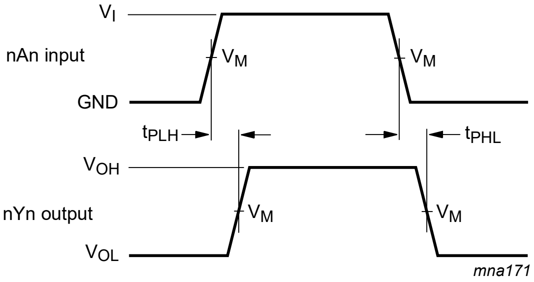
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz
f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = total load switching outputs
$\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs

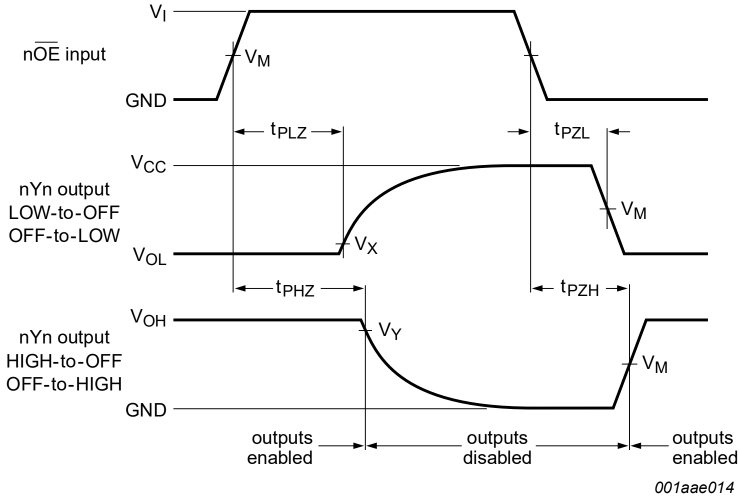
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The input (nAn) to output (nYn) propagation delays



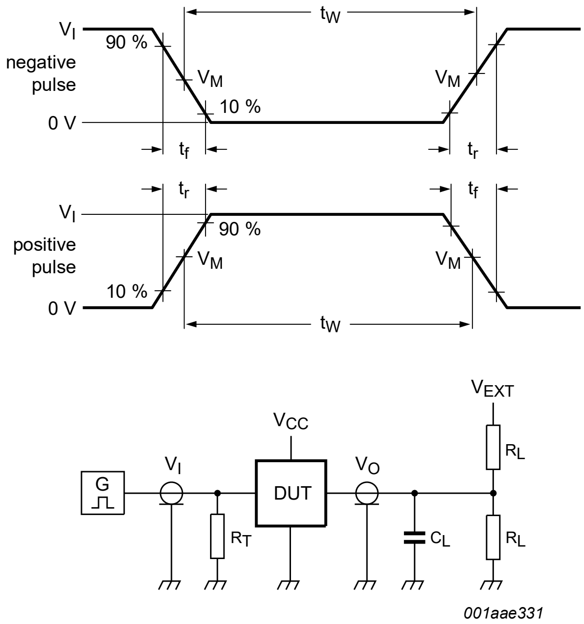
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2	V_{CC}	0.5 x V_{CC}	0.5V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
1.8 V	V_{CC}	0.5 x V_{CC}	0.5V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 x V_{CC}	0.5V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

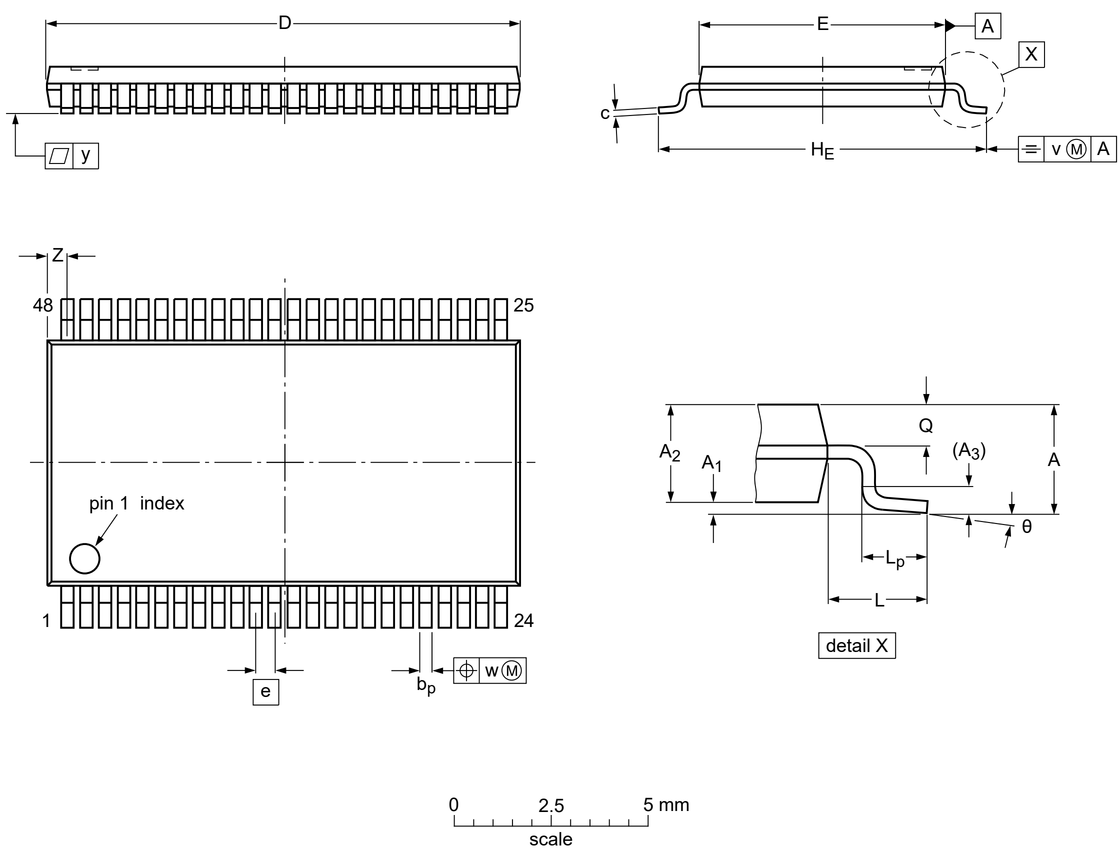
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
1.8 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC_ALVCH16244 v.6	20210722	Product data sheet	-	74ALVC_ALVCH16244 v.5
Modifications:	• Type number 74ALVC16244DL (SOT370-1/SSOP48) removed. • Section 1 and Section 2 updated. • Section 7: derating values for P_{tot} total power dissipation updated.			
74ALVC_ALVCH16244 v.5	20190115	Product data sheet	-	74ALVC_ALVCH16244 v.4
Modifications:	• Type number 74ALVCH16244DL (SOT370-1) removed.			
74ALVC_ALVCH16244 v.4	20170612	Product data sheet	-	74ALVC_ALVCH16244 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVC_ALVCH16244 v.3	20030514	Product specification	-	74ALVC_ALVCH16244 v.2
74ALVC_ALVCH16244 v.2	19980629	Product specification	-	74ALVCH16244 v.1
74ALVCH16244 v.1	19970321	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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