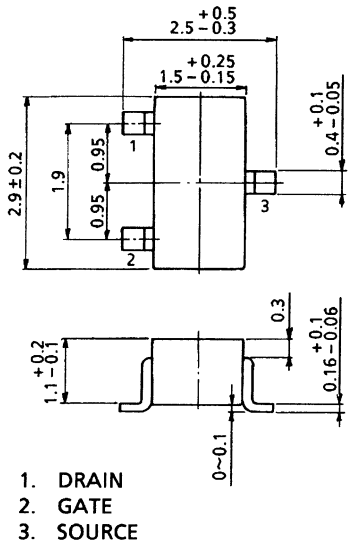
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

2SK302

FM Tuner, VHF RF Amplifier Applications

- Low reverse transfer capacitance: C_{rss} = 0.035 pF (typ.)
- Low noise figure: NF = 1.7dB (typ.)
- High power gain: G_{ps} = 28dB (typ.)
- Recommend operation voltage: 5~15 V

Unit: mm



JEDEC	TO-236
JEITA	—
TOSHIBA	2-3F1C

Weight: 0.012 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

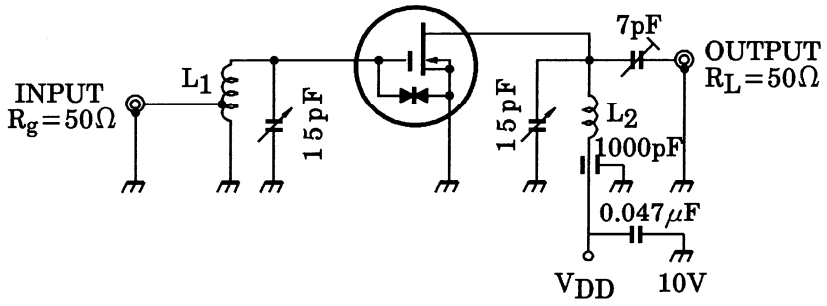
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	±5	V
Drain current	I_D	30	mA
Drain power dissipation	P_D	150	mW
Channel temperature	T_{ch}	125	°C
Storage temperature	T_{stg}	−55~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±5 V	—	—	±50	nA
Drain-source voltage	V_{DSX}	V_{GS} = −4 V, I_D = 100 μA	20	—	—	V
Drain current	I_{DSS} (Note)	V_{DS} = 10 V, V_{GS} = 0 V	1.5	—	14	mA
Gate-source cut-off voltage	$V_{GS\ (OFF)}$	V_{DS} = 10 V, I_D = 100 μA	—	—	−2.5	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	—	10	—	mS
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	3.0	—	pF
Reverse transfer capacitance	C_{rss}		—	0.035	0.050	pF
Power gain	G_{PS}	V_{DS} = 10 V, V_{GS} = 0 V, f = 100 MHz (Figure 1)	—	28	—	dB
Noise figure	NF		—	1.7	3.0	dB

Note: I_{DSS} classification O: 1.5~3.5 mA, Y: 3.0~7.0 mA, GR: 6.0~14.0 mA

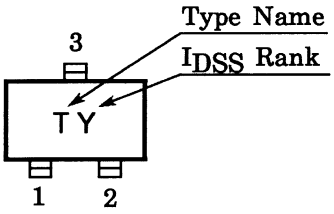


L_1: 1.0 mmϕ silver plated copper wire 4.0 T, 8 mmϕ ID TAP at 1.0 T from coil end

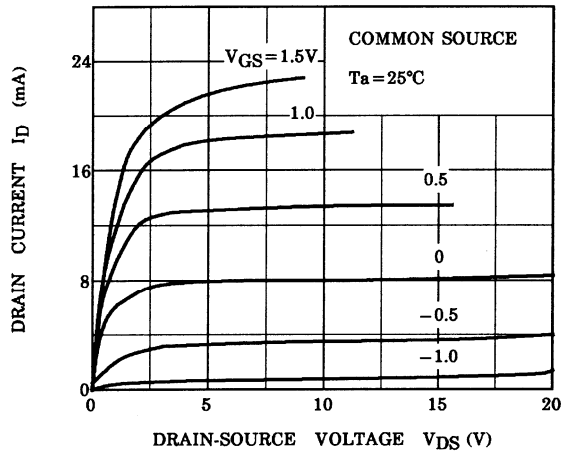
L_2: 1.0 mmϕ silver plated copper wire 3.0 T, 8 mmϕ ID, 10 mm length

Figure 1 G_{ps}, NF Test Circuit

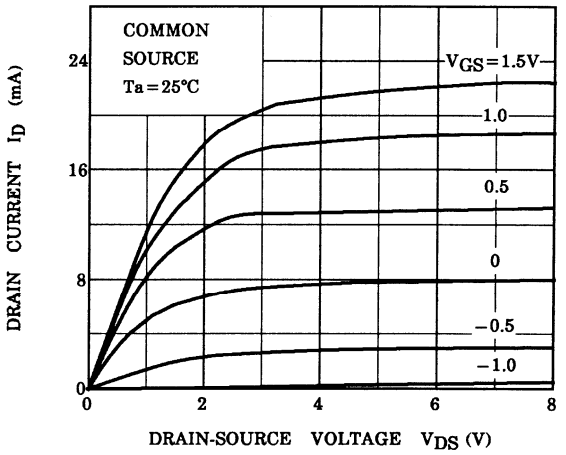
Marking



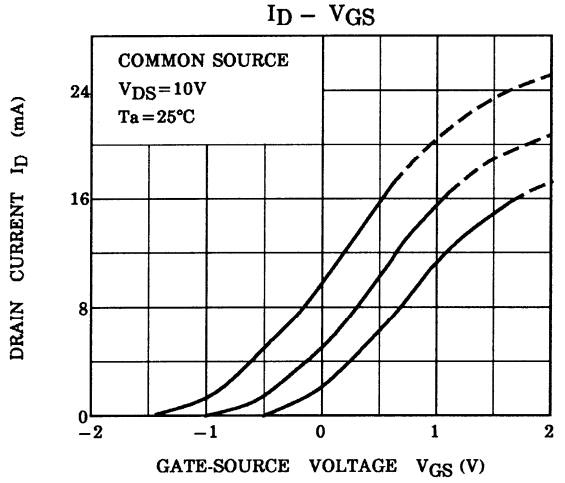
$I_D - V_{DS}$



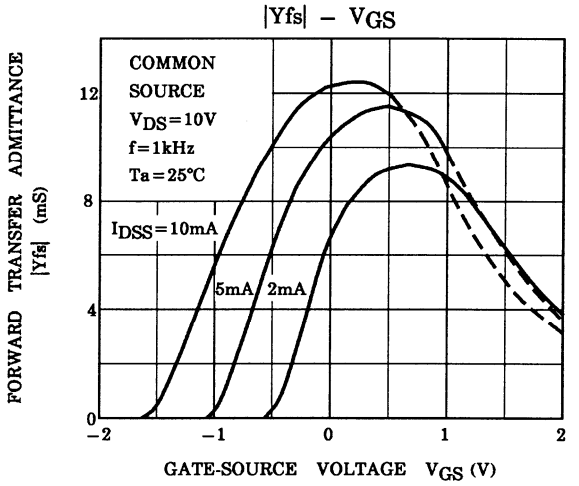
$I_D - V_{DS}$ (LOW VOLTAGE REGION)



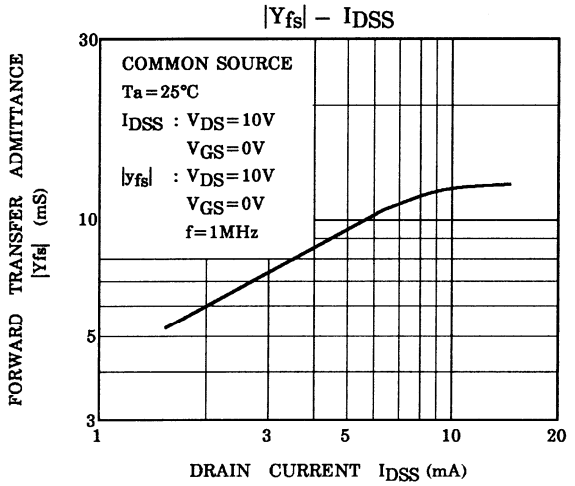
$I_D - V_{GS}$



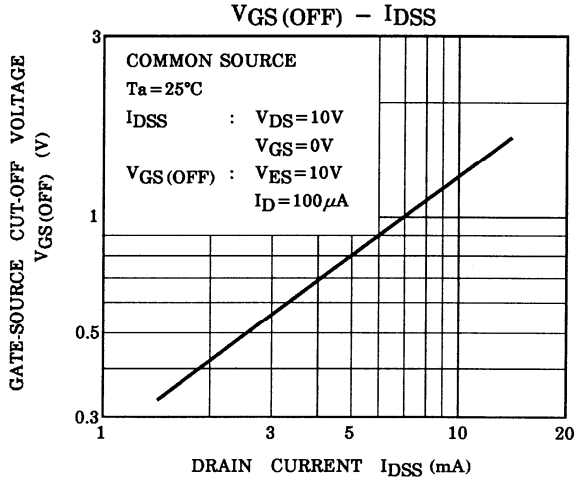
$|Y_{fs}| - V_{GS}$



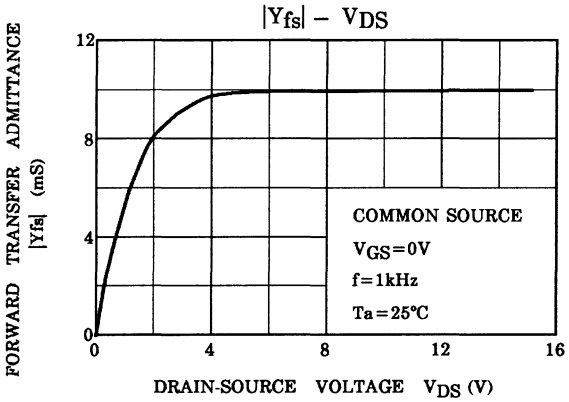
$|Y_{fs}| - I_{DSS}$



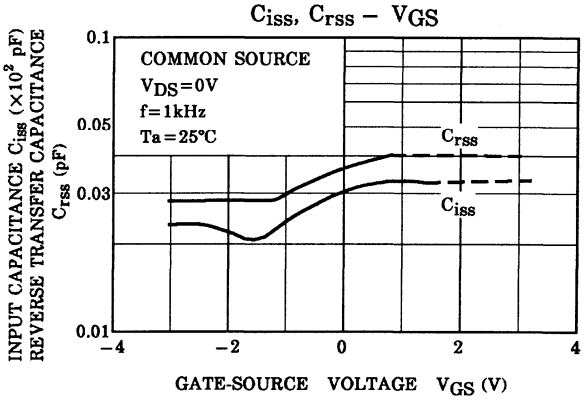
$V_{GS\,(OFF)} - I_{DSS}$



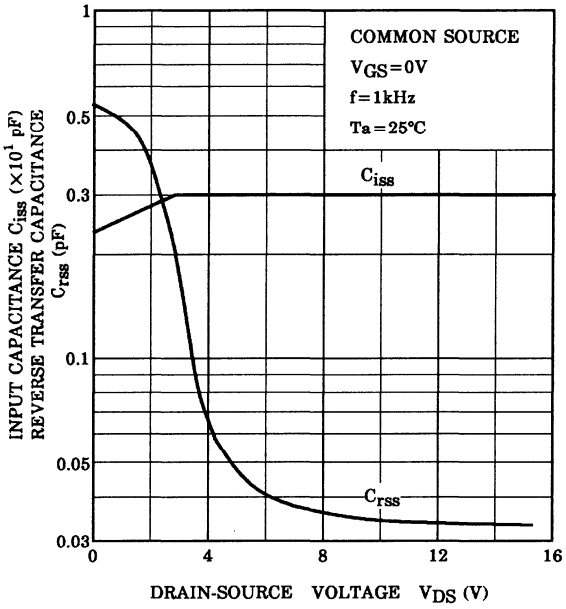
$|Y_{fs}|$ – V_{DS}



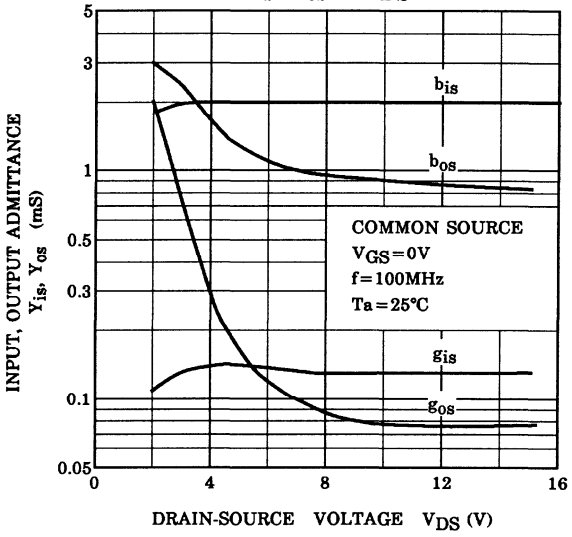
C_{iss}, C_{rss} – V_{GS}



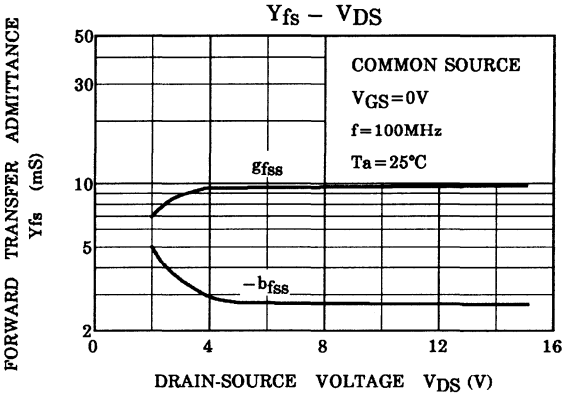
C_{iss}, C_{rss} – V_{DS}



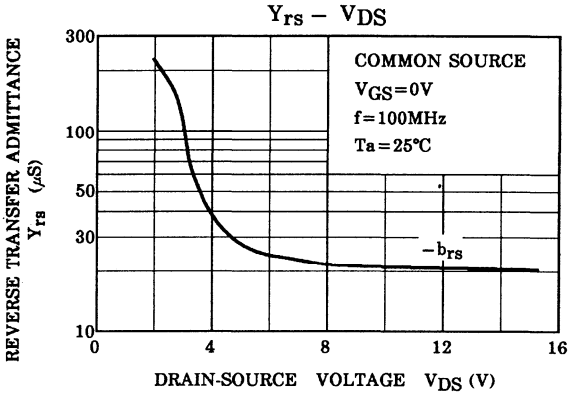
Y_{is}, Y_{os} – V_{DS}



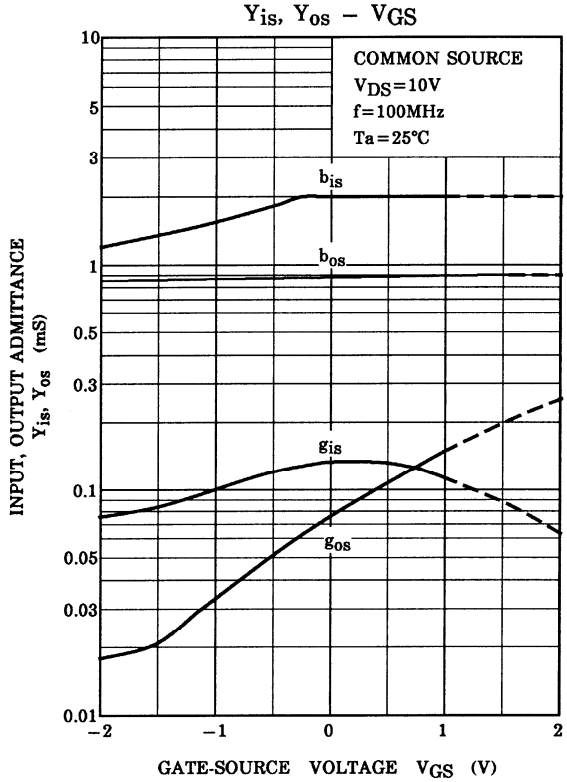
Y_{fs} – V_{DS}



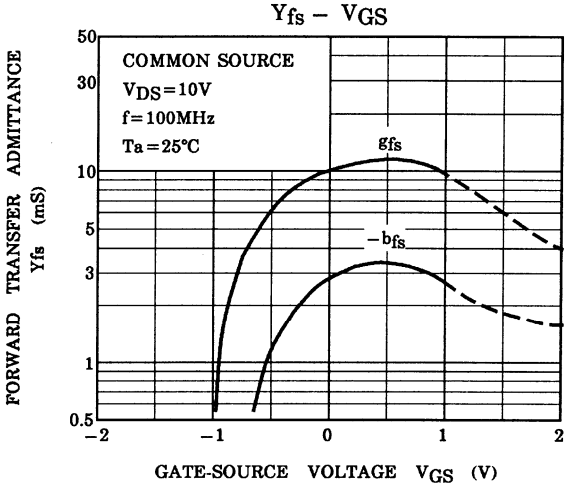
Y_{rs} – V_{DS}



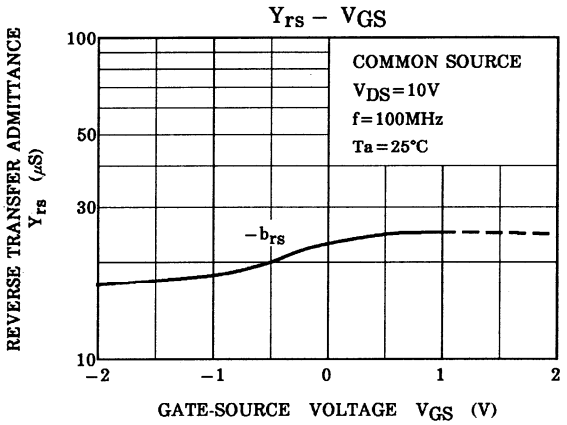
Y_{is}, Y_{os} – V_{GS}



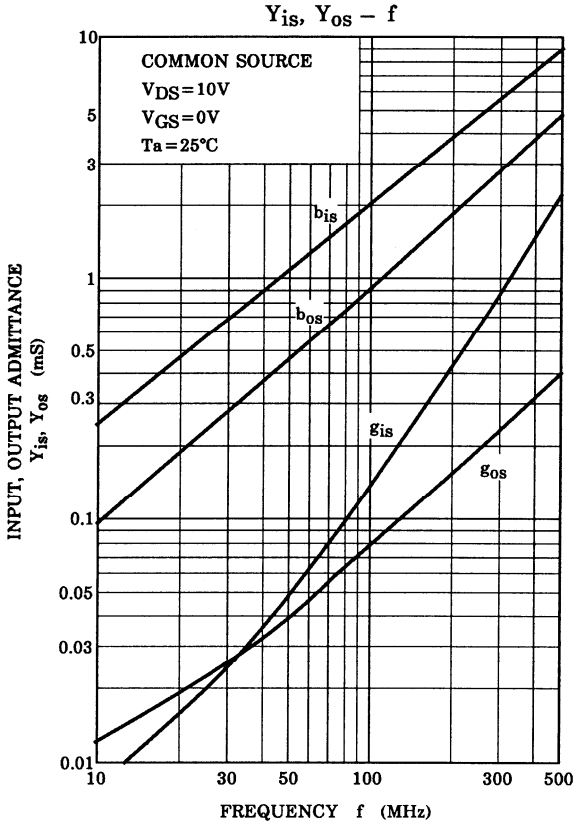
Y_{fs} – V_{GS}



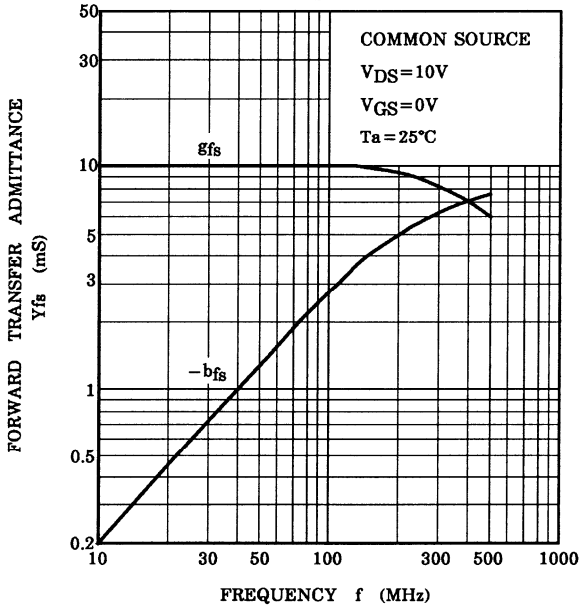
Y_{rs} – V_{GS}



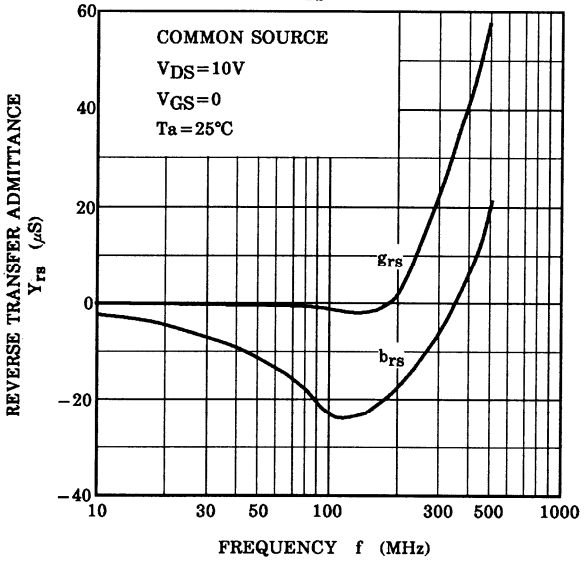
Y_{is}, Y_{os} – f



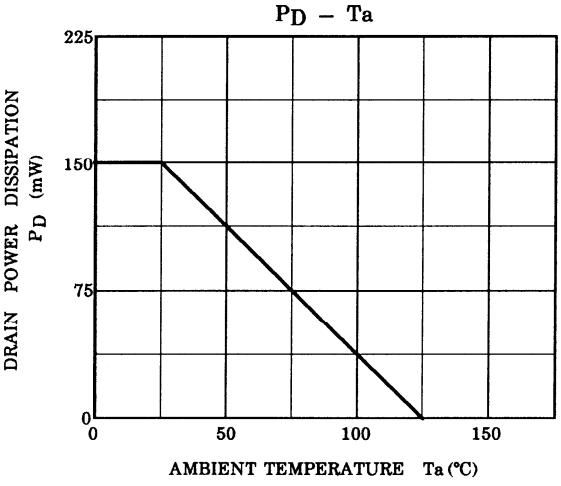
Y_{fs} – f



Y_{rs} – f



P_D – Ta



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