



# 2N7002PS

60 V, 320 mA dual N-channel Trench MOSFET

23 November 2020

Product data sheet

## 1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

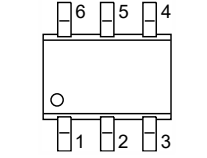
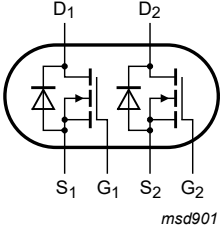
Table 1. Quick reference data

| Symbol   | Parameter                        | Conditions   | Min | Typ | Max | Unit     |
|--|----------------------------------|--|-----|-----|-----|----------|
| <b>Per transistor</b>                          |                                  |  |     |     |     |          |
| $V_{DS}$                                       | drain-source voltage             | $T_{amb} = 25\text{ °C}$   | -   | -   | 60  | V        |
| $V_{GS}$                                       | gate-source voltage              |  | -20 | -   | 20  | V        |
| $I_D$  | drain current                    | $V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$   | [1] | -   | 320 | mA       |
| <b>Static characteristics (per transistor)</b> |                                  |  |     |     |     |          |
| $R_{DSon}$                                     | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 500\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01; T_j = 25\text{ °C}$ | -   | 1   | 1.6 | $\Omega$ |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline   | Graphic symbol  |
|-----|--------|-------------|--|---|
| 1   | S1     | source1     |  <p>TSSOP6 (SOT363)</p> |  <p>msd901</p> |
| 2   | G1     | gate1       |  |   |
| 3   | D2     | drain2      |  |   |
| 4   | S2     | source2     |  |   |
| 5   | G2     | gate2       |  |   |
| 6   | D1     | drain1      |  |   |

## 6. Ordering information

Table 3. Ordering information

| Type number | Package |   |         |
|-------------|---------|---|---------|
|             | Name    | Description   | Version |
| 2N7002PS    | TSSOP6  | plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body | SOT363  |

## 7. Marking

Table 4. Marking codes

| Type number | Marking code <sup>[1]</sup> |
|-------------|-----------------------------|
| 2N7002PS    | M8%                         |

[1] % = placeholder for manufacturing site code

## 8. Limiting values

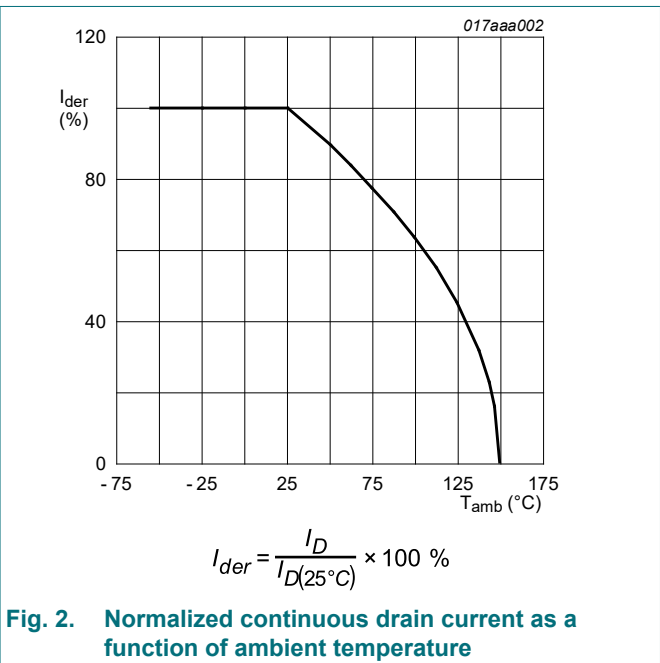
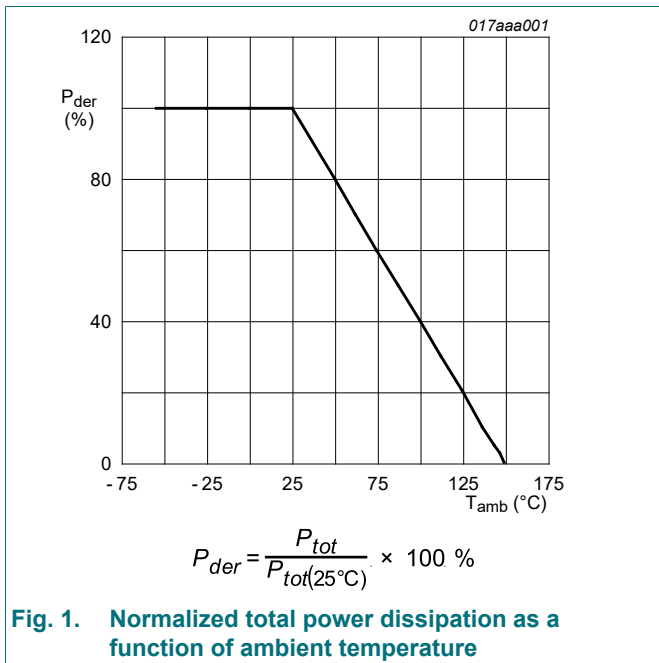
**Table 5. Limiting values**

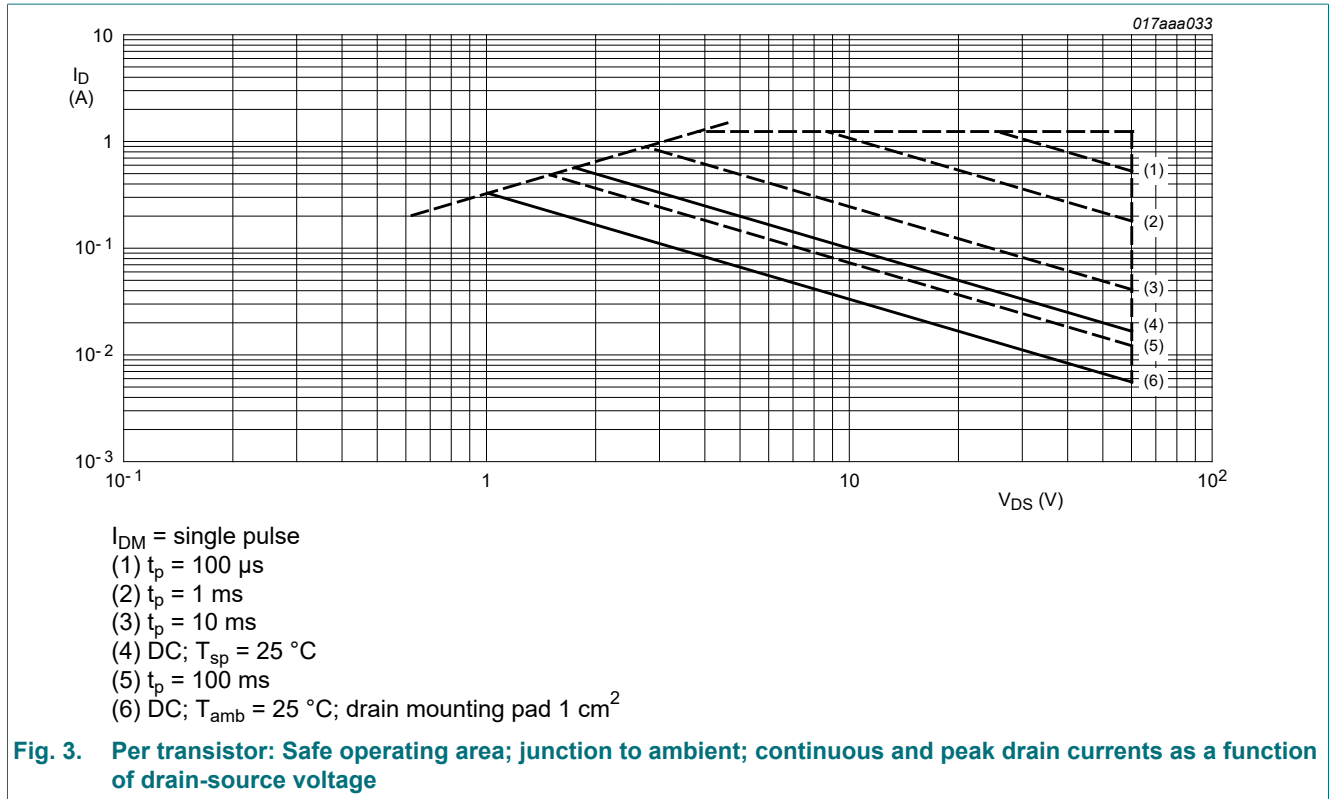
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                    | Parameter               | Conditions   |     | Min | Max | Unit |
|---------------------------|-------------------------|--|-----|-----|-----|------|
| <b>Per transistor</b>     |                         |  |     |     |     |      |
| V <sub>DS</sub>           | drain-source voltage    | T <sub>amb</sub> = 25 °C                                       |     | -   | 60  | V    |
| V <sub>GS</sub>           | gate-source voltage     |  |     | -20 | 20  | V    |
| I <sub>D</sub>            | drain current           | V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C               | [1] | -   | 320 | mA   |
|                           |                         | V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C              | [1] | -   | 240 | mA   |
| I <sub>DM</sub>           | peak drain current      | T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs |     | -   | 1.2 | A    |
| P <sub>tot</sub>          | total power dissipation | T <sub>amb</sub> = 25 °C                                       | [2] | -   | 280 | mW   |
|                           |                         |  | [1] | -   | 320 | mW   |
|                           |                         | T <sub>sp</sub> = 25 °C  |     | -   | 990 | mW   |
| <b>Per device</b>         |                         |  |     |     |     |      |
| P <sub>tot</sub>          | total power dissipation | T <sub>amb</sub> = 25 °C                                       | [2] | -   | 420 | mW   |
| T <sub>j</sub>            | junction temperature    |  |     | -   | 150 | °C   |
| T <sub>amb</sub>          | ambient temperature     |  |     | -55 | 150 | °C   |
| T <sub>stg</sub>          | storage temperature     |  |     | -65 | 150 | °C   |
| <b>Source-drain diode</b> |                         |  |     |     |     |      |
| I <sub>S</sub>            | source current          | T <sub>amb</sub> = 25 °C                                       | [1] | -   | 320 | mA   |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





## 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol                | Parameter  | Conditions  | Min | Typ | Max | Unit |
|-----------------------|--|-------------|-----|-----|-----|------|
| <b>Per device</b>     |  |             |     |     |     |      |
| $R_{th(j-a)}$         | thermal resistance from junction to ambient      | in free air | [1] | -   | 300 | K/W  |
| <b>Per transistor</b> |  |             |     |     |     |      |
| $R_{th(j-a)}$         | thermal resistance from junction to ambient      | in free air | [1] | 390 | 445 | K/W  |
|                       |  |             | [2] | 340 | 390 | K/W  |
| $R_{th(j-sp)}$        | thermal resistance from junction to solder point |             | -   | -   | 130 | K/W  |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

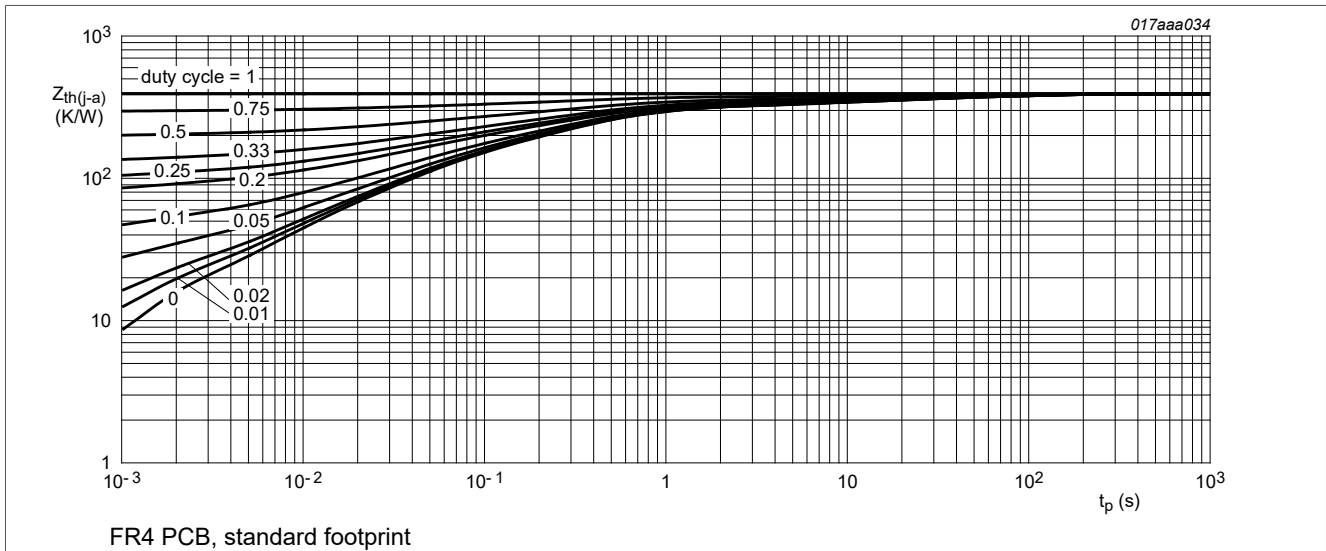


Fig. 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

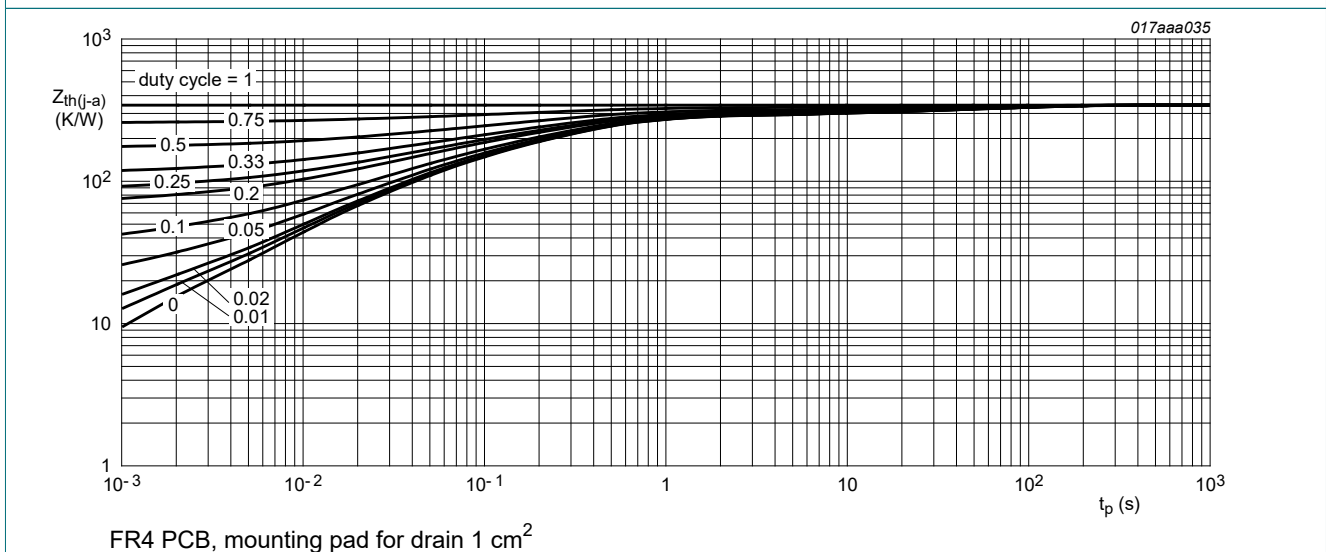
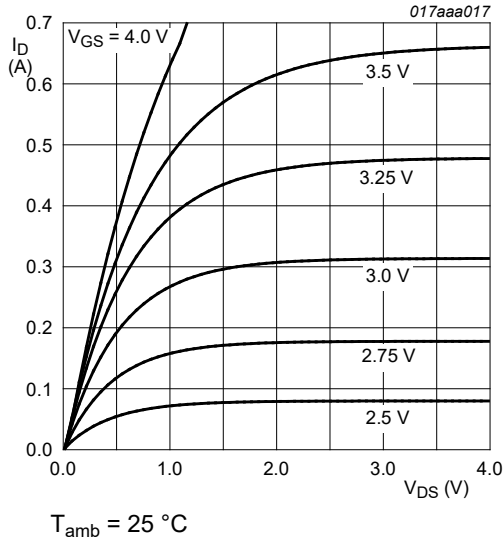


Fig. 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

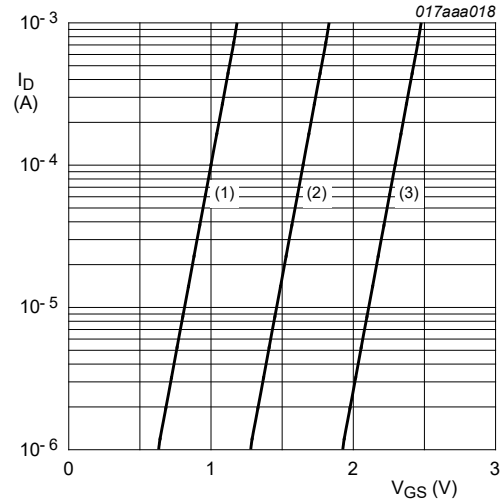
## 10. Characteristics

**Table 7. Characteristics**

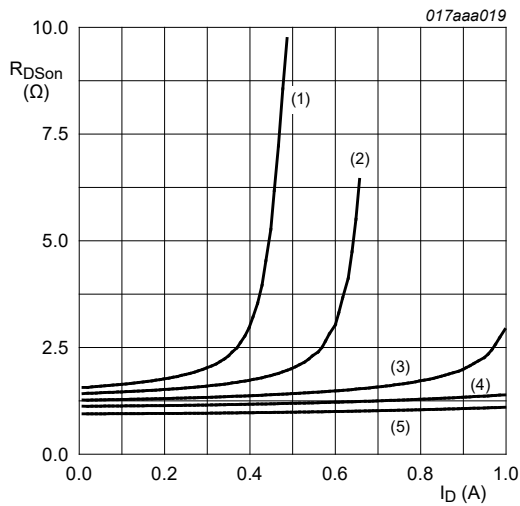
| Symbol  | Parameter                        | Conditions  | Min  | Typ  | Max  | Unit          |
|---|----------------------------------|---|------|------|------|---------------|
| <b>Static characteristics (per transistor)</b>  |                                  |   |      |      |      |               |
| $V_{(BR)DSS}$                                   | drain-source breakdown voltage   | $I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | 60   | -    | -    | V             |
| $V_{GSth}$                                      | gate-source threshold voltage    | $I_D = 250 \mu\text{A}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$   | 1.1  | 1.75 | 2.4  | V             |
| $I_{DSS}$                                       | drain leakage current            | $V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -    | -    | 1    | $\mu\text{A}$ |
|   |                                  | $V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$   | -    | -    | 10   | $\mu\text{A}$ |
| $I_{GSS}$                                       | gate leakage current             | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -    | -    | 100  | nA            |
|   |                                  | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -    | -    | -100 | nA            |
| $R_{DSon}$                                      | drain-source on-state resistance | $V_{GS} = 5 \text{ V}; I_D = 50 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; T_j = 25 \text{ }^\circ\text{C}$   | -    | 1.3  | 2    | $\Omega$      |
|   |                                  | $V_{GS} = 10 \text{ V}; I_D = 500 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; T_j = 25 \text{ }^\circ\text{C}$ | -    | 1    | 1.6  | $\Omega$      |
| $g_{fs}$  | forward transconductance         | $V_{DS} = 10 \text{ V}; I_D = 200 \text{ mA}; \text{pulsed}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; T_j = 25 \text{ }^\circ\text{C}$ | -    | 400  | -    | mS            |
| <b>Dynamic characteristics (per transistor)</b> |                                  |   |      |      |      |               |
| $Q_{G(tot)}$                                    | total gate charge                | $V_{DS} = 30 \text{ V}; I_D = 300 \text{ mA}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$                                    | -    | 0.6  | 0.8  | nC            |
| $Q_{GS}$  | gate-source charge               |   | -    | 0.2  | -    | nC            |
| $Q_{GD}$  | gate-drain charge                |   | -    | 0.2  | -    | nC            |
| $C_{iss}$                                       | input capacitance                | $V_{DS} = 10 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -    | 30   | 50   | pF            |
| $C_{oss}$                                       | output capacitance               |   | -    | 7    | -    | pF            |
| $C_{rss}$                                       | reverse transfer capacitance     |   | -    | 4    | -    | pF            |
| $t_{d(on)}$                                     | turn-on delay time               | $V_{DS} = 50 \text{ V}; R_L = 250 \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ\text{C}$                  | -    | 3    | 6    | ns            |
| $t_r$   | rise time                        |   | -    | 4    | -    | ns            |
| $t_{d(off)}$                                    | turn-off delay time              |   | -    | 10   | 20   | ns            |
| $t_f$   | fall time                        |   | -    | 5    | -    | ns            |
| <b>Source-drain diode (per transistor)</b>      |                                  |   |      |      |      |               |
| $V_{SD}$  | source-drain voltage             | $I_S = 115 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | 0.47 | 0.75 | 1.1  | V             |



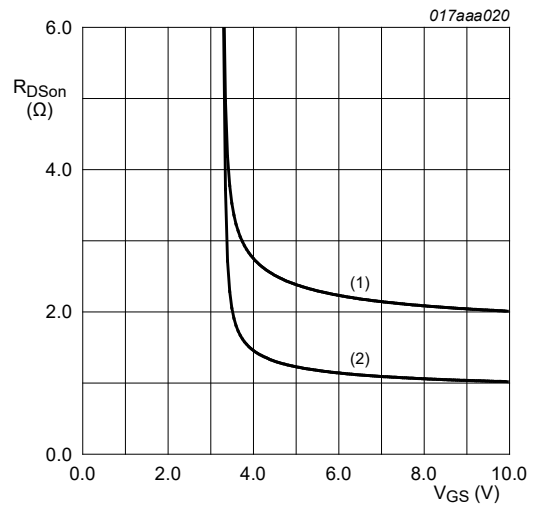
**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**  
 (1) minimum values  
 (2) typical values  
 (3) maximum values



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**

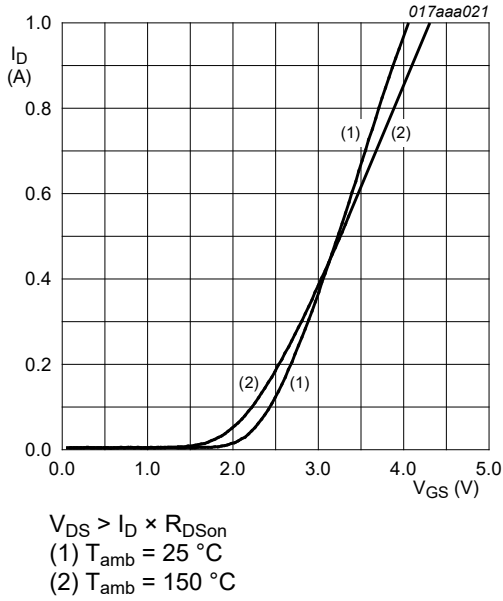


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

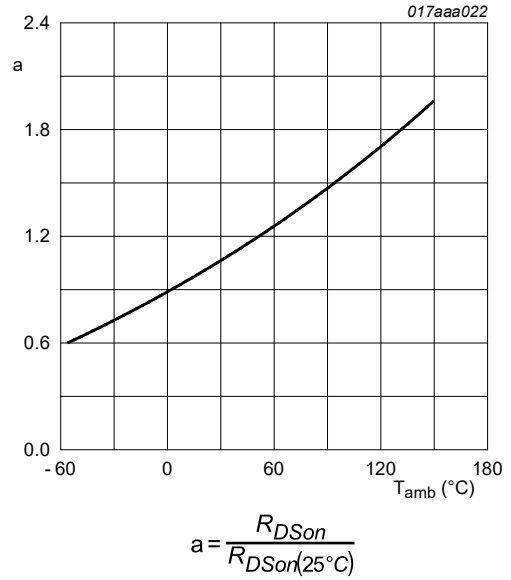


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

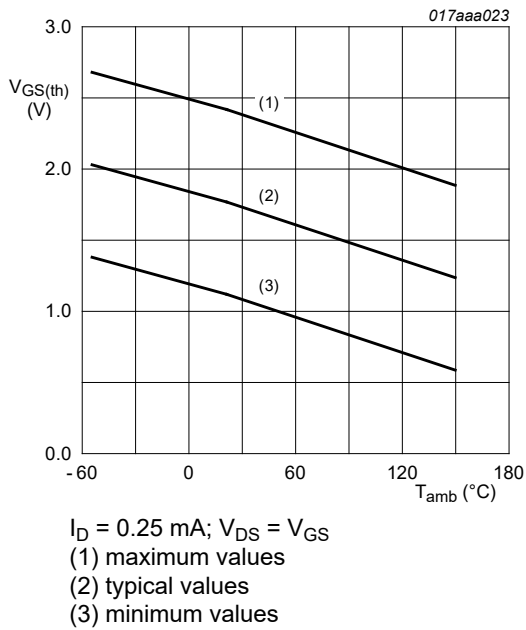


Fig. 12. Gate-source threshold voltage as a function of ambient temperature

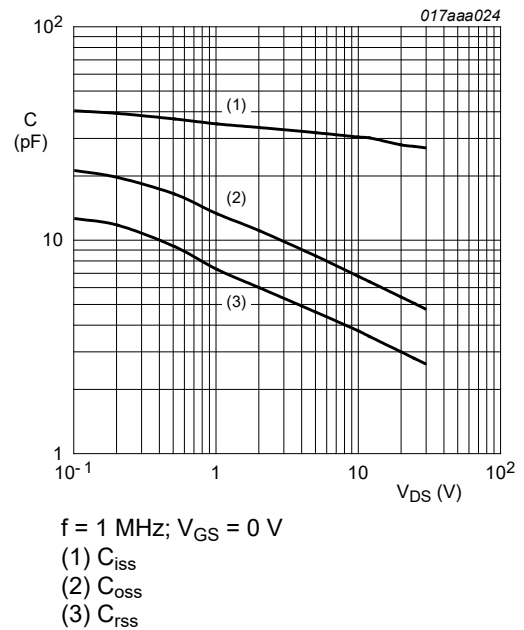
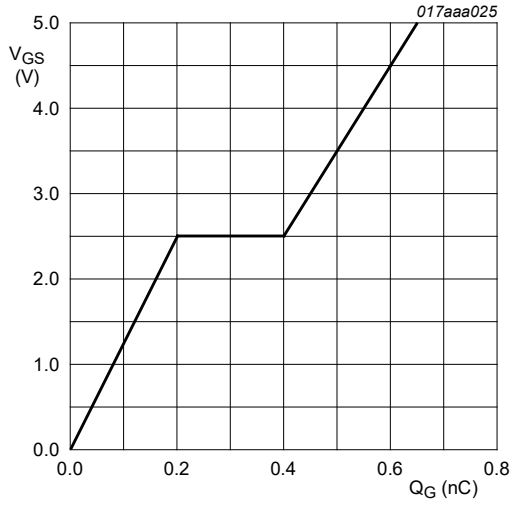


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = 300$  mA;  $V_{DS} = 30$  V;  $T_{amb} = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

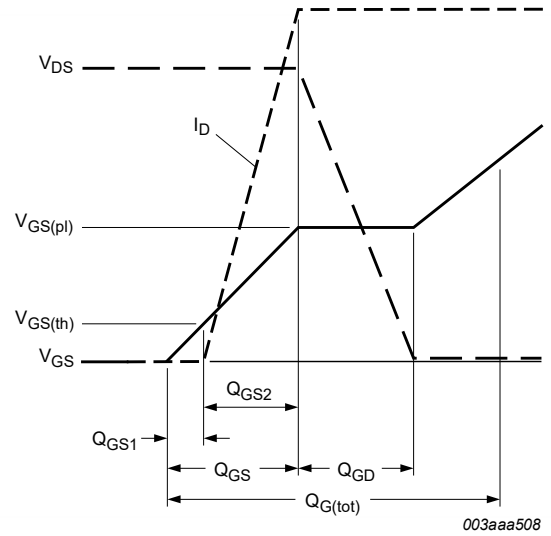
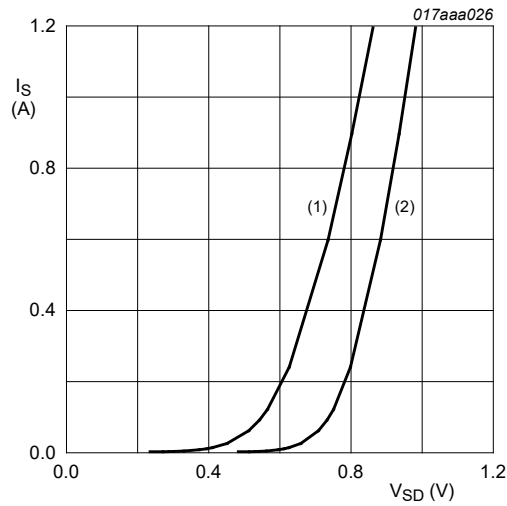


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V  
 (1)  $T_{amb} = 150$  °C  
 (2)  $T_{amb} = 25$  °C

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information



Fig. 17. Duty cycle definition

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

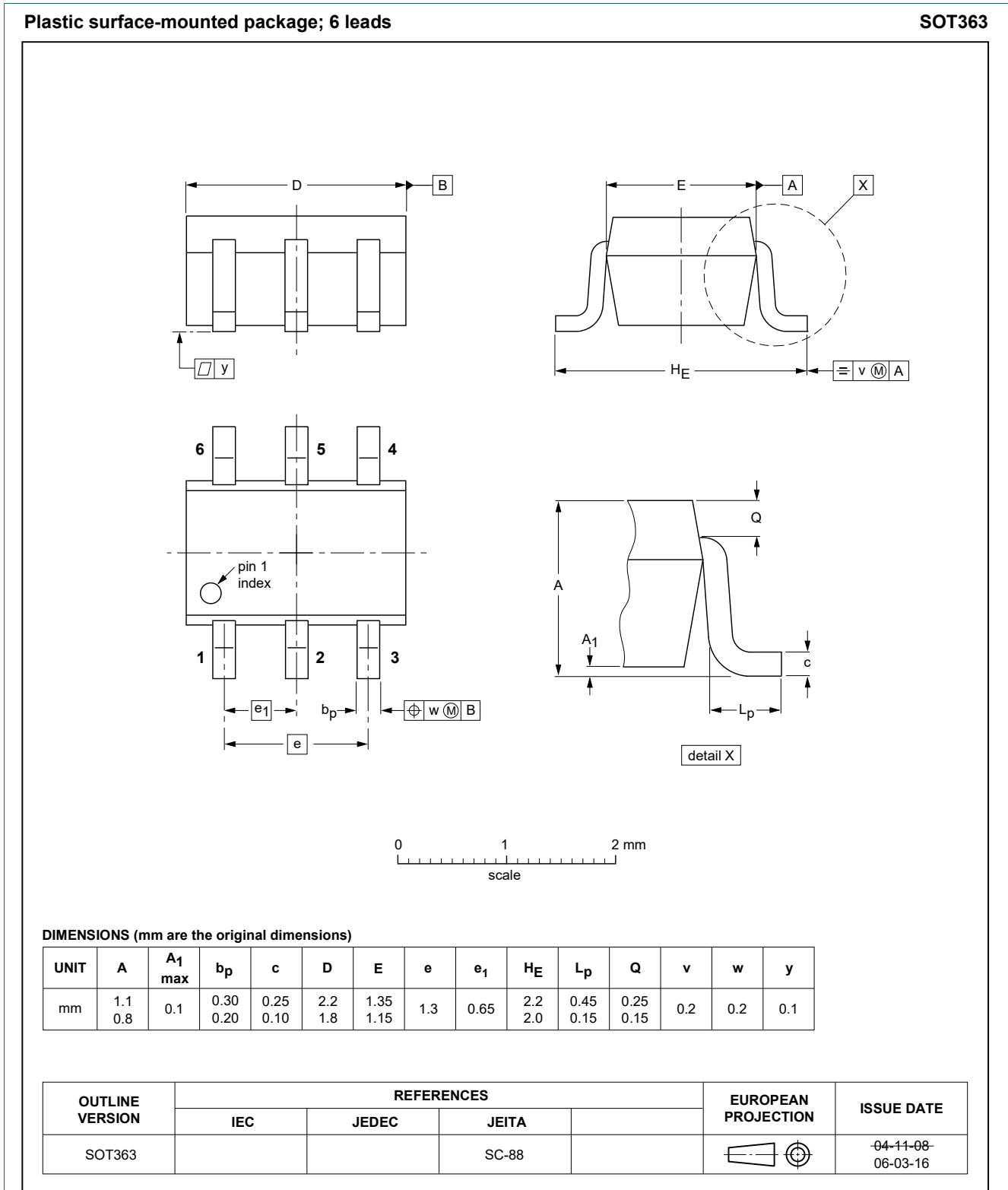


Fig. 18. Package outline TSSOP6 (SOT363)

### 13. Soldering

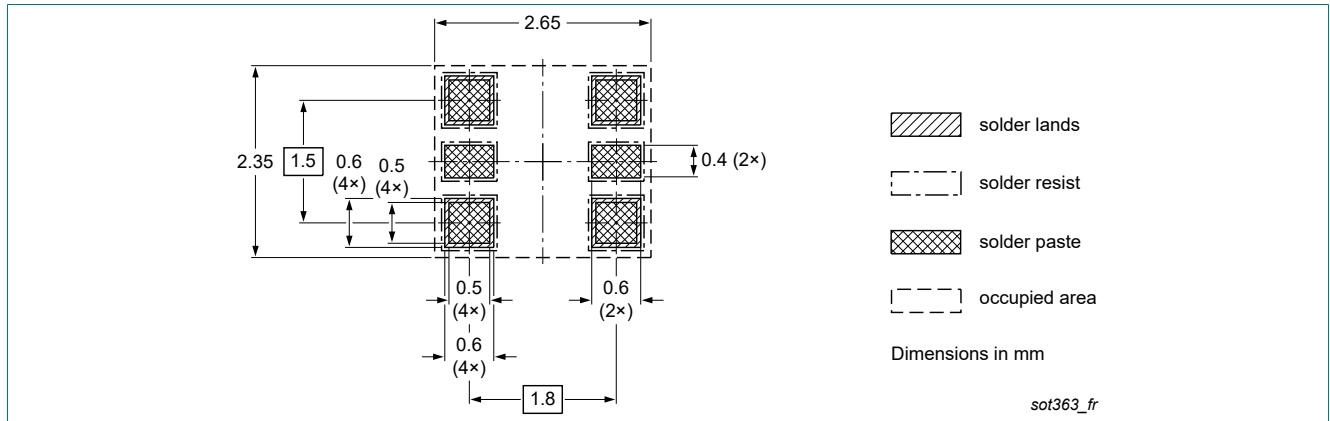


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

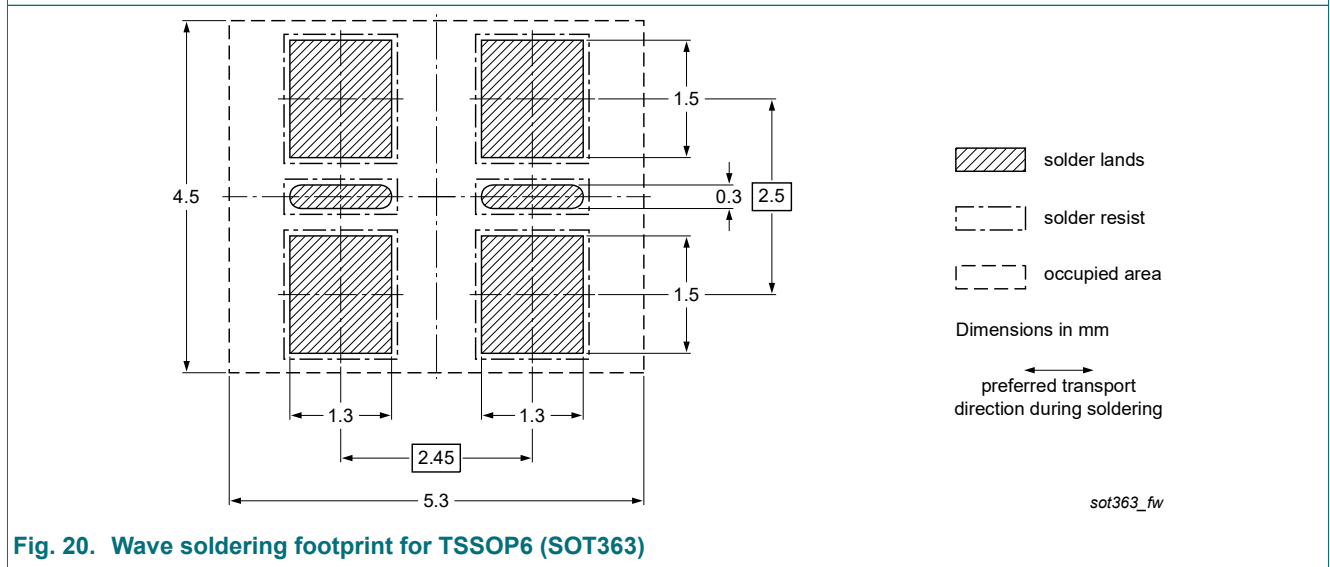


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

## 14. Revision history

**Table 8. Revision history**

| Data sheet ID  | Release date  | Data sheet status  | Change notice | Supersedes   |
|----------------|---|--------------------|---------------|--------------|
| 2N7002PS v.2   | 20201123  | Product data sheet | -             | 2N7002PS v.1 |
| Modifications: | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Chapter "Characteristics": Typo correction for <math>I_{GSS}</math> and switching times.</li></ul> |                    |               |              |
| 2N7002PS v.1   | 20100701  | Product data sheet | -             | -            |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 23 November 2020

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