EiceDRIVER™ Compact

High voltage gate driver IC

2EDL family

600 V half bridge gate drive IC
2EDL05I06PF
2EDL05I06PJ
2EDL05I06BF
2EDL05N06PF
2EDL05N06PJ

EiceDRIVER™ Compact

Final datasheet

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
<Revision 0.85>, 16.04.2013	
all	change term VCC in VDD
pp.16	Introduced Iopk+ and Iopk- values
all	introduced 2EDL05N06PJ
all	introduced 2EDL05I06PJ
<Revision 2.6>, 01.06.2016	
Update maximum Ta from 95°C to 105°C in Table 5	

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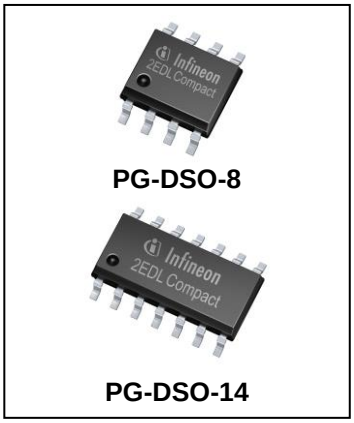
EiceDRIVER™ Compact
600 V half bridge gate drive IC



1 Overview

Main features

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Individual control circuits for both outputs
- Filtered detection of under voltage supply
- All inputs clamped by diodes
- Active shut down function
- Asymmetric undervoltage lockout thresholds for high side and low side
- Qualified according to JEDEC[1] (high temperature stress tests for 1000h) for target applications

Product highlights

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Ultra fast bootstrap diode

Typical applications

- Home appliances
- Consumer electronics
- Fans, pumps
- General purpose drives

Product family

Table 1 Members of 2EDL family

Sales Name	Special function	output current	Target transistor	typ. LS UVLO-thresholds	Bootstrap diode	Package
2EDL05I06PF 2EDL05I06PJ	deadtime, interlock	0.5 A	IGBT	12.5 V / 11.6 V	Yes	DSO-8 DSO-14
2EDL05I06BF	–	0.5 A	IGBT	12.5 V / 11.6 V	Yes	DSO-8
2EDL05N06PF 2EDL05N06PJ	deadtime, interlock	0.5 A 0.5 A	MOSFET	9.1 V / 8.3 V	Yes	DSO-8 DSO-14

[1] J-STD-020 and JESD-022

Description

The 2EDL family contains devices, which control power devices like MOS-transistors or IGBTs with a maximum blocking voltage of +600V in half bridge configurations. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

The two independent drivers outputs are controlled at the low-side using two different CMOS resp. LSTTL compatible signals, down up to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic which are optimised either for IGBT or MOSFET.

Those parts, which are designed for IGBT have asymmetric undervoltage lockout levels, which support strongly the integrated ultrafast bootstrap diode. Additionally, the offline gate clamping function provides an inherent protection of the transistors for parasitic turn-on by floating gate conditions, when the IC is not supplied via VDD.

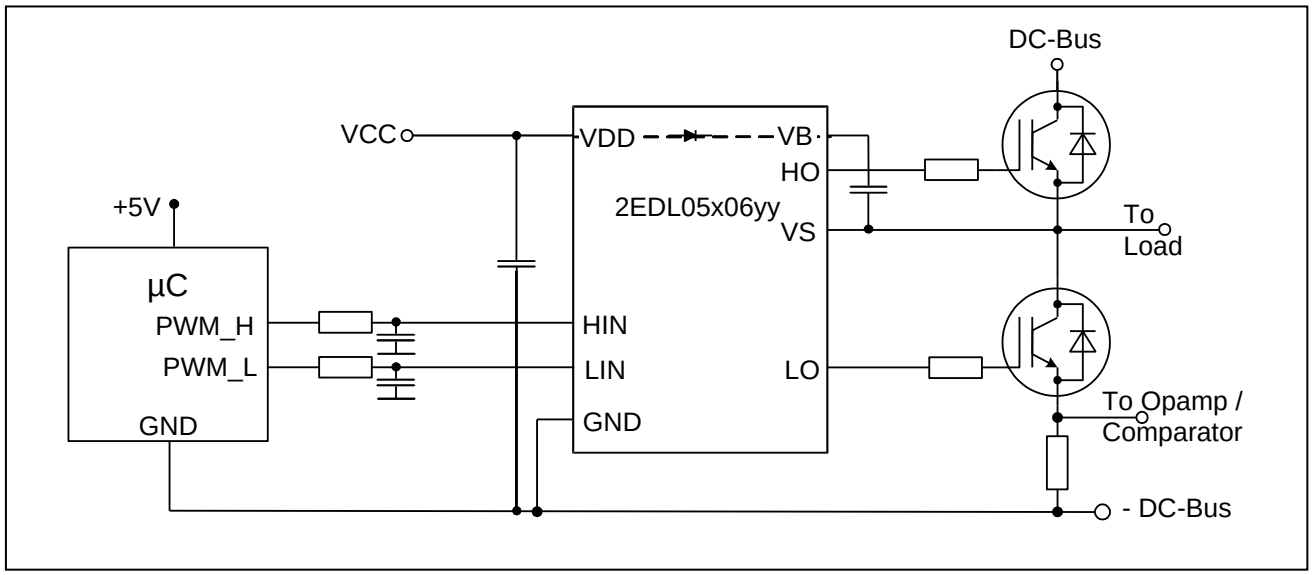


Figure 1 Typical Application
SO8 / SO14 package 0.5 A

2 Blockdiagram

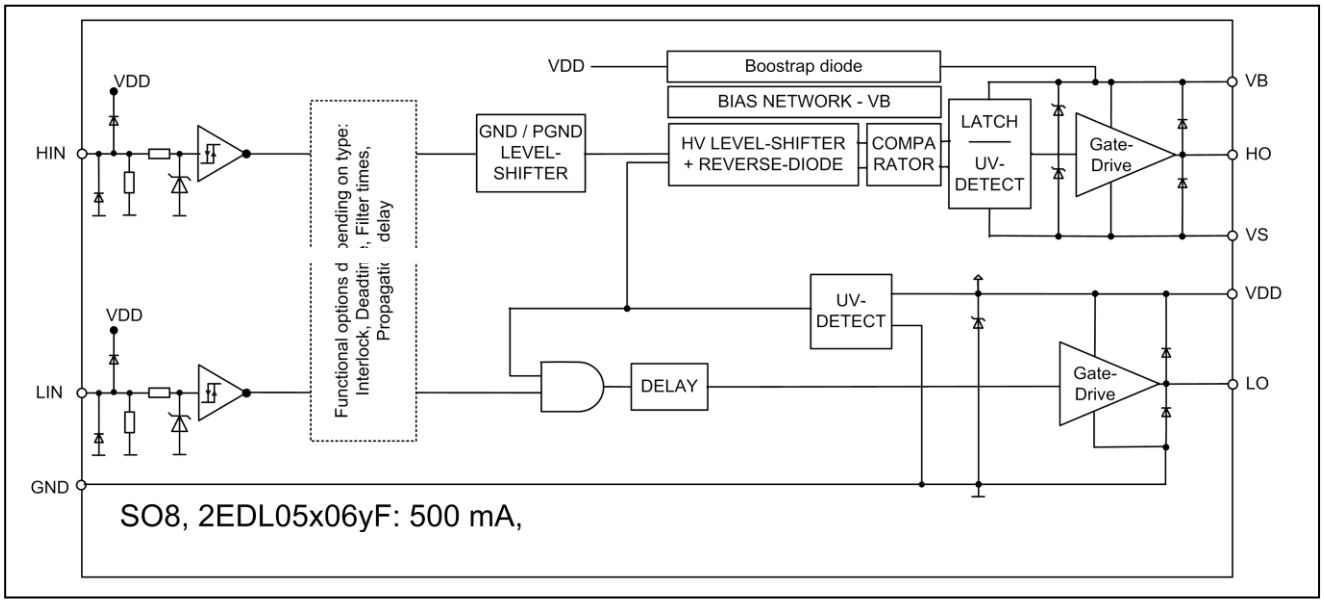


Figure 2 Block diagram for 2EDL05x06Py

3 Pin configuration, description, and functionality

3.1 Pin Configuration and Description

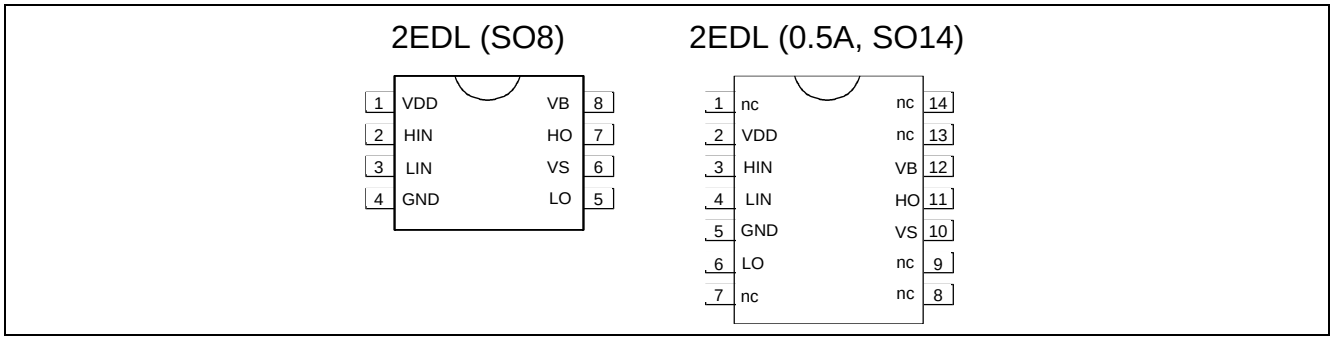


Figure 3 Pin Configuration of 2EDL family

Table 2 Pin Description

Symbol	Description
VDD	Low side power supply
GND	Logic ground
HIN	High side logic input
LIN	Low side logic input
VB	High side positive power supply
HO	High side gate driver output
VS	High side negative power supply
LO	Low side gate driver output
nc	Not Connected

3.2 Low Side and High Side Control Pins (LIN, HIN)

3.2.1 Input voltage range

All input pins have the capability to process input voltages up to the supply voltage of the IC. The inputs are therefore internally clamped to VDD and GND by diodes. An internal pull-down resistor is high ohmic, so that it can keep the IC in a safe state in case of PCB crack.

3.2.2 Switching levels

The Schmitt trigger input threshold is such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. The input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4 and Figure 5. Please note, that the switching levels of the input structures remain constant even though they can accept amplitudes up to the IC supply level.

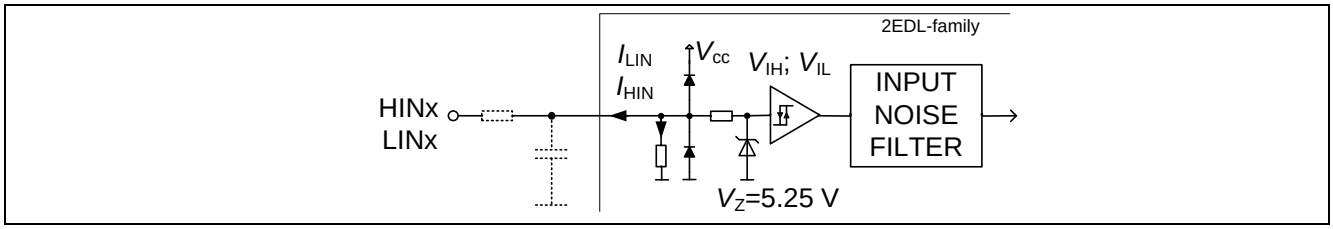


Figure 4 Input pin structure

3.2.3 Input filter time

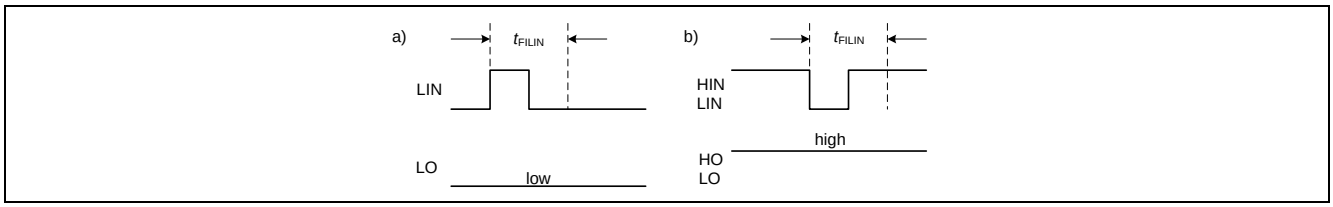


Figure 5 Input filter timing diagram

Short pulses are suppressed by means of an input filter. All IC, which have undervoltage lockout (UVLO) thresholds for MOSFET, have an input filter time of t_{FILIN} = 75ns typ. and 150ns max. All IC having UVLO thresholds for IGBT have filter times of t_{FILIN} = 150ns min and 200ns typ.

3.3 VDD and GND

VDD is the low side supply and it provides power to both the input logic and the low side output power stage. The input logic is referenced to GND ground as well as the under-voltage detection circuit. Output power stage is also referenced to GND ground.

The undervoltage lockout circuit enables the device to operate at power on when a typical supply voltage higher than V_{DDUV+} is present. Please see section 3.6 “Undervoltage lockout”” for further information.

A filter time of typ. 1.8µs[1] helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

3.4 VB and VS (High Side Supplies)

VB to VS is the high side supply voltage. The high side circuit can float with respect to GND following the external high side power device emitter/source voltage. Due to the low power consumption, the floating driver stage can be supplied by bootstrap topology connected to VDD. A filter time of typ. 1.8µs[1] helps to suppress noise from the UVLO circuit, so that negative going voltage spikes at the supply pins will avoid parasitic UVLO events.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage higher than V_{DDUV+} is present. Please see section 3.6 “Undervoltage lockout” for further information. Details on bootstrap supply section and transient immunity can be found in application note EiceDRIVER™ 2EDL family: Technical description.

3.5 LO and HO (Low and High Side Outputs)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive for IGBT and MOSFET devices. Low side output is state triggered by the respective input, while high side output is edge triggered by the respective input. In particular, after an undervoltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the high side output. In contrast, the low side outputs switch to the state of their respective inputs after an undervoltage condition of the VDD supply.

The output current specification I_{O+} and I_{O-} is defined in a way, which considers the power transistors miller voltage.This helps to design the gate drive better in terms of the application needs. Nevertheless, the devices are also characterised for the value of the pulse short circuit value I_{Opk+} and $I_{Opk–}$.

3.6 Undervoltage lockout (UVLO)

Two different UVLO options are required for IGBT and MOSFET. The types 2EDL05I06Px and 2EDL05I06BF are designed to drive IGBT. There are higher levels of undervoltage lockout for the low side UVLO than for the high side. This supports an improved start up of the IC, when bootstrapping is used. The thresholds for the low side are typically V_{DDUV+} = 12.5 V (positive going) and V_{DDUV-} = 11.6 V (negative going). The thresholds for the high side are typically V_{BSUV+} = 11.6 V (positive going) and V_{BSUV-} = 10.7 V (negative going).

The types 2EDL05N06Px are designed to drive power MOSFET. A similar distinction for the high side and low side UVLO threshold as for IGBT is not realised here. The IC shuts down all the gate drivers power outputs, when the supply voltage is below typ. V_{DDUV-} = 8.3 V (min. / max. = 7.5 V / 9 V). The turn-on threshold is typ. V_{DDUV+} = 9.1 V (min. / max. = 8.3 V / 9.9 V)

3.7 Bootstrap diode

An ultra fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when charging the bootstrap capacitor initially.

3.8 Deadtime and interlock function

The IC provides a hardware fixed deadtime. The deadtime is different for the two MOSFET types (2EDL05N06Px) and for the two IGBT types (2EDL05I06Px). The deadtimes are particularly typ. 380 ns for IGBT and typ. 75 ns for MOSFET. An additional interlock function prevents the two outputs from being activated simultaneously.

The part 2EDL05I06BF does not have the deadtime feature and also not the interlock function. Here, the two outpus can be activated simultaneously.

[1] Not subject of production test, verified by characterisation

4 Electrical Parameters

4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a=25°C)

Table 3 Abs. maximum ratings

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage(Note 1)		V_S	V_{DD}-V_{BS}-6	600	V
High side offset voltage (t_p<500ns, Note 1)			V_{DD} -V_{BS} – 50	–	
High side offset voltage(Note 1)		V_B	V_{DD} – 6	620	
High side offset voltage (t_p<500ns, Note 1)			V_{DD} – 50	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)		V_{DD}	-1	20	
Low side output voltage (V_{LO} vs. V_{GND})		V_{LO}	-0.5	V_{GND} + 0.5	
Input voltage LIN,HIN		V_{IN}	-0.5	V_{DD} + 0.5	
Power dissipation (to package) (Note 2)	DSO8 DSO14	P_D	– –	0.6 0.85	W
Thermal resistance (junction to ambient, see section 6)	DSO8 DSO14	$R_{th(j-a)}$	– –	195 139	K/W
Junction temperature (Note 3)		T_J	–	150	°C
Storage temperature		T_S	- 40	150	
offset voltage slew rate (Note 4)		dV_S/dt	–	50	V/ns

Note :The minimum value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side (VDD, HIN, LIN, GND, LO) and pins connected inside each high side itself (VB, HO, VS) is guaranteed up to 1.5kV (Human Body Model) respectively.

Note 1 : In case V_{DD} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VDD and VB in case of activated bootstrap diode. Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization.

Note 2: Consistent power dissipation of all outputs. All parameters are inside operating range.

Note 3: Qualification stress tests cover a max. junction temperature of 150°C for 1000 h.

Note 4: Not subject of production test, verified by characterisation.

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a = 25°C)

Table 4 Required Operation Conditions

Parameter	Symbol	Min.	Max.	Unit
High side offset voltage (Note 1)	V_B	7	620	V
Low side supply voltage (internally clamped)	V_{DD}	10	20	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{GND} -potential unless otherwise specified. (T_a = 25°C)

Table 5 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{DD} - V_{BS} -1	500	V
High side floating supply offset voltage (V_B vs. V_{DD}, statically)		V_{BDD}	-1.0	500	
High side floating supply voltage (V_B vs. V_S, Note 1)	IGBT-Types	V_{BS}	13	17.5	
	MOSFET-Types		10	17.5	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	10	V_{BS}	
Low side output voltage (V_{LO} vs. V_{GND})		V_{LO}	0	V_{DD}	
Low side supply voltage	IGBT-Types	V_{DD}	13	17.5	
	MOSFET-Types		10	17.5	
Logic input voltages LIN,HIN (Note 2)		V_{IN}	0	17.5	
Pulse width for ON or OFF (Note 3)	IGBT-Types	t_{IN}	0.8	–	µs
	MOSFET-Types		0.3	–	
Ambient temperature		T_a	-40	105	°C
Thermal coefficient (junction to top, see section 6)	DSO8 DSO14	$\Psi_{th(j\text{-}top)}$	– –	8.0 6.0	K/W

Note 1 : Logic operational for V_B (V_B vs. V_{GND}) > 7.0V

Note 2 : All input pins (HIN, LIN) are internally clamped (see abs. maximum ratings)

Note 3 : The input pulse may not be transmitted properly in case of input pulse width at LIN and HIN below 0.8µs (IGBT types) or 0.3 µs (MOSFET) respectively

4.4 Static logic function table

VDD	VBS	LO	HO
$<V_{DDUV-}$	X	0	0
15V	$<V_{BSUV-}$	LIN	0
15V	15V	0	0
15V	15V	0	0
15V	15V	LIN	HIN

all voltages with reference to GND

4.5 Static parameters

V_{DD} = V_{BS} = 15V unless otherwise specified. (T_a = 25°C)

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
High level output voltage	LO HO	V_{OH}	– –	V_{DD} -0.45 V_B -0.45	V_{DD} -1 V_B -1		I_O = - 20 mA
Low level output voltage	LO HO	V_{OL}	– –	V_{GND}+0.13 V_S+0.13	V_{GND}+0.3 V_S +0.3		I_O = 20 mA
V_{DD} supply undervoltage positive going threshold	IGBT-types	V_{DDUV+}	11.8	12.5	13.2		
	MOSFET types		8.3	9.1	9.9		
V_{BS} supply undervoltage positive going threshold	IGBT-types	V_{BSUV+}	10.9	11.6	12.4		
	MOSFET types		8.3	9.1	9.9		
V_{DD} supply undervoltage negative going threshold	IGBT-types	V_{DDUV-}	10.9	11.6	12.4		
	MOSFET types		7.5	8.3	9		
V_{BS} supply undervoltage negative going threshold	IGBT-types	V_{BSUV-}	10	10.7	11.7		
	MOSFET types		7.5	8.3	9		
V_{DD} and V_{BS} supply UVLO hysteresis	IGBT-types	V_{DDUVH}	0.5	0.9	–		
	MOSFET types	V_{BSUVH}	0.5	0.9	–		
High side leakage current betw. VS and GND		I_{LVS+}	–	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and GND		I_{LVS+} [1]	–	10	–		T_J = 125 °C, V_S = 600 V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	–	170	300		HO = low depending on current types
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	–	170	300		HO = high depending on

[1] Not subject of production test, verified by characterisation

Table 6 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
						current types
Quiescent current VDD supply (VDD only)	I_{QDD1}	–	0.3	0.6	mA	V_{LIN} = float.
Quiescent current VDD supply (VDD only)	I_{QDD2}	–	0.28	0.6		V_{LIN} = 3.3 V, V_{HIN}=0
Quiescent current VDD supply (VDD only)	I_{QDD3}	–	0.28	0.6		V_{LIN}=0 , V_{HIN}=3.3 V
Input bias current	I_{LIN+}	15	35	60	µA	V_{LIN} = 3.3 V
Input bias current	I_{LIN-}	–	0	–		V_{LIN} = 0
Input bias current	I_{HIN+}	15	35	60		V_{HIN} = 3.3 V
Input bias current	I_{HIN-}	–	0	–		V_{HIN} = 0
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	0.18	0.23	–	A	C_L = 22 nF
Peak output current turn on (single pulse)	I_{Opk+} [1]	–	0.36	–		R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	0.39	0.48	–		C_L = 22 nF
Peak output current turn off (single pulse)	I_{Opk-} [1]	–	0.70	–		R_L = 0 Ω, t_p <10 µs
Bootstrap diode forward voltage between VDD and VB	$V_{F,BSD}$	–	1.0	1.2	V	I_F = 0.3 mA
Bootstrap diode forward current between VDD and VB	$I_{F,BSD}$	30	55	80	mA	$V_{DD} - V_B$ = 4 V
Bootstrap diode resistance	R_{BSD}	20	36	54	Ω	V_{F1} = 4 V, V_{F2} = 5 V

[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

V_{DD} = V_{BS} = 15 V, V_S = V_{GND}, C_L = 180 pF unless otherwise specified. (T_A=25°C)

Table 7 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay	IGBT types	t_{on}	280	420	610	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
	MOSFET types		210	310	460		
Turn-off propagation delay	IGBT types	t_{off}	260	400	590		
	MOSFET types		200	300	440		
Turn-on rise time		t_r	–	48	80		$V_{LIN/HIN}$ = 0 or 3.3 V C_L = 1 nF
Turn-off fall time		t_f	–	24	40		
Input filter time at LIN/HIN for turn on and off	IGBT types	t_{FILIN}	120	192	–		$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types HIN LIN		 50 100	 100 150	 170 250		
Dead time (not for 2EDL05I06BF)	IGBT types	DT	260	380	540	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
	MOSFET types		30	75	140		
Dead time matching abs(DT_LH – DT_HL) for single IC (not for 2EDL05I06BF)	IGBT types	MDT	–	10	80		ext. dead time 0ns
	MOSFET types			10	50		
Matching delay ON, abs(ton_HS - ton_LS)		MT_{ON}	–	10	60		external dead time > 500 ns
Matching delay OFF, abs(toff_HS-toff_LS)		MT_{OFF}	–	10	60		external dead time >500 ns
Output pulse width matching. PW_{in}-PW_{out}	IGBT types	PM	–	20	80		PW_{in} > 1 µs
	MOSFET types		–	20	70		

5 Timing diagrams

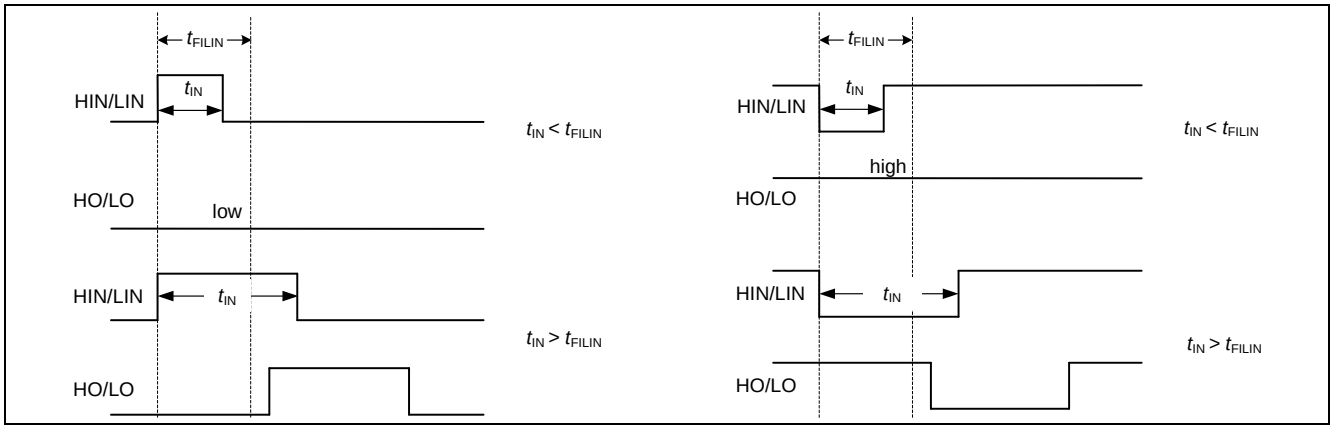


Figure 6 Timing of short pulse suppression

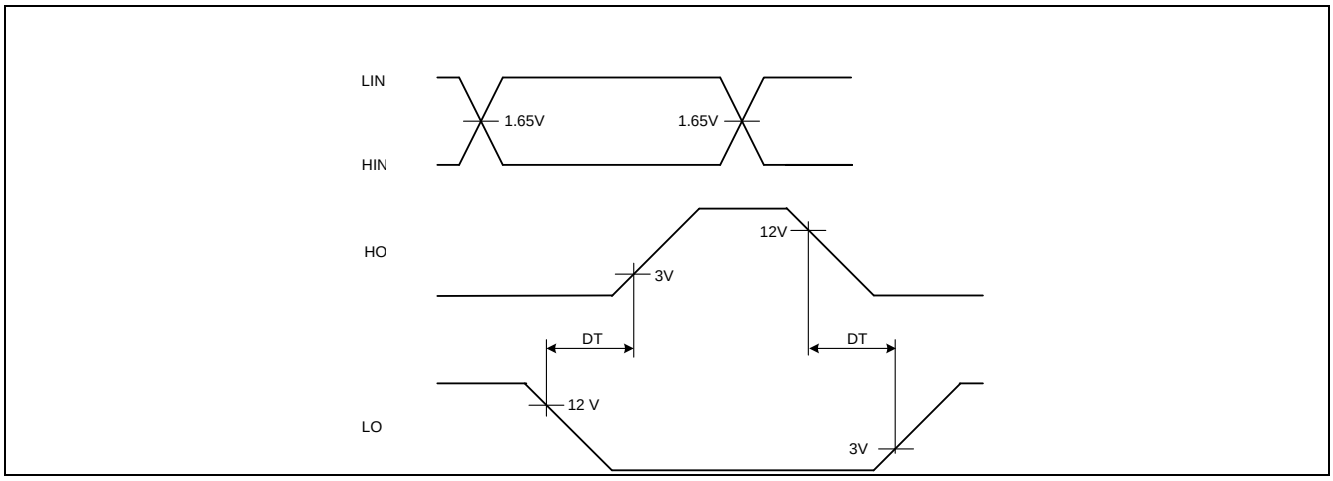


Figure 7 Timing of of internal deadtime

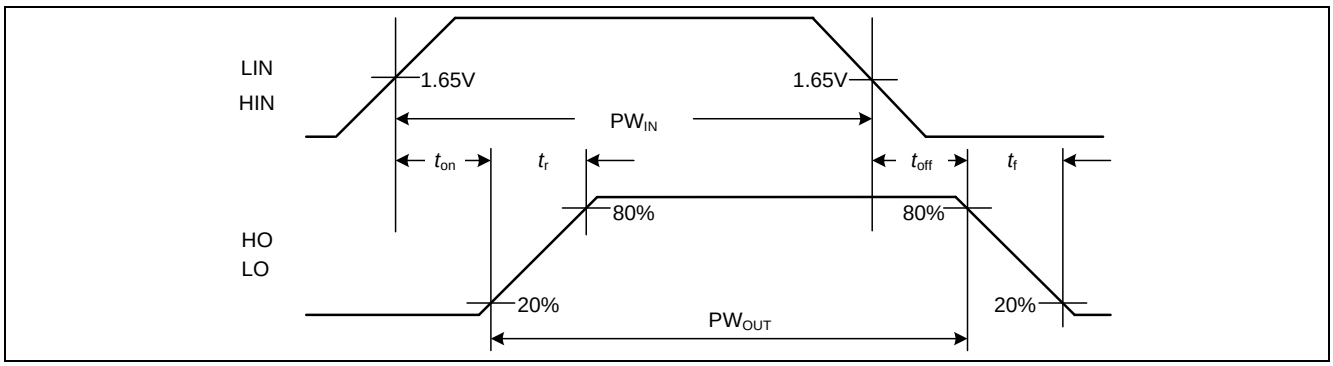


Figure 8 Input to output propagation delay times and switching times definition

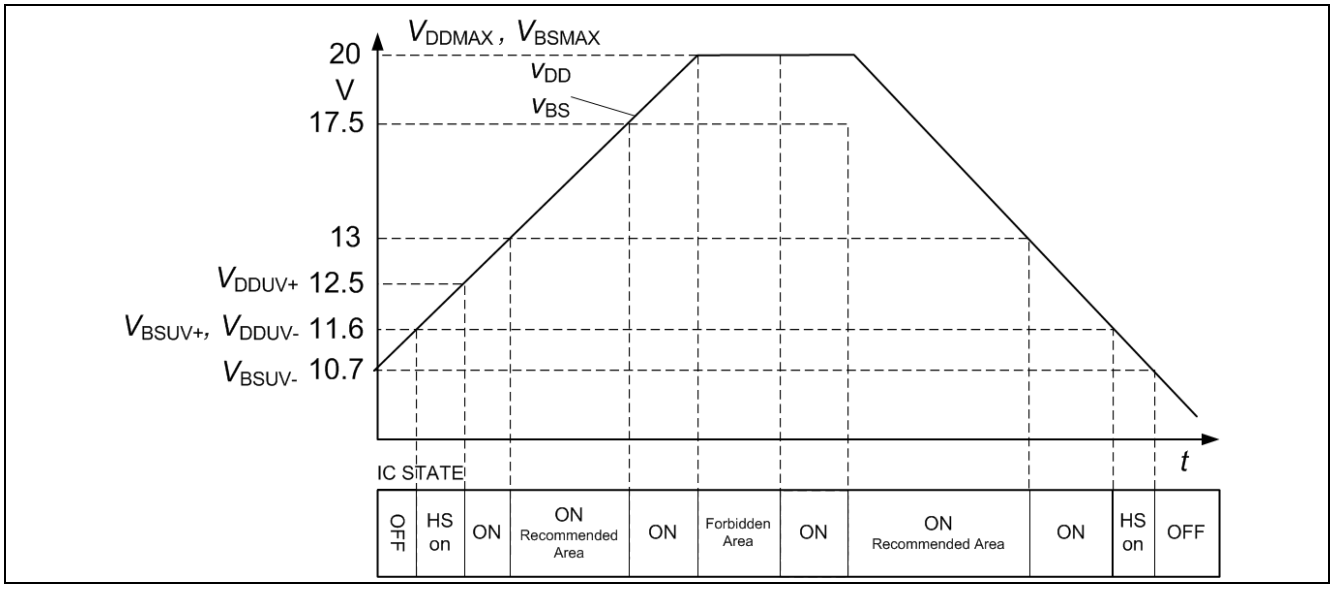


Figure 9 Operating areas (IGBT UVLO levels)

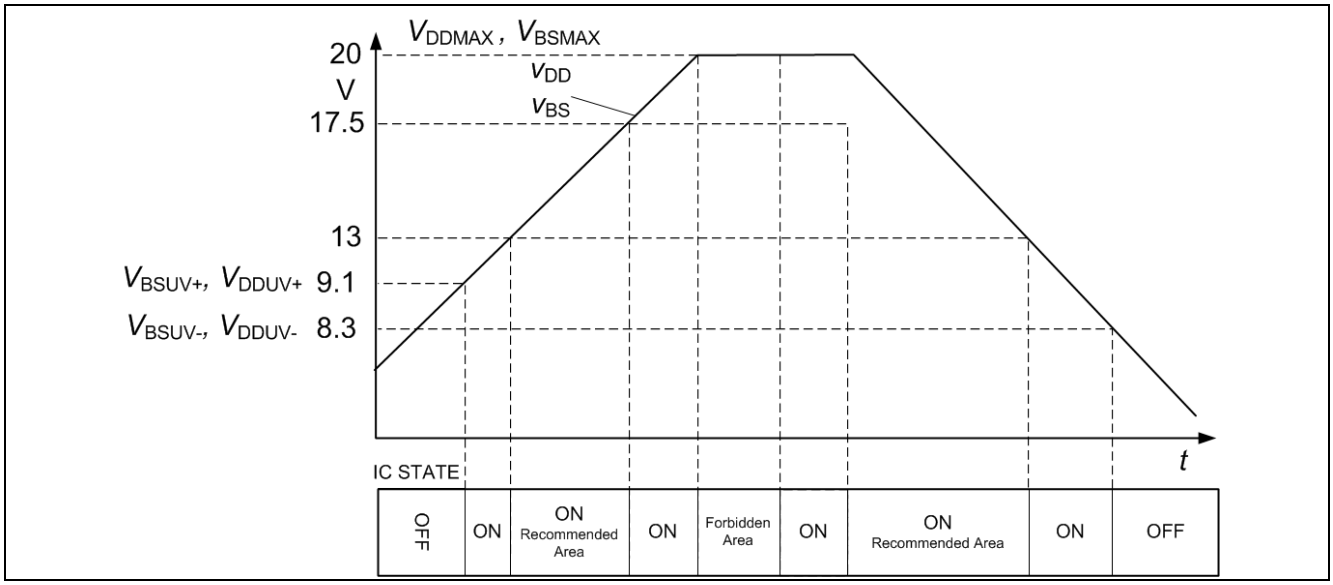


Figure 10 Operating areas (MOSFET UVLO levels)

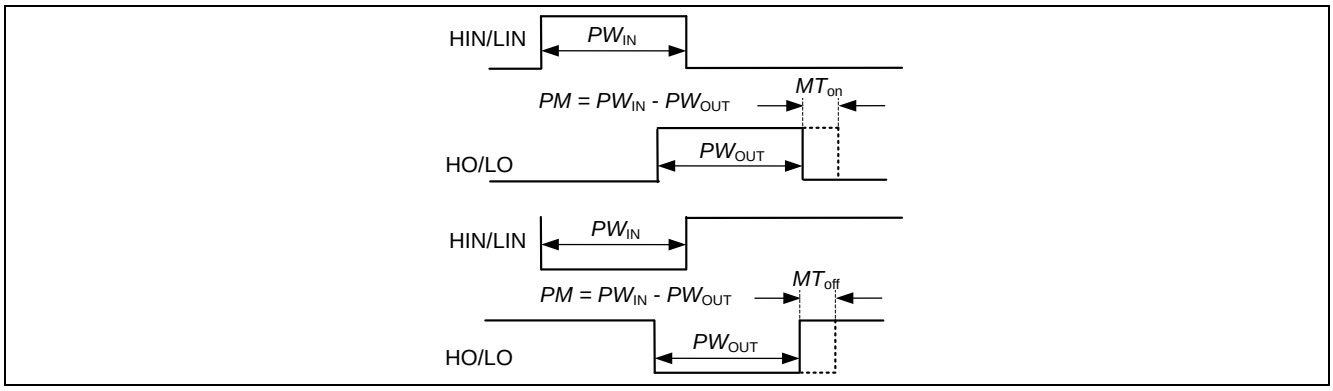
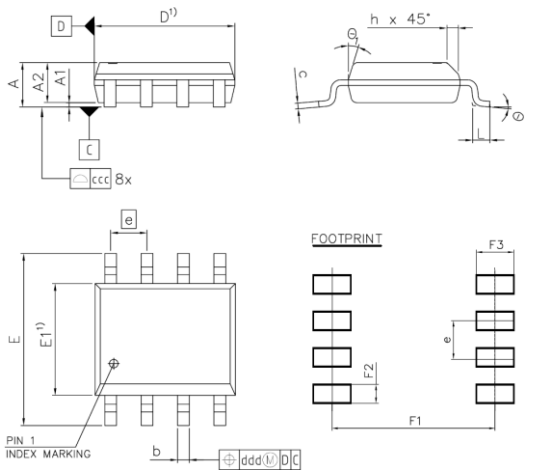


Figure 11 Output pulse width timing and matching delay timing diagram for positive logic

6 Package

6.1 PG-DSO-8



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

Max. reflow solder temperature: 265°C acc. JEDEC
Max. wave solder temperature: 245°C acc. JEDEC

Figure 12 Package drawing

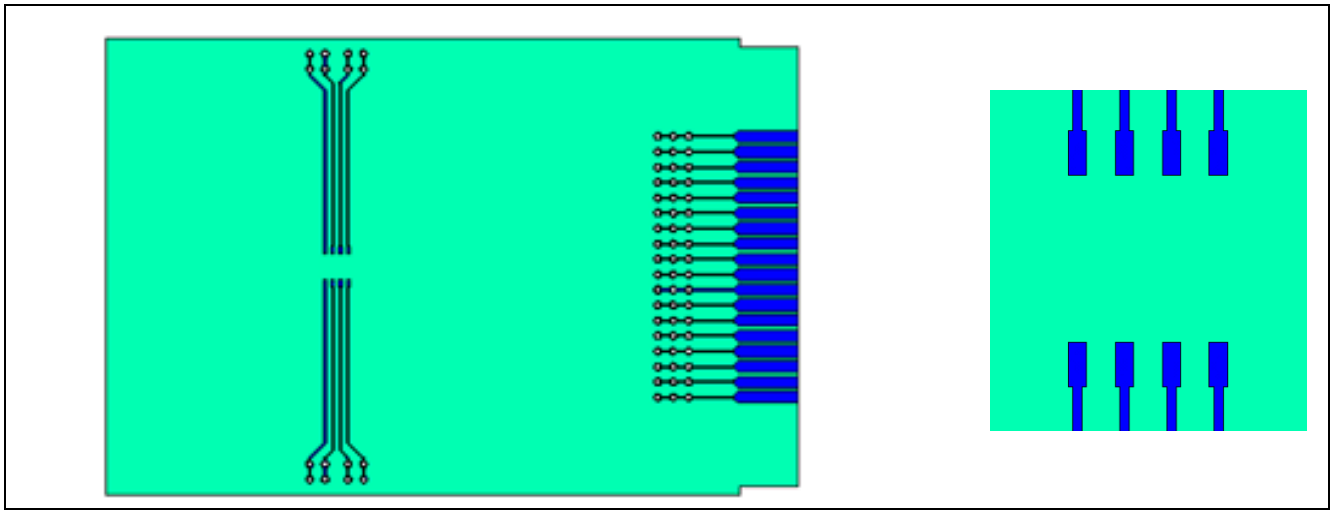


Figure 13 PCB reference layout
left: Reference layout
right: detail of footprint

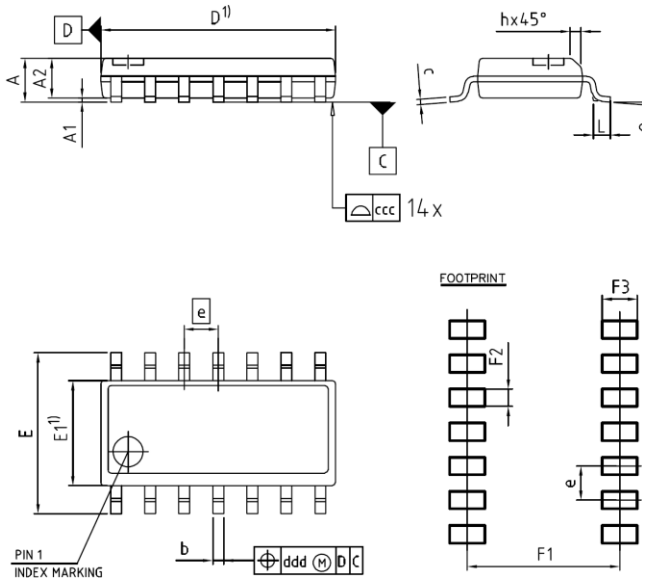
The thermal coefficient is used to calculate the junction temperature, when the IC surface temperature is measured. The junction temperature is

$$T_j = \Psi_{th(j\text{-}top)} \cdot P_d + T_{top}$$

Table 8 Data of reference layout

Dimensions	Material	Metal (Copper)
76.2 × 114.3 × 1.5 mm³	FR4 (λ_{therm} = 0.3 W/mK)	70µm (λ_{therm} = 388 W/mK)

6.2 PG-DSO-14



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	-	0.049	-
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.55	8.75	0.337	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
N	14		14	
L	0.39	0.89	0.015	0.035
h	0.25	0.50	0.010	0.020
Θ	0°	8°	0°	8°
ccc	0.10		0.004	
ddd	0.20		0.008	
F1	5.69		0.224	
F2	0.65		0.026	
F3	1.31		0.052	

Max. reflow solder temperature: 265°C acc. JEDEC
Max. wave solder temperature: 245°C acc. JEDEC

Figure 14 Package drawing

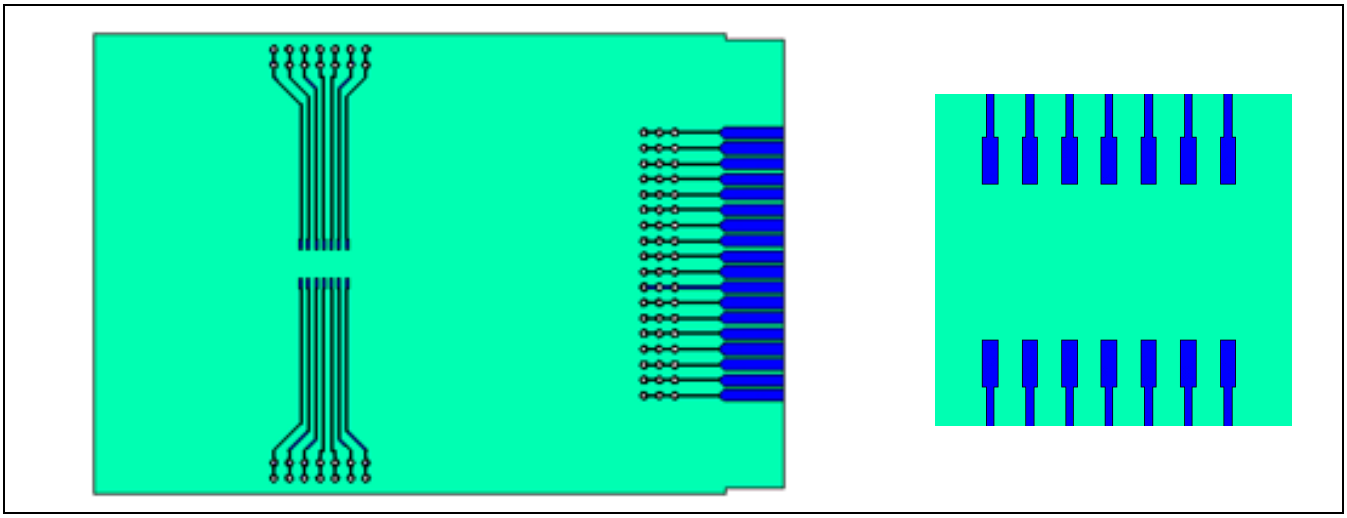


Figure 15 PCB reference layout (according to JEDEC 1s0P)
left: Reference layout
right: detail of footprint

The thermal coefficient is used to calculate the junction temperature, when the IC surface temperature is measured. The junction temperature is

$$T_j = \Psi_{th(j\text{-}top)} \cdot P_d + T_{top}$$

Table 9 Data of reference layout

Dimensions	Material	Metal (Copper)
76.2 × 114.3 × 1.5 mm³	FR4 (λ_{therm} = 0.3 W/mK)	70µm (λ_{therm} = 388 W/mK)

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