EiceDRIVER™

2ED300C17-S

2ED300C17-ST

Dual IGBT Driver Board

For Infineon Medium and High Power IGBT Modules

Power Management & Drives

Never stop thinking

Edition2009-03-10

Published by
Infineon Technologies AG
59568 Warstein, Germany

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- Commissioning is prohibited if there is visible damage by inappropriate handling or transportation.
- Ensure ESD protection during handling.
- Connect or disconnect only with power turned off.
- Always keep sufficient safety distance during commissioning without closed protective housing.
- Contact under live condition is strictly prohibited.
- Work after turn-off is impermissible until the absence of supply voltage has been verified.
- During work after turn-off it has to be observed that components heat up during operation. Contact with these can cause burns.
- The drivers are mounted electrically and mechanically on a PCB by soldering. The mechanical strength has to be verified by the user and, if necessary, assured with appropriate tests.
- The drivers are designed for use with Infineon IGBT Modules type IHM, EconoPACK+, PrimePACK™, 62mm. In case of ulterior use, safe operation cannot be ensured.

General Information 2ED300C17-S/ -ST:

This datasheet describes the dual channel IGBT driver 2ED300C17-S for industrial applications and the 2ED300C17-ST for traction applications. The electrical function and the mechanical dimensions of both versions are similar. The 2ED300C17-ST will be only be referred to where necessary.
The 2ED300C17-S is one of the *EiceDRIVER*™ driver family. (**e**upec **I**GBT **c**ontrolled **e**fficiency **DRIVER**).
The 2ED300C17-S IGBT driver is designed for use with Infineon IGBT modules of the 1200V and 1700V series. Functions of the 2ED300C17-S such as “soft shut down” or V_{CEsat} reference curves have to be adapted to the individual modules. This is described in the following chapters.

The 2ED300C17-S is designed for applications with high safety and reliability requirements and aims for power ratings of 75kW to 1MW.

To offer high interference suppression, +15V is generally used for control. The entire logic processing is also done with +15V. The integrated transformer is separated into three sections:
Two pulse transformers and a dual channel DC-DC switch mode power supply. These are designed such that they offer lowest coupling capacitances and high isolation stability.
The 2ED300C17-S is additionally equipped with a feedback ”Sense” input. This input can **optionally** be connected with the active clamping or di/dt and dv/dt control.

The clearance and creepage distances comply with VDE0110 and VDE0160 / EN50178 and are designed for pollution degree 3. Materials of the transformer meet requirements of UL94V2.
Degree of protection is IP00.

To protect from undefined switching of IGBTs in case of a gate-emitter short circuit of IGBT, the supply voltage $V_{A;B+}$; $V_{A;B-}$ is internally fused. In case of a gate-emitter short the secondary circuit is interrupted and thus the primary voltage maintained.

Exclusion clause:

The datasheet is part of the Infineon IGBT driver 2ED300C17-S. To ensure safe and reliable operation it is **necessary** to read and understand this datasheet.
The Infineon IGBT driver 2ED300C17-S is only intended for control of Infineon IGBT modules. Infineon cannot warrant against damage and/or malfunction if IGBT modules used not produced by Infineon.
In this context, Infineon retains the right to change technical data and product specifications without prior notice to the course of improvement.

The 2E300C17-S has been designed for an ambient temperature range starting at -25°C whereas the 2ED300C17-ST temperature range starts at -40°C.

AP99007		
Revision History:	2008-04	V3.1
Previous Version:	V3.0	
Page	Subjects (major changes since last revision)	
all	General review	

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1 Datasheet

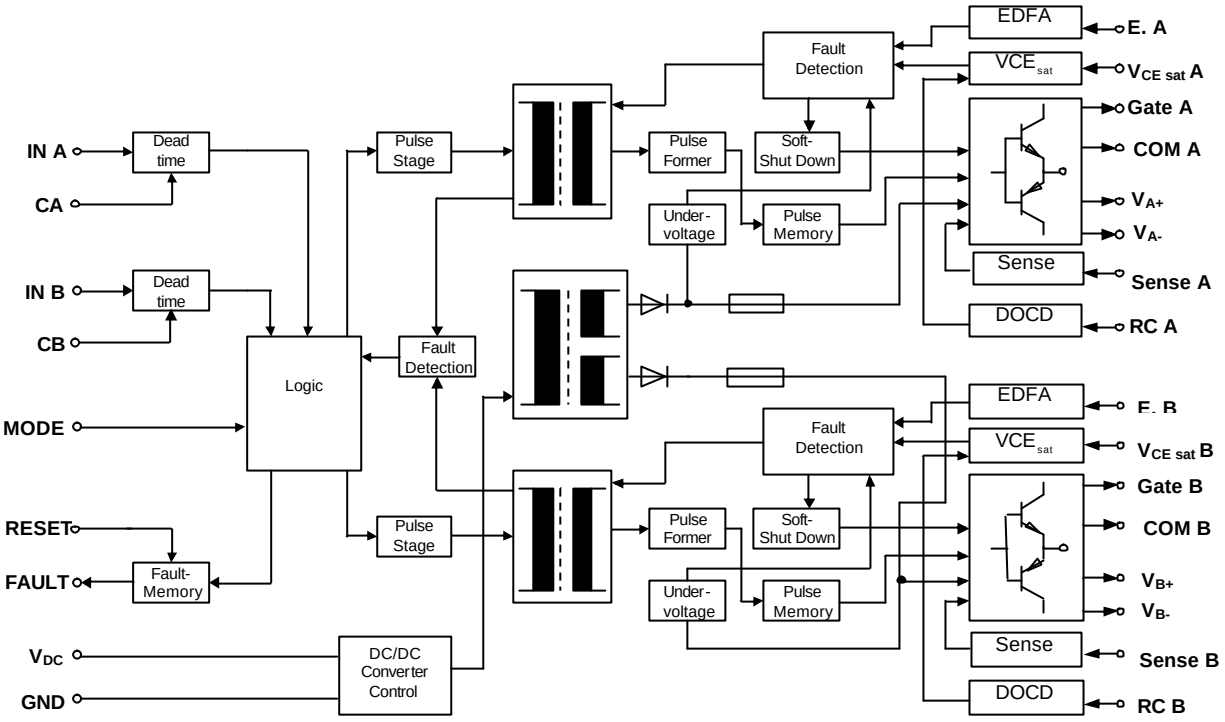
1.2 Features

- Dual channel IGBT driver
- For 600V, 1200V and 1700V Infineon IGBT modules
- V_{CEsat} monitoring
- Soft Shut Down for fault conditions
- Reinforced isolation according to EN50178
- Integrated DC-DC SMPS
- High peak output current
- ±15 V secondary drive voltage
- Short propagation delay time
- Optional "**Sense**"-function
- High RFI immunity

1.3 Key Data

Isolation test voltage According to EN50178 protection class II	**V_{isol}** pulse transformer and DC/DC	5000	V_{AC}
Max. output current:	**I_G** per channel	± 30	A
Max. output power	**$P_{DC/DC}$** per driver channel	4	W
Propagation delay time	**$t_{pd(on)}$; $t_{pd(off)}$**	<670	ns
Minimal pulse suppression	**t_{md}** turn on and turn off	400	ns
PWM drive voltage	**V_{in}** drive level for channel A and B	+15	V
Supply voltage	Operating voltage V_{DC} to ground	+15	V_{DC}
dv/dt stability	**dv/dt** (*during test)	50*	kV/µs
Operating temperature Direct on driver surface	**T_{op}** 2ED300C17-S	-25 bis 85	°C
Operating temperature Direct on driver surface	**T_{op}** 2ED300C17-ST	-40 bis 85	°C

1.4 Block Diagram



1.5 Inputs and Outputs 2ED300C17-S / -ST

IN A; IN B	PWM signal inputs for channel A and channel B
CA; CB	Inputs for external interlock delay time generation for channel A and B in half-bridge mode
Mode	Input for operating mode selection. Direct mode GND; half-bridge mode: +15V
Reset	With reset and operating PWM signals the primary fault memory is reset. Reset has active high logic. A high signal activates the reset.
Fault	A LOW signal on the fault output indicates a fault. The fault output is open-collector.
V_{DC}	Supply for the DC-DC SMPS
V_{DD}	Electronic supply
GND	GND is ground and reference point for all primary signals and supply voltage
E.A; E.B	External fault input is used to set the fault memory by an external signal.
V_{CE} sat A; B	Input for the saturation voltage monitoring
Gate A; B	Driver output to the IGBT module gate via an external gate resistor
COM A; B	COM A; B is connected to the auxiliary emitters of the IGBT module
V_{A+}; V_{A-} ; V_{B+}; V_{B-}	Supply voltage referenced to COM A; B for additional use and connection of the buffer capacitors
Sense	Control input for the optional di/dt or dv/dt control, setting of the soft shut down or active clamping
RC A; RC B	RC network for $V_{CE\,sat}$ reference curve

1.6 Pin Configuration of the 2ED300C17-S /- ST

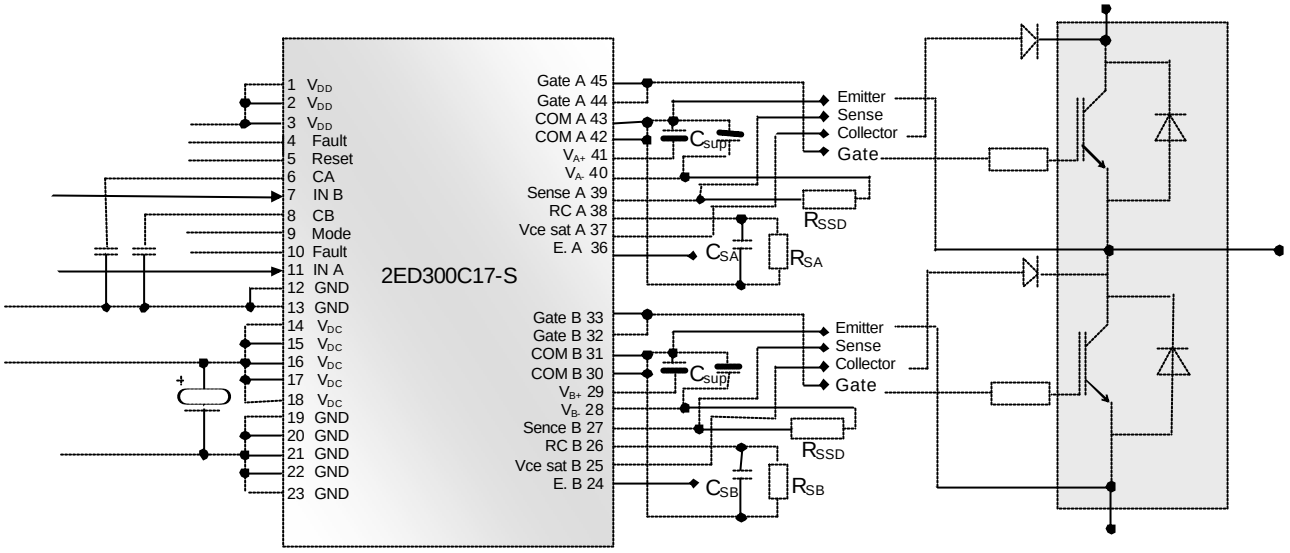


Figure 1.6 Pin configuration of the 2ED300C17-S

Pin	Label	Function	Pin	Label	Function
1	V_{DD}	+15V for electronics primary			
2	V_{DD}	+15V for electronics primary	**45**	Gate A	Gate channel A
3	V_{DD}	+15V for electronics primary	**44**	Gate A	Gate channel A
4	Fault	Fault output	**43**	COM A	Reference point A
5	Reset	Logic level to reset channel A and B	**42**	COM A	Reference point A
6	CA	Delay time ch. A “half-bridge mode”	**41**	V_{A+}	+16V external buffer capacitor
7	IN B	PWM input B	**40**	V_{A-}	-16V external buffer capacitor
8	CB	Delay time ch. B “half-bridge mode”	**39**	Sense	SSD / clamping input
9	Mode	Mode selection	**38**	RC	Reference RC network channel A
10	Fault	Fault output	**37**	$V_{CE\ sat}$	Collector sense channel A
11	IN A	PWM input A	**36**	E. A	External fault input channel A
12	GND	Ground for electronics primary	**35**		Physically non existent
13	GND	Ground for electronics primary	**34**		Physically non existent
14	V_{DC}	+15V for SMPS	**33**	Gate B	Gate channel B
15	V_{DC}	+15V for SMPS	**32**	Gate B	Gate channel B
16	V_{DC}	+15V for SMPS	**31**	COM B	Reference point B
17	V_{DC}	+15V for SMPS	**30**	COM B	Reference point B
18	V_{DC}	+15V for SMPS	**29**	V_{B+}	+16V external buffer capacitor
19	GND	Ground for SMPS	**28**	V_{B-}	-16V external buffer capacitor
20	GND	Ground for SMPS	**27**	Sense	Active clamping / SSD
21	GND	Ground for SMPS	**26**	RC	Reference RC network channel B
22	GND	Ground for SMPS	**25**	$V_{CE\ sat}$	Collector sense channel B
23	GND	Ground for SMPS	**24**	E. B	External fault input channel B

Note: The connection Ground for electronics primary and Ground for SMPS is permissible.

1.7 Absolute Maximum Ratings

Supply voltage	V_{DC}	Maximum primary supply voltage	+16	V
PWM signal input voltage	V_{in}	Max. voltage on inputs IN A; IN B	±20	V
Logic signal input voltage	V_{iH}	Max. voltage (Mode; Reset)	±20	V
Output voltage	V_o	Fault output blocking voltage	20	V
Logic signal output current	I_{OC}	Fault output; max. continuous current open collector	20	mA
Peak output current ON	I_{Gon}	Max. driver peak output current	+30	A
Peak output current OFF	I_{Goff}	Max. driver peak output current	-30	A
Output current supplied by DC/DC	$I_{out\,DC}$	Average value per secondary supply voltage[1)]	133	mA
Maximum output power	$P_{DC/DC}$	$P_{DC/DC}$ channel A + channel B	8	W
Maximum IGBT voltage	V_{CES}	Maximum collector-emitter voltage on IGBT	1700	V
Gate resistor	$R_{G\,min}$	Min. gate resistor (module internal + external gate resistor)	1	Ω
Gate charge	Q_{Gmax}	Maximum IGBT gate charge	52	µC
	dv/dt	Voltage slew rate secondary to primary side	50 [2)]	kV/µs
	T_{op}	Operating temperature 2ED300C17-S	-25...+85	°C
	T_{op}	Operating temperature 2ED300C17-ST	-40...+85	°C
	T_{sto}	Storage temperature	-40…+85	°C
Switching frequency	$f_{s\,max}$	Max. switching frequency (Top < 65°C)	60000	Hz
Supply current	$I_{DC\,max}$	Sum of current supplied to V_{DC} and V_{DD}	670	mA
Duty cycle	**d**	Maximum duty cycle	100	%

1) Current supplied from gate and supply output added

2) during test

1.8 Recommended Operating Parameters

		Min.	Typ.	Max.	Recommend.	
Supply voltage primary DC-DC	V_{DC}	+14	+15	+16	+15	V
Power DC-DC SMPS	P_{DC-DC}			8		W
Supply voltage electronics	V_{DD}	+14	+15	+16	+15	V
Switching frequency[4)]	f_S	0		60		kHz
Duty cycle	**d**	0		100		%
Reference voltage for the $V_{CE\,sat}$ – monitoring	V_{CEstat}	2		9	8 [3)]	V
Signal level **(IN A/B; Reset; Mode)**	V_{Level}		15			V
Reactivation after fault condition and IN A/B Low[2)]	t_{BK}	50			60	ms

1) “Conditions to be defined“

2) See chapter 3.4

3) See chapter 3.7

4) Max. switching frequency depends on load and environmental conditions

1.9 Electrical Characteristics

All values at 25 °C		Min.	Typ.	Max.	
No load input current	I_{DC}		80		mA
Supply current logic	I_{DD}		8		mA
Propagation delay time switch on	$t_{pd\ on}$		670		ns
Propagation delay time switch off	$t_{pd\ off}$		580		ns
Transition time differences	t_{dif}		50		ns
Minimal pulse suppression	t_{md}		400		ns
Threshold level	V_{Level}		8		V
Interlock delay time half-bridge mode	t_{TD}	1.6			µs
Coupling capacitance primary/secondary	C_{ps}		18		pF
Coupling capacitance sec. channel A to B	C_{ss}		15		pF

1.10 Insulation Characteristics

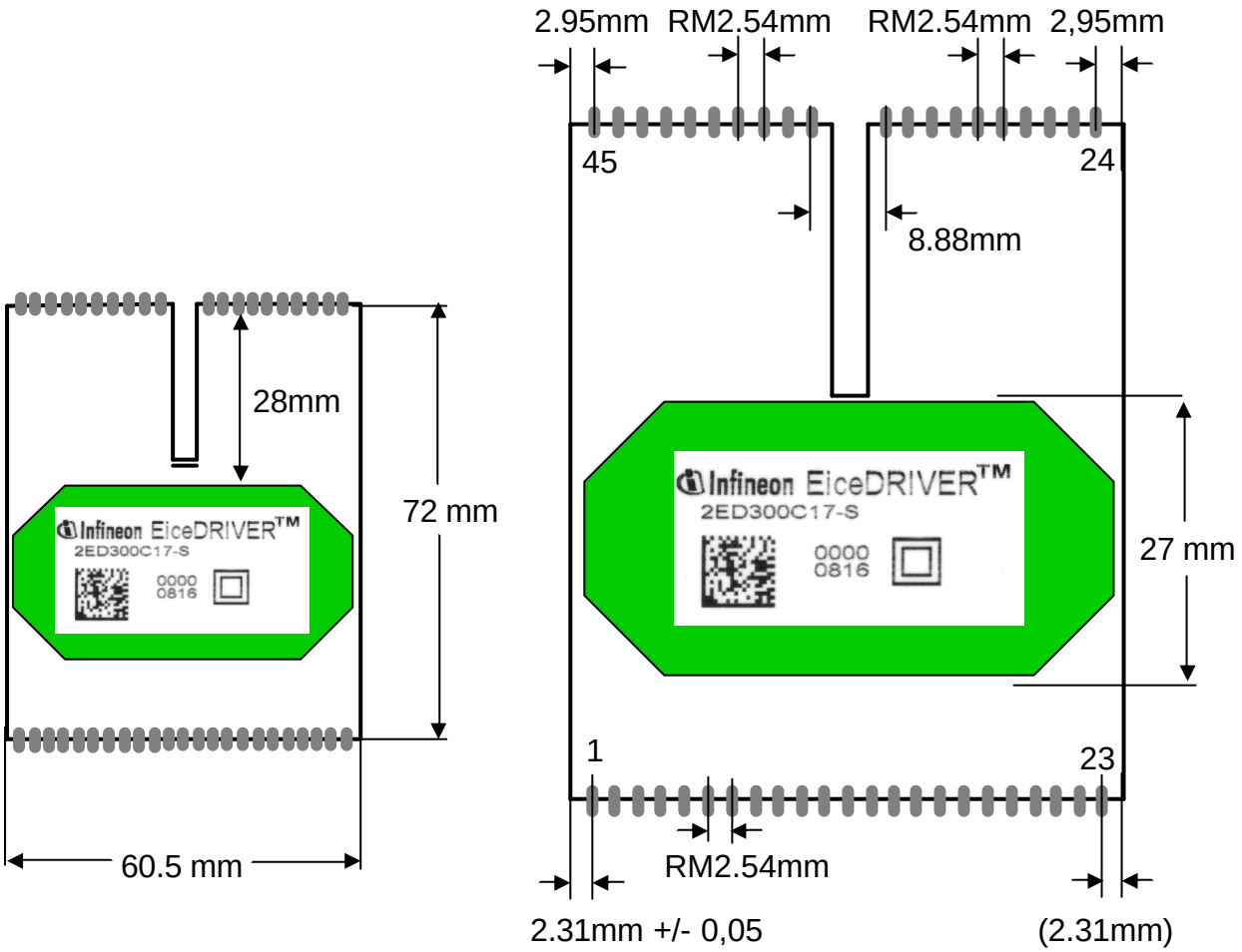
Isolation test voltage	$V_{isol\ IO}$	Input- Output (RMS, 50Hz, 1s)	5000	V
Isolation test voltage	$V_{isol\ 12}$	Output A - Output B (RMS, 50Hz, 1s)	2250	V
Surge voltage test	$V_{isol\ Su}$	Surge test according to EN50178 input to output	9600	V

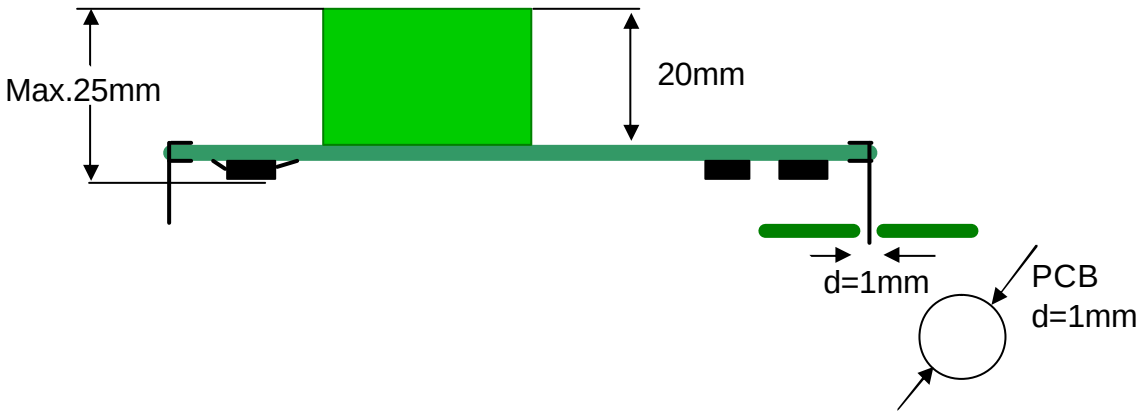
Clearance distance and creepage Primary/ Secondary	>15	mm
Clearance distance Secondary/ Secondary	>6	mm
Creepage Secondary/ Secondary	>14	mm

1.11 Mechanical Dimensions

Note!

The soldering pins of the design –ST are not coated.





1.12 Processing

The device has been designed to be soldered onto a carrier board as a through-hole component either by dual wave soldering process or by selective soldering. For more information see IFX Additional Information, DS1, March 2008

The "-ST" version varies from the "-S" version through the use of a coating and use different OP-Amp. The coating used is type 1306N made by the company Peters. The soldering pins are not coated. When further coating processes are carried out, e.g. on the customer assembly, the compatibility of the coated type has to be established first.

2 The transformer

2.1 Reinforced isolation Protection Class II according to EN50178

The reinforced isolation between primary and secondary side of the two transformers and the switch mode power supply is the basis for the 2ED300C17-S.

Highly insulated coil wires, core insulated ferrites and a special sealing compound (UL94 V-0) are used for this purpose. The design makes sure that all windings are physically separated from each other. There are no overlapping primary and secondary windings. The winding connections are terminated directly to the pins which are cast into the housing. All that is contained in a plastic housing certified to UL 94.

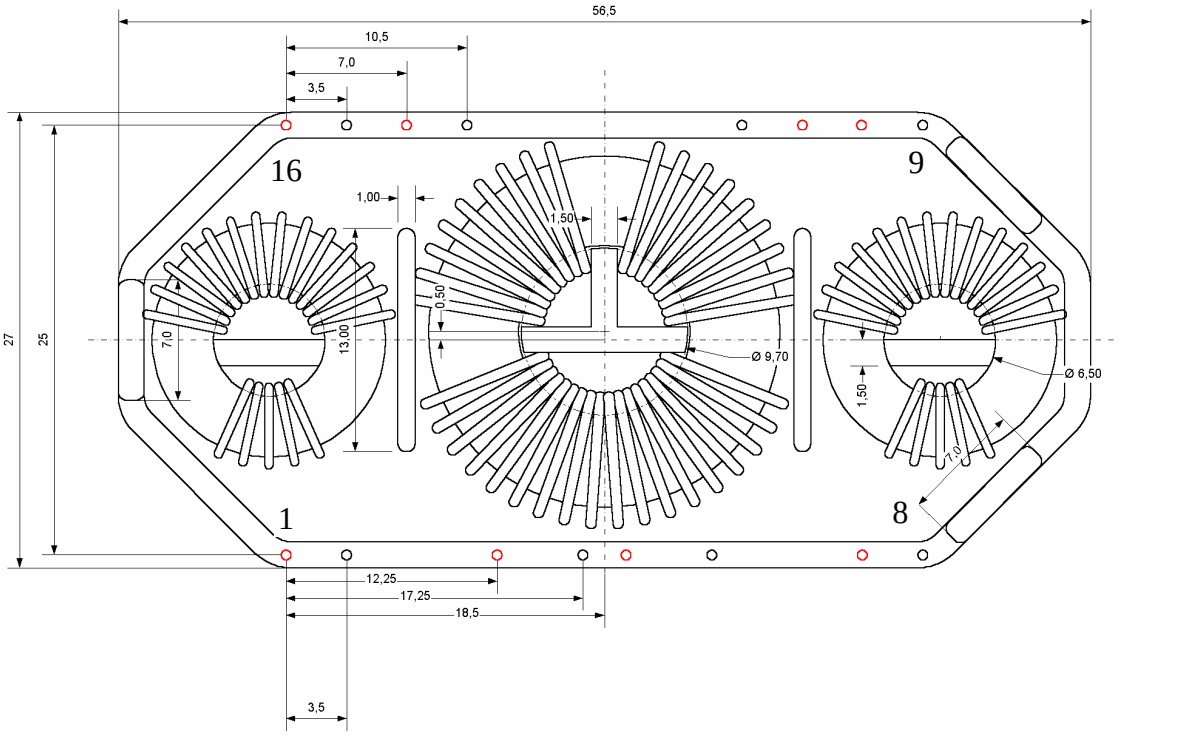


Figure 2.1 Complete transformers with cores in position

The transformer is designed for use in industrial and traction applications. The test voltage applied between all inputs and all outputs is 5kV AC for 1 second. The test voltage applied between the secondaries is 2.25kV AC for 1 second. (EN50178 Table18) (Individual test).

The insulation test is completed by the surge voltage test stipulated by EN50178.

Surge voltage test according to (EN50178 table 17) is 1.2/50µs with 9.6kV.

The partial discharge extinction voltage stipulated by the standard (EN50178 table19) is above 1920V peak value (series test).

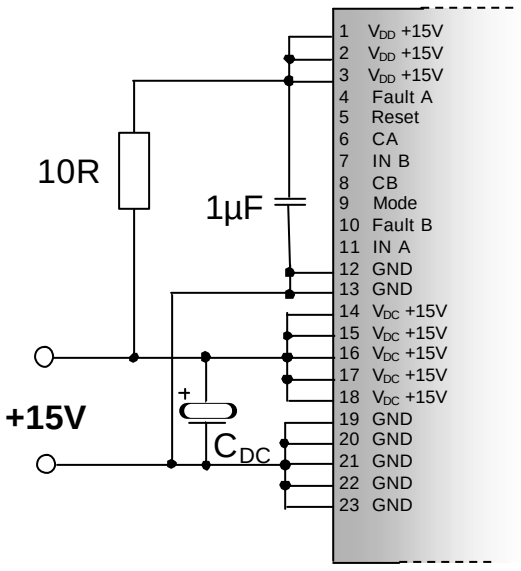
3 Application of the 2ED300C17-S / -ST

3.1 Power supply

The 2ED300C17-S has an integrated DC-DC switch mode inverter, which generates the required secondary voltages. The generated voltages are for the top and bottom channel with +15V primaries each ±16V secondaries.

Hence the 2ED300C17-S only requires one external power supply of +15V. The 2ED300C17-S is operated on a stabilized +15V (±1V) supply. It is distinguished between $\mathbf{V_{DD}}$ and $\mathbf{V_{DC}}$. All inputs are switched with +15V, where $\mathbf{V_{DC}}$ should be additionally stabilized by a capacitor $\mathbf{C_{DC}}$ (see figure 3.1). This stabilizing capacitor C_{DC} should be 220µF.

All GND pins have to be connected. To prevent a ground loop there is no internal connection of the DC-DC SMPS ground and the primary electronics.



Note!

If the driver is turned on with +15V, a low voltage fault may be tripped depending on the voltage slew rate. This will be reset after 60ms if both signal levels IN A and IN B remain Low during this time.

Note!

No potential difference greater than 20V may occur between V_{DD} and V_{DC}.

Figure 3.1 Pin configuration of +15V voltage supply

Note!

The 2ED300C17-S features secondary UVLO monitoring. If one of the secondary supply voltage drops below typical +12V or -12V, a fault condition will occur. This turns off the driver and is transferred to the primary as well.

Warning: There is no monitoring of the primary supply voltage referring to under-voltage. The supply voltage applied has to be monitored.

3.2 Mode selection

The 2ED300C17-S features two operating functions to drive Infineon Technologies IGBT modules. These are the direct mode and the half-bridge mode.

- The direct mode:

In this mode there is no link between the two channels of the 2ED300C17-S. Both channels IN A and IN B are working independently from each other and may both be turned on at once. The inputs IN A and IN B are switched with +15V PWM signals.
The direct mode is activated by taking pin 9 **"Mode selection"** to **GND** (e.g.: pin 12/13).
The inputs **CA** pin 6 and **CB** pin 8 are not connected.

Note!
In the direct mode the inputs CA and CB must not be connected to +15V or GND. For EMC reasons it is recommended to connect the inputs CA and CB with 470pF to GND.

- The half-bridge mode:

This mode generates an interlock time between the two channels of the 2ED300C17-S. I.e. there is always only one channel active. The interlock time between the switching events may be selected. This is done with the inputs **CA** pin 6 and **CB** pin 8.
The half-bridge mode is activated by taking pin 9 "**Mode selection**" to $\mathbf{V_{DD}}$ (pin 1/2/3).
The inputs **IN A** and **IN B** are switched with **PWM inputs**.

Explanation:
There is always only one channel turned on. If there is a high signal on one channel, this is turned on after the interlock time has ended. If during this time there is a high signal for the second channel, it will be ignored until the first turned on channel has turned off.

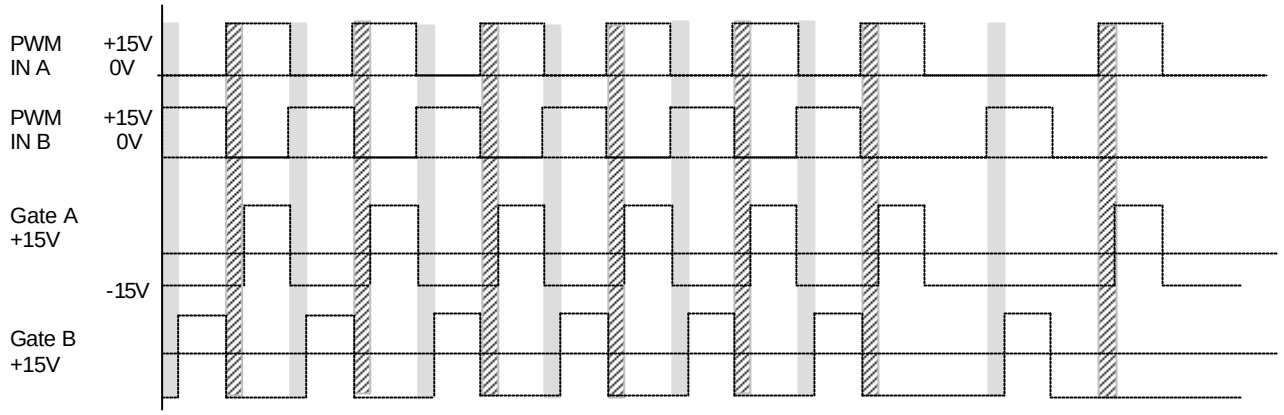


Figure 3.2 Switching diagram with interlock delay times

3.3 Interlock delay times

In half-bridge mode the 2ED300C17-S generates a minimal internal interlock delay time between the two channels. This minimal interlock time t_{TD} is pre-set to 1.6 µs. By adding a capacitance to the two inputs CA and CB this interlock time is extended and adapted to the requirements of the application. The capacitance is externally added between CA and CB to GND (see page 7 – 1.6 Pin configuration).
The capacitance for the required interlock time is derived from the following table:

Delay time	CA / CA
1.6µs	n.c.
2µs	47pF
2.4µs	100pF
3.4µs	220pF
4.3µs	330pF
5.4µs	470pF
9.6µs	1nF

Table 3.3 Interlock delay time settings for half bridge mode

NOTE !
It is not permitted to connect the inputs CA and CB directly to a voltage potential.

The tolerance of the interlock delay times depends mainly on the tolerance of the external capacitors. This needs to be considered when choosing the capacitors!

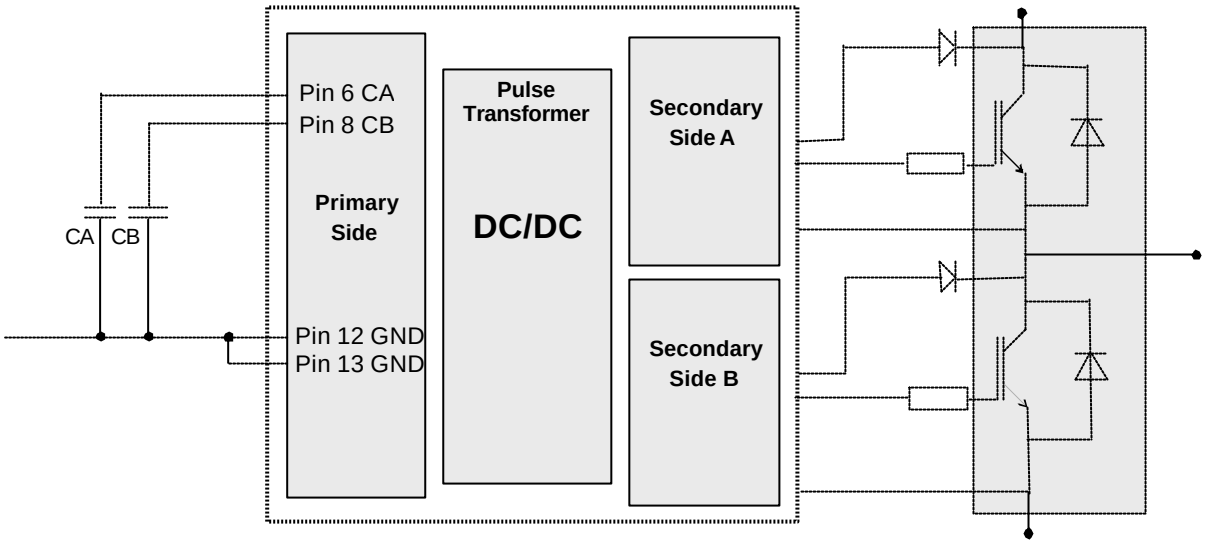


Figure 3.3 Connection of the external capacitors to increase the interlock times

3.4 Logic level

The term “logic level” concerns the fault output and the reset input as well as the input for operating mode selection described in chapter 3.2.

- Logic inputs

The two inputs (reset and mode) may be stressed with a maximum voltage of 20V. The switching threshold is at **8V**, so the existing +15V offers itself as switching signal.
1) Mode: see chapter 3.2
2) Reset: The driver can be reset via the reset input after a fault has been indicated. The reset input is active high, i.e. a ***high signal activates the reset***. The threshold level is 8V. If reset is used by the PWM inputs IN A and IN B, the reset input is inactive and pin 5 (Reset) has to be permanently connected to GND.
If both PWM signals are **“low”** for more than **60ms**, the driver is reset.

- Logic outputs

The driver core recognizes short circuit current faults of the IGBTs and faults of the supply voltage. Additionally the 2ED300C17-S features an external fault input. If a fault is detected through the $V_{CE\ sat}$ monitoring, an under-voltage or the external fault input, the driver core is immediately turned off. With these faults on the secondary side, the IGBT is shut down via a soft shut down. Each fault is stored until a reset signal on Pin 5 is present. The reset is also activated when the input signal on both channels is low for more than 39ms.

Indication of a fault occurs in any case via a common fault line on the logic output **FAULT**. The fault is brought out twice via Pin4 and Pin10.
These outputs are configured as open collector. The outputs can operate at up to **20V** and can switch a maximum of **20mA**. They are designed to provide signals with 15V CMOS level.

If a fault is recognized, the internal transistor switches and pulls the fault output to GND.

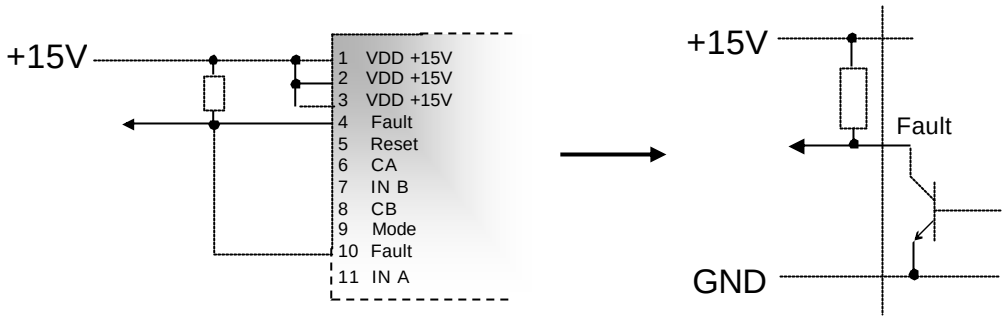


Figure 3.4 Fault output

Note!
The fault outputs are internally connected.
There is only one fault output for both channels.

3.5 Signal level

In both the direct mode and the half-bridge mode the input IN A of the 2ED300C17-S controls channel A and input IN B controls channel B. The inputs feature a Schmitt-Trigger and an active high logic. A high level turns the IGBT on and a low level turns it off.
The two signal inputs may be operated with a maximum of 20V per channel. Brief negative peaks of equal voltage will not lead to damage of the inputs. The switching threshold is **at** +8V to GND.
The input impedance is 3.3kOhm for each channel. For long cables it may be necessary to connect an external burst suppression network.
Note:
The 2ED300C17-S features a minimal pulse suppression. Pulses with less than 400ns will be suppressed by the driver.

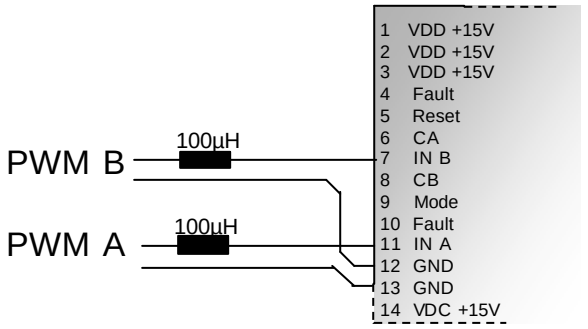


Figure 3.5 Input signals

3.6 IGBT connection

The 2ED300C17-S features two independent channels to drive the IGBTs. It is possible to drive individual IGBTs, single IGBT-modules or IGBT-modules connected in parallel.
The maximum size of the IGBT-modules depends mainly on the IGBT input capacitance and on the switching frequency.
When considering the gate currents, note that these are not determined by the external gate resistors alone. Many Infineon Technologies IGBT modules have internal gate resistors. Additionally, the 2ED300C17-S features a low output impedance. Never the less a gate current calculated via the external gate resistor will never be realized in practice. An approximation for the drive power and peak current can be achieved with:

- Driver power

$$P_G = f_S \bullet \Delta V_{GE} \bullet Q_g$$
$$P = P_{DD} + P_G$$

- Max. driver current

$$I_{G\,max} = \frac{\Delta V_{GE}}{R_{G\,(min)}}$$

f_S = switching frequency
Q_g = IGBT gate charge (datasheet)
P_{DD} = driver dissipation
ΔV_{GE} = 30V at ±15V
$R_{G(min)}$=$R_{G\,extern}$+$R_{G\,intern}$

- Gate connection

The gate of the IGBT is connected to **Gate A** or **Gate B** via the external gate resistor. The associated auxiliary emitter is connected directly to the **COM** outputs.
The gate output voltage is ±15V with respect to COM A and COM B (considering chapter 3.1).

By utilizing the external gate resistors it is possible to realize turn-on and turn-off with different gate resistances. Additionally to the gate resistor a gate-emitter resistor and gate clamping should be used. These would be placed between the gate and the aux. emitter. As R_{GE} a resistor <10kOhm is recommended. The gate clamping is done with TVS diodes (transient voltage suppressor). These diodes prevent the gate voltage to rise to inadmissible levels through parasitic effects (e.g. Miller capacity).

The external gate resistors are defined in the Infineon Technologies IGBT datasheet. The value of the internal gate resistor is also provided in the IGBT datasheet.

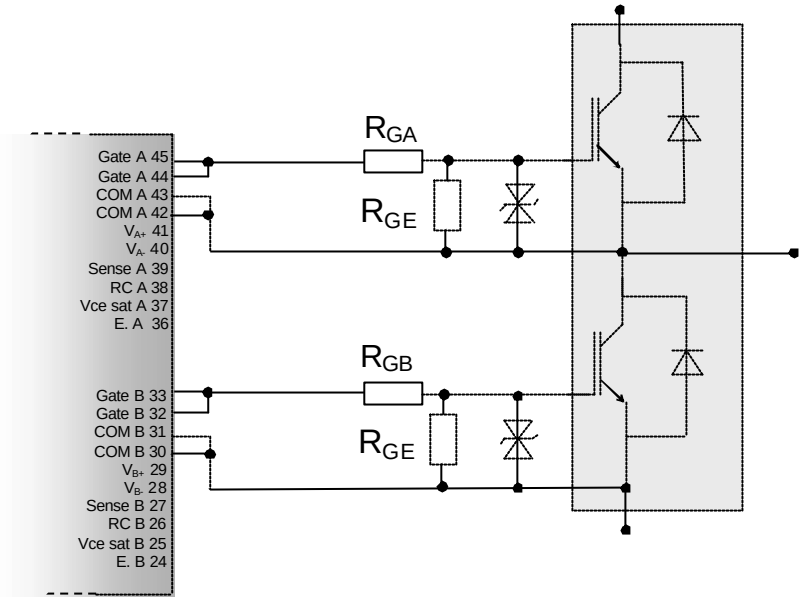


Figure 3.61 Gate connection

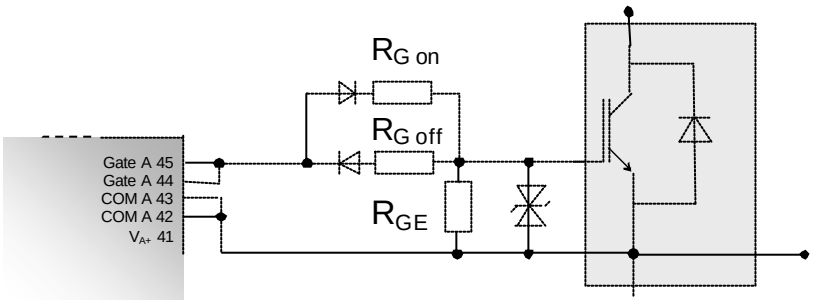


Figure 3.62 Gate connection with $R_{G\ on}$ and $R_{G\ off}$

- Collector connection

The 2ED300C17-S is able to measure and evaluate the voltage between collector and emitter of an IGBT. This is used to recognize a short circuit and then shut-down. For the optional function of DVRC or active clamping the connection to the collector is also required.

For the short circuit shut-down function the auxiliary collector is connected to **V_{CEsat} channel A** or **V_{CEsat} channel B**. To block the high DC-link voltage during shut-down a diode D_X with high reverse blocking voltage has to be connected between the collector and the "$V_{CE\,sat}$" input. The reverse blocking capability of these diodes should be higher than the IGBT-module voltage (600V/1200V/1700V). Further the diode has to follow the switching frequency and therefore has to be accordingly fast. Two or three diodes in series is an option to achieve the required blocking capability.

Application and adjustment of the short circuit shut-down is described in detail in the next chapter 3.7.

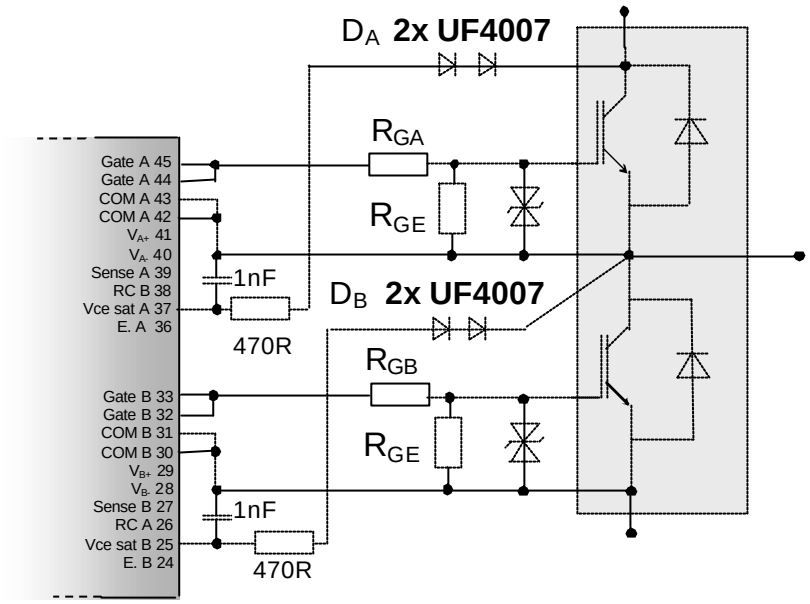


Figure 3.63 Collector connection for $V_{ce\ sat}$ measurement

Note!
The R_{GE}, the gate-emitter clamping diodes, the gate resistor and the collector diodes D_X should be placed in the closest possible vicinity of the module.

Note!
If wire links are used between the drivers and the IGBTs, the gate lead should be twisted together with the respective emitter and collector leads. These connections should be as short as possible. Lengths of more than 20cm are to be avoided.

3.7 IGBT short circuit and over-current shut-down with SSD "Soft Shut Down"

A short circuit is detected by the integrated V_{CE} measurement in the 2ED300C17-S (see chapter 3.6). The 2ED300C17-S measures the V_{CE} voltage while the IGBT is turned on. If the V_{CE} rises above the preset reference voltage during this period, a fault is triggered and the IGBT is turned off via the internal soft shut-down. For Infineon Technologies IGBT-modules with NPT and FS-technology the soft shut-down reduces the voltage over-shoot by a slower turn-off.

- The reference curve

The reference curve is only adjustable via an external **R_{SX}** and **C_{SX}**. With R_{SX} the reference voltage is set and with C_{SX} the reference time.

The resistor and the capacitor are connected between **RC A** and **COM A** or **RC B** and **COM B.** The reference time elapses directly with the turn-on of the respective driver side (See figure 3.7.2).

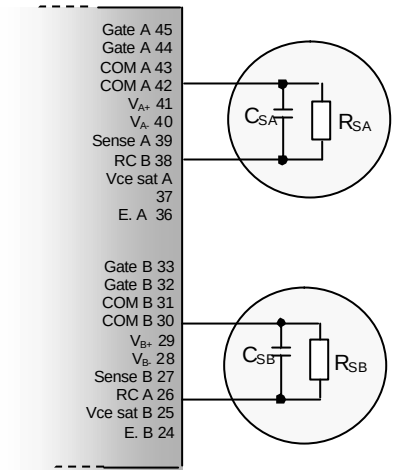


Figure 3.7.1 R_{SX} and C_{SX} connection to adjust the reference curve

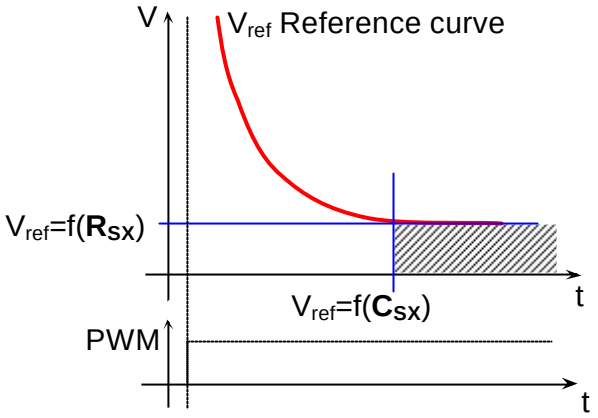


Figure 3.7.2 Reference curve

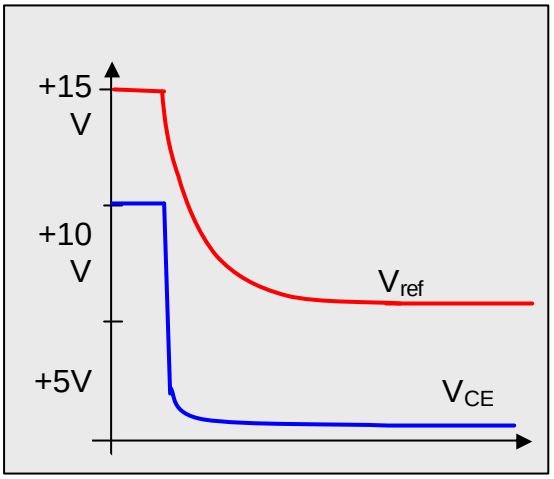
Reference voltage V_{ref}	R_{SX}
2V	2kΩ
4V	5.4kΩ
6V	12kΩ
8V	32kΩ
9V	70kΩ

Reference time t_{ref}	C_{SX} at V_{ref}=2V	C_{SX} at V_{ref}=4V	C_{SX} at V_{ref}= 6V
1µs	-	-	120pF
3µs	60pF	100pF	340pF
5µs	150pF	220pF	570pF
6µs	200pF	300pF	800pF

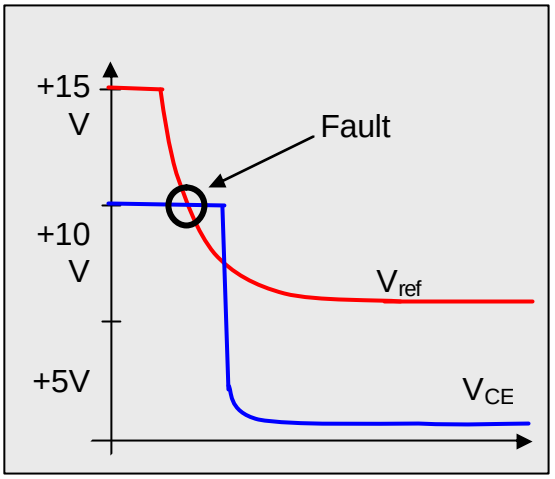
Table 3.7 gives reference voltage V_{ref} and reference time t_{ref} until the reference voltage is reached

Example: In case of Infineon PrimeSTACKs and ModSTACKs with EiceDRIVER for C_{SX} = 220pF and R_{SX} = 68k are used.

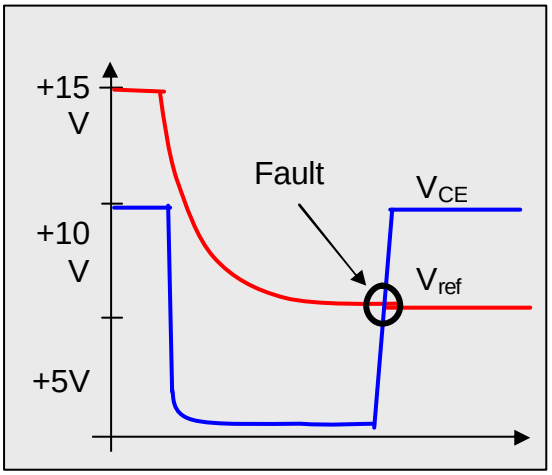
A comparator inside the 2ED300C17-S compares the voltage at the $V_{CE\ sat}$ input with the reference voltage V_{ref}. The maximum V_{CE} voltage at the comparator will be 10V. With the turn-on of the IGBT the V_{CE} voltage drops to its threshold value depending on the load current I_C. To suppress commutation effects during turning on the IGBT there is the settable reference curve V_{ref}. This drops, depending on the external C_{SX} and R_{SX} network, from 16V to the set voltage level. If the V_{CE} voltage rises above the reference voltage at any time, a fault is tripped and the driver is locked.
The various different operating conditions are depicted in the four cases below. If the fault occurs, the IGBT is turned off via the SSD (**S**oft **S**hut **D**own) function.



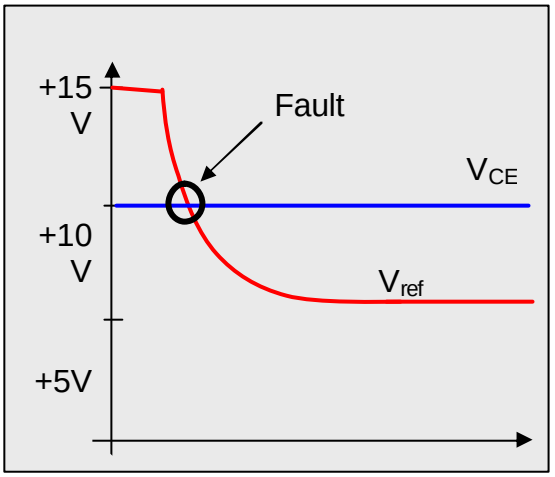
Case 1. Usual case



Case 2. IGBT turns on too slowly or reference time is too short



Case 3. Short circuit during operation



Case 4. Short circuit during turn-on

Figure 3.7.3 Different faults depicted

- Trigger suppression for the Vce sat measurement

To vary the sensitivity of the V_{CE} the 2ED300C17-S uses an RC timing network. This network is used to set the sensitivity of the $V_{CE\ SAT}$ monitoring as required by the individual application. One has to keep in mind that this RC network provides a timing function. Accordingly, reaching the reference voltage and in this connection the detection of the temporal short circuit current in the IGBT depends on the charging process of the C_{VCE} capacitor. This can easily be defined by measuring in front of C_{VCE} once and in comparison to this $V_{CE\ sat\ X}$ directly at the input.
The RC combination is able to extend the operating time till the IGBT switches off in case of a short circuit. This is to say that in addition to reference time t_{ref} (table 3.7)

and SSD cycle time t_{SD}=5µs and system cycle time t_{SD}=1µs, the trigger suppression time has to be taken into account. As a standard, a value of R_{VCE} =470R and C_{VCE} =1nF is recommended. Should the $V_{CE\ sat}$ monitoring react too sensitively the C_{VCE} value can be increased. This of course extends the trigger time of the short circuit turn-off. In a contrary case, it is certainly recommended to decrease the C_{VCE} value or the R_{VCE} value. One always has to make sure that the short circuit across the IGBT is switched off within 10µs.

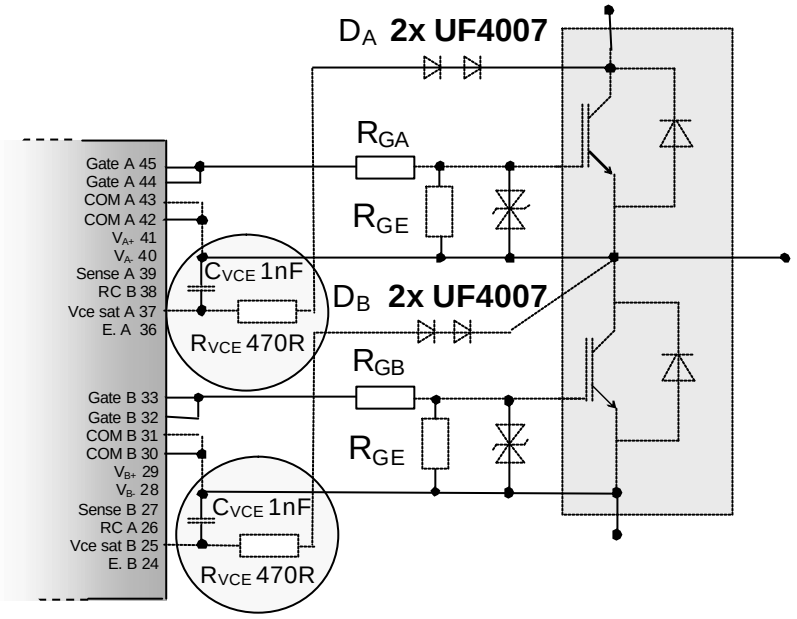


Figure 3.7.4 Trigger suppression of the $V_{ce\ sat}$ measurement

3.8 SSD “Soft Shut Down“

The SSD “Soft Shut Down“ is used to softly shut down the IGBT if a fault occurs. This is useful in order to avoid destruction of the IGBT due to high voltage overshoots during turn-off. If set correctly, the SSD will reduce the turn-off di/dt of all Infineon Technologies IGBT products and hence the voltage overshoot during fault conditions.
The “Soft Shut Down“ is set with resistor R_{SSD}. This resistor is externally connected between **Sense** and **–16V** (see figure 3.8.1).

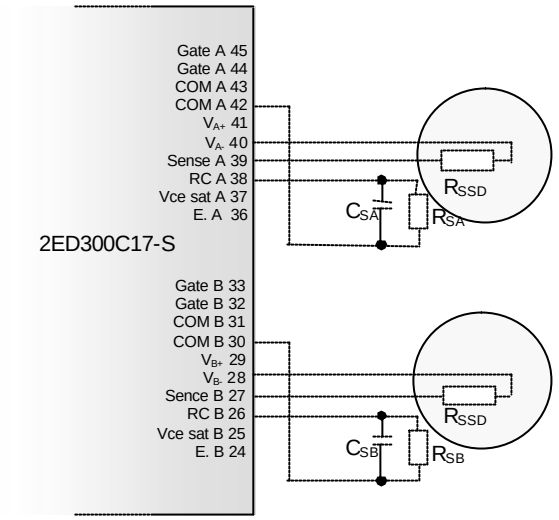


Figure 3.8.1 Connection of R_{SSD}

The “Soft Shut Down“ has to be adapted to the IGBT type used. Since the turn-off behavior and the resulting voltage overshoot depends on the IGBT type and the construction of the entire application, the resistance of the R_{SSD} resistor has to be found in a practical manner (For more information see IFX AN 2007-05).

As guidance one can use the module **FS450R17KE3** with an **R_{SSD} = 10k**Ω.
IGBT modules with a greater input capacitance C_{ies} will need a lower R_{SSD} value, IGBT modules with a lower input capacitance C_{ies} will need a greater R_{SSD} value. The dissipation of the resistor is calculated as follows:

$$P_{SSD}[W] = \frac{1024}{R_{SSD}}$$

If a fault is recognized and the “Soft Shut Down“ is activated, the capacitances of the internal bipolar- output stage go through the charge reversal and thus the IGBT input capacitance C_{ies} and the Miller capacitance C_{res} are discharged slowly. This process is limited to t_{SD}= **4µs**. After this time the output of 2ED300C17-S turns off hard.
The driver has to be reactivated by a “Reset“ (see chapter 3.4 logic levels).

Note!
The “Soft Shut Down“ may slightly increase the V_{GE}. Hence the gate clamping described in chapter 3.6 IGBT connection has to be observed.

Note!
Infineon Technologies IGBT modules are generally designed for short circuits of up to $t_P \leq$ 10µs.

Note!
The “Soft Shut Down” is not 100% protection from voltage overshoots during fault turn-off!

Should a short circuit occur and at the same time the natural PWM pulse go to Low Level, the SSD can not be commenced. This case is rare but can occur. Active Clamping will then protect against over-voltage (see 3.10).

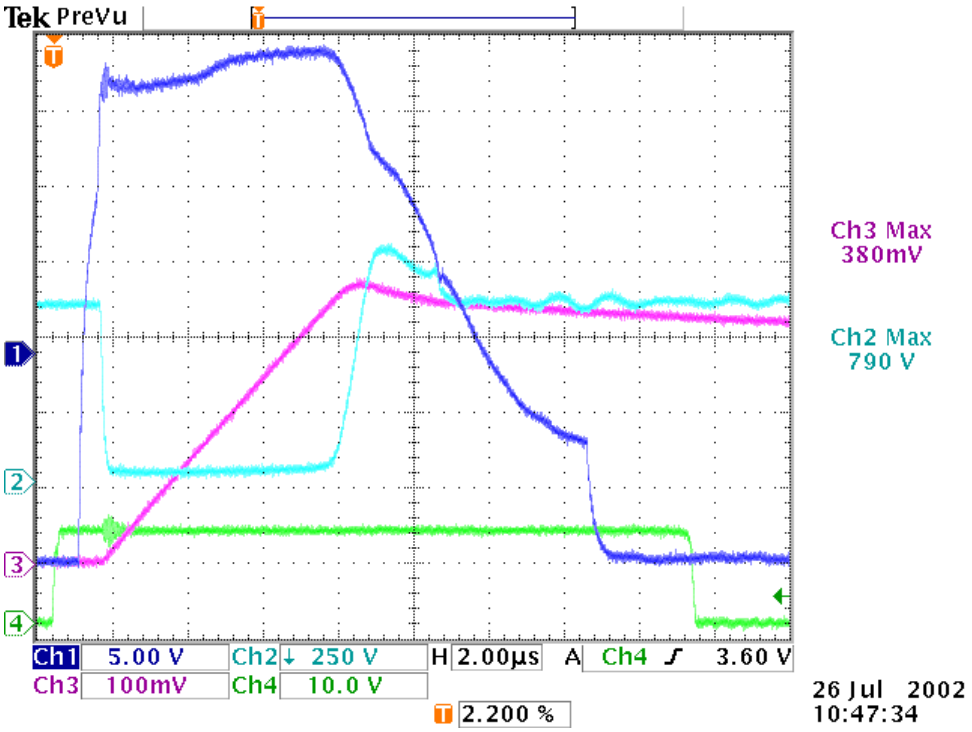


Figure 3.8.2: Typical short circuit turn-off with SSD

The short circuit turn-off depicted in Fig. 3.8.2 clearly shows the course of the Gate-Emitter voltage with SSD.

3.9 External fault input

The 2ED300C17-S features an external fault input **E.A** and **E.B**. These are used to set the internal fault memory by a high gate output signal and to trigger a fault. The fault inputs E.A and E.B have an active high logic. Switching level is at 5V, so that a high signal will trigger a fault. The maximum level for the input is V_{A+} or V_{B+} referenced to the adjoining COM.
This input is considered for example to detect an over-temperature and/or over-current and so to shut down the driver. **Note that the inputs E.A and E.B may rise up to DC-link potential!**

Note !
If the inputs E.A and/or E.B are not used, they have to be connected to COM A / COM B.

3.10 "Sense" input (SSD "Soft Shut Down", optional DVRC or active clamping)

A special feature of the 2ED300C17-S is the ability to directly manipulate the driver output stage. This is a bipolar output stage externally accessible via the "**Sense**" input.
This is necessary to limit the voltage overshoot through the di/dt during turn-off of the IGBTs. (See also chapter 3.8 SSD).
With an additional circuit and by using the sense input it is possible to control this di/dt in every operating point during turn-off of the IGBT and hence prevents inadmissibly high turn-off voltage overshoots.

A further application of the "Sense" input is the use of an **active clamping**** with direct feedback to the output stage. In this case the TVS diodes used are only minimally loaded which makes for example transile diodes possible. This can then be combined with an active clamping directly to the gate. (For more information see IFX AN 2007-05).

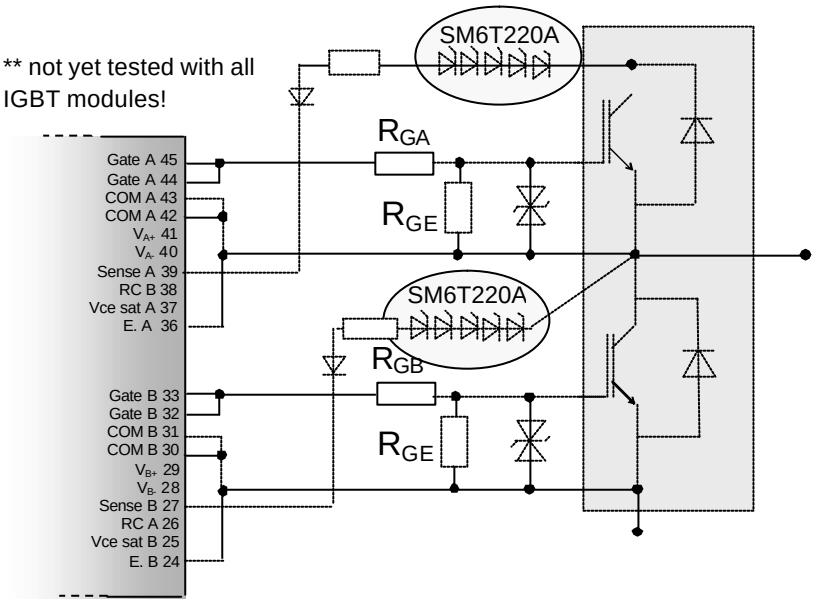


Figure 3.10 Utilization of the "Sense" input with active clamping

The standard application with the 2ED300C17-S /-ST is the "Soft Shut Down". This is a quasi- linear turn-off during fault condition. The "Soft Shut Down" has to be adapted to each module type. For this an external resistor R_{SSD} is connected between "Sense" and -16V.
(See chapter 3.8 Short circuit/over-current turn-off with "Soft Shut Down")

Note!
The "Soft Shut Down" is the standard setting of the 2ED300C17-S (-ST). For this a resistor R_{SSD} should be connected between "Sense" and –16V. If active clamping is used the R_{SSD} can also be utilized.

3.11 Additional output voltage / buffer capacitors

Depending on the utilization of the internal DC-DC SMPS an additional use of the secondary supply voltage is possible. This is made available on the outputs **+16V** and **–16V** and is referenced to the respective **COM**. This voltage is potential separated to the primary side. The ground COM is here referenced to the emitter of the respective IGBT. The outputs **+16V** and **–16V** are also used to connect buffer capacitors C_{sup}. These prevent voltage drops with high pulse currents. The buffer capacitors should be placed in closest vicinity to the 2ED300C17-S (-ST) and **must always be** used.

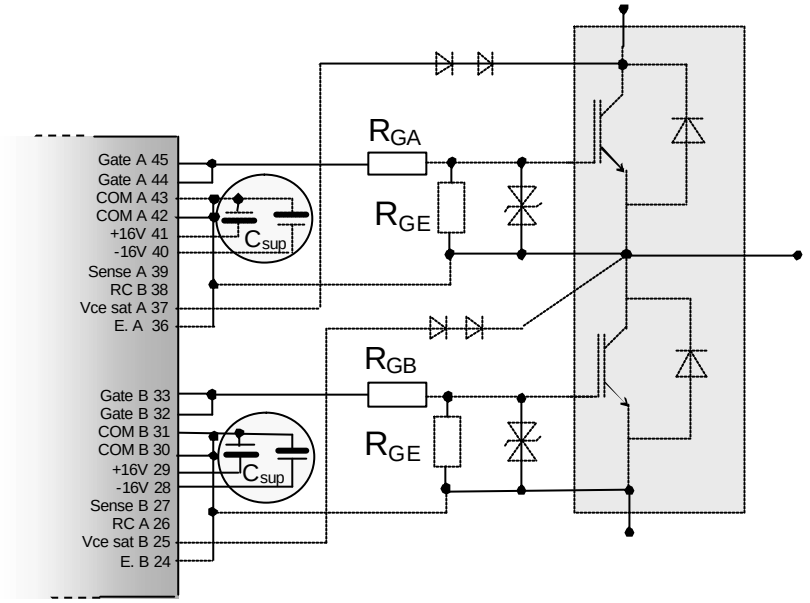


Figure 3.11 2ED300C17-S with external buffer capacitors

Note!
The additional electrolytics C_{sup} always have to be connected. When selecting these capacitors take note of the high ripple current requirement and ensure to design for application lifetime. Meaning, only caps with low impedance are to be used.

Our recommendation: 220uF max total capacitance per channel, should not to be exceeded. Ceramic caps may be considered as an alternative in applications requiring life times.

3.12 Application example 2ED300C17-S

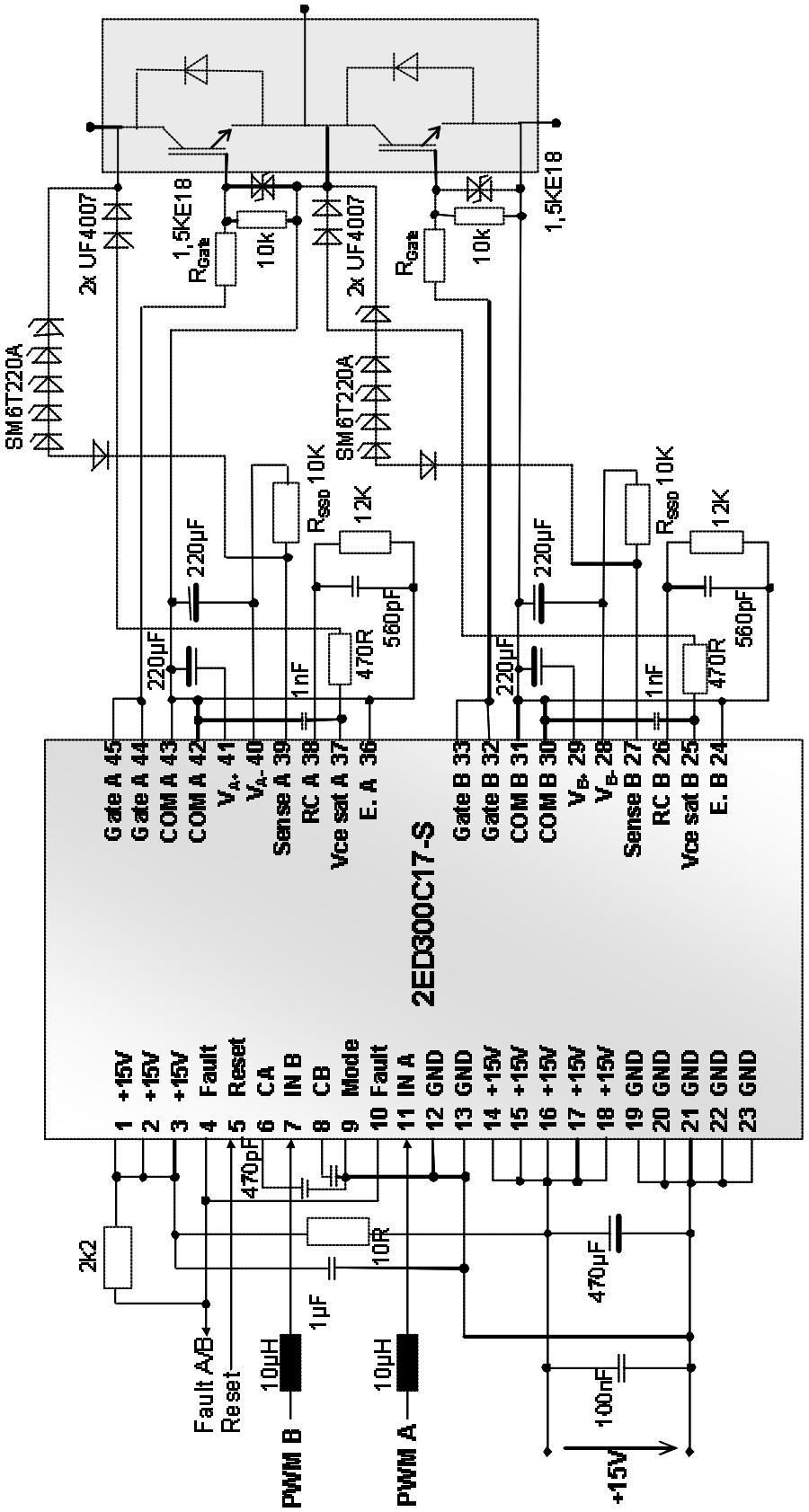


Fig. 3.12 Commissioning circuit in the direct mode:
(Both channels can be switched independently)

4 General

4.1 Designations and symbols

C_{ps}	coupling capacity primary/secondary
C_{RR}	coupling capacity sec. channel A to B
C_{sup}	buffer capacitor
C_{ies}	IGBT input capacity
$C_{ies\ max}$	max. admissible IGBT- Gate- capacity
C_{SX}	reference capacitor for time setting
C_{VCE}	$V_{CE\ sat}$ trigger suppression
COM	reference point
d	duty cycle
DVRC	Dynamic Voltage Rise Control
DOCD	dynamic over-current detection
dv/dt	voltage slew rate
di/dt	current rise time
EDFA	logic external fault input
f_S	switching frequency
f_{Smax}	max. admissible switching frequency
I_C	IGBT collector current
I_{DC}	current draw DC-DC
I_{DD}	current draw electronics
I_G	output peak current
$I_{G\ on}$	output peak current “On”
$I_{G\ off}$	output peak current “Off”
I_{OC}	logic signal output current
I_{out}	output current of $V_{A\cdot B\pm}$
$\lvert I_G \rvert_{AV}$	summed average gate current
$\lvert I_{out} \rvert_{AV}$	summed average output current
$I_{DC\ max}$	maximum primary current draw
$P_{DC/DC}$	peak output power
P_{SSD}	power of the SSD resistor
P_{DD}	driver power dissipation
P_G	maximum gate power dissipation
Q_G	max. IGBT gate charge at 15V
R_G	gate resistor
$R_{G\ min}$	minimum gate resistor
$R_{G\ intern}$	IGBT chip internal gate resistor
$R_{G\ extern}$	IGBT external gate resistor (Datasheet)
R_{GE}	gate-emitter resistor
R_{SSD}	Soft Shut Down resistor
R_{BX}	reference resistor voltage setting
R_{VCE}	$V_{CE\ sat}$ trigger suppression
SSD	Soft Shut Down
t_{TD}	interlock delay time
$t_{TD\ min}$	minimum interlock delay time
t_{BK}	reactivating time
t_{dif}	transition time difference
t_{md}	minimal pulse suppression
t_P	short circuit time
t_{ref}	reference time DOCD
t_{SD}	transition time SSD
t_{sys}	system transition times
t_{pd}	signal transition time
T_{op}	operating temperature
T_{stg}	storage temperature
V_{Level}	logic switching level
V_{DD}	supply voltage electronics primary
V_{DC}	primary DC/DC supply voltage
V_{iH}	maximum voltage of the logic levels
V_{iHS}	switching threshold logic signals
V_{in}	signal input voltage
V_{isol}	isolation test voltage
$V_{isol\ IO}$	isolation test input-output
$V_{isol\ 12}$	isolation test output A-output B
$V_{isol\ Su}$	surge test voltage input-output
V_{CE}	IGBT collector-emitter voltage
$V_{CE\ sat}$	IGBT saturation voltage
$V_{CE\ stat}$	$V_{CE\ sat}$ monitoring reference voltage
V_{ref}	reference voltage of the DOCD
V_{GE}	gate-emitter voltage
$V_{A;B+}$	secondary positive voltage
$V_{A;B-}$	secondary negative voltage

4.2 Type designation

EiceDRIVER™ **e**upec **I**GBT **c**ontrolled **e**fficiency DRIVER

For example: 2ED300C17-S

Isolationsklasse:
F = funktion isolation
S = safety isolation

Voltage class:
06 = 600V
12 = 1200V
17 = 1700V und 1200V
33 = 3300V
65 = 6500V

Driver type:
C = Driver core with DC/DC
E = Evaluation board
I = Driver IC (Coreless Transformer)
L = Driver IC (Level shifter)

Maximum output current:
z.B.
004 = 0.4 A
020 = 2.0 A
300 = 30.0 A

eupec IGBT driver

Driver channels
1 = single driver
2 = halfbride driver
6 = SixPACK driver

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