25AA128/25LC128

128K SPI Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25LC128	2.5-5.5V	64 Byte	I,E	P, SN, ST, MF
25AA128	1.8-5.5V	64 Byte	I	P, SN, ST, MF

Features

- Max. Clock 10 MHz
- Low-power CMOS Technology
  - Max. Write Current: 5 mA at 5.5V, 10 MHz
  - Read Current: 5 mA at 5.5V, 10 MHz
  - Standby Current: 5 μA at 5.5V
- 16,384 x 8-bit Organization
- 64 Byte Page
- Self-timed Erase and Write Cycles (5 ms max.)
- Block Write Protection
  - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection
  - Power-on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Sequential Read
- High Reliability
  - Endurance: 1,000,000 erase/write cycles
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Temperature Ranges Supported;
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C
- Pb-free and RoHS Compliant

Pin Function Table

Name	Function
CS	Chip Select Input
SO	Serial Data Output
WP	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
HOLD	Hold Input
Vcc	Supply Voltage

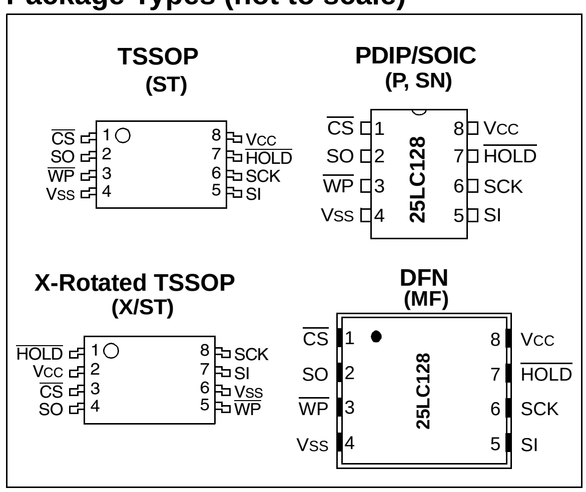
Description

The Microchip Technology Inc. 25AA128/25LC128 (25XX128*) are 128k-bit Serial Electrically Erasable PROMs. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (CS) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25XX128 is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead DFN and 8-lead TSSOP.

Package Types (not to scale)



* 25XX128 is used in this document as a generic part number for the 25AA128, 25LC128 devices.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.5V

All inputs and outputs w.r.t. V_{SS} .... -0.6V to V_{CC} +1.0V

Storage temperature .... -65°C to 150°C

Ambient temperature under bias .... -40°C to 125°C

ESD protection on all pins .... 4 kV

† NOTICE**:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
D001	V_{IH1}	High-level input voltage	.7 V_{CC}	V_{CC}+1	V	
D002	V_{IL1}	Low-level input voltage	-0.3	0.3V_{CC}	V	$V_{CC} \geq 2.7V$
D003	V_{IL2}		-0.3	0.2V_{CC}	V	V_{CC} < 2.7V
D004	V_{OL}	Low-level output voltage	—	0.4	V	I_{OL} = 2.1 mA
D005	V_{OL}		—	0.2	V	I_{OL} = 1.0 mA, V_{CC} < 2.5V
D006	V_{OH}	High-level output voltage	V_{CC} -0.5	—	V	I_{OH} = -400 μA
D007	I_{LI}	Input leakage current	—	±1	μA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} TO V_{CC}
D008	I_{LO}	Output leakage current	—	±1	μA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} TO V_{CC}
D009	C_{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	T_A = 25°C, CLK = 1.0 MHz, V_{CC} = 5.0V **(Note)**
D010	I_{CC} Read	Operating Current	— —	5 2.5	mA mA	V_{CC} = 5.5V; F_{CLK} = 10.0 MHz; SO = Open V_{CC} = 2.5V; F_{CLK} = 5.0 MHz; SO = Open
D011	I_{CC} Write		— —	5 3	mA mA	V_{CC} = 5.5V V_{CC} = 2.5V
D012	I_{CCS}	Standby Current	— —	5 1	μA μA	$\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS}, 125°C $\overline{CS}$ = V_{CC} = 5.5V, Inputs tied to V_{CC} or V_{SS}, 85°C

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	F_{CLK}	Clock Frequency	— — —	10 5 3	MHz MHz MHz	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
2	T_{CSS}	$\overline{CS}$ Setup Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
3	T_{CSH}	$\overline{CS}$ Hold Time	100 200 250	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
4	T_{CSD}	$\overline{CS}$ Disable Time	50	—	ns	—
5	T_{SU}	Data Setup Time	10 20 30	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
6	T_{HD}	Data Hold Time	20 40 50	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
7	T_R	CLK Rise Time	—	100	ns	**(Note 1)**
8	T_F	CLK Fall Time	—	100	ns	**(Note 1)**
9	T_{HI}	Clock High Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
10	T_{LO}	Clock Low Time	50 100 150	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
11	T_{CLD}	Clock Delay Time	50	—	ns	—
12	T_{CLE}	Clock Enable Time	50	—	ns	—
13	T_V	Output Valid from Clock Low	— — —	50 100 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
14	T_{HO}	Output Hold Time	0	—	ns	**(Note 1)**
15	T_{DIS}	Output Disable Time	— — —	40 80 160	ns ns ns	4.5V ≤ Vcc ≤ 5.5V**(Note 1)** 2.5V ≤ Vcc ≤ 4.5V**(Note 1)** 1.8V ≤ Vcc ≤ 2.5V**(Note 1)**
16	T_{HS}	$\overline{HOLD}$ Setup Time	20 40 80	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V

Note 1: This parameter is periodically sampled and not 100% tested.

2: T_{WC} begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I): T_A = -40°C to +85°C V_{CC} = 1.8V to 5.5V Automotive (E): T_A = -40°C to +125°C V_{CC} = 2.5V to 5.5V			
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
17	T_{HH}	$\overline{\text{HOLD}}$ Hold Time	20 40 80	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
18	T_{HZ}	$\overline{\text{HOLD}}$ Low to Output High-Z	30 60 160	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V**(Note 1)** 2.5V ≤ Vcc < 4.5V**(Note 1)** 1.8V ≤ Vcc < 2.5V**(Note 1)**
19	T_{HV}	$\overline{\text{HOLD}}$ High to Output Valid	30 60 160	— — —	ns ns ns	4.5V ≤ Vcc ≤ 5.5V 2.5V ≤ Vcc < 4.5V 1.8V ≤ Vcc < 2.5V
20	T_{WC}	Internal Write Cycle Time	—	5	ms	**(NOTE 2)**
21	—	Endurance	1,000,000	—	E/W Cycles	Page Mode, 25°C, V_{CC} = 5.5V **(NOTE 3)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: T_{WC} begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

3: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
V_{LO} = 0.2V	—
V_{HI} = V_{CC} - 0.2V	**(Note 1)**
V_{HI} = 4.0V	**(Note 2)**
C_L = 50 pF	**—**
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For V_{CC} ≤ 4.0V

2: For V_{CC} > 4.0V

FIGURE 1-1: HOLD TIMING

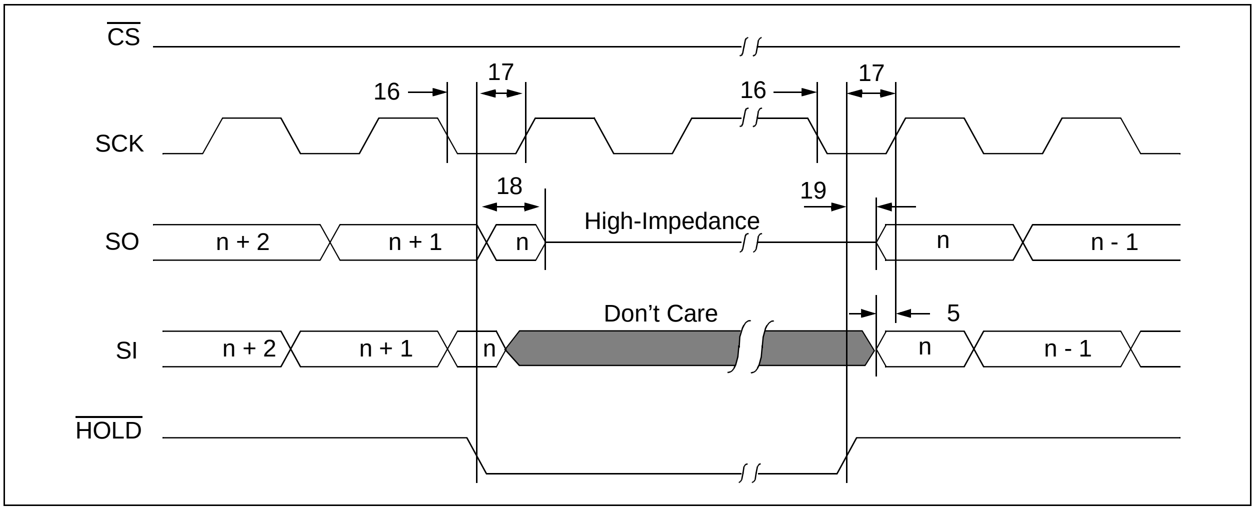


FIGURE 1-2: SERIAL INPUT TIMING

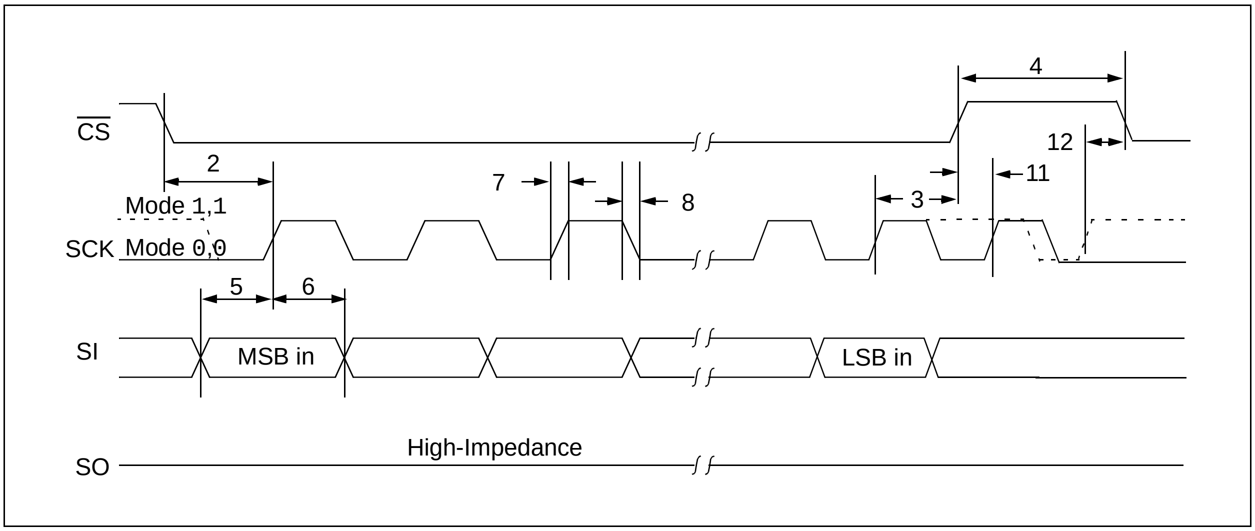
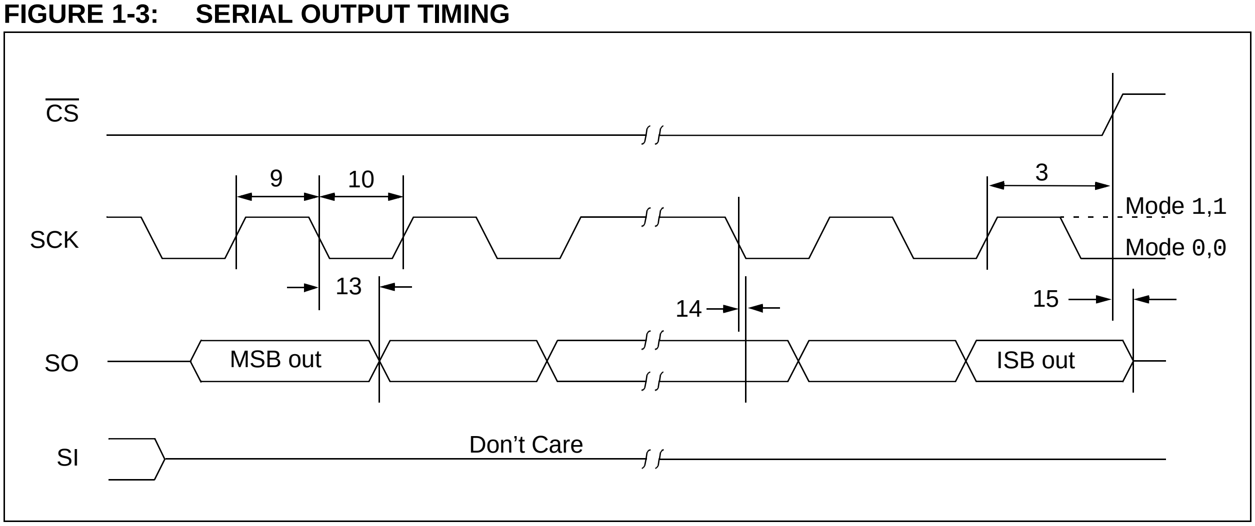


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25XX128 is a 16,384 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX128 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25XX128 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

2.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit `READ` instruction is transmitted to the 25XX128 followed by the 16-bit address, with two MSBs of the address being "don't care" bits. After the correct `READ` instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (3FFFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25XX128, the write enable latch must be set by issuing the `WREN` instruction (Figure 2-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX128. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the `WREN` instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a `WRITE` instruction, followed by the 16-bit address, with two MSBs of the address being "don't care" bits, and then the data to be written. Up to 64 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note:	Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the STATUS register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

BLOCK DIAGRAM

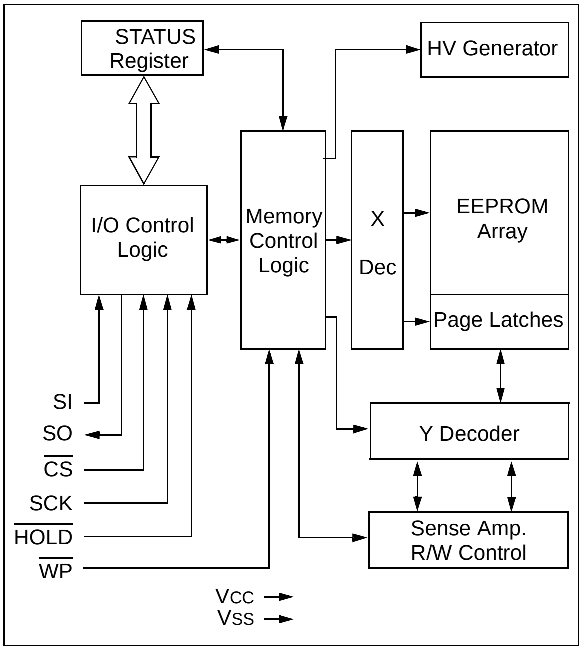


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register

FIGURE 2-1: READ SEQUENCE

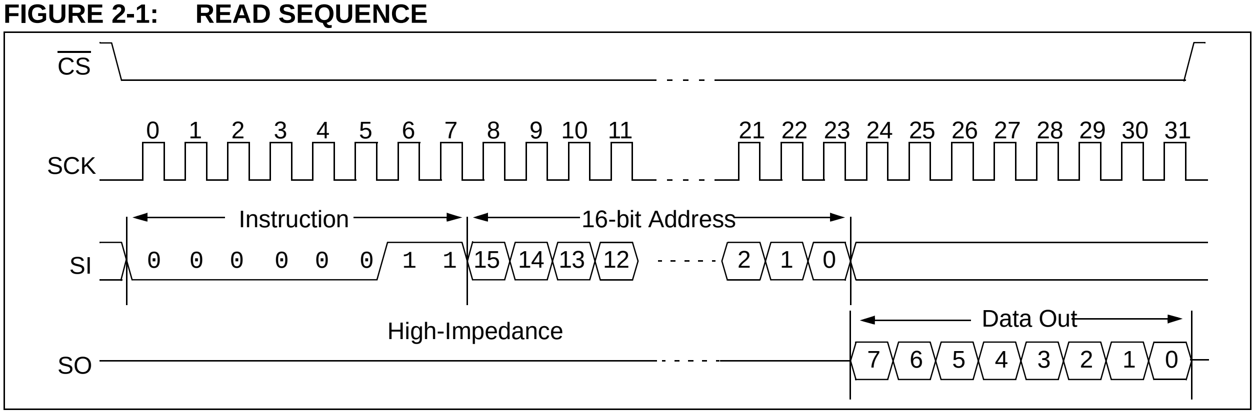


FIGURE 2-2: BYTE WRITE SEQUENCE

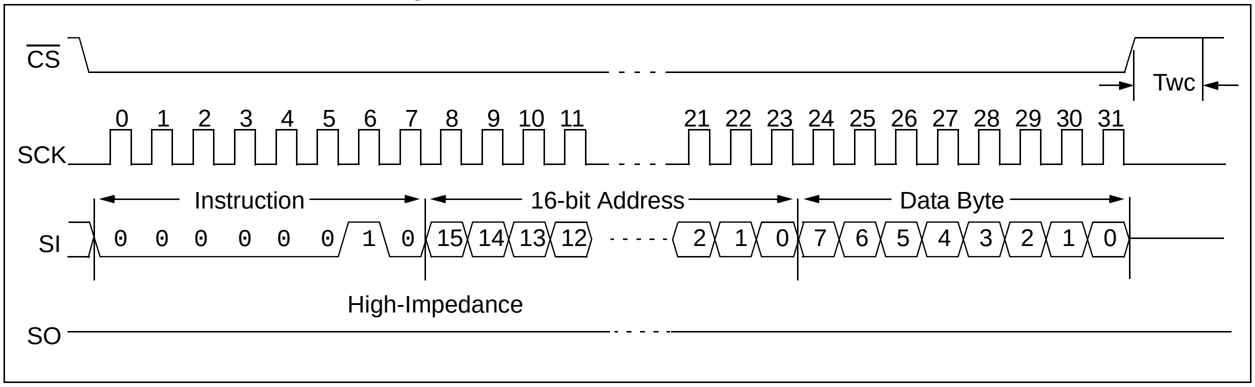
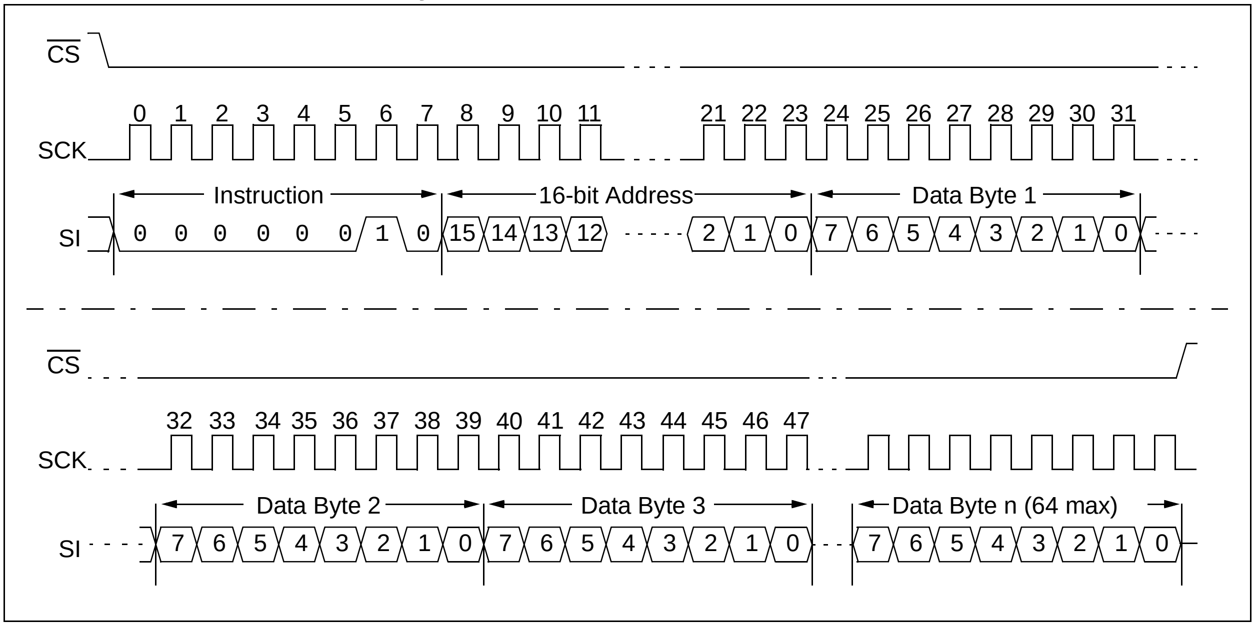


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX128 contains a write enable latch. See Table 2-4 for the Write-Protect functionality matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

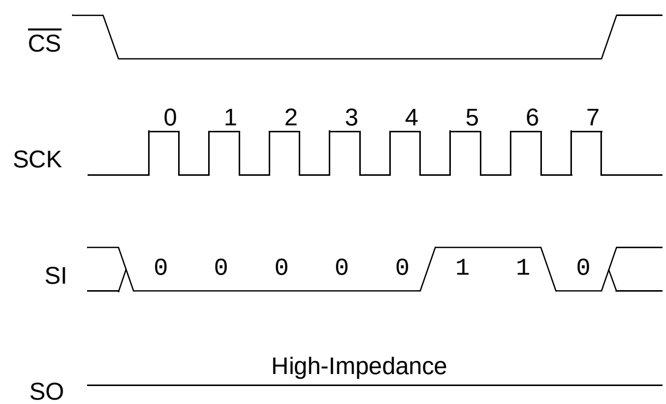
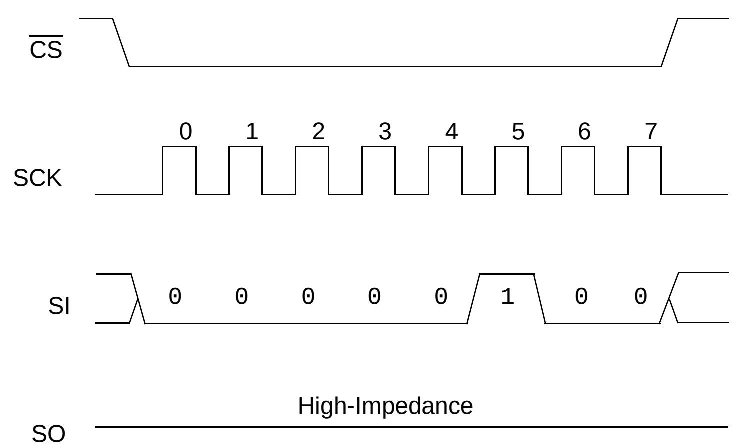


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	–	–	–	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

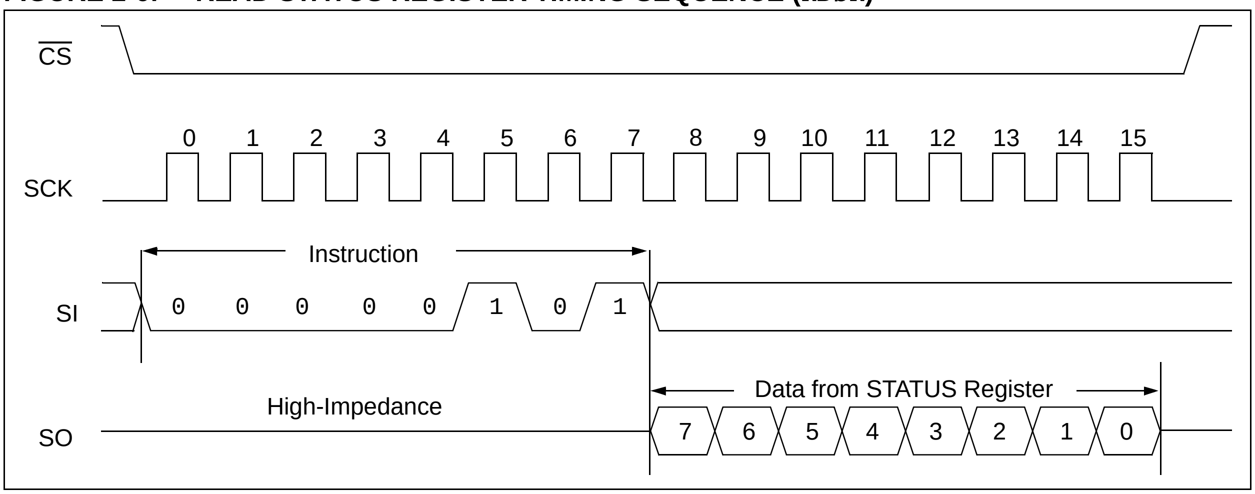
The **Write-In-Process (WIP)** bit indicates whether the 25XX128 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 2-3.

See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



2.6 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as shown in Table 2-3.

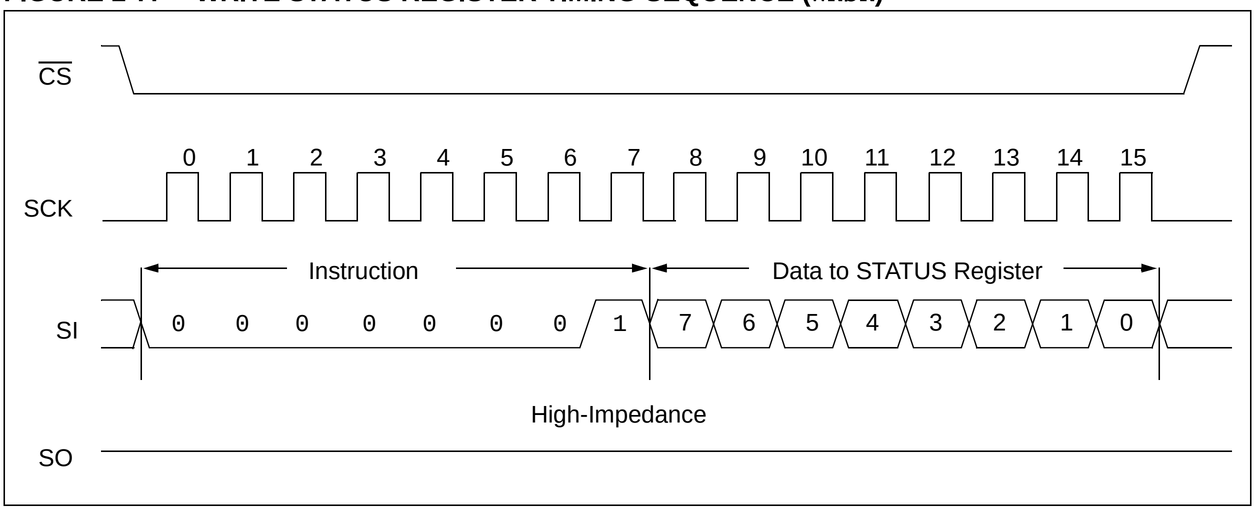
The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 2-4 for a matrix of functionality on the WPEN bit.

See Figure 2-7 for the WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (3000h-3FFFh)
1	0	upper 1/2 (2000h-3FFFh)
1	1	all (0000h-3FFFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



Note: An internal write cycle (T_{WC}) is initiated on the rising edge of $\overline{CS}$ after a valid write STATUS register

2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{\text{CS}}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25XX128 powers on in the following state:

- The device is in low-power Standby mode ($\overline{\text{CS}}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{\text{CS}}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{\text{WP}}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	X-Rotated Pin Number	Function
$\overline{\text{CS}}$	1	3	Chip Select Input
SO	2	4	Serial Data Output
$\overline{\text{WP}}$	3	5	Write-Protect Pin
VSS	4	6	Ground
SI	5	7	Serial Data Input
SCK	6	8	Serial Clock Input
$\overline{\text{HOLD}}$	7	1	Hold Input
VCC	8	2	Supply Voltage

Note: The exposed pad on the DFN package can be connected to VSS or left floating.

3.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX128. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{\text{WP}}$)

This pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{\text{WP}}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register is disabled. All other operations function normally. When $\overline{\text{WP}}$ is high, all functions, including writes to the nonvolatile bits in the STATUS register, operate normally. If the WPEN bit is set, $\overline{\text{WP}}$ low during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{\text{WP}}$ going low will have no effect on the write.

The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the 25XX128 in a system with $\overline{\text{WP}}$ pin grounded and still be able to write to the STATUS register. The $\overline{\text{WP}}$ pin functions will be enabled when the WPEN bit is set high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX128. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

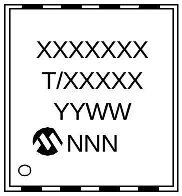
3.6 Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to suspend transmission to the 25XX128 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{\text{HOLD}}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{\text{HOLD}}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX128 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{\text{HOLD}}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

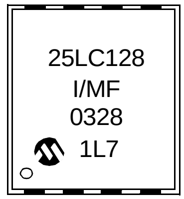
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

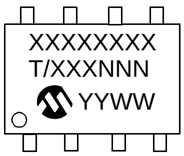
8-Lead DFN



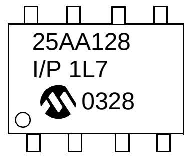
Example:



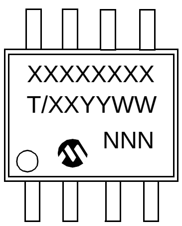
8-Lead PDIP



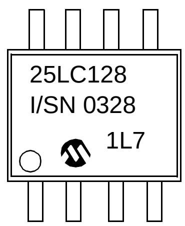
Example:



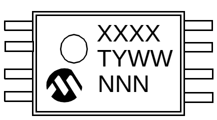
8-Lead SOIC



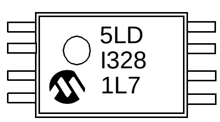
Example:



8-Lead TSSOP



Example:



TSSOP 1st Line Marking	
Device	**std mark**
25AA128	5AD
25AA128X	5ADX
25LC128	5LD
25LC128X	5LDX

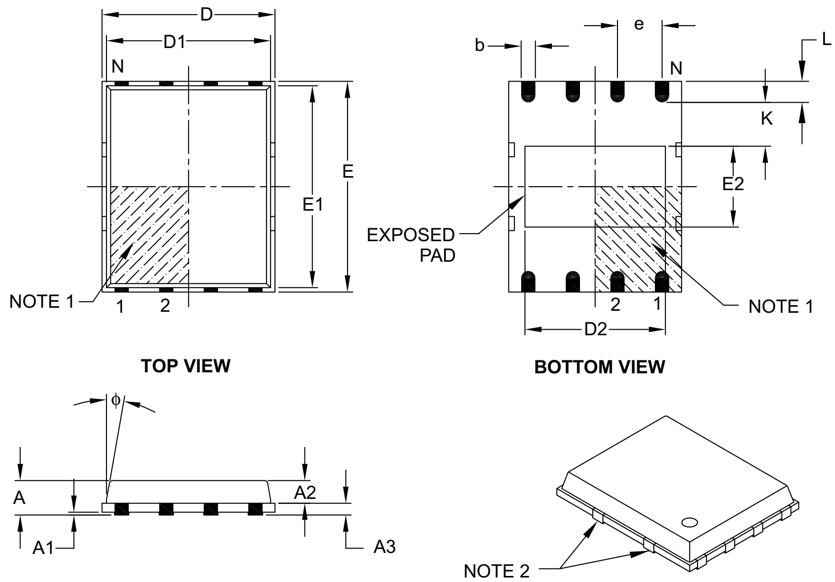
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	0.85	1.00
Molded Package Thickness	A2	–	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–
Model Draft Angle Top	ϕ	–	–	12°

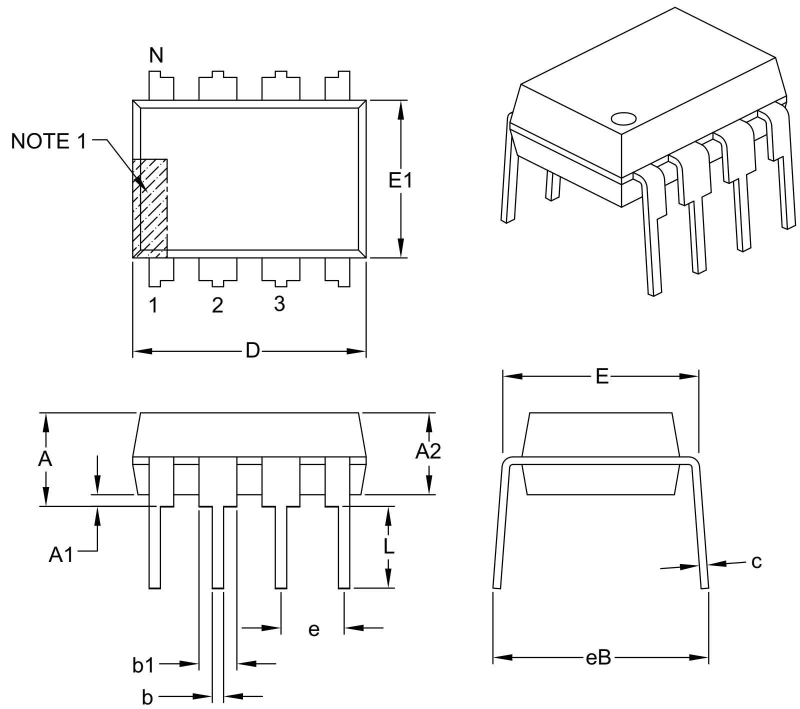
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

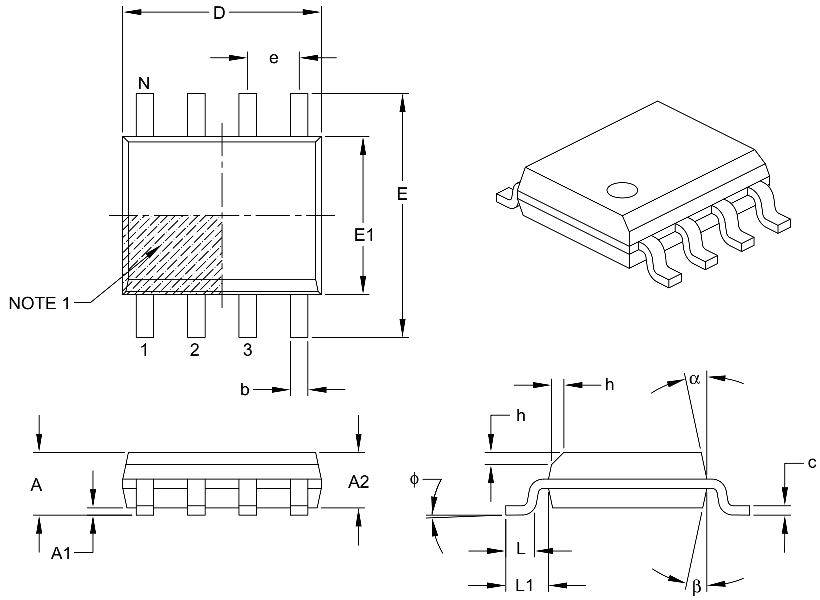
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

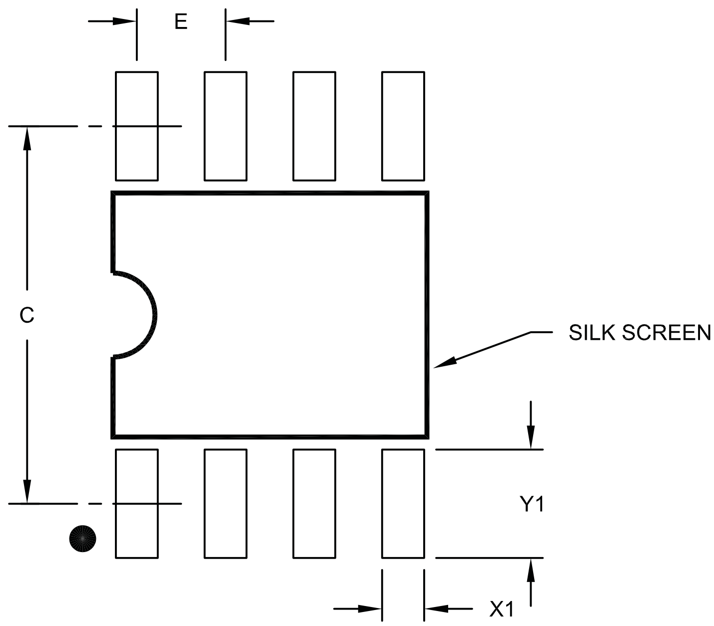
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

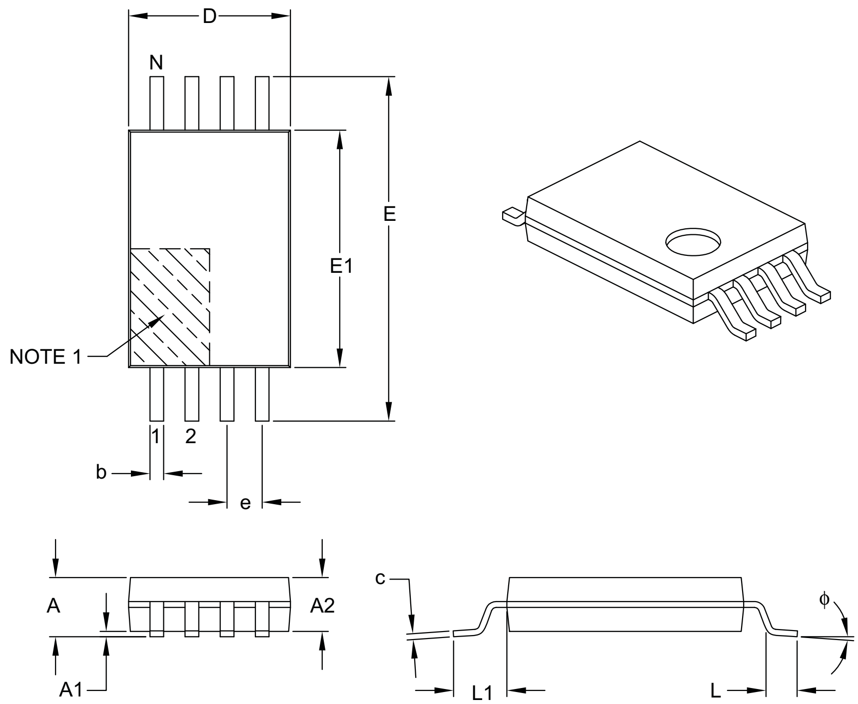
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

APPENDIX A: REVISION HISTORY

Revision B

Corrections to Section 1.0, Electrical Characteristics.

Revision C (5/07)

Removed Preliminary status; Revised Table 1-2, Para. 7 and 8; Revised Table 1-3, CL; Revised trademarks; Replaced Package drawings (Rev. AP); Replaced On-Line Support; Revised Product ID section.

Revision D (06/09)

Added X-Rotated TSSOP to package types; Revised Table 1-2, Param. 21; Revised Table 3-1; Revised TSSOP Line Marking table; Added SOIC Land Pattern; Revised Product ID section.

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____

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5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

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____

7. How would you improve this document?

____

____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	X	/XX
Device	Tape & Reel		Temp Range	Package

Device:	25AA128	=	128k-bit, 1.8V, 64-Byte Page, SPI Serial EEPROM
	25LC128	=	128k-bit, 2.5V, 64-Byte Page, SPI Serial EEPROM
	25AA128X	=	128k-bit, 1.8V, 64-Byte Page, SPI Serial EEPROM in alternate pinout (ST only)
	25LC128X	=	128k-bit, 2.5V, 64-Byte Page, SPI Serial EEPROM in alternate pinout (ST only)
Tape & Reel:	Blank	=	Standard packaging (tube)
	T	=	Tape & Reel
Temperature Range:	I	=	-40°C to+85°C
	E	=	-40°C to+125°C
Package:	MF	=	Micro Lead Frame (6 x 5 mm body), 8-lead
	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (3.90 mm body), 8-lead
	ST	=	TSSOP, 8-lead

Examples:

a) 25AA128T-I/SN = 128k-bit, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package

b) 25AA128T-I/ST = 128k-bit, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, TSSOP package

c) 25LC128-I/P = 128k-bit, 2.5V Serial EEPROM, Industrial temp., P-DIP package

d) 25LC128T-E/MF = 128k-bit, 2.5V Serial EEPROM, Extended temp., Tape & Reel, DFN package

e) 25LC128XT-I/ST = 128k-bit, 2.5V Serial EEPROM, Industrial temp., Tape & Reel, Rotated pinout, TSSOP package

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