SAMA5D27 SOM1

SAMA5D27 MPU, 1Gbit (128MB) DDR2 SDRAM, 10/100 Ethernet PHY, 64Mbit (8MB) Flash, Power Management IC, 1Kbit EEPROM

Introduction

The Microchip SAMA5D27 SOM1 is a small single-sided System-On-Module (SOM) based on the high-performance System-in-Package 32-bit Arm® Cortex®-A5 processor-based MPU SAMA5D27 and 1Gb DDR2 SDRAM running up to 500 MHz.

The SAMA5D27 SOM1 is built on a common set of proven Microchip components to reduce time to market by simplifying hardware design and software development.

The SOM also limits design rules of the main application board, reducing overall PCB complexity and cost. The SAMA5D27 SOM1 is delivered with a free Linux distribution and bare metal C examples.

Figure 1. SAMA5D27 SOM1

Features

- System-In-Package (SAMA5D27C-D1G-CU) including:
    - Arm Cortex-A5 processor-based SAMA5D2 MPU
    - 1Gbit DDR2 SDRAM
- On-Board Power Management Unit (MIC2800-G1JJYML)
- 1Kb Serial EEPROM with EUI-48™ Node Identity (24AA02E48T-I/OT)

- 64Mb Serial Quad I/O Flash Memory (SST26VF064BT-104I/MF)
- 10Base-T/100Base-TX Ethernet PHY (KSZ8081RNAIA)
- 40 x 38 mm Module, Pitch 0.8mm, solderable by hand
- 103 I/Os
- Up to 7 Tampers
- One USB Device, one USB Host and one HSIC Interface
- Shutdown and Reset Control Pins
- Independent Power Supplies Available for Camera Sensor, for SD Card and for Backup depending on Voltage Domains
- Operational Specifications:
  - Main operating voltage: 3.3V ± 5%
  - Temperature range: -40°C to 85°C
  - Integrated crystals, internal voltage regulators
  - Multiple interfaces and I/Os for easy application development

Applications

- Industrial Applications
- Motor Control
- Human Machine Interface
- Home Automation

Table of Contents

1. Description

The SAMA5D27 SOM1 is a high-performance System-On-Module based on the 32-bit ARM Cortex-A5 RISC SAMA5D2 processor. The SAMA5D27 SOM1 is certified for industrial operating conditions over a -40 to 85°C temperature range.

The system of the SAMA5D27 SOM1 operates at a maximum CPU operating frequency of 500 MHz and a maximum bus speed of 166 MHz. It features up to:

- 1 Gbit of DDR2 SDRAM memory (SAMA5D27C-D1G-CU)
- 1 Kb of EEPROM memory (24AA02E48T-I/OT) with EUI-48
- 64 Mb of QSPI Flash (SST26VF064BT-104I/MF) memory

The SAMA5D27 SOM1 is a 176-pin, 0.8mm pad pitch module with a 40mm x 38mm size.

The SAMA5D27 SOM1 offers an extensive peripheral set, including High-speed USB Host and Device, HSIC Interface, 10Base-T/100Base-TX Ethernet Interface, system control and up to 103 I/Os featuring:

- Up to 4 UARTS
- Up to 4 Flexcoms
- Up to 6 Capacitive Touch lines for up to 9 touch buttons
- Up to 4 ADC Inputs
- Up to 2 CAN
- Up to 7 Tamper Pins
- Serial Interfaces such as SPI, TWI, QSPI, SSC and I²S
- SD/MMC, eMMC, SDIO Interfaces
- Up to 24-bit LCD RGB Interface
- CMOS Camera Interface
- Mono PDMIC and Full-Bridge Class-D Stereo

Tip: Each I/O of the SAMA5D27 SOM1 is configurable, as either a general-purpose I/O line only, or as an I/O line multiplexed with up to six peripheral I/Os. As the multiplexing is hardware-defined, the hardware designer and programmer must carefully determine the configuration of the PIO Controllers required by their application.

2. Reference Documents

The SAMA5D27 SOM1 is equipped with various Microchip silicon devices. The relevant documentation is listed in the table below.

Type	Document Title	Available	Ref. No./Product
Datasheet	SAMA5D2	www.microchip.com/ SAMA5D2	DS60001476
Datasheet	SAMA5D2 System-In-Package (SIP)	www.microchip.com/ SAMA5D2 SIP	DS60001484
Datasheet	Serial EEPROMs with EUI-48 Node Identity	www.microchip.com/ 24AA02E48	24AA02E48T-I/OT
Datasheet	10BASE-T/100BASE-TX Ethernet PHY	www.microchip.com/ksz8081	KSZ8081RNAIA
Datasheet	Serial Quad I/O (SQI) Flash Memory	www.microchip.com/ sst26vf064b	SST26VF064BT-104I/MF
Datasheet	Digital Power Management IC	www.microchip.com/mic2800	MIC2800-G1JJYML

3. Block Diagram

Figure 3-1. SAMA5D27 SOM1 Block Diagram
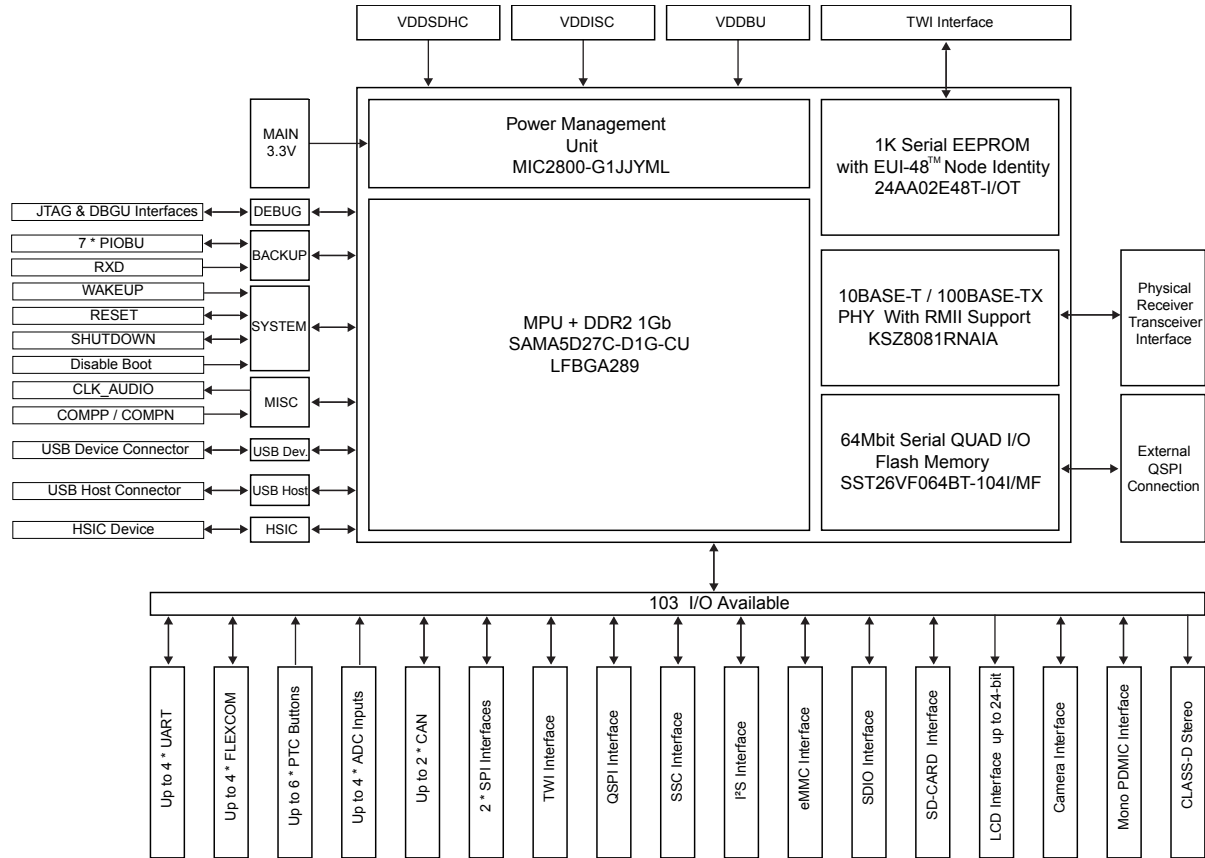
4.   Pinout

4.1   Pinout Overview

The categories of pins are listed below:

- Red: Power Supplies
- Black: Ground
- Blue: Signals
- Orange: Reserved for future use

Figure 4-1. SAMA5D27 SOM1 Pinout Overview

4.2 Pin List

The pin list of the SAMA5D27 SOM1 is provided in the following tables.

Table 4-1. System-On-Module Pin Description: PIOA

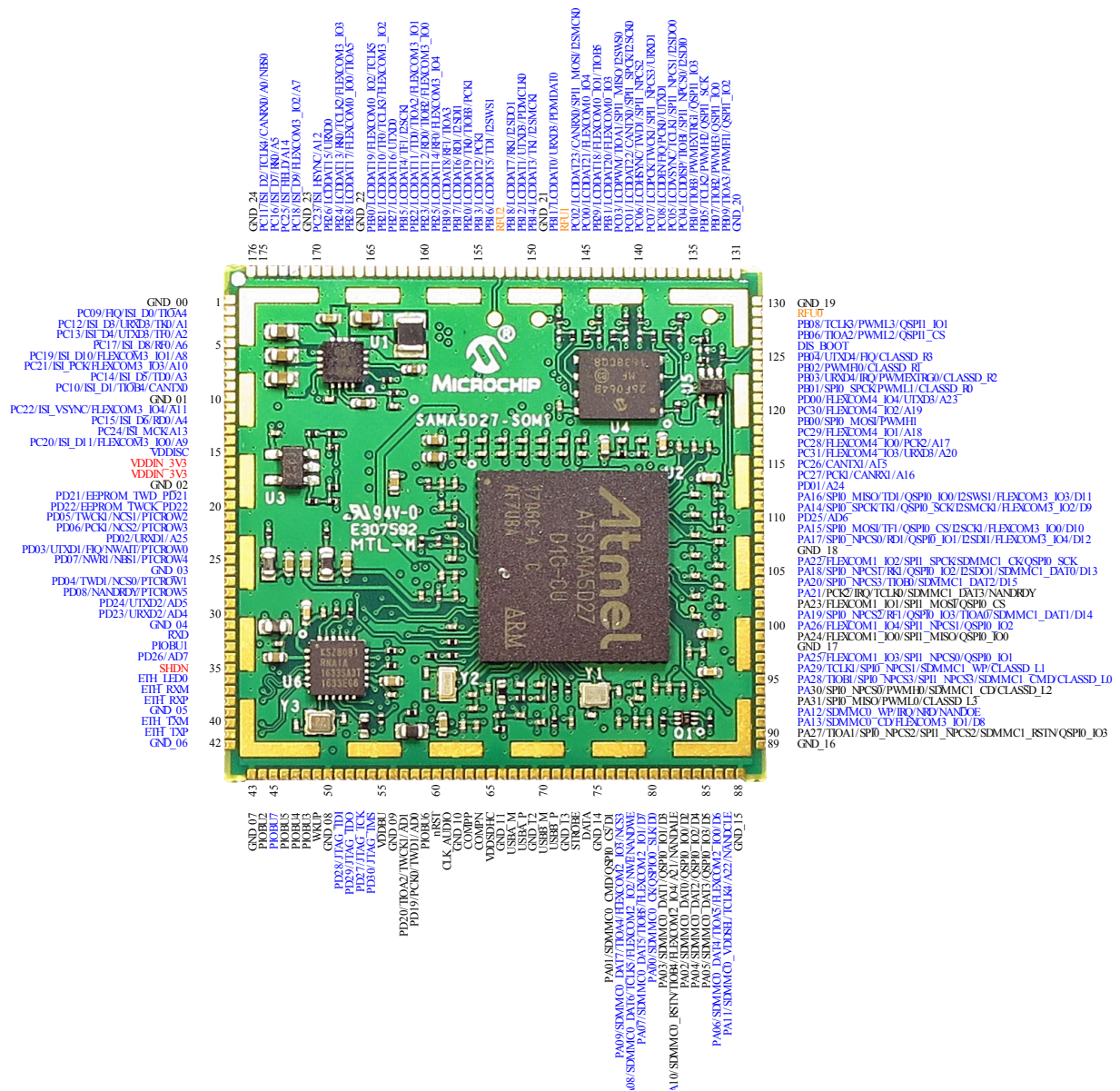| Pin Number	PIO	Power Rail	Other Features	Type
80	PA00	VDDSDHC	SDMMC0_CK/QSPIO0_SLK/D0	I/O
76	PA01	VDDSDHC	SDMMC0_CMD/QSPI0_CS/D1	I/O
83	PA02	VDDSDHC	SDMMC0_DAT0/QSPI0_IO0/D2	I/O
81	PA03	VDDSDHC	SDMMC0_DAT1/QSPI0_IO1/D3	I/O
84	PA04	VDDSDHC	SDMMC0_DAT2/QSPI0_IO2/D4	I/O
85	PA05	VDDSDHC	SDMMC0_DAT3/QSPI0_IO3/D5	I/O
86	PA06	VDDSDHC	SDMMC0_DAT4/TIOA5/FLEXCOM2_IO0/D6	I/O
79	PA07	VDDSDHC	SDMMC0_DAT5/TIOB5/FLEXCOM2_IO1/D7	I/O
78	PA08	VDDSDHC	SDMMC0_DAT6/TCLK5/FLEXCOM2_IO2/NWE/NANDWE	I/O
77	PA09	VDDSDHC	SDMMC0_DAT7/TIOA4/FLEXCOM2_IO3/NCS3	I/O
82	PA10	VDDSDHC	SDMMC0_RSTN/TIOB4/FLEXCOM2_IO4/A21/NANDALE	I/O
87	PA11	VDDIN_3V3	SDMMC0_VDDSEL/TCLK4/A22/NANDCLE	I/O
92	PA12	VDDIN_3V3	SDMMC0_WP/IRQ/NRD/NANDOE	I/O
91	PA13	VDDIN_3V3	SDMMC0_CD/FLEXCOM3_IO1/D8	I/O
111	PA14	VDDIN_3V3	SPI0_SPCK/TK1/QSPI0_SCK/I2SMCK1/FLEXCOM3_IO2/D9	I/O
109	PA15	VDDIN_3V3	SPI0_MOSI/TF1/QSPI0_CS/I2SCK1/FLEXCOM3_IO0/D10	I/O
112	PA16	VDDIN_3V3	SPI0_MISO/TD1/QSPI0_IO0/I2SWS1/FLEXCOM3_IO3/D11	I/O
108	PA17	VDDIN_3V3	SPI0_NPCS0/RD1/QSPI0_IO1/I2SDI1/FLEXCOM3_IO4/D12	I/O
105	PA18	VDDIN_3V3	SPI0_NPCS1/RK1/QSPI0_IO2/I2SDO1/SDMMC1_DAT0/D13	I/O
101	PA19	VDDIN_3V3	SPI0_NPCS2/RF1/QSPI0_IO3/TIOA0/SDMMC1_DAT1/D14	I/O

Pin Number	PIO	Power Rail	Other Features	Type
104	PA20	VDDIN_3V3	SPI0_NPCS3/TIOB0/ SDMMC1_DAT2/D15	I/O
103	PA21	VDDIN_3V3	PCK2/IRQ/TCLK0/SDMMC1_DAT3/ NANDRDY	I/O
106	PA22	VDDIN_3V3	FLEXCOM1_IO2/SPI1_SPCK/ SDMMC1_CK/QSPI0_SCK	I/O
102	PA23	VDDIN_3V3	FLEXCOM1_IO1/SPI1_MOSI/ QSPI0_CS	I/O
99	PA24	VDDIN_3V3	FLEXCOM1_IO0/SPI1_MISO/ QSPI0_IO0	I/O
97	PA25	VDDIN_3V3	FLEXCOM1_IO3/SPI1_NPCS0/ QSPI0_IO1	I/O
100	PA26	VDDIN_3V3	FLEXCOM1_IO4/SPI1_NPCS1/ QSPI0_IO2	I/O
90	PA27	VDDIN_3V3	TIOA1/SPI0_NPCS2/SPI1_NPCS2/ SDMMC1_RSTN/QSPI0_IO3	I/O
95	PA28	VDDIN_3V3	TIOB1/SPI0_NPCS3/SPI1_NPCS3/ SDMMC1_CMD/CLASSD_L0	I/O
96	PA29	VDDIN_3V3	TCLK1/SPI0_NPCS1/SDMMC1_WP/ CLASSD_L1	I/O
94	PA30	VDDIN_3V3	SPI0_NPCS0/PWMH0/ SDMMC1_CD/CLASSD_L2	I/O
93	PA31	VDDIN_3V3	SPI0_MISO/PWML0/CLASSD_L3	I/O

Table 4-2. System-On-Module Pin Description: PIOB

Pin Number	PIO	Power Rail	Other Features	Type
119	PB00	VDDIN_3V3	SPI0_MOSI/PWMH1	I/O
122	PB01	VDDIN_3V3	SPI0_SPCK/PWML1/CLASSD_R0	I/O
124	PB02	VDDIN_3V3	PWMFI0/CLASSD_R1	I/O
123	PB03	VDDIN_3V3	URXD4/IRQ/PWMEXTRG0/ CLASSD_R2	I/O
125	PB04	VDDIN_3V3	UTXD4/FIQ/CLASSD_R3	I/O
134	PB05	VDDIN_3V3	TCLK2/PWMH2/QSPI1_SCK	I/O
127	PB06	VDDIN_3V3	TIOA2/PWML2/QSPI1_CS	I/O
133	PB07	VDDIN_3V3	TIOB2/PWMH3/QSPI1_IO0	I/O
128	PB08	VDDIN_3V3	TCLK3/PWML3/QSPI1_IO1	I/O
132	PB09	VDDIN_3V3	TIOA3/PWMFI1/QSPI1_IO2	I/O

Pin Number	PIO	Power Rail	Other Features	Type
135	PB10	VDDIN_3V3	TIOB3/PWMEXTRG1/QSPI1_IO3	I/O
148	PB11	VDDIN_3V3	LCDDAT0/URXD3/PDMDAT0	I/O
151	PB12	VDDIN_3V3	LCDDAT1/UTXD3/PDMCLK0	I/O
155	PB13	VDDIN_3V3	LCDDAT2/PCK1	I/O
150	PB14	VDDIN_3V3	LCDDAT3/TK1/I2SMCK1	I/O
162	PB15	VDDIN_3V3	LCDDAT4/TF1/I2SCK1	I/O
154	PB16	VDDIN_3V3	LCDDAT5/TD1/I2SWS1	I/O
157	PB17	VDDIN_3V3	LCDDAT6/RD1/I2SDI1	I/O
152	PB18	VDDIN_3V3	LCDDAT7/RK1/I2SDO1	I/O
158	PB19	VDDIN_3V3	LCDDAT8/RF1/TIOA3	I/O
156	PB20	VDDIN_3V3	LCDDAT9/TK0/TIOB3/PCK1	I/O
164	PB21	VDDIN_3V3	LCDDAT10/TF0/TCLK3/ FLEXCOM3_IO2	I/O
161	PB22	VDDIN_3V3	LCDDAT11/TD0/TIOA2/ FLEXCOM3_IO1	I/O
160	PB23	VDDIN_3V3	LCDDAT12/RD0/TIOB2/ FLEXCOM3_IO0	I/O
168	PB24	VDDIN_3V3	LCDDAT13/RK0/TCLK2/ FLEXCOM3_IO3	I/O
159	PB25	VDDIN_3V3	LCDDAT14/RF0/FLEXCOM3_IO4	I/O
169	PB26	VDDIN_3V3	LCDDAT15/URXD0	I/O
163	PB27	VDDIN_3V3	LCDDAT16/UTXD0	I/O
167	PB28	VDDIN_3V3	LCDDAT17/FLEXCOM0_IO0/TIOA5	I/O
144	PB29	VDDIN_3V3	LCDDAT18/FLEXCOM0_IO1/TIOB5	I/O
165	PB30	VDDIN_3V3	LCDDAT19/FLEXCOM0_IO2/TCLK5	I/O
143	PB31	VDDIN_3V3	LCDDAT20/FLEXCOM0_IO3	I/O

Table 4-3. System On Module Pin Table : PIOC

Pin Number	PIO	Power Rail	Other Features	Type
145	PC00	VDDIN_3V3	LCDDAT21/FLEXCOM0_IO4	I/O
141	PC01	VDDIN_3V3	LCDDAT22/CANTX0/SPI1_SPCK/ I2SCK0	I/O
146	PC02	VDDIN_3V3	LCDDAT23/CANRX0/SPI1_MOSI/ I2SMCK0	I/O

Pin Number	PIO	Power Rail	Other Features	Type
142	PC03	VDDIN_3V3	LCDPWM/TIOA1/SPI1_MISO/I2SWS0	I/O
136	PC04	VDDIN_3V3	LCDDISP/TIOB1/SPI1_NPCS0/I2SDI0	I/O
137	PC05	VDDIN_3V3	LCDVSYNC/TCLK1/SPI1_NPCS1/I2SDO0	I/O
140	PC06	VDDIN_3V3	LCDHSYNC/TWD1/SPI1_NPCS2	I/O
139	PC07	VDDIN_3V3	LCDPCK/TWCK1/SPI1_NPCS3/URXD1	I/O
138	PC08	VDDIN_3V3	LCDDEN/FIQ/PCK0/UTXD1	I/O
2	PC09	VDDISC	FIQ/ISI_D0/TIOA4	I/O
9	PC10	VDDISC	ISI_D1/TIOB4/CANTX0	I/O
175	PC11	VDDISC	ISI_D2/TCLK4/CANRX0/A0/NBS0	I/O
3	PC12	VDDISC	ISI_D3/URXD3/TK0/A1	I/O
4	PC13	VDDISC	ISI_D4/UTXD3/TF0/A2	I/O
8	PC14	VDDISC	ISI_D5/TD0/A3	I/O
12	PC15	VDDISC	ISI_D6/RD0/A4	I/O
174	PC16	VDDISC	ISI_D7/RK0/A5	I/O
5	PC17	VDDISC	ISI_D8/RF0/A6	I/O
172	PC18	VDDISC	ISI_D9/FLEXCOM3_IO2/A7	I/O
6	PC19	VDDISC	ISI_D10/FLEXCOM3_IO1/A8	I/O
14	PC20	VDDISC	ISI_D11/FLEXCOM3_IO0/A9	I/O
7	PC21	VDDISC	ISI_PCK/FLEXCOM3_IO3/A10	I/O
11	PC22	VDDISC	ISI_VSYNC/FLEXCOM3_IO4/A11	I/O
170	PC23	VDDISC	ISI_HSYNC/A12	I/O
13	PC24	VDDISC	ISI_MCK/A13	I/O
173	PC25	VDDISC	ISI_FIELD/A14	I/O
115	PC26	VDDIN_3V3	CANTX1/A15	I/O
114	PC27	VDDIN_3V3	PCK1/CANRX1/A16	I/O
117	PC28	VDDIN_3V3	FLEXCOM4_IO0/PCK2/A17	I/O
118	PC29	VDDIN_3V3	FLEXCOM4_IO1/A18	I/O
120	PC30	VDDIN_3V3	FLEXCOM4_IO2/A19	I/O
116	PC31	VDDIN_3V3	FLEXCOM4_IO3/URXD3/A20	I/O

Table 4-4. System-On-Module Pin Description: PIOD

Pin Number	PIO	Power Rail	Other Features	Type
121	PD00	VDDIN_3V3	FLEXCOM4_IO4/UTXD3/A23	I/O
113	PD01	VDDIN_3V3	A24	I/O
23	PD02	VDDIN_3V3	URXD1/A25	I/O
24	PD03	VDDIN_3V3	UTXD1/FIQ/NWAIT/PTCROW0	I/O
27	PD04	VDDIN_3V3	TWD1/NCS0/PTCROW1	I/O
21	PD05	VDDIN_3V3	TWCK1/NCS1/PTCROW2	I/O
22	PD06	VDDIN_3V3	PCK1/NCS2/PTCROW3	I/O
25	PD07	VDDIN_3V3	NWR1/NBS1/PTCROW4	I/O
28	PD08	VDDIN_3V3	NANDRDY/PTCROW5	I/O
58	PD19	VDDIN_3V3	PCK0/TWD1/AD0	I/O
57	PD20	VDDIN_3V3	TIOA2/TWCK1/AD1	I/O
19	PD21	VDDIN_3V3	EEPROM_TWD_PD21	I/O
20	PD22	VDDIN_3V3	EEPROM_TWCK_PD22	I/O
30	PD23	VDDIN_3V3	URXD2/AD4	I/O
29	PD24	VDDIN_3V3	UTXD2/AD5	I/O
110	PD25	VDDIN_3V3	AD6	I/O
34	PD26	VDDIN_3V3	AD7	I/O
53	PD27	VDDIN_3V3	JTAG_TCK	I/O
51	PD28	VDDIN_3V3	JTAG_TDI	I/O
52	PD29	VDDIN_3V3	JTAG_TDO	I/O
54	PD30	VDDIN_3V3	JTAG_TMS	I/O

Table 4-5. System-On-Module Pin Description: System

Pin Number	PIO	Power Rail	Designation	Type
61	CLK_AUDIO	VDDIN_3V3	Audio clock	Output
64	COMPN	VDDBU	External analog comparator input	Input
63	COMPP	VDDBU	External analog comparator input	Input
126	DIS_BOOT	VDDIN_3V3	QSPI Interface Disable pin	Input
67	USBA_M	VDDIN_3V3	USB Device High Speed Data -	–
68	USBA_P	VDDIN_3V3	USB Device High Speed Data +	–
70	USBB_M	VDDIN_3V3	USB Host Port B High Speed Data -	–
71	USBB_P	VDDIN_3V3	USB Host Port B High Speed Data +	–

Pin Number	PIO	Power Rail	Designation	Type
74	DATA	VDDHSIC	USB High-Speed Inter-Chip Data	–
73	STROBE	VDDHSIC	USB High-Speed Inter-Chip Strobe	–
60	NRST	VDDIN_3V3	Microprocessor reset	Input / Active Low
33	PIOBU1	VDDBU	Tamper or Wakeup input	Input
44	PIOBU2	VDDBU	Tamper or Wakeup input	Input
48	PIOBU3	VDDBU	Tamper or Wakeup input	Input
47	PIOBU4	VDDBU	Tamper or Wakeup input	Input
46	PIOBU5	VDDBU	Tamper or Wakeup input	Input
59	PIOBU6	VDDBU	Tamper or Wakeup input	Input
45	PIOBU7	VDDBU	Tamper or Wakeup input	Input
32	RXD	VDDBU	Low Power Asynchronous Receiver	Input
35	SHDN	VDDBU	Shutdown Control	Output
49	WKUP	VDDBU	Wakeup	Input
36	ETH_LED0	VDDIN_3V3	Status LED control for Ethernet ports	Output
37	ETH_RXM	± 2.5V	Physical receive or transmit signal (– differential)	I/O
38	ETH_RXP	± 2.5V	Physical receive or transmit signal (+ differential)	I/O
40	ETH_TXM	± 2.5V	Physical receive or transmit signal (– differential)	I/O
41	ETH_TXP	± 2.5V	Physical receive or transmit signal (+ differential)	I/O

Table 4-6. System-On-Module Pin Description: Power

Pin Number	PIO	Description	Comments
16,17	VDDIN_3V3	Main 3.3V Supply inputs. Used for Peripheral I/O lines and MIC2800-G1JJYML supplies.	–
55	VDDBU	Input supply for Slow Clock Oscillator, internal 32 kHz RC Oscillator and a part of the System Controller	–
65	VDDSDHC	SDMMC I/O lines supply input	–
15	VDDISC	Image Sensor I/O lines supply input	For decoupling guidelines, refer to the section "Design Guidelines".

Pin Number	PIO	Description	Comments
1, 10, 18, 26, 31, 39, 42, 43, 50, 56, 62, 66, 69, 72, 75, 88, 89, 98, 107, 130, 131, 149, 166, 171, 176	GND	Ground connections	Must be connected together
129	RFU0	Reserved for future use	Must be left floating
147	RFU1	Reserved for future use	Must be left floating
153	RFU2	Reserved for future use	Must be left floating

5. Functional Description

5.1 SAMA5D27 System-In-Package

The SAMA5D2 System-In-Package (SIP) (SAMA5D27C-D1G-CU) integrates the ARM Cortex-A5 processor-based SAMA5D2 MPU with 1 Gbit DDR2-SDRAM in a single package.

By combining the high-performance, ultra-low-power SAMA5D2 with DDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced. This makes board design easier and lowers the overall cost of bill of materials. Board design is more robust by facilitating design for EMI, ESD and signal integrity.

For more information about the SIP, see "Reference Documents". This section lists the sole reference documents for product information on the SAMA5D2 and the DDR2-SDRAM memory.

The SAMA5D27C-D1G-CU is available in a 289-ball TFBGA package.

Connections of the supplies and the system pins of the SAMA5D27C-D1G-CU are described in the following schematics.

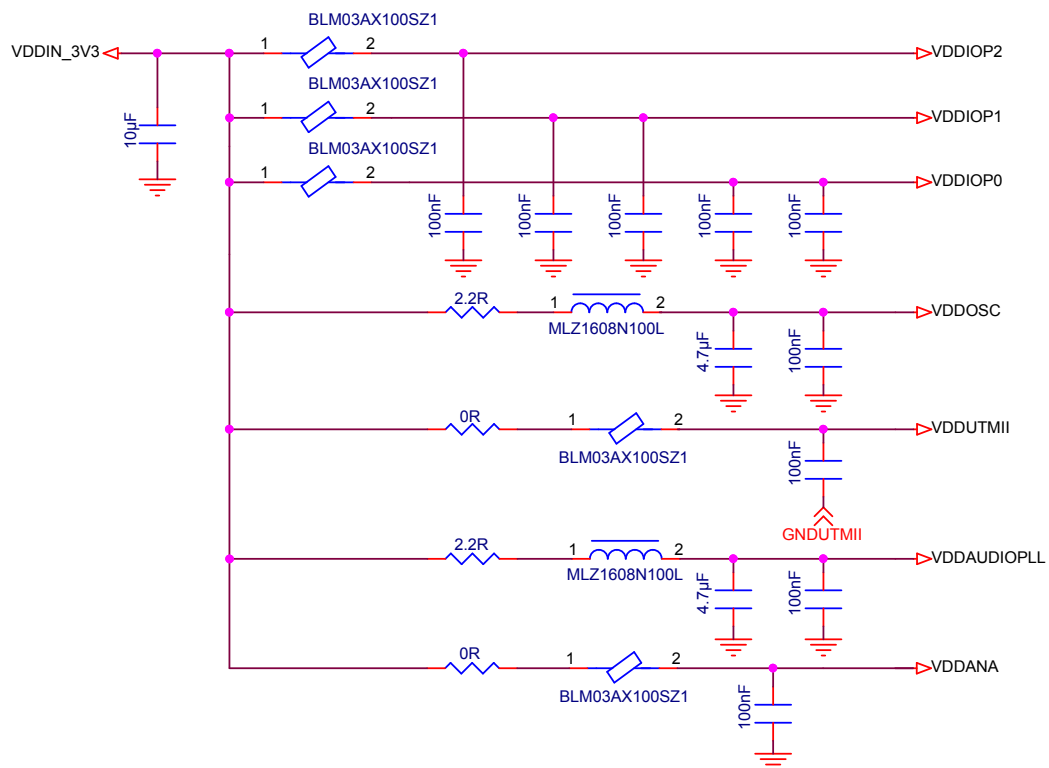**Figure 5-1. SAMA5D27C-D1G-CU Supplies Distribution Schematic**

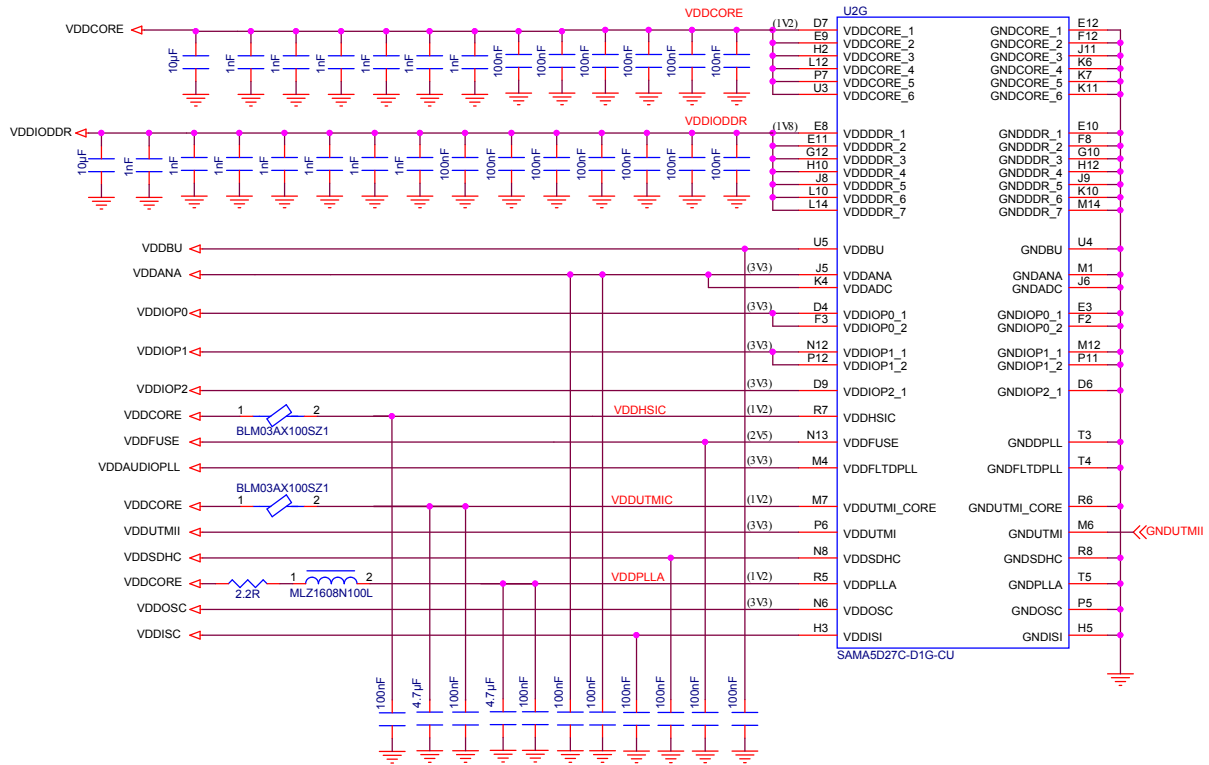**Figure 5-2. SAMA5D27C-D1G-CU Supplies Decoupling Schematic**

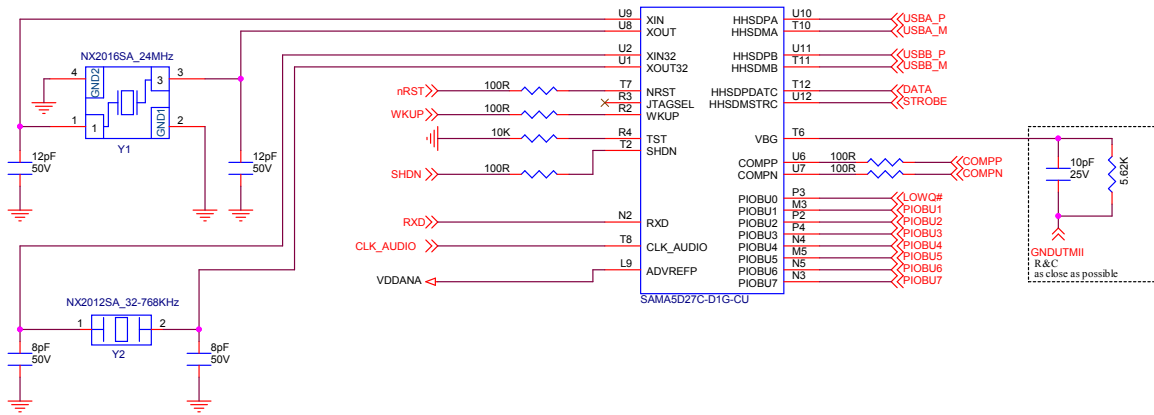**Figure 5-3. SAMA5D27C-D1G-CU System Schematic**

Table 5-1. SAMA5D27C-D1G-CU External Crystal

Item	Designation	Type	Manufacturer	Manufacturer Specification Number
Y1	24MHz Crystal	NX2016SA	NDK	EXS00A-CS08664
Y2	32.768kHz Crystal	NX2012SA	NDK	EXS00A-MU00626

5.2 Power Supplies

The SAMA5D27 SOM1 is supplied by an external 3.3V and generates its own internal supplies by interfacing with the Microchip MIC2800-G1JJYML power management unit.

The MIC2800 is a high-performance power management IC, providing three output voltages with maximum efficiency and is optimized to respect the MPU power up and down cycles.

Integrating a 2 MHz DC/DC converter with an LDO post regulator, the MIC2800 gives two high-efficiency outputs with a second, 300mA LDO for maximum flexibility. The DC-to-DC converter uses small values of L and C to reduce board space while still retaining efficiency over 90% at load currents up to 600mA.

The three outputs supply the following internal nodes:
- DCDC set @ 1.8V supplies SAMA5D27C-D1G-CU DDR2 pads and device.
- LDO1 set @ 1.2V supplies SAMA5D27C-D1G-CU Core.
- LDO2 set @ 2.5V supplies SAMA5D27C-D1G-CU VDDFUSE pad.

The MIC2800 is a µCap design, operating with very small ceramic output capacitors and inductors for stability.

It is available in fixed output voltages in the 16-pin 3mm x 3mm MLF$^®$ lead-less package. For more information, refer to the product web page.

**Figure 5-4. Power Management Unit Schematic**
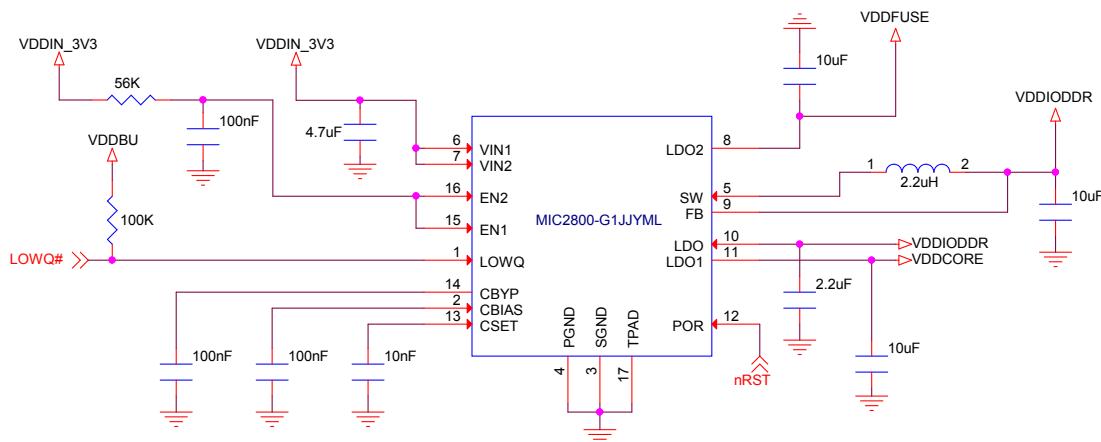
5.3 System Control

The SAMA5D27 SOM1 provides global system Reset (NRST) and Shutdown (SHDN) pins to the application board.

- The NRST pin is an output pin generated by the internal Power Management Unit (MIC2800-G1JJYML) in respect with power sequence timing. It can be forced externally in case of a system crash and must be connected as described in the example schematic below.
- The SHDN pin is an output pin and is managed by the software application. It switches the Main 3.3V Supply ON or OFF.

Figure 5-5. Internal System Control Schematic
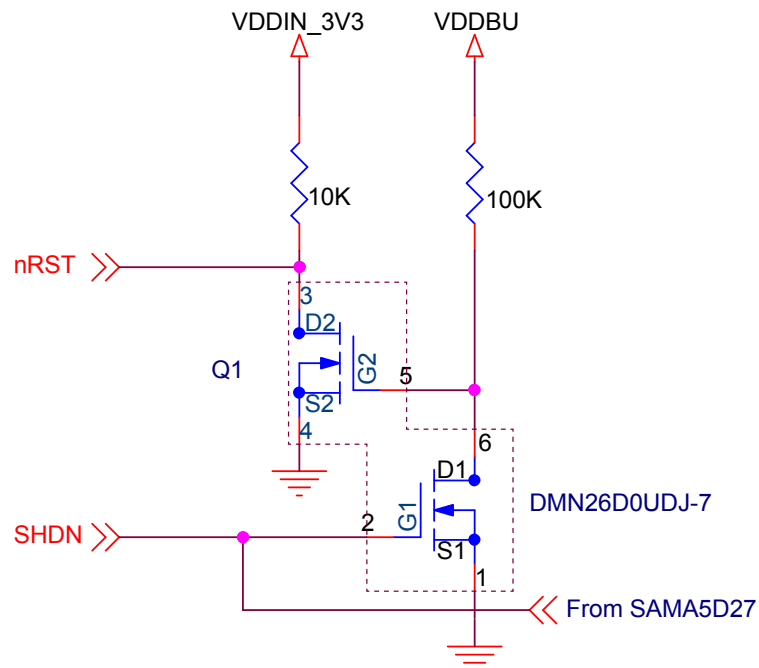
5.4 Ethernet PHY

The Microchip SAMA5D27 SOM1 embeds a single-supply 10BASE-T/100BASE-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNAIA is a highly-integrated PHY solution. The KSZ8081RNAIA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors.

The KSZ8081RNAIA is available in 24-pin, lead-free QFN packages. For more information, refer to the product web page.
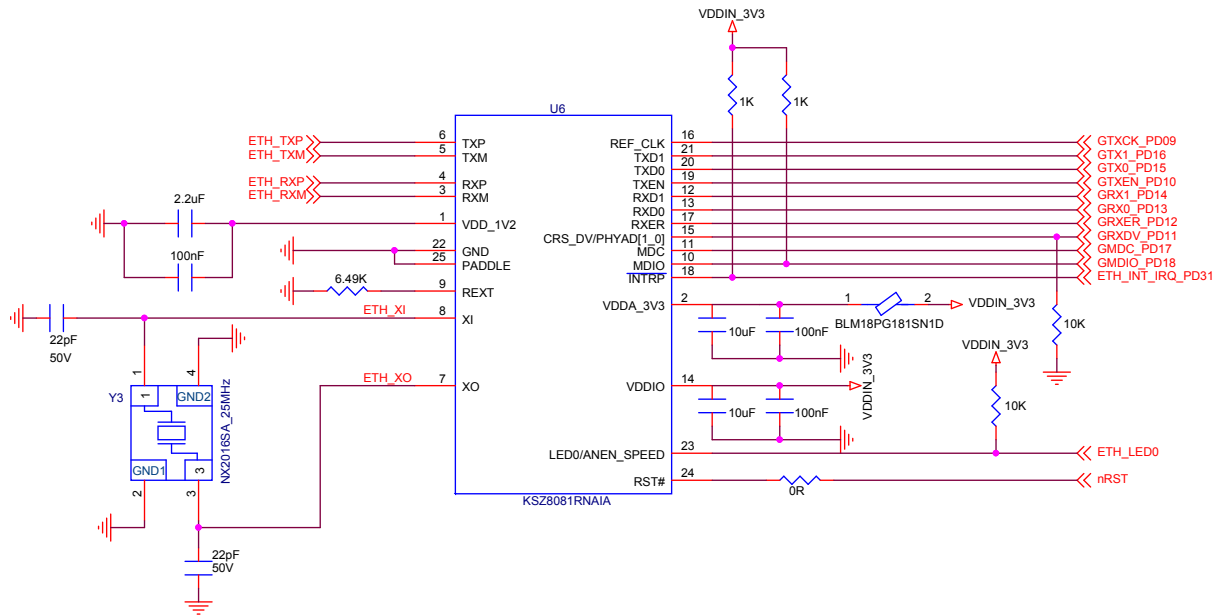
Figure 5-6. Ethernet PHY Schematic

Table 5-2. KSZ8081RNAIA External Crystal

| Item	Designation	Type	Manufacturer	Manufacturer Specification Number
Y3	25MHz Crystal	NX2016SA	NDK	EXS00A-CS10694

5.5   QSPI Memory

The SAMA5D27 SOM1 embeds the SST26VF064BT-104I/MF, a 64Mb Serial Quad I/O Flash memory.

The SST26VF064BT-104I/MF SQI features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package.

The SST26VF064BT-104I/MF is available in 8-lead WDFN package with 6mm × 5mm dimensions.

For more information, refer to the product web page.

Figure 5-7. QSPI Memory Schematic
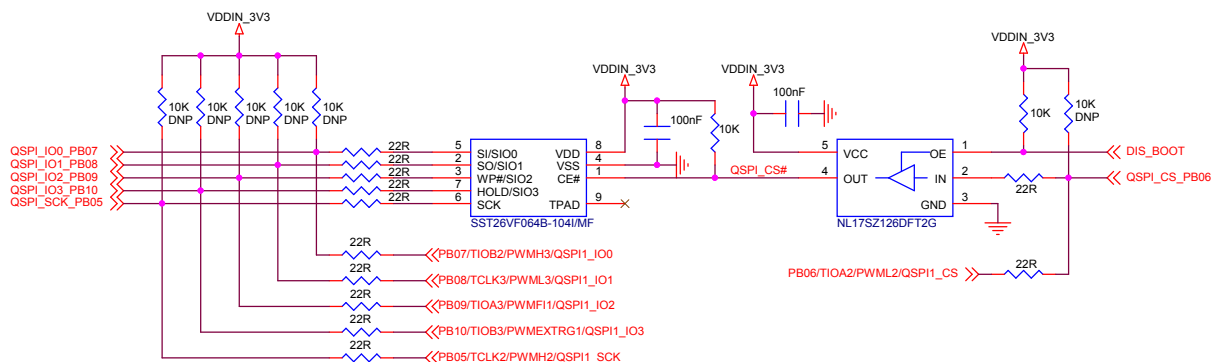
> **Tip:** In case of non-use at application level of the QSPI embedded in SAMA5D27 SOM1, it is possible to reassign the signals dedicated to QSPI memory to another PIO function as defined in the table below. To do so, the DIS_BOOT pin (SAMA5D27 SOM1 pad 126) must be forced to ground.

Table 5-3. Other GPIO Possibilities for QSPI Interface in Case of Non-use

Pin Number	Power Rail	Primary		PIO Peripheral				Reset State
		Signal	Dir	Func	Signal	Dir	IOset	
134	VDDIN_3V3	PB05	I/O	A	TCLK2	I	1	PIO, I, PU, ST
				C	PWMH2	O	1	
				D	QSPI1_SCK	O	2	
127	VDDIN_3V3	PB06	I/O	A	TIOA2	I/O	1	PIO, I, PU, ST
				C	PWML2	O	1	
				D	QSPI1_CS	O	2	
133	VDDIN_3V3	PB07	I/O	A	TIOB2	I/O	1	PIO, I, PU, ST
				C	PWMH3	O	1	
				D	QSPI1_IO0	I/O	2	
128	VDDIN_3V3	PB08	I/O	A	TCLK3	I	1	PIO, I, PU, ST
				C	PWML3	O	1	
				D	QSPI1_IO1	I/O	2	
132	VDDIN_3V3	PB09	I/O	A	TIOA3	I/O	1	PIO, I, PU, ST
				C	PWMFI1	I	1	
				D	QSPI1_IO2	I/O	2	
135	VDDIN_3V3	PB10	I/O	A	TIOB3	I/O	1	PIO, I, PU, ST
				C	PWMEXTRG1	I	1	
				D	QSPI1_IO3	I/O	2	

> **Tip:** The QSPI interface can be shared with another external device. To do so, the QSPI_CS# node must stay at "High" level. That means that the DIS_BOOT pin (SAMA5D27 SOM1 pad 126) must be forced to ground.

5.6   EEPROM Memory

The SAMA5D27 SOM1 embeds the 24AA02E48T-I/OT, a 1Kb Serial EEPROM with pre-programmed EUI-48 MAC address.

The device is organized as one block of 128 x 8-bit memory with a 2-wire serial interface. The second block is reserved for MAC Address storage.

The 24AA02E48T-I/OT also has a page write capability for up to 8 bytes of data.

The 24AA02E48T-I/OT is available in the standard 5-lead SOT-23 package. For more information, see the product web page.

Figure 5-8. EEPROM Memory Schematic
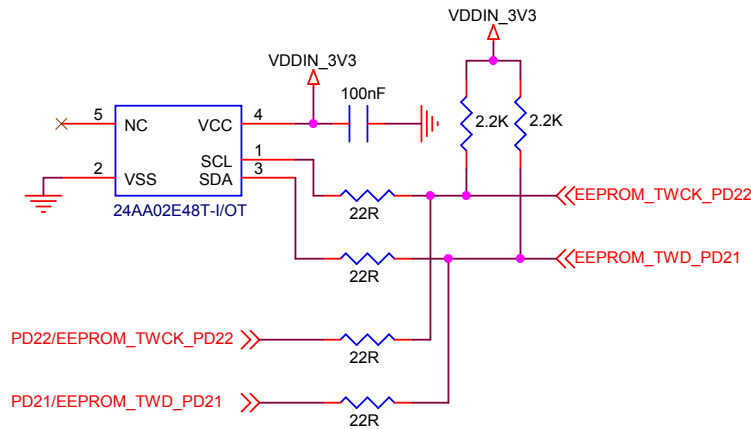
Tip: The 2-Wire serial interface can be externally shared with another device. 2-Wire Data Signal (SAMA5D27 SOM1Pad 19) and 2-Wire Clock Signal (SAMA5D27 SOM1Pad 20) are used.

Important: If the 2-Wire serial interface is used externally, the device connected must have a different I²C address than the embedded EEPROM. The embedded EEPROM has the following I²C address range: 0x40 – 0x47

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6. Power Supply Connections and Timing Sequences

The SAMA5D27 SOM1 can be supplied in different ways depending on application needs.

Four power domains must be supplied and can be connected differently. The four different power connections are described below:

- Power Configuration #1: All supplies are connected to the Main 3.3V Supply.
- Power Configuration #2: Backup domain is connected to a coin-cell and the rest to the Main 3.3V Supply.
- Power Configuration #3: Backup domain is connected to a coin-cell. Camera sensor is connected to a separate power supply and the rest to the Main 3.3V Supply.
- Power Configuration #4: All supply domains are connected to separate power supplies.

For each power configuration, a Power-On and Power-Off timing sequences to respect are described below.

6.1 Power Supply Configuration #1

The SAMA5D27 SOM1 is supplied by only one main supply.

In this configuration mode, all supplies are connected together and supplied by the main 3.3V supply. All PIOs have VDDIN_3V3 Power Rail as voltage reference.

Figure 6-1. Power Configuration #1
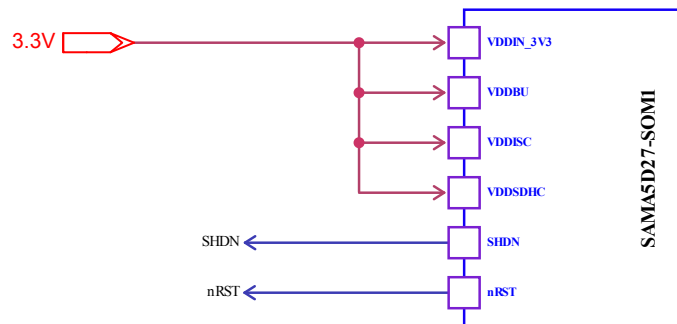
In this configuration mode, the two following timing sequences are applied.

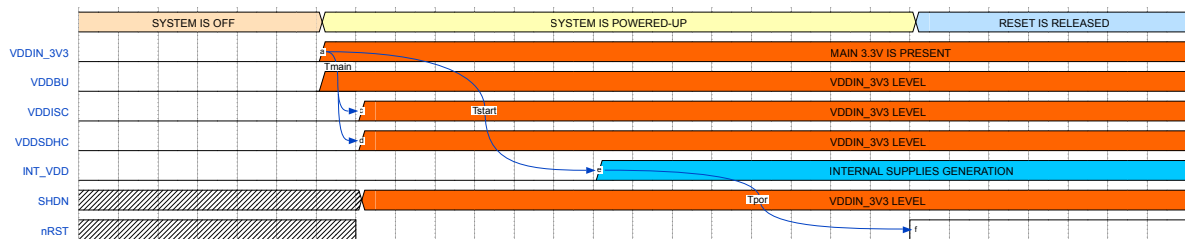**Figure 6-2. Power-On Sequence Timing Diagram**

Figure 6-3. Power-Off Sequence Timing Diagram

Table 6-1. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}[1]	Main 3.3V Startup Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:

1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than 800µs. VDDBU must be applied at the same time as VDDIN_3V3 or just before. It is forbidden to apply VDDBU after VDDIN_3V3.

6.2   Power Supply Configuration #2

The SAMA5D27 SOM1 is supplied by different power supplies.

- Backup domain is connected to a coin-cell.
- The rest of the power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have VDDBU Power Rail as reference. All other PIO have VDDIN_3V3 Power Rail as reference.

- COMPP and COMPN
- PIOBU1 to PIOBU7
- RXD, SHDN and WKUP

Figure 6-4. Power Configuration #2

In this configuration, the two following timing sequences are applied.

Figure 6-5. Power-On Sequence Timing Diagram
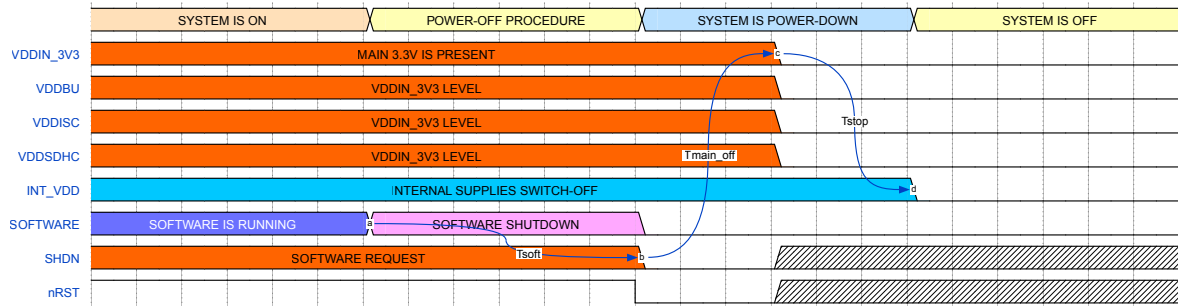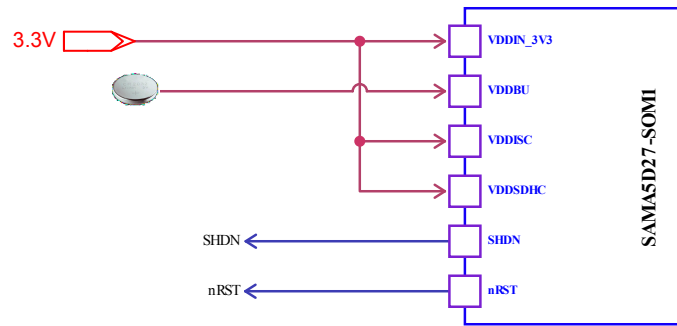

Figure 6-6. Power-Off Sequence Timing Diagram
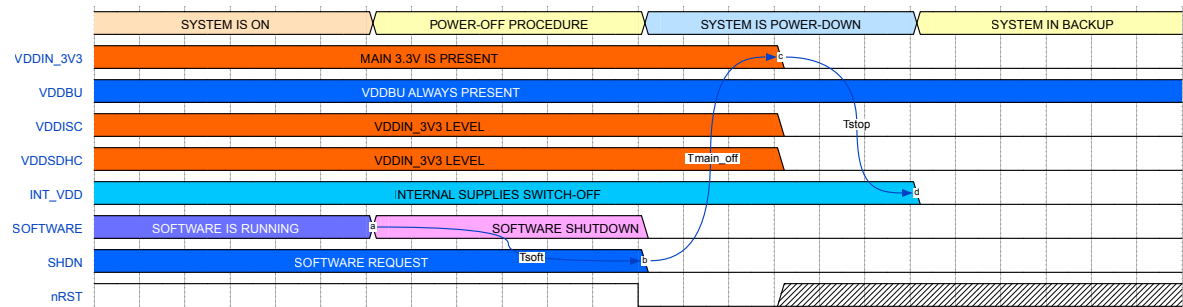
Table 6-2. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}[1]	Main 3.3V Startup Time	–	–	1	ms
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time	–	–	1	ms
t_{stop}	Internal Delay before switching-off System Core Supplies	1	–	3	ms

Note:

1. The three supplies VDDIN_3V3, VDDISC and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than t_{start}.

6.3   Power Supply Configuration #3

Some power inputs of the SAMA5D27 SOM1 are grouped and others are supplied by a separated power supplies.

- Backup domain is connected to a coin cell.
- Camera sensor power input (VDDISC) is connected to a separate power supply set at one of the following voltage levels (1.8V/2.5V/2.8V/3.0V or 3.3V) depending on the camera sensor technology used in the application.
- The remaining power inputs are connected to the main 3.3V supply.

In this configuration, the following PIOs have:
- VDDBU Power Rail as reference
    - COMPP and COMPN
    - PIOBU1 to PIOBU7
    - RXD, SHDN and WKUP
- VDDISC Power Rail as reference
    - PC09 to PC25
- All other PIOs have VDDIN_3V3 Power Rail as reference.

Figure 6-7. Power Configuration #3
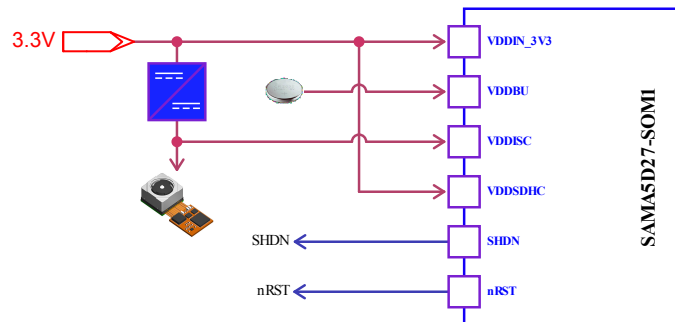
In this configuration mode, the two following timing sequences are applied.
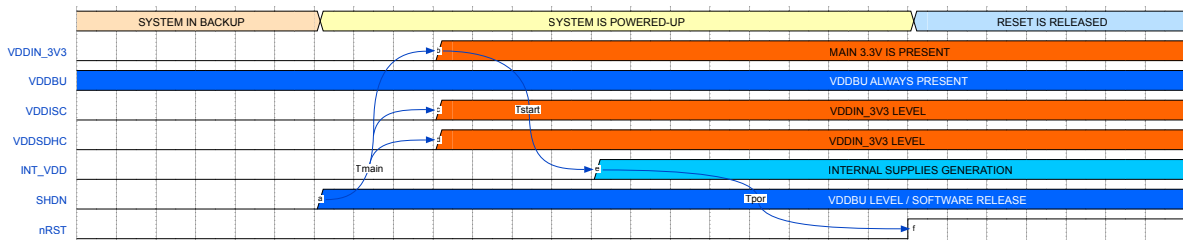
Figure 6-8. Power-On Sequence Timing Diagram

Figure 6-9. Power-Off Sequence Timing Diagram
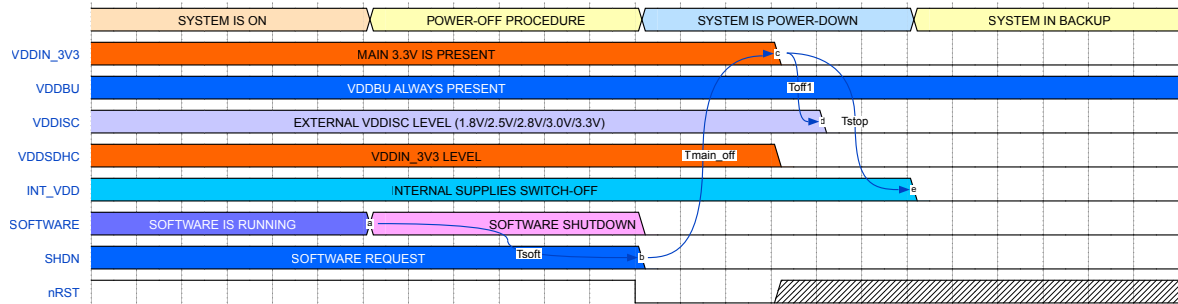
Table 6-3. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}[1]	Main 3.3V Startup Time (From regulator available on the motherboard)	–	–	1	ms
t_{on1}	VDDISC Regulator Startup Time (From regulator available on the motherboard)	–	–	800	µs
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off1}	VDDISC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:

1. The supplies VDDIN_3V3 and VDDSDHC must be applied at the same time. If a delay is implemented, it must be lower than t_{start}.

6.4   Power Supply Configuration #4

Each power input of the SAMA5D27 SOM1 is supplied by separate power supplies.

- Backup domain is connected to a coin cell.
- Camera sensor power input (VDDISC) is connected to a separate power supply set at one of the following voltage levels (1.8V/2.5V/2.8V/3.0V or 3.3V) depending on the camera sensor technology used in the application.
- SD Card power input (VDDSDHC) is connected to a separate power supply set at one of the following voltage levels (1.8V or 3.3V) depending on the SD Card Technology/Speed used in the application.
- VDDIN_3V3 power input is connected to the main 3.3V supply.

In this configuration, the following PIOs have:

- VDDBU Power Rail as reference
    - COMPP and COMPN
    - PIOBU1 to PIOBU7
    - RXD, SHDN and WKUP
- VDDISC Power Rail as reference
    - PC09 to PC25
- VDDSDHC Power Rail as reference
    - PA00 to PA10
- All other PIOs have VDDIN_3V3 Power Rail as reference.

Figure 6-10. Power Configuration #4
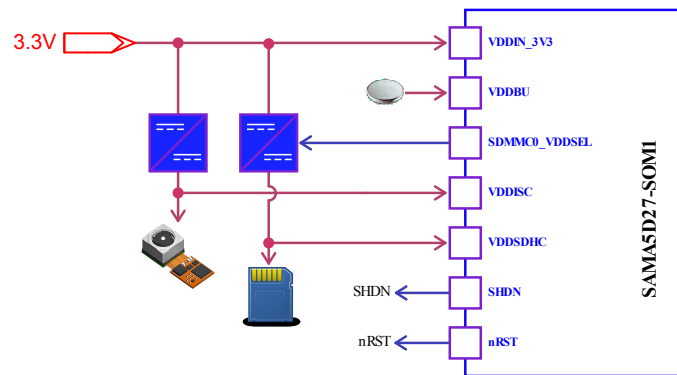
In this configuration mode, the two following timing sequences are applied.

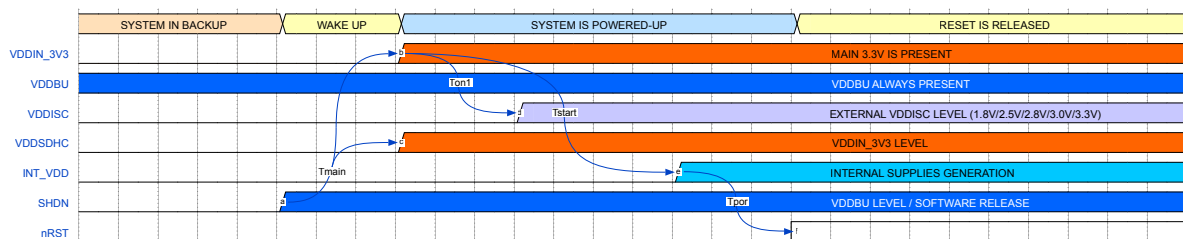**Figure 6-11. Power-On Sequence Timing Diagram**
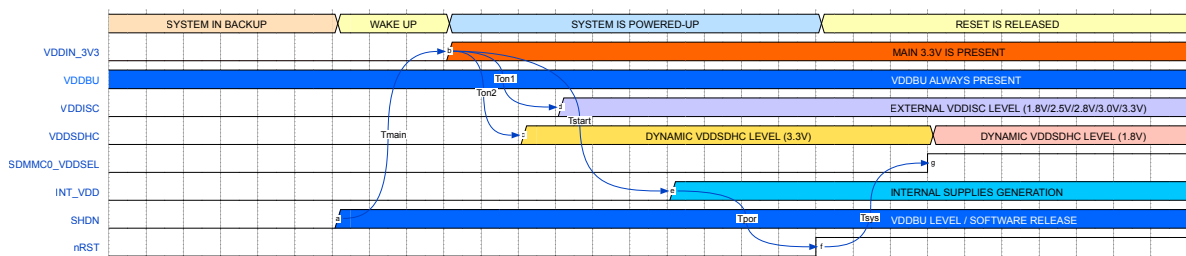
Figure 6-12. Power-Off Sequence Timing Diagram
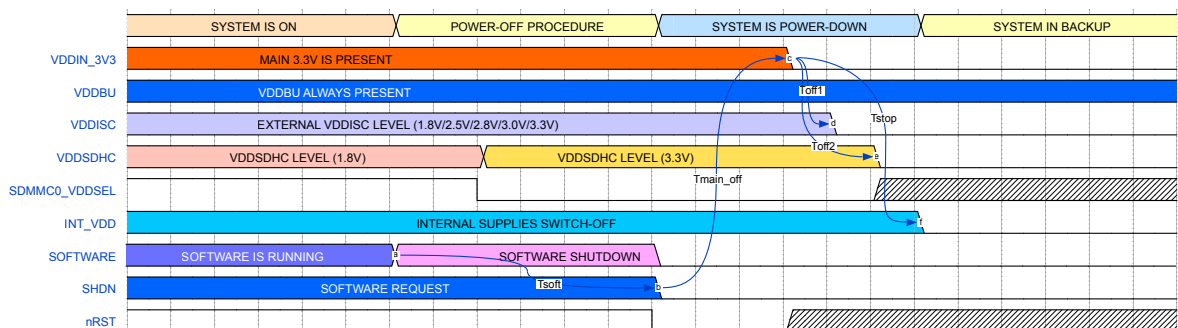
Table 6-4. Timing Values

Symbol	Description	Min.	Typ.	Max.	Unit
t_{main}	Main 3.3V Startup Time (From regulator available on the mother board)	–	–	1	ms
t_{on1}	VDDISC Regulator Startup Time (From regulator available on the mother board)	–	–	800	µs
t_{on2}	VDDSDHC Regulator Startup Time (From regulator available on the mother board)	–	–	800	µs
t_{start}	Internal Delay before starting System Core Supplies	1	–	3	ms
t_{por}	Power-On Reset Delay	–	10	11	ms
t_{sys}	Low Speed to High Speed card timing[1]	Depending on system off time			ms
t_{soft}	Software Shutdown Time	Depending on system off time			ms
t_{main_off}	Main 3.3V Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off1}	VDDISC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{off2}	VDDSDHC Regulator Power-off Time (From regulator available on the motherboard)	–	–	1	ms
t_{stop}	Internal Delay before switching off System Core Supplies	1	–	3	ms

Note:
1. Timing depends on the system boot time. No particular recommendations to apply.

7.   Booting Guidelines

This section provides an overview of how to program a Non Volatile Memory (NVM) and boot from it.

The SAMA5D27 SOM1 embeds a Quad I/O Flash Memory as a source for boot. Another type of NVM may be located on the motherboard. This section explains how to program, select and boot from an NVM.

7.1   Boot Process

The system always boots from the ROM memory at address 0x0. The ROM code is a boot program contained in the embedded ROM. It is also called "First level bootloader". The SAMA5D2 can be configured to run a Standard Boot mode or a Secure Boot mode. More information on how the Secure Boot mode can be enabled, and how the chip operates in this mode, is provided in the document "SAMA5D2x Secure Boot Strategy", document no. 44040. To obtain this application note and additional information about the secure boot and related tools, contact a Microchip sales representative.

By default, the chip starts in Standard Boot Mode.

The ROM code standard sequence is executed as follows:
*   Basic chip initialization: crystal or external clock frequency detection.
*   Attempt to retrieve a valid code from external non-volatile memories (NVM).
*   Execution of a monitor called SAM-BA Monitor, in case no valid application has been found on any NVM [1].

Note:
1.   This may be the case during the first start-up or after an NVM erase or when a "boot disable jumper" is used on the memory Chip Select, in order to force an update.

7.2   Boot Configuration

The boot sequence is controlled using a Boot Configuration Word in the Fuse area. The Boot Configuration Word allows several customizations of the Boot Sequence:
*   To configure the IO Set where the external memories used to boot are connected (see Section 16.4.8 "Hardware and Software Constraints" for a description of the IO sets)
*   To disable the boot on selected memories
*   To configure the UART port used as a terminal console
*   To configure the JTAG pins used for debug. Refer to Debug Considerations.

See the section "Boot Configuration Word" of the SAMA5D2 datasheet, document no. DS60001476, for a detailed description of all the bitfields in this word. By default, the value of this word is 0x0. During prototyping phases, the value of this fuse word can be overridden by the content of a backup register. The conditions to enable this feature are as follows:
*   The fuse bit DISABLE_BSCR must not be set (default value).
*   The Boot Sequence Controller Configuration Register (BSC_CR) must have the BUREG_VALID bit set and indicate in BUREG_INDEX which register has to be used.

Using BUREG allows the user to test several boot configuration options, including Secure Boot Mode, without burning fuses.
Note: VDDBU must be connected in order to benefit from this feature. However, in production, it is highly recommended to disable this feature and to write the boot configuration in fuses.

7.3   NVM Programming

The SAMA5D27 SOM1 is delivered with SAM-BA® In-System Programmer, a comprehensive tool to program boot memories.

In case the boot code does not find a valid program in NVM, the SAM-BA monitor is launched in order to program the considered NVM.

The SAM-BA monitor principle is to:

- Initialize DBGU and USB.
- Check if USB Device enumeration occurred.
- Check if characters are received on the DBGU.

Once the communication interface is identified, the application runs in an infinite loop waiting for different commands.

The firmware can be sent and programmed in the NVM.

For more information, refer to the following link. http://www.at91.com/linux4sam/bin/view/Linux4SAM/Sama5d2XplainedMainPage#Using_SAM_BA_to_flash_components

7.4   Boot From External Memory

Several types of external memories such as NAND Flash, SDCard, SPI Flash, QSPI Flash, etc. can be connected to the SAMA5D27 SOM1 and placed on the motherboard.

For details of the Boot sequence, refer to the "NVM Bootloader Program Description for MRL C Parts" diagram of the SAMA5D2 datasheet, document no. DS60001476.

The table below provides the list of external memory types and interfaces that enable connection to the SAMA5D27 SOM1:

Table 7-1. External Memory Connections

Memory Type	Interface	PIO	Comments
SDCard	SD-MMC0	PA0 to PA13	If external SDMMC0 interface is not used, bit SDMMC_0 in *Boot Configuration Word* must be set to 1.
	SD-MMC1	PA18 to PA22, PA27 to PA30	If external SDMMC1 Interface is not used, bit SDMMC_1 in *Boot Configuration Word* must be set to 1.
eMMC	SD-MMC0	PA0 to PA10, PA13	If external SDMMC0 Interface is not used, bit SDMMC_0 in *Boot Configuration Word* must be set to 1.
NAND Flash	NFC	PA0 to PA21, PC11 to PC31, PD0 to PD8	Field NFC in *Boot Configuration Word* must be set to "01". IOSET2 is selected. (See Notes below)
QSPI Flash	QSPI0	PA0 to PA5	Field QSPI_0 in *Boot Configuration Word* must be set to "00". IOSET1 is selected. (See Notes below)

Memory Type	Interface	PIO	Comments
		PA14 to PA19	Field QSPI_0 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
		PA22 to PA27	Field QSPI_0 in **Boot Configuration Word** must be set to "10". IOSET3 is selected. (See Notes below)
	QSPI1	PB5 to PB10	Need to tie DIS-BOOT pin to GND. Bits QSPI_1 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
SPI Flash	SPI0	PA14 to PA17	Bits SPI_0 in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)
		PA30, PA31, PB0, PB1	Bits SPI_0 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
	SPI1	PA22 to PA25	Bits SPI_1 in **Boot Configuration Word** must be set to "01". IOSET2 is selected. (See Notes below)
		PC1 to PC4	Bits SPI_1 in **Boot Configuration Word** must be set to "00". IOSET1 is selected. (See Notes below)

Note: For these external memory configurations, set the EXT_MEM_BOOT_ENABLE bit to "1" in **Boot Configuration Word**.

Note: The Boot Configuration Word allows several customizations of the boot sequence. For details, refer to the section "Boot Configuration" in the SAMA5D2 datasheet, document no. DS60001476.

8. Debug Considerations

The SAMA5D27 SOM1 JTAG access is disabled during the execution of the ROM code sequence. It is re-enabled when jumping into SRAM when a valid code has been found on an external NVM, at the same time the ROM memory and fuses are hidden. If no valid boot is found on an external NVM, the ROM code

- enables the USB connection and one UART serial port
- starts the standard SAM-BA monitor
- locks access to the ROM memory
- re-enables the JTAG connection

The SAMA5D27 SOM1 has multiple debug and JTAG settings. For more information, refer to the SAMA5D2 datasheet, document no. DS60001476, "SECUMOD JTAG Protection Control Register", "Customer Fuse Matrix" and "Special Function Bits".

The JTAG I/O set can be configured. For correct operations, the I/O set to be used is JTAG_IOSET_3, i.e., the field JTAG_IO_SET in the Boot Configuration Word must be written with value '2'.[1]

Note: Due to IO conflict on line PA22, JTAG_IOSET_4 must not be implemented when SDMMC1 is used as an NVM boot media. See the SAMA5D2 datasheet, document no. DS60001476, "Boot Configuration Word".

9. Electrical Characteristics

This section provides an overview of the electrical characteristics of the SAMA5D27 SOM1 module. Absolute maximum ratings for the SAMA5D27 SOM1 module are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the module at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

9.1 Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings

Parameter	Conditions	Min.	Max.
Storage Temperature	–	-60°C	+150°C
Maximum Operating Temperature	–	-40°C	+85°C
Voltage on Inputs Pins	With respect to ground	-0.3V	+4.0V
Maximum Voltage	On VDDIN_3V3 Pads	–	+4.0V
	On VDDBU Pad	–	+4.0V
	On VDDSDHC Pad	–	+4.0V
	On VDDISC Pad	–	+4.0V

Important: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Operational Characteristics

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-2. Table 7. Power Supplies Operating Conditions

Pad	Parameters	Conditions	Min.	Typ.	Max.
VDDIN_3V3	DC Supply	–	3.0V	3.3V	3.6V
	Maximum Input Current	–	–	–	450mA
VDDBU	DC Supply	Must be established first or at the same time as VDDIN_3V3.	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	0.1 mA

Pad	Parameters	Conditions	Min.	Typ.	Max.
VDDSDHC	DC Supply	SDHC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA
VDDISC	DC Supply	ISC I/Os Lines	1.65V	3.3V	3.6V
	Maximum Input Current	–	–	–	30mA

9.3 DC Electrical Characteristics

9.3.1 Standard Interfaces

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-3. DC Electrical Characteristicsfor GPIO Inputs

Pad	Parameters	Conditions	Min.	Typ.	Max.
V_{IL}	Low-level Input Voltage	All GPIO @ 3.3V	-0.3V	–	0.4V
V_{IH}	High-level Input Voltage	All GPIO @ 3.3V	2.3V	–	3.6V
V_{OL}	Low-level Output Voltage	I_O Max.	–	–	0.41V
V_{OH}	High-level Output Voltage	I_O Max.	2.9V	–	--
I_{IL}	Low-level Input Current	All GPIO @ 3.3V	-1µA	–	1µA
I_{IH}	High-level Input Current	All GPIO @ 3.3V	-1µA	–	1µA
I_{OL}	Low-level Output Current	All GPIO @ 3.3V / Low	-2mA	–	--
		All GPIO @ 3.3V / High	-32mA	–	--
I_{OH}	High-level Output Current	All GPIO @ 3.3V / Low	–	–	2mA
		All GPIO @ 3.3V / High	–	–	32mA
R_{PULLUP}	Pull-up Resistors	All GPIO @ 3.3V and PDxx in AD mode.	280kΩ	380kΩ	480kΩ
		All IOs in GPIO mode @3.3V.	40kΩ	66kΩ	130kΩ
$R_{PULLDOWN}$	Pull-down Resistors	All GPIO @ 3.3V and PDxx in AD mode	280 kΩ	380kΩ	480kΩ
		All IOs in GPIO mode @3.3V.	40kΩ	77kΩ	160kΩ

Note: This table applies to all the following pads: PA0–PA31, PB0–PB31, PC0–PC31, PD0–PD8, PD19-PD30.

9.3.2 Other PIOs

The following characteristics are applicable to the operating temperature range T_A = -40°C to +85°C, unless otherwise specified.

Table 9-4. Table 7. DC Electrical Characteristics for System Inputs

Pad	Parameters	Conditions	Min.	Typ.	Max.
V_{IL}	Low-level Input Voltage	DIS_BOOT	–	–	1.0V
V_{IH}	High-level Input Voltage	DIS_BOOT	2.3V	–	–

10. Mechanical Characteristics

10.1 Module Dimensions

The SAMA5D27 SOM1 has dimensions of 40mm x 38mm with the specific following mechanical characteristics.

Figure 10-1. System-On-Module Dimensions
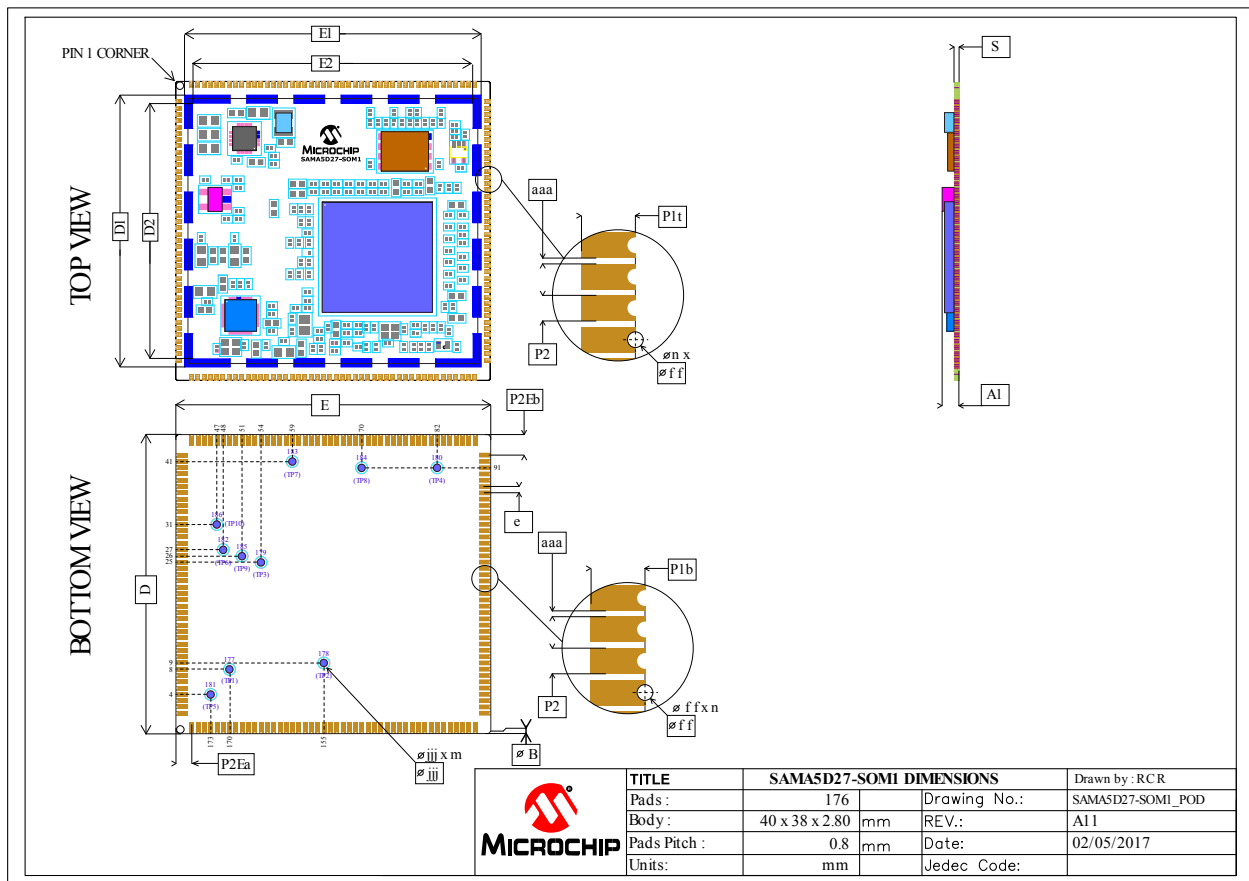
Table 10-1. System-On-Module Dimensions

		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
Body Size	X	E	--	40.000	40.100	–
	Y	D	--	38.000	38.100	–
Pad Pitch		e	--	0.800	--	–
PCB Thickness		S	1.150	1.200	1.250	–
Total Thickness		A1	--	2.750	2.800	–
PCB Angle Hole Diameter[1]		B	–	0.200	–	–
Pad Length[1]	Bottom Side	P1b	–	1.500	–	–

		Symbol	Common Dimensions			Comments
			Min.	Typ.	Max.	
	Top Side	P1t	–	0.800	–	–
Pad Width[1]		P2	–	0.600	–	Solder Mask defined 0.550
Pad Space[1]		aaa	–	0.200	–	–
Opening Drilling Diameter		fff	–	0.400	–	0.400 typic minus metallization
Pad Count		n	–	176	–	–
Edge Center to Center	X	E1	37.550	37.630	37.700	–
	Y	D1	34.400	34.480	34.550	–
	X	E2	35.550	35.630	35.700	–
	Y	D2	32.400	32.480	32.550	–
Pad Axis to Edge[1]	X	P2Ea	–	2.000	–	–
	Y	P2Eb	–	2.600	–	–

Note:

1. Tolerances are defined upon:
    –   IPC A600 - Class2
    –   IPC 2615

Warning: Test points placed on the bottom side are used for factory test only. It is not possible to connect external devices on these test points.

10.2   Module Land Pattern

The SAMA5D27 SOM1 Module has the following recommended Land Pattern characteristics.
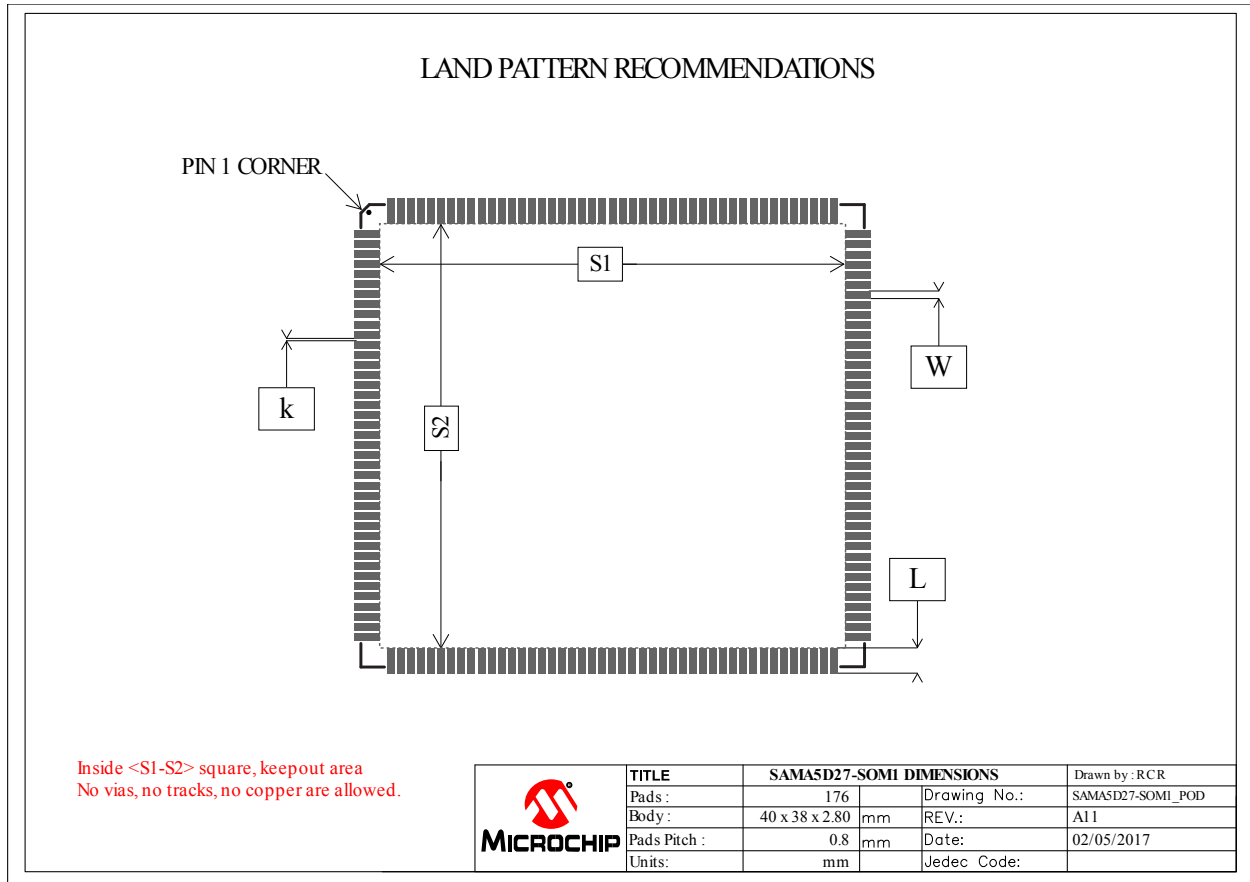
Figure 10-2. System-On-Module Land Pattern

LAND PATTERN RECOMMENDATIONS

Inside <S1-S2> square, keepout area
No vias, no tracks, no copper are allowed.

TITLE	SAMA5D27-SOM1 DIMENSIONS		Drawn by : RCR
Pads :	176	Drawing No.:	SAMA5D27-SOM1_POD
Body :	40 x 38 x 2.80 mm	REV.:	A11
Pads Pitch :	0.8 mm	Date:	02/05/2017
Units:	mm	Jedec Code:	

Table 10-2. System-On-Module Land Pattern Dimensions

|	Symbol	Common Dimensions			Comments
		Min.	Typ.	Max.	
Land Pattern Pad Width	W	–	0.600	–	Solder Mask Defined 0.550
Land Pattern Pad Length	L	–	2.000	–	–
Land Pattern Pad X Space	S1	–	37.000	–	–
Land Pattern Pad Y Space	S2	–	35.000	–	–
Land Pattern Pad Space	k	–	0.200	–	–

11. Reflow Profile

The SAMA5D27 SOM1 was assembled using standard lead-free reflow profile IPC/JEDEC JSTD-020.

The SAMA5D27 SOM1 can be soldered to the host PCB by using the standard leaded and lead-free solder reflow profile. To avoid damage to the module, follow these recommendations:

- Follow solder reflow recommendations provided in Microchip Technology Application Note "AN233 Solder Reflow Recommendation (DS00233)".
- Do not exceed the peak temperature (T_P) of 250ºC.
- Refer to the solder paste datasheet for specific reflow profile recommendations.
- Use no-clean flux solder paste. Use no-clean flux solder paste
- Use only one flow. If the PCB requires multiple flows, mount the module at the time of the final flow.

Figure 11-1. Reflow Profile Example used for Soldering SAMA5D27 SOM1 Module on SAMA5D27-SOM1-EK1 board
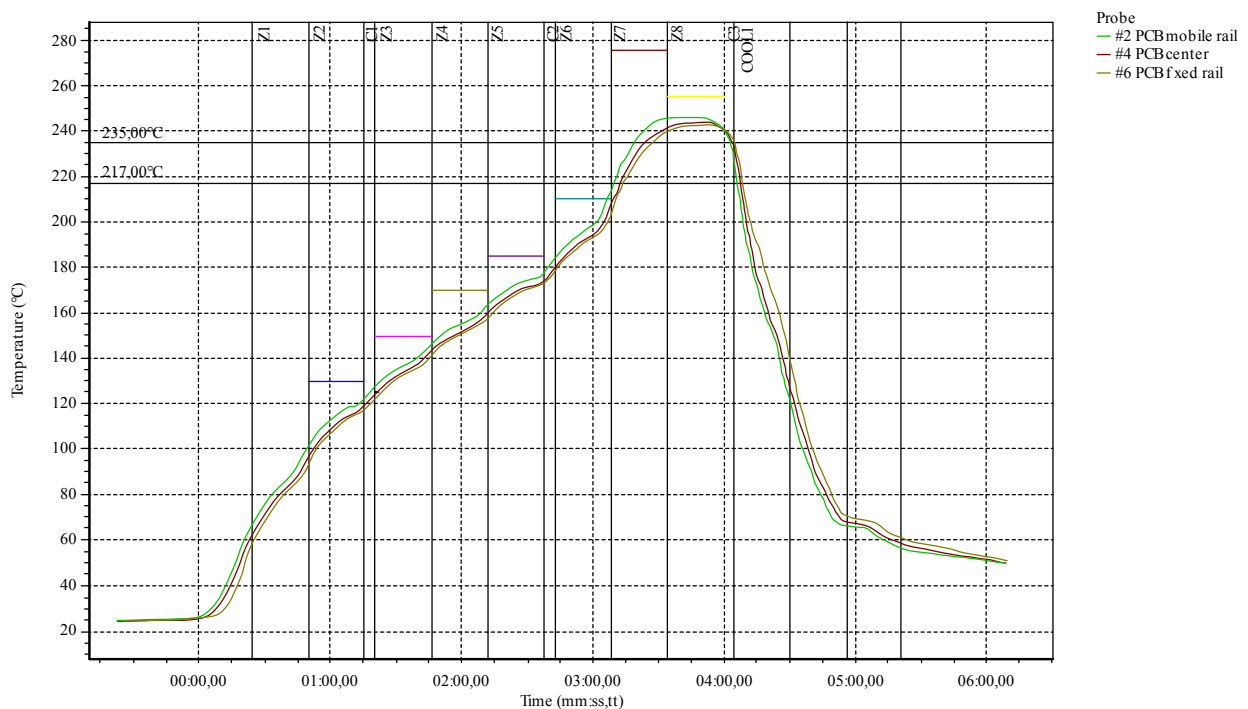
12.   Ordering Information

Table 12-1. Ordering Information

Ordering Code	Version	Package	Carrier Type	Operating Temperature Range
ATSAMA5D27-SOM1	1	176-pin 38x40mm	Tray	-40°C to +85°C
ATSAMA5D27-SOM1-EVAL	–	176-pin 38x40mm	Tray	Room temperature

13. Revision History

Table 13-1. SAMA5D27 SOM1 Datasheet, Rev. DS60001521A, Oct-2017

Changes
First issue.

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ATSAMA5 D27 - SOM1

Architecture

Product Group

System on Module
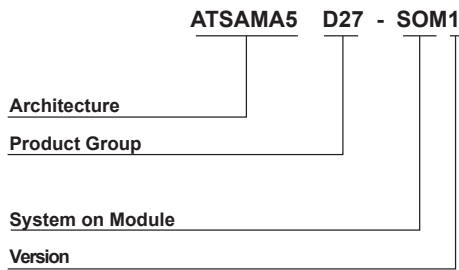
Version

Architecture:	SAMA5
Product Group:	D27
System on Module:	SOM
Version:	1

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